CS221: Digital Design

FPGA and HDL: Programmable Devices

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Outline

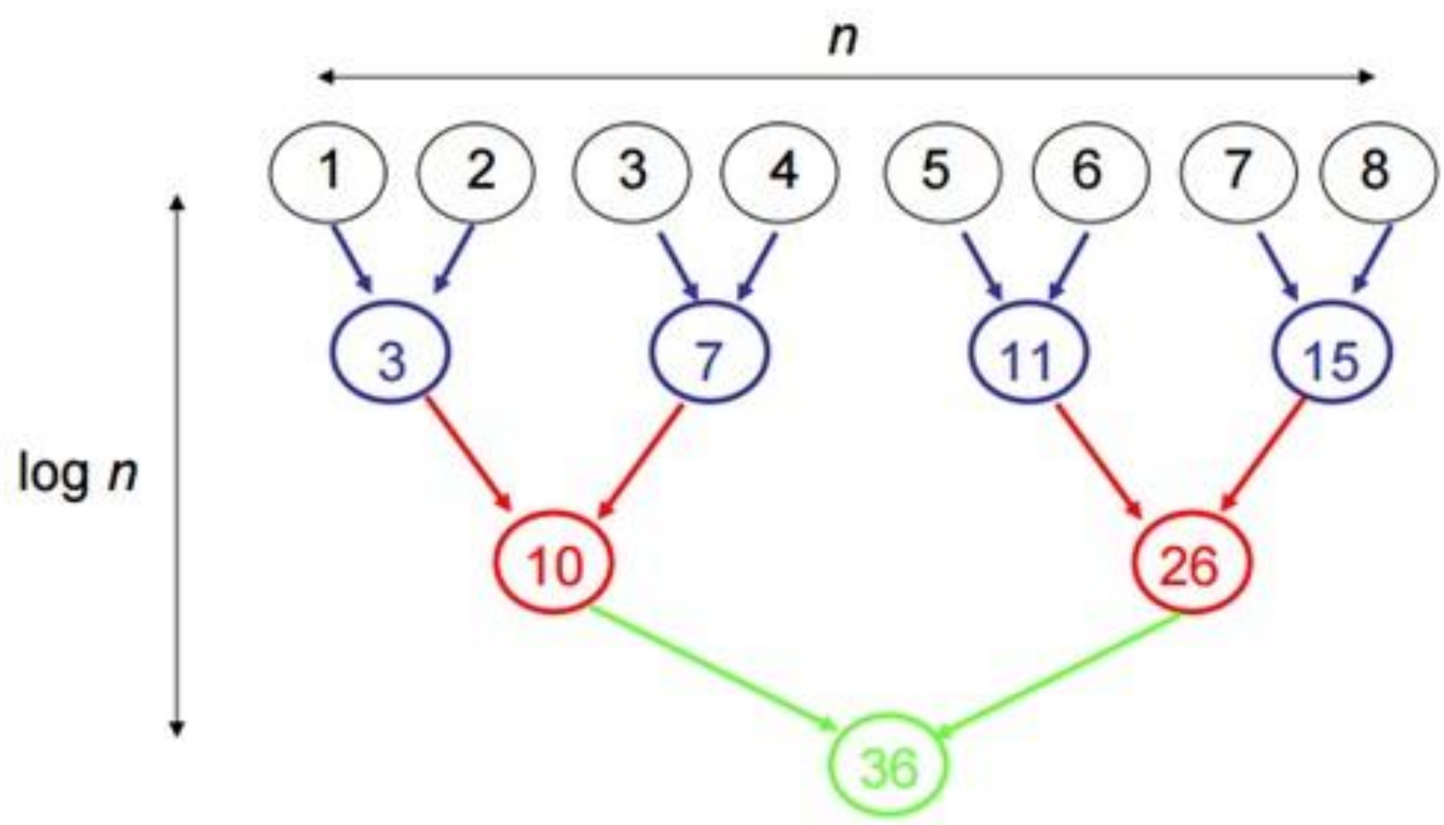
- EDA : Can we automate Digital Design Process
- IC Design process, FPGA
- HDL Requirement of VHDL, Model
- IC and FPGA Based Design Process

Digital Design Automation

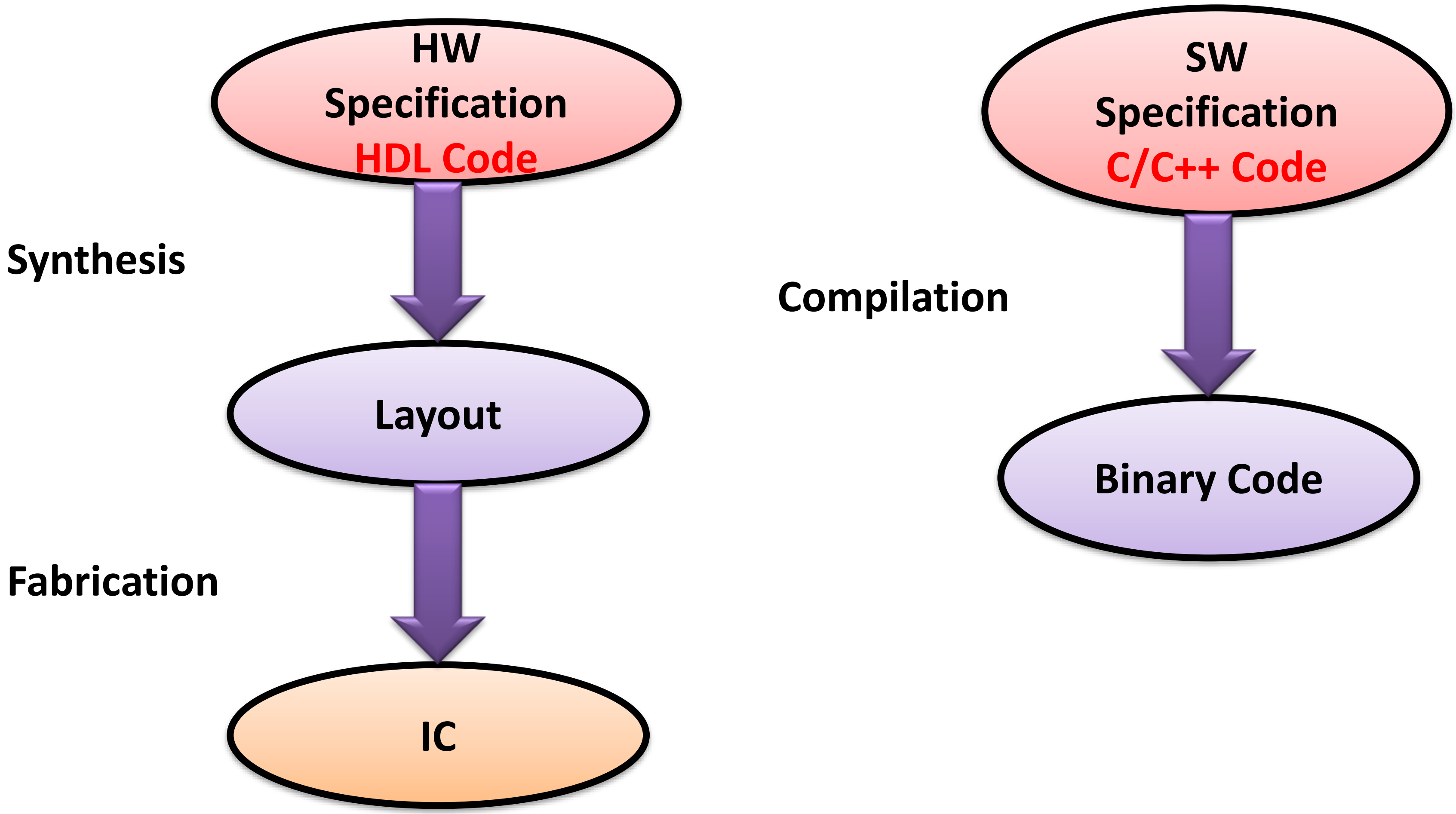
- Electronics Design Automation
  - Automation of Chip Design
  - Automation of Comb. Circuit Optimization
  - Automation of Sequential Circuit Generation : **Given a C like Statement of System: Ex- sum of 1^{st} n odd number**
    - Generate ASM Automatically : Using Program
    - Infer Data Path and FSM/CP automatically: Using Program
    - Take Constraints: Size, Power, Components
- Simulation and Prototype: ModelSim, FPGA
- Specification Language: HDL

Serial Code Vs Parallel

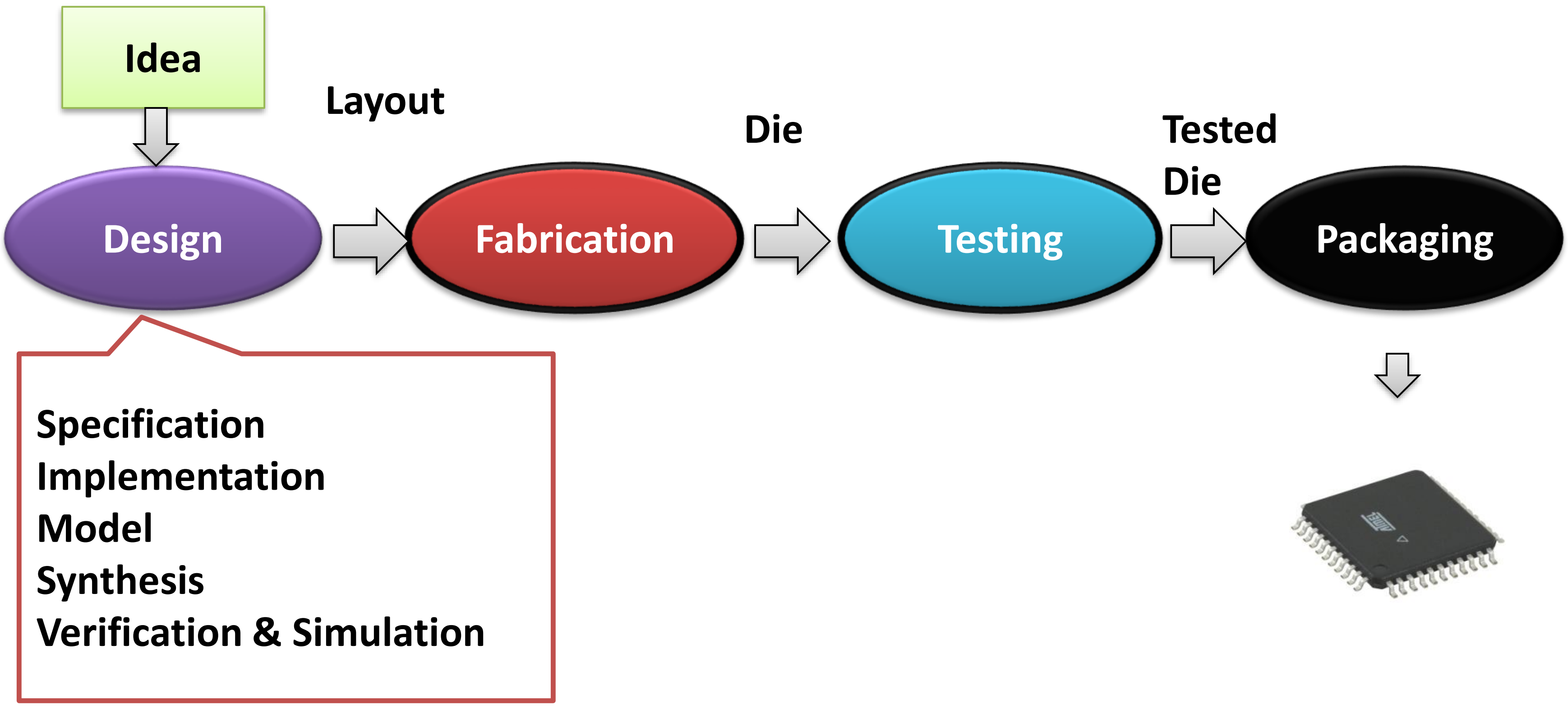
- C Code: For (i=0;i<8;i++) S= S+X[i];
- In H/W



Design Flow: Hardware Vs Software

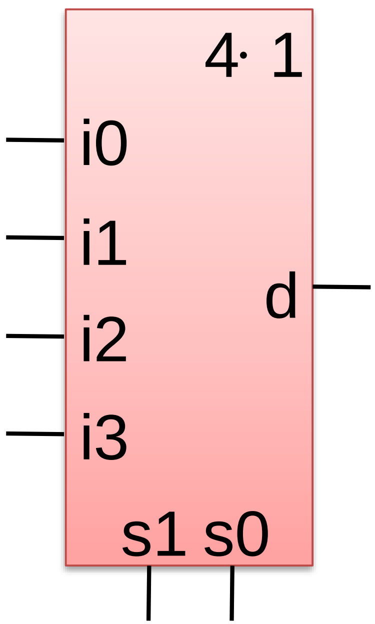


IC Design Process

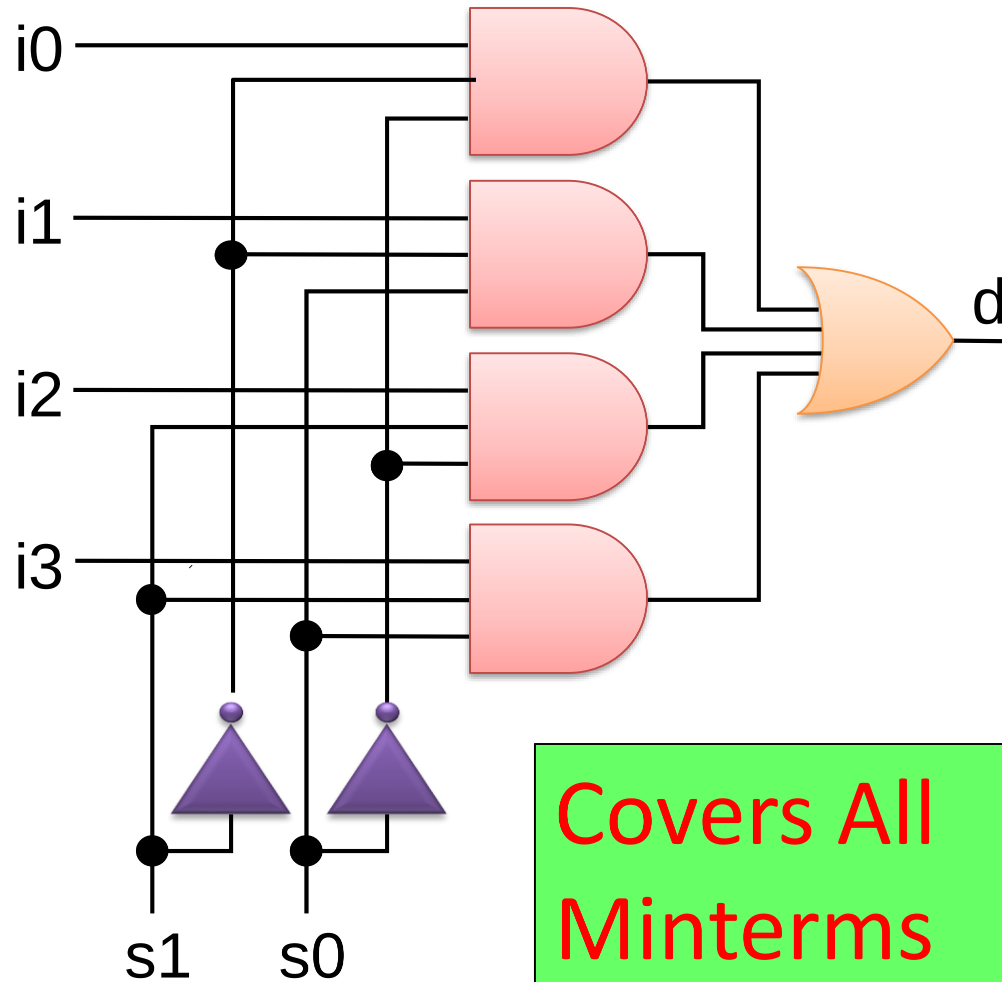


FPGA:-
Field Programmable Gate Array

Multiplexor (Mux)

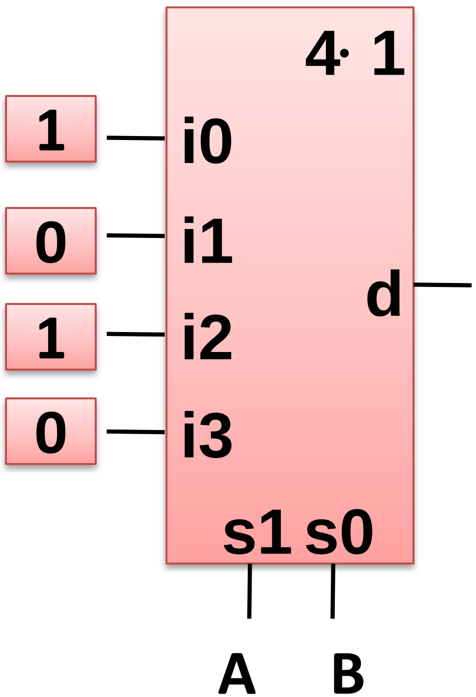


4x1 mux



Covers All Minterms

Implementing logic Function using MUX



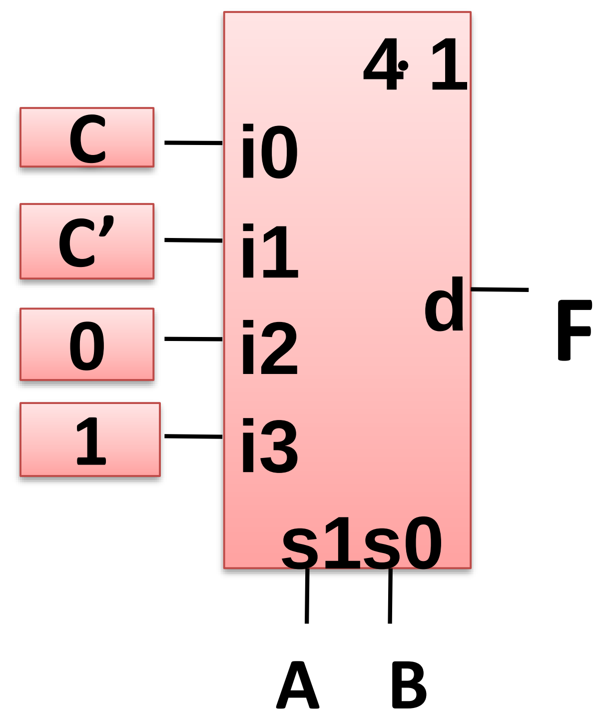
$F\ (A, B) = \sum m(0,2)$

4x1 mux

Implementing 3 Inputs Logic Function using 4x1 MUX

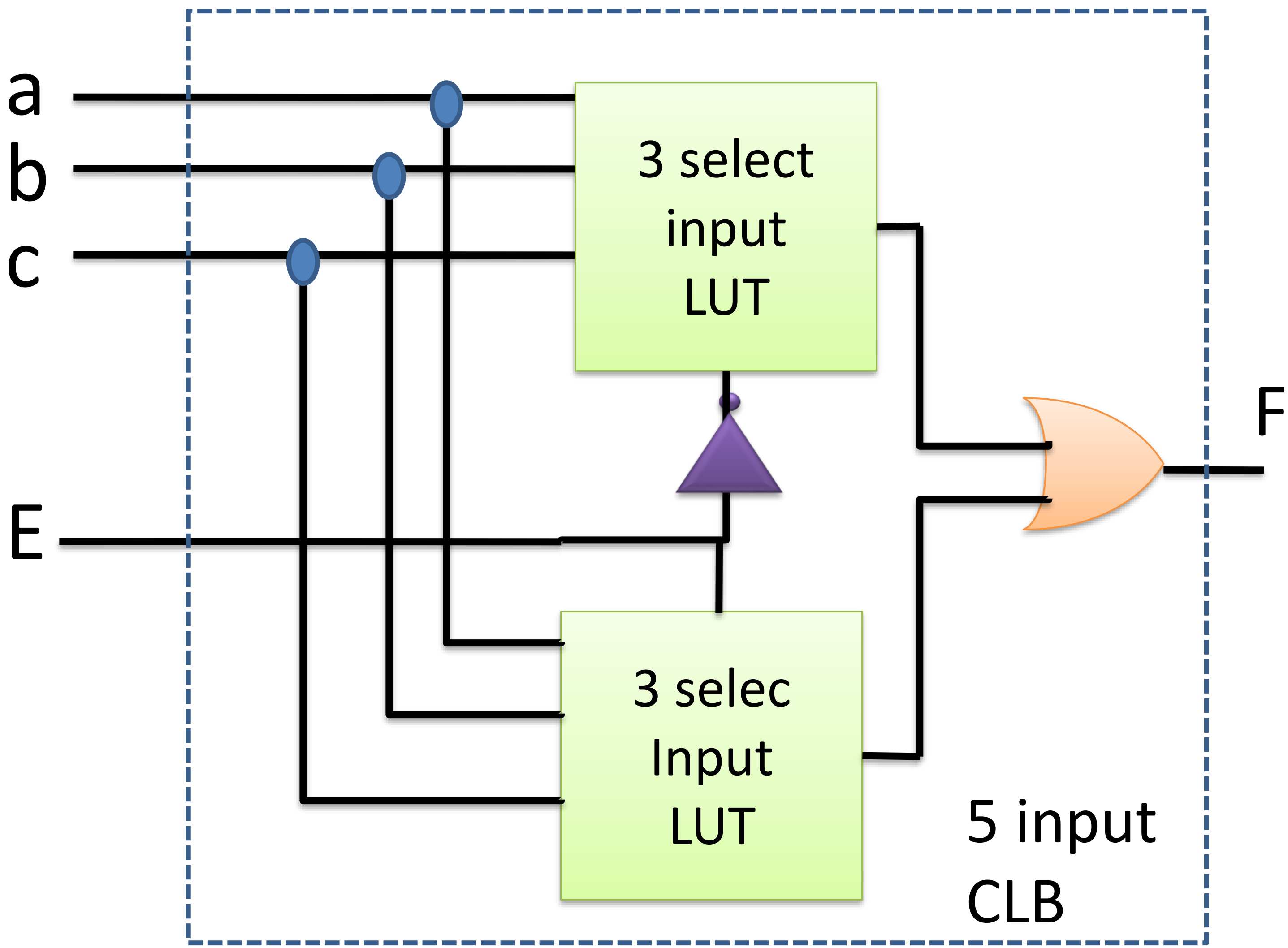
$F\ (A, B, C) = \sum m(1,2,6,7)$

A	B	C	F	F
0 0	0 0	0 1	0 1	C
0 0	1 1	0 1	1 0	C’
1 1	0 0	0 1	0 0	0
1 1	1 1	0 1	1 1	1

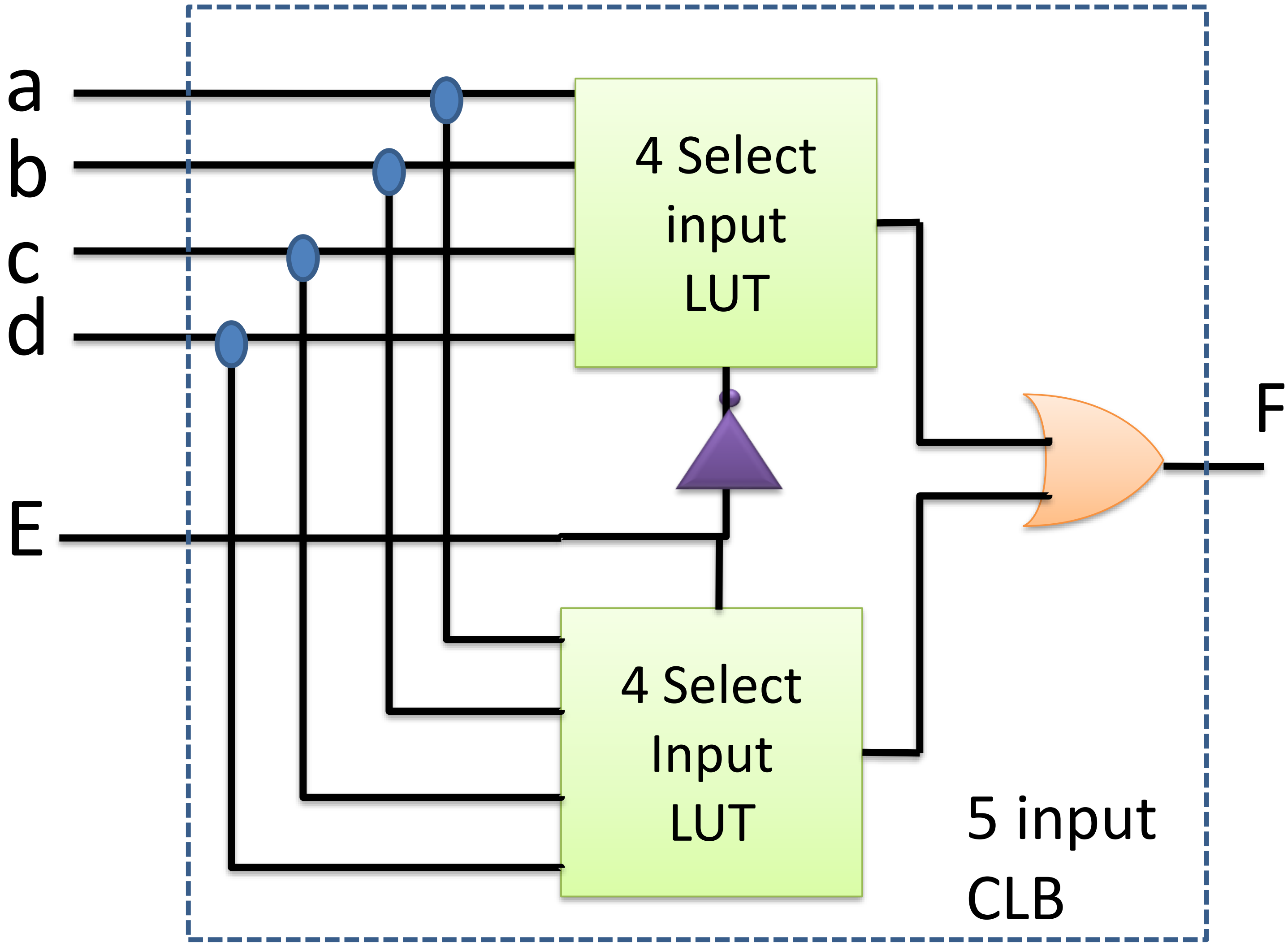


4x1 mux

Implementing 4 Inputs Logic Function using two 8x1 MUX



Implementing 5 Inputs Logic Function using two 16x1 MUX



Shannon's expansion theorem

Used to implement many variable logic functions using MUX and LUTs

f(x1, x2, …, xn) = x1 f(0, x2, .., xn) + x1 f(1, x2, …, xn)

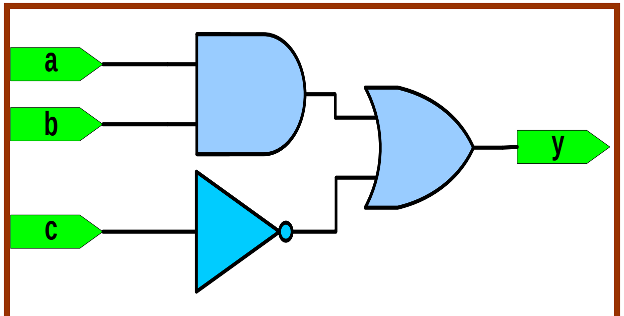
Since x1 is a boolean variable, we need to look at only two cases: x1 = 0 and x1 = 1.

- Setting x1 = 0 in the above expression, we have:
  - f(0, x2, …, xn)   = 1 f(0, x2, …, xn) + 0 f(1, x2, …, xn)
    = f(0, x2, …, xn)
- Setting x1 = 1, we have:
  - f(1, x2, …, xn)   =0 f(0, x2, …, xn) + 1 f(1, x2, …, xn)
    = f(1; x2; …; xn)

LUT: Look up Table

- LUT is a RAM with data width of 1bit.
- The contents are programmed at power up

Required Function

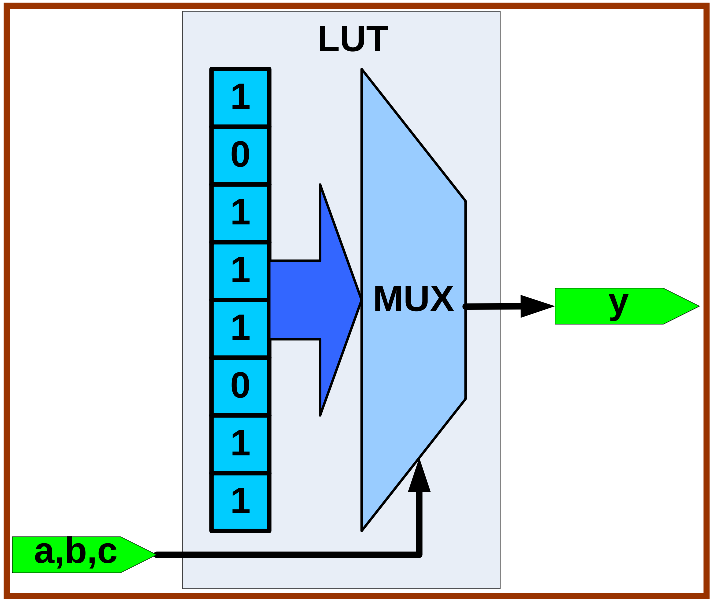


$$y = a \bullet b + \overline{c}$$

Truth Table

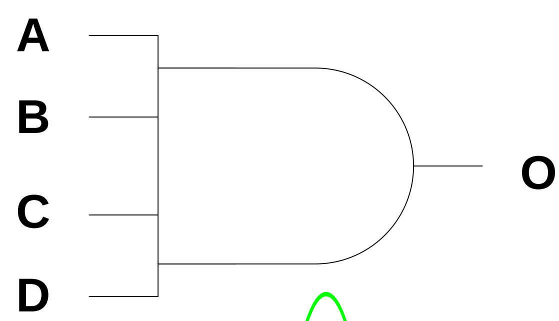
a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

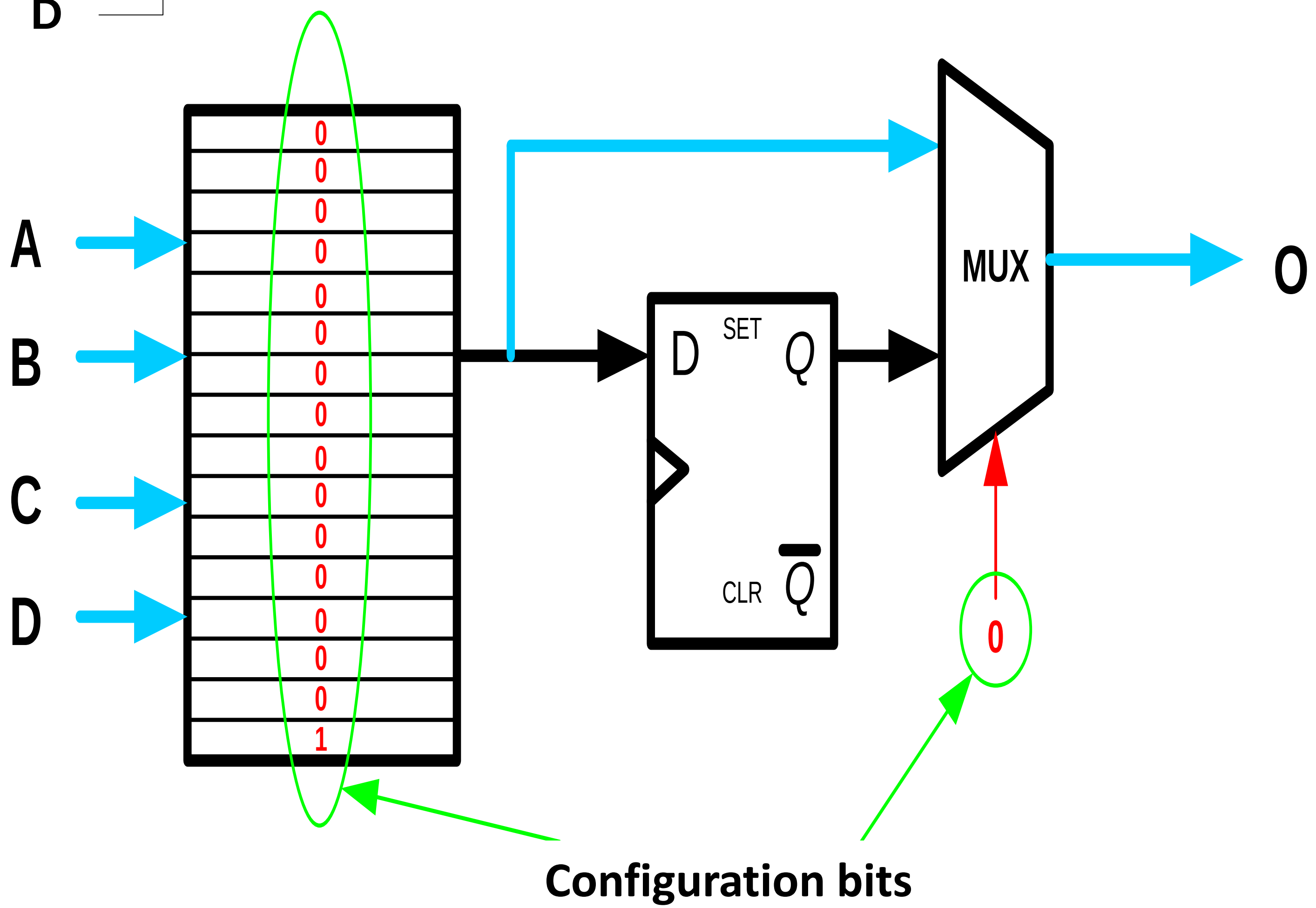
Programmed LUT



Example: 4-input AND gate

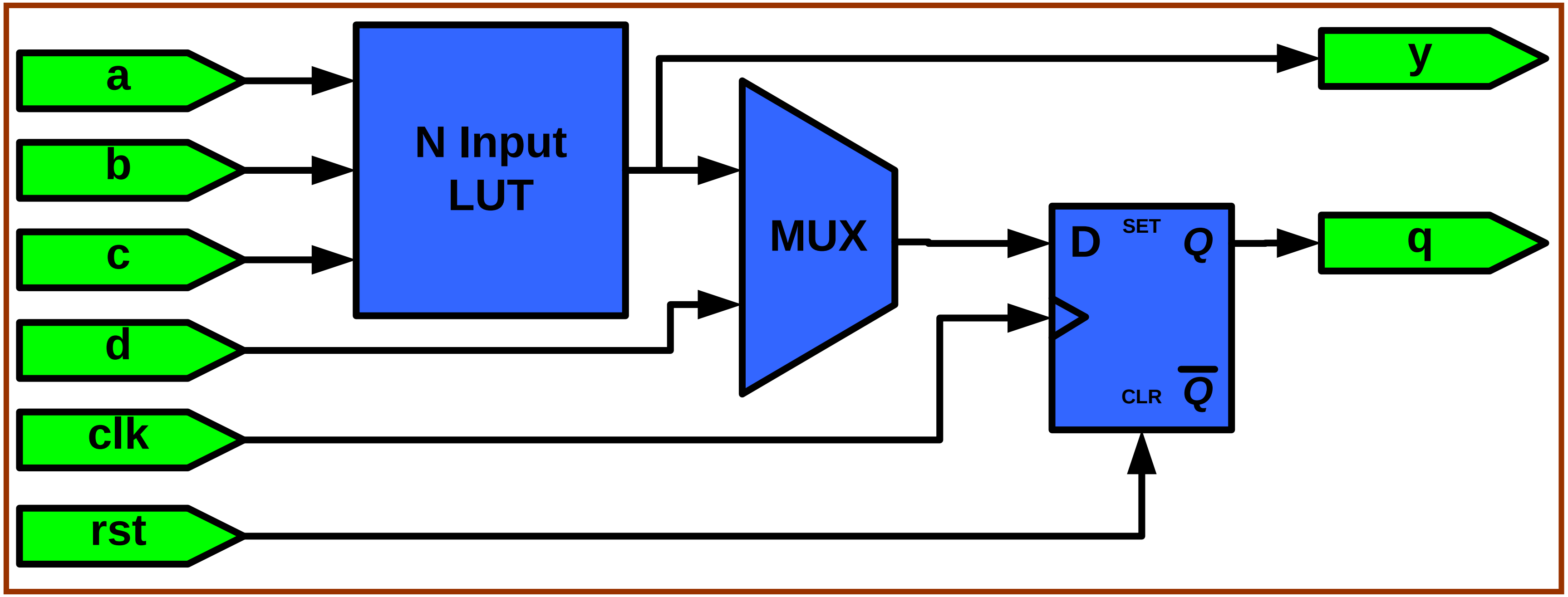
A	B	C	D	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1





FPGA - Field Programmable Gate Array

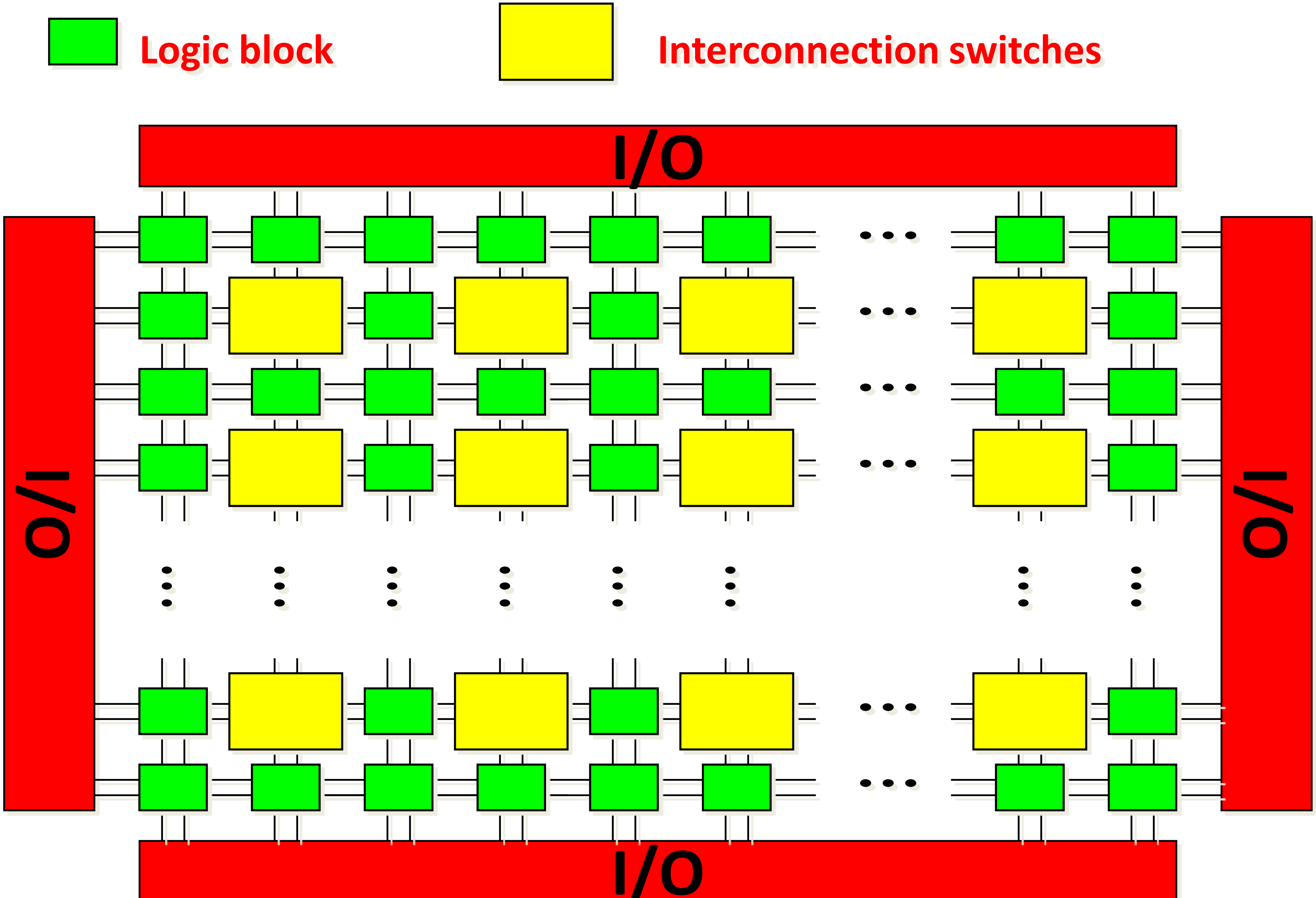
- Programmable logic blocks or CLB
  - (Logic Element “LE”)
  - Implement combinatorial and sequential logic. Based on LUT and DFF.



FPGA - Field Programmable Gate Array

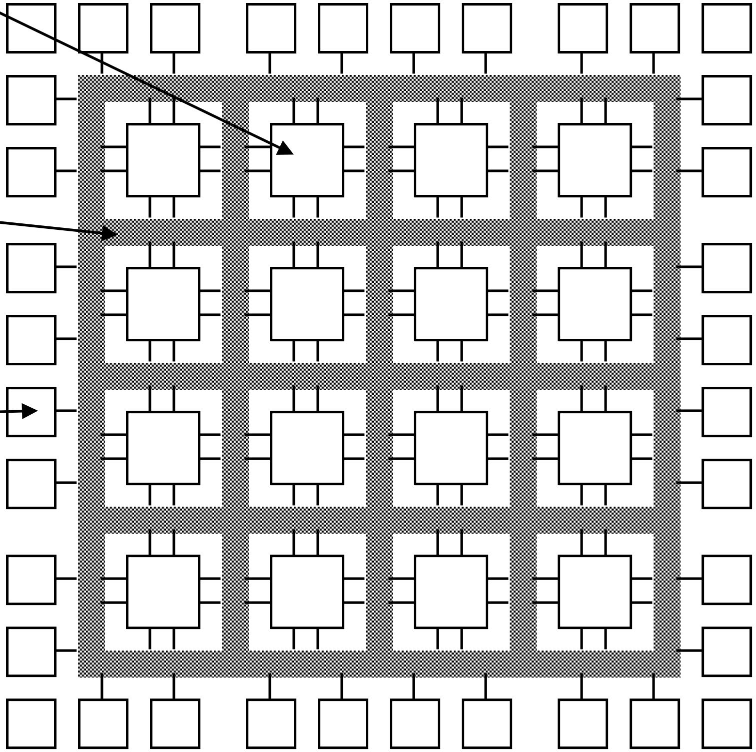
- Programmable logic blocks (Logic Element "LE") or CLB
  - Implement combinatorial and sequential logic. Based on LUT and DFF.
- Programmable I/O blocks
  - Configurable I/Os for external connections supports various voltages and tri-states.
- Programmable interconnect
  - Wires to connect inputs , outputs and logic blocks.
  - Clocks
  - short distance local connections
  - long distance connections across chip

FPGA - Field Programmable Gate Array



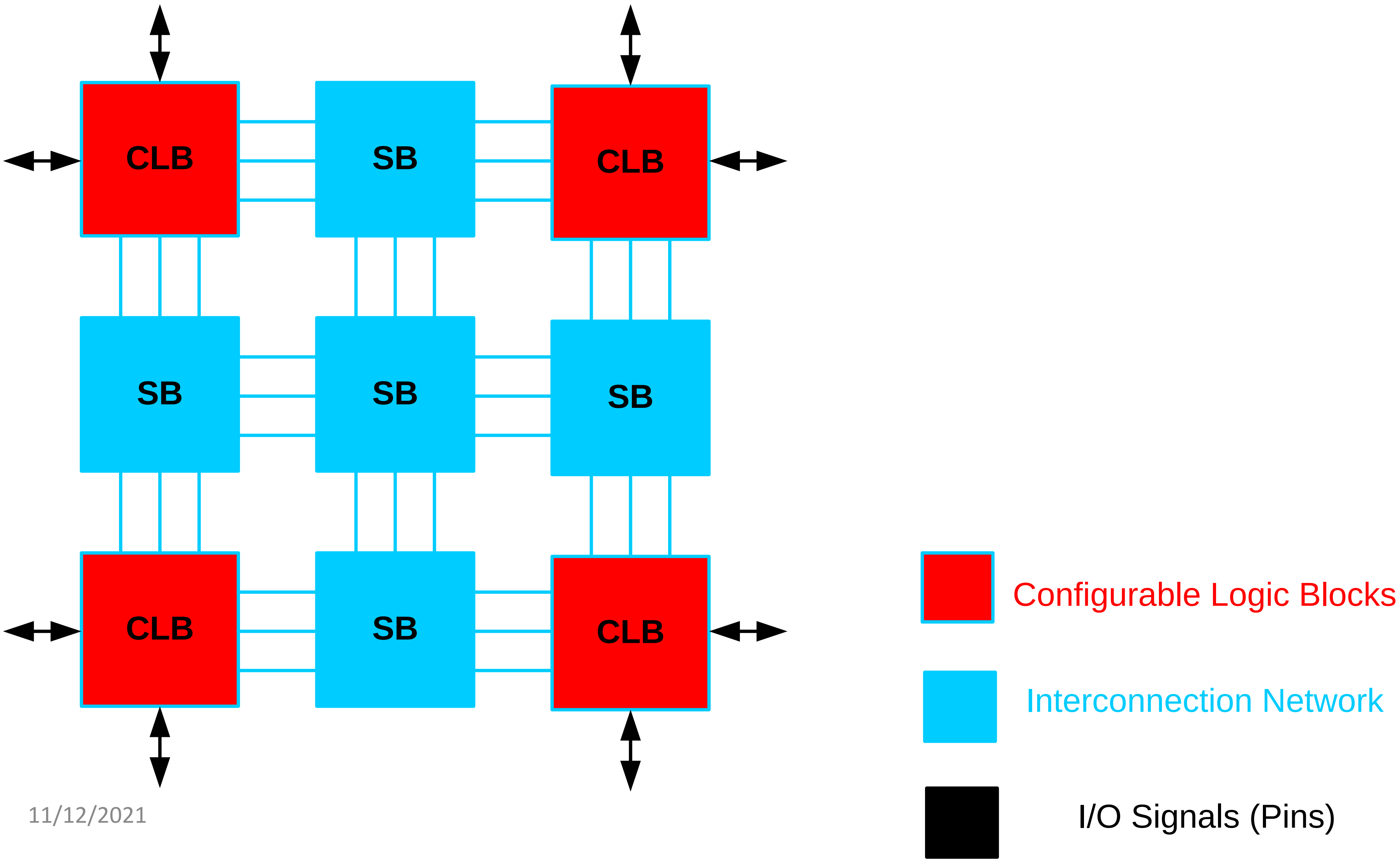
Field-Programmable Gate Arrays structure

- **Logic blocks**
  - To implement combinational and sequential logic
- **Interconnect**
  - Wires to connect inputs and outputs to logic blocks
- **I/O blocks**
  - Special logic blocks at periphery of device for external connections

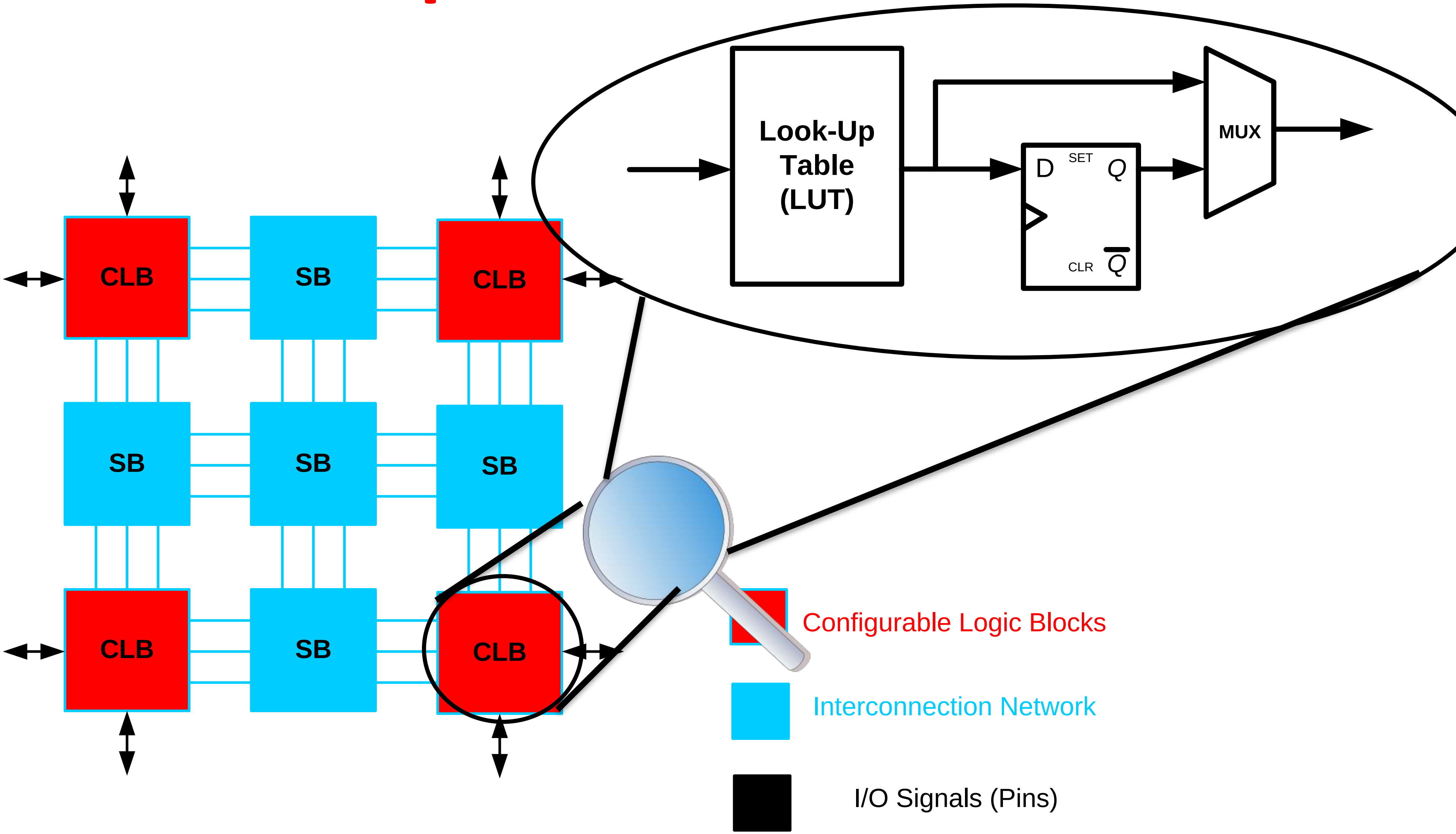


- **Key questions:**
  - How to make logic blocks programmable?
  - How to connect the wires?

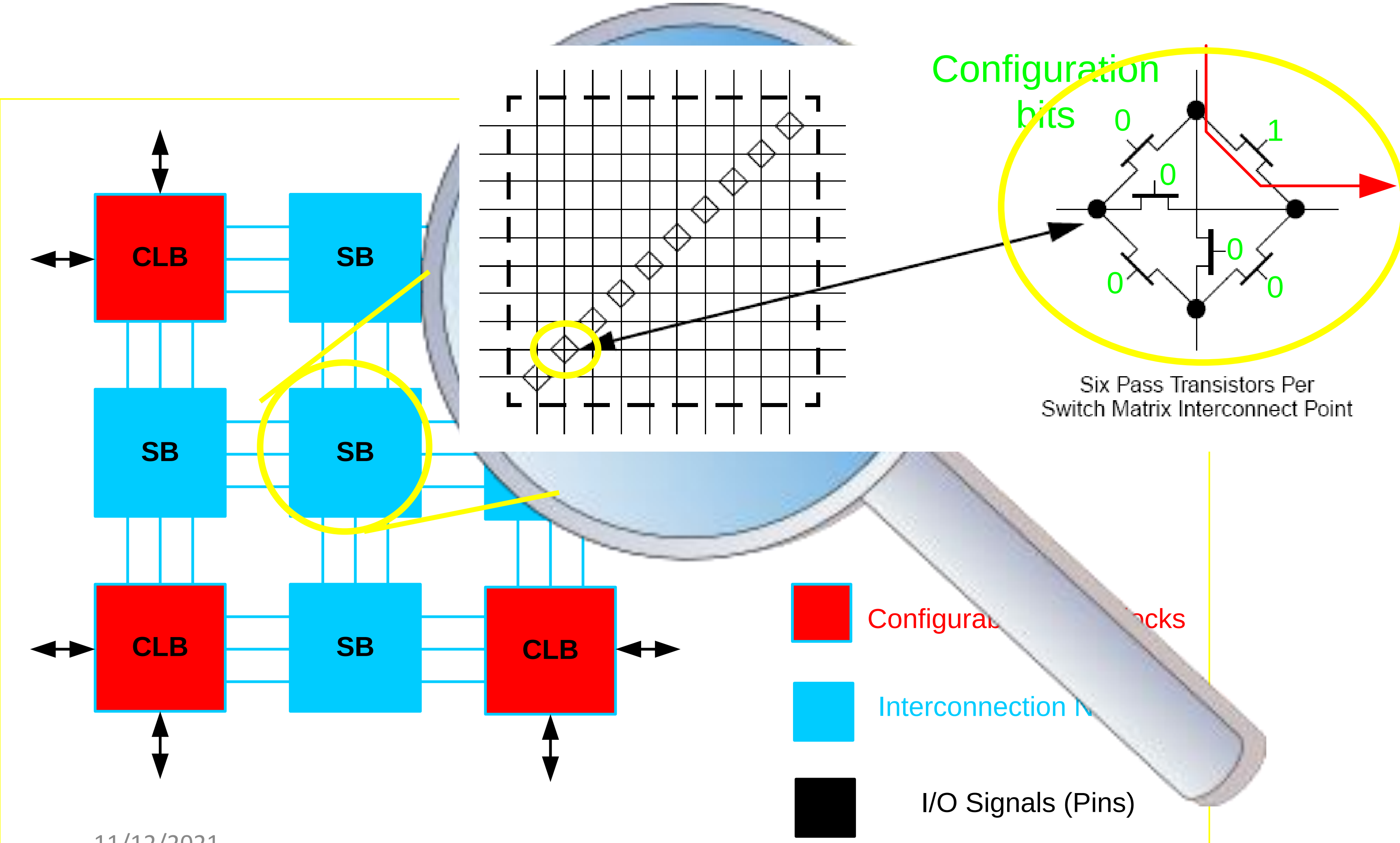
FPGA structure



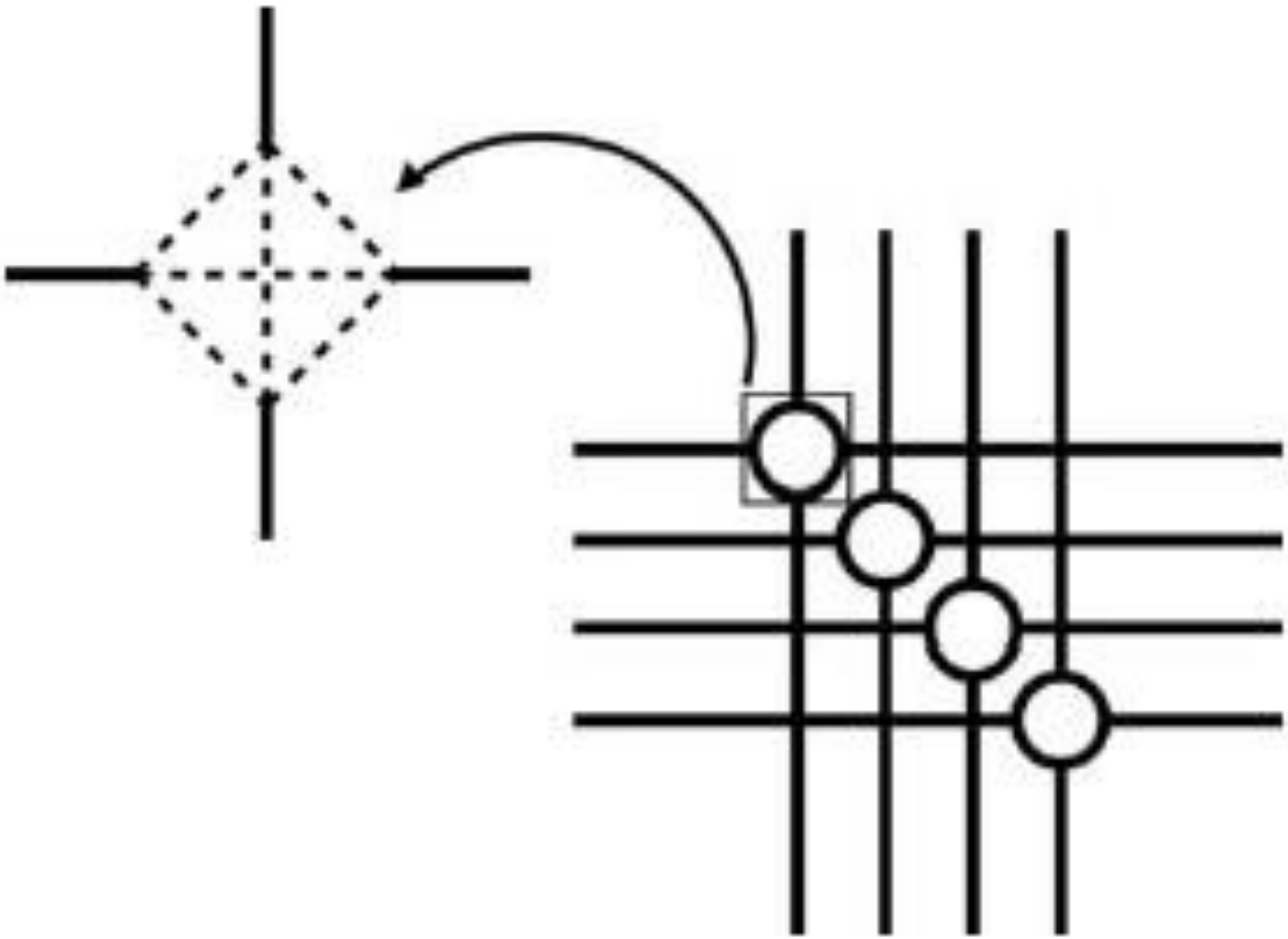
Simplified CLB Structure



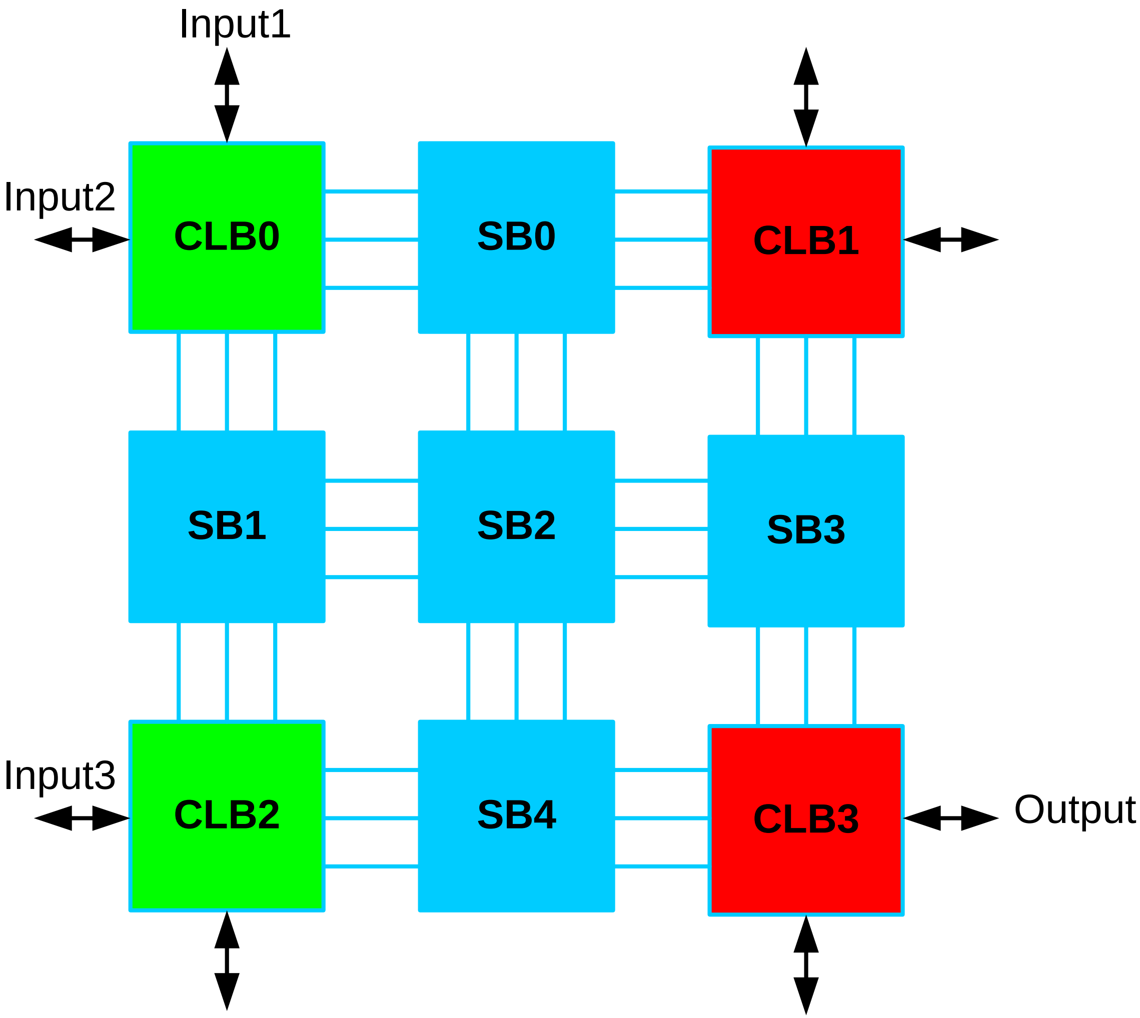
Interconnection Network



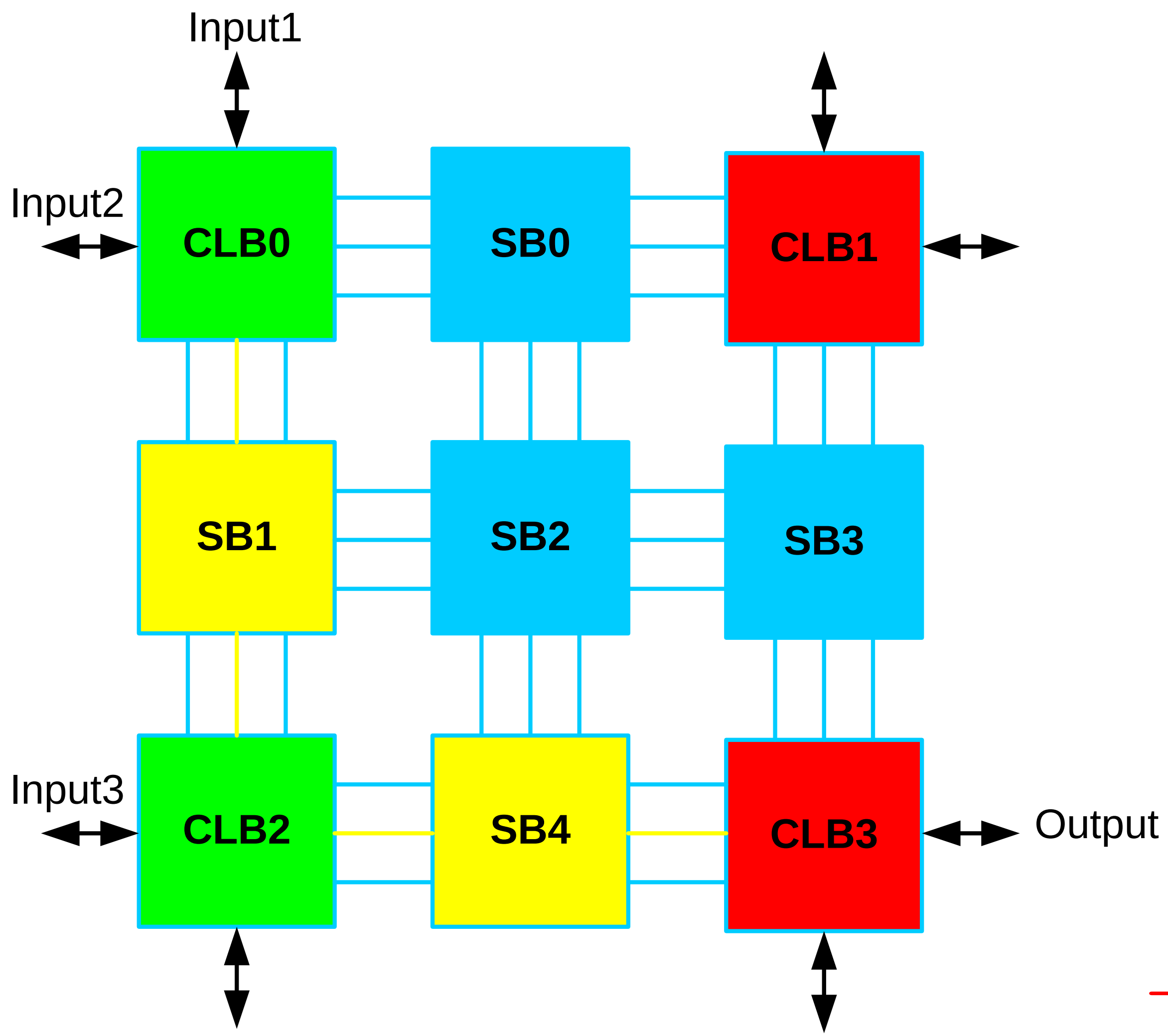
Configurable Interconnect

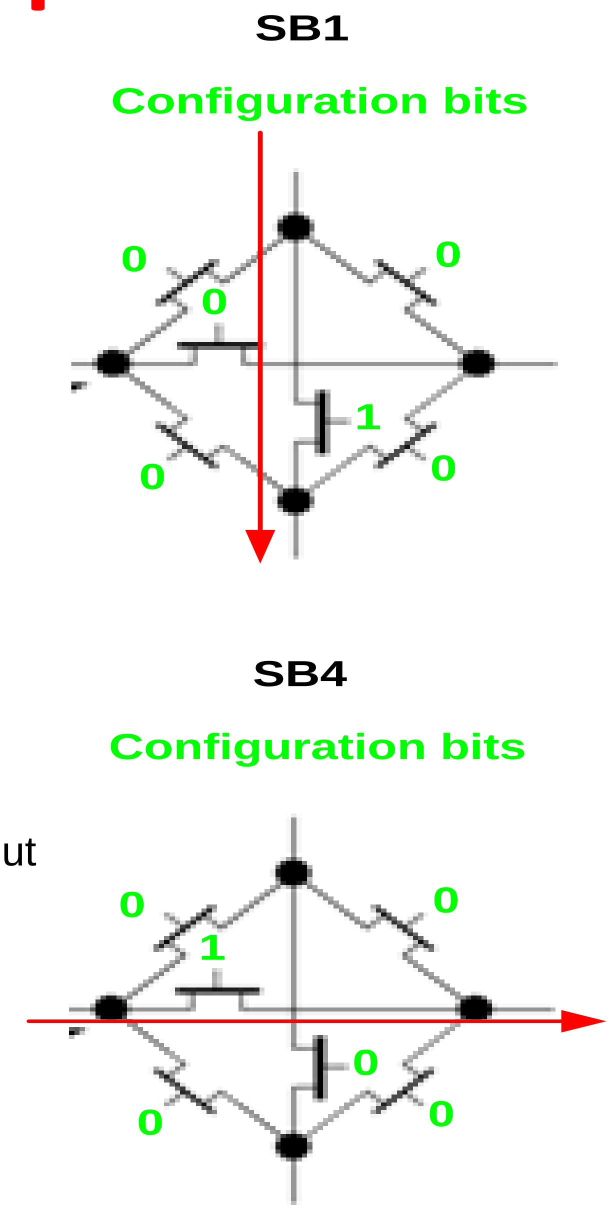


Placement: Select CLBs



Routing: Select path





FPGA Advantages

- **Designing with FPGA: Faster, Cheaper**
- **Ideal for customized designs**
  - Product differentiation in a fast-changing market
- **Offer the advantages of high integration**
  - High complexity, density, reliability
  - Low cost, power consumption, small phy. size
- **Avoid the problems of ASICs**
  - high NRE cost, long delay in design and testing
  - increasingly demanding electrical issues

FPGA Advantages

- **Very fast custom logic**
  - massively parallel operation
- **Faster than micro-controllers/and processors**
  - much faster than DSP engines
- **More flexible than dedicated chipsets**
  - allows unlimited product differentiation
- **More affordable and less risky than ASICs**
  - no NRE, min order size, or inventory risk
- **Reprogrammable at any time**
  - in design, in manufacturing, after installation

User Expectations

- **Logic capacity at reasonable cost**
  - 100,000 to a several million gates
  - On-chip fast RAM
- **Clock speed**
  - 150 MHz and above, global clocks, clock management
- **Versatile I/O**
  - To accommodate a variety of standards
- **Design effort and time**
  - synthesis, fast compile times, tested and proven cores
- **Power consumption**
  - must stay within reasonable limits

Field Programmable Device

- **Basic Section of FPD:**
  - Logical Block
  - Routing (Switch Matrix)
  - Input Output Block
- **More Advanced FPD Contains:**
  - On-chip Memory
  - Embedded Processor
  - Clock Management
  - High-Speed Transceiver

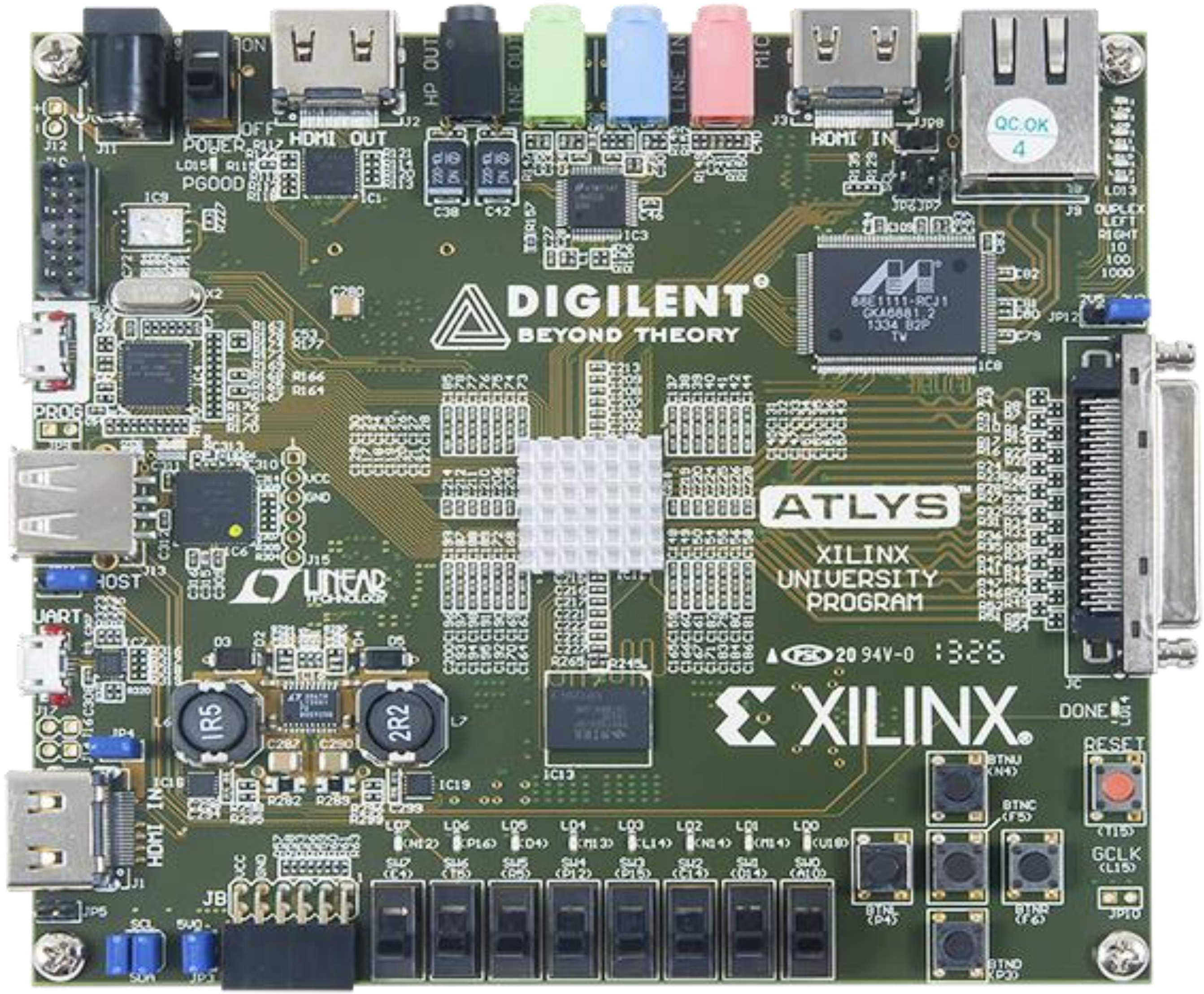
Special FPGA functions

- Internal SRAM
- Embedded Multipliers and DSP blocks
- Embedded logic analyzer
- **Embedded CPUs**
- High speed I/O (~10GHz)
- DDR/DDRII/DDRIII SDRAM interfaces
- PLLs

Digilent Xilinx Atlys FPGA Board

- Xilinx Spartan-6 LX45 FPGA,
- 6,822 slices : four 6-input LUTs and eight flip-flops
- 2.1Mbits of block RAM, 128 MB DDR2
- 58 DSP slices
- JTAG programming , RJ-45 Ethernet port
- 4 HDMI video ports
- AC-97 Audio Codec mic, & headphone
- Two on-board USB2
- USB-UART and USB-HID port
- GPIO includes 8 LEDs, 6 buttons, and 8 slide switches

Digilent Xilinx Atlys FPGA Board



Digilent Xilinx Basys 3 FPGA Board

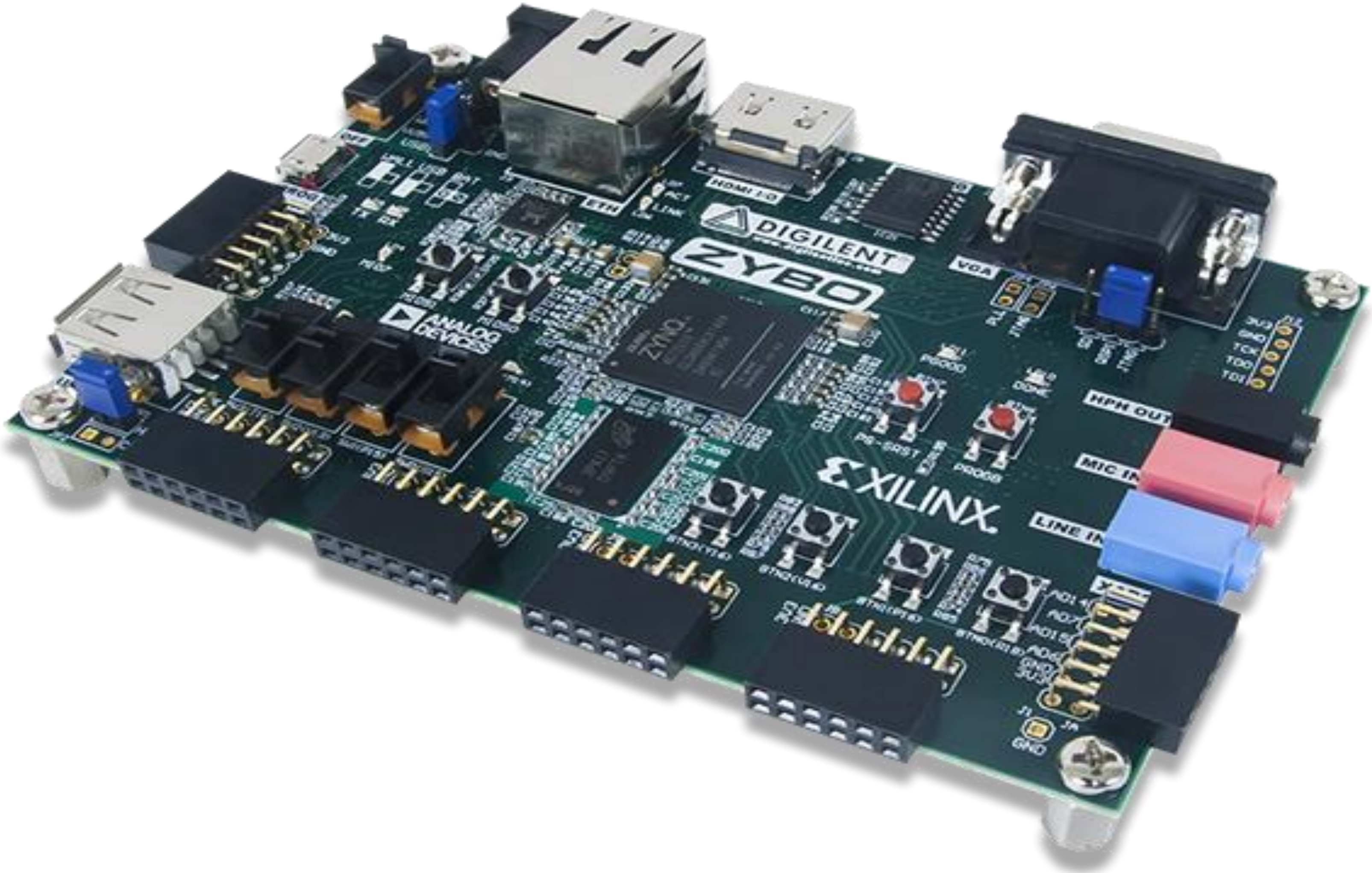
- Xilinx Artix-7 FPGA
- 33,280 logic cells in 5200 slices (four 6-input LUTs and 8 flip-flops)
  1,800 Kbits of fast block RAM
- 90 DSP slices
- ADC, USB-JTAG port, USB-UART Bridge , 12-bit VGA output
- USB HID Host for mice, keyboards
- 16 user switches, 16 user LEDs, 5 user pushbuttons , 4-digit 7-segment display

Digilent Xilinx Basys 3 FPGA Board

Digilent Xilinx Zybo FPGA Board

- Xilinx Zynq-7000 (XC7Z010-1CLG400C)
- 28,000 logic cells
- 240 KB Block RAM
- 80 DSP slices , Dual channel, 12-bit, ADC
- **650 MHz dual-core Cortex™-A9 processor**
- JTAG programming and UART to USB converter
- 1G Ethernet, USB 2.0, SDIO, SPI, UART, I2C
- Dual-role HDMI port , VGA port, Ethernet PHY
- OTG USB 2.0 PHY (supports host and device)
- GPIO: 6 pushbuttons, 4 slide switches, 5 LEDs

Digilent Xilinx ZYBO FPGA Board



FPGA Design flow