CS221: Digital Design

Digital Counter

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Outline

- Counter
- Asynchronous or Ripple Counter
  - Binary
  - Modulo Counter : Count decimal 000 to 999
- Synchronous counter
  - Binary , Modulo, Up-Down
- Ring Counter, Register based counter
- Case Study: Design of Digital Clock

Counter

- It simply count: 4 bit counter : count 0000 to 1111 & repeat
- Other optional functions and variations
  - Start count at Specific point (say from 5 : 0101)
  - Stop count at Specific point (Say at 9: 1001)
  - Count only even numbers: 0, 2, 4, ..14, 0, 2
  - Count only odd numbers: 1, 3, 5,..15, 1
  - Count specific num in specific order & repeat:

    1, 9, 4, 6, 7, 8. 3, 1, 9 ,4,…

Mostly used 4 bit counter

- Example of 4 bit counter
- Count from 0000 to 1111 and repeat
- Up counter : 0000 to 1111
- Down counter : 1111 to 0000
- Mod N counter:
  - Mod 10 counter : 0000 to 1001 (0 to 9) and repeat (Decimal Number)
  - Mod 6 counter : 000 to 101 (0 to 5) and repeat (Digital Clock 60 second, 60 minutes, 12)

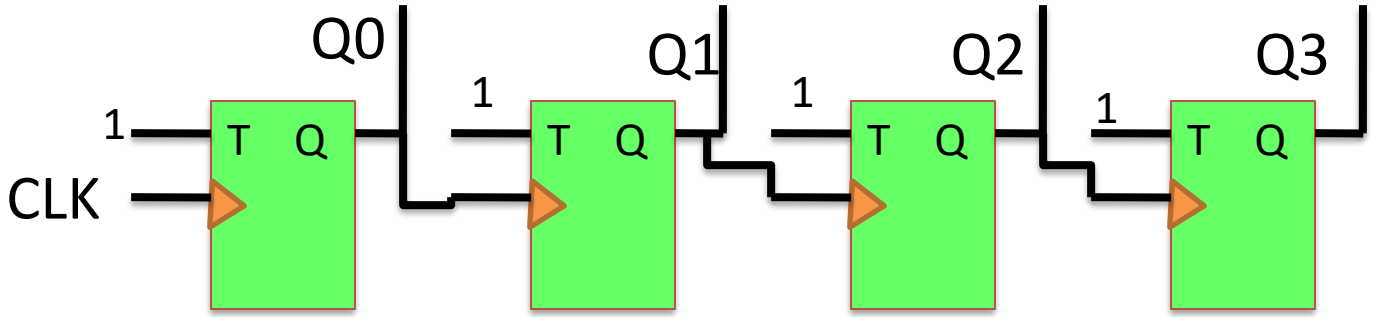
How to design a simple counter

- Q0 change every time
- Q1 change in two time
- Q2 change in every four time
- Q3 changes in every eight time

- Q0, Q1, Q2 and Q3 changes can be modeled
  - Q0 can be modeled using T FF
  - Q1 : in term of Q0 and T FF
  - Q2 : in term of Q1 and T FF…
  - Q3 : in term of Q2 and T FF…

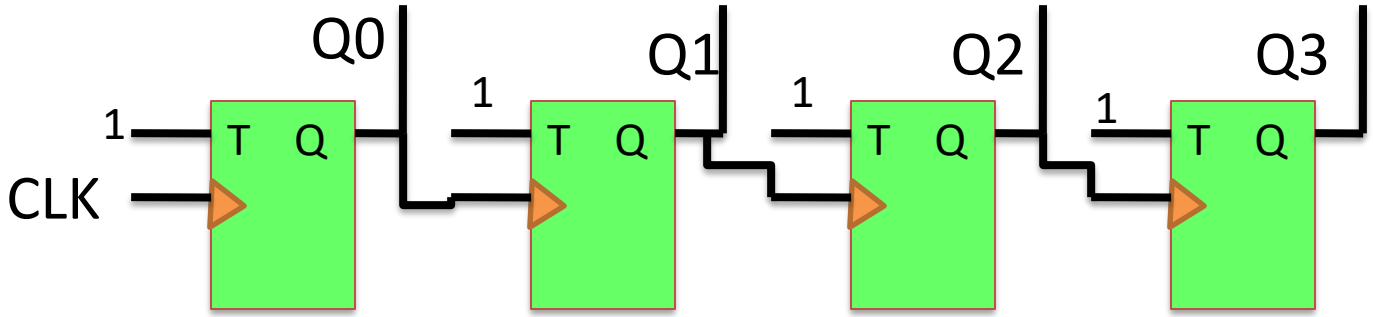
Q3	Q2	Q1	Q0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1

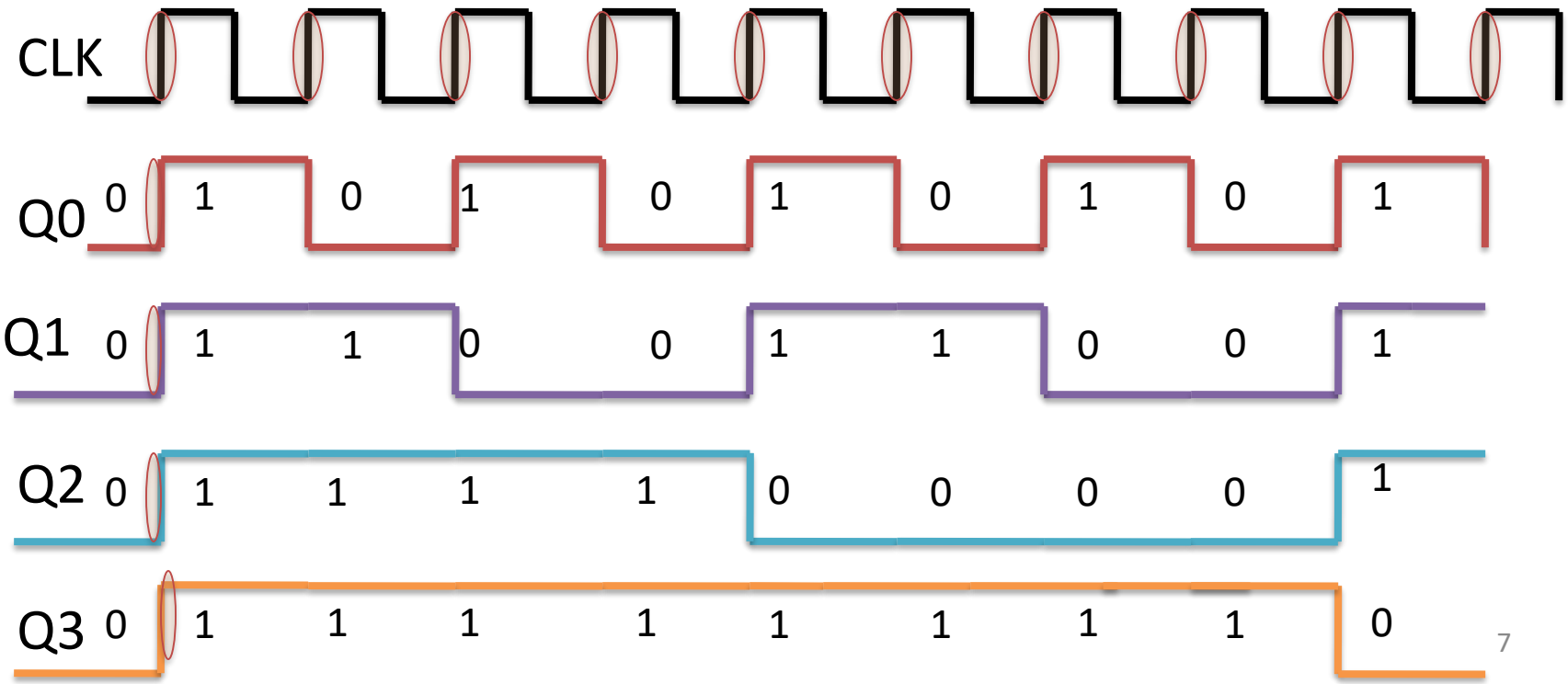
Binary Counter: using T FF



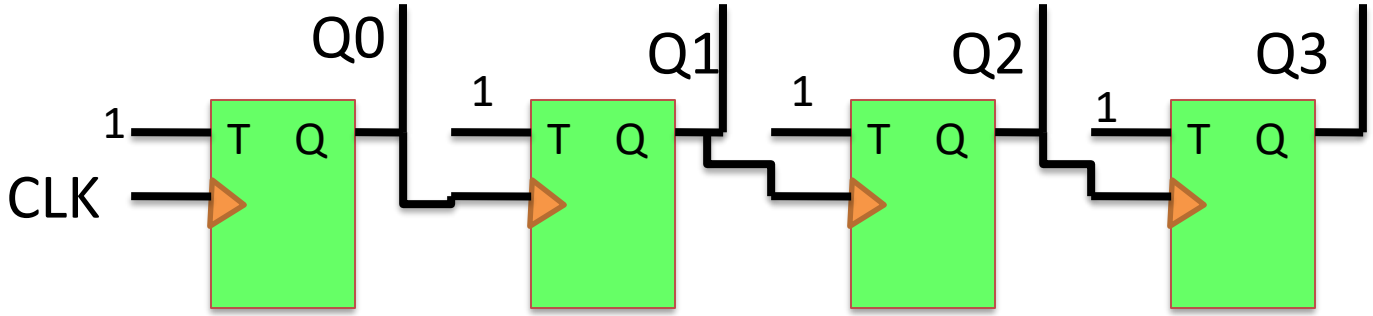
Does this circuit solve our purpose ?

Binary Counter: using T FF



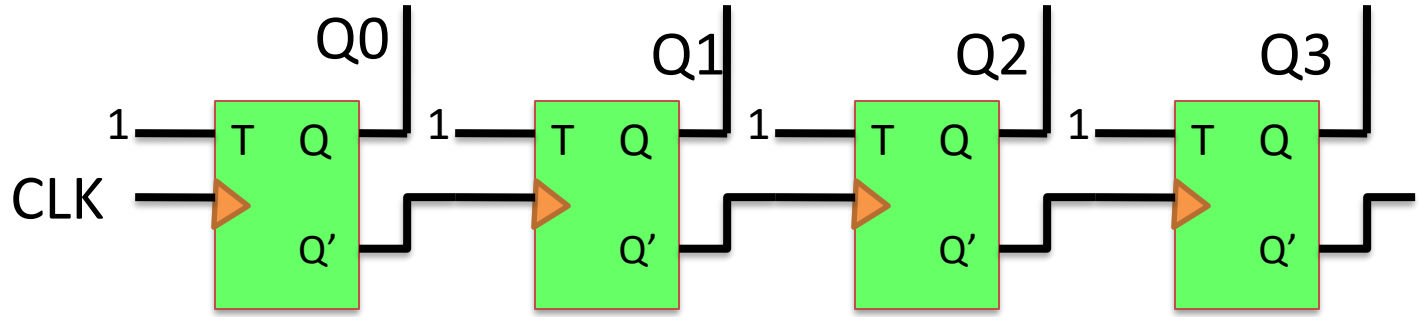


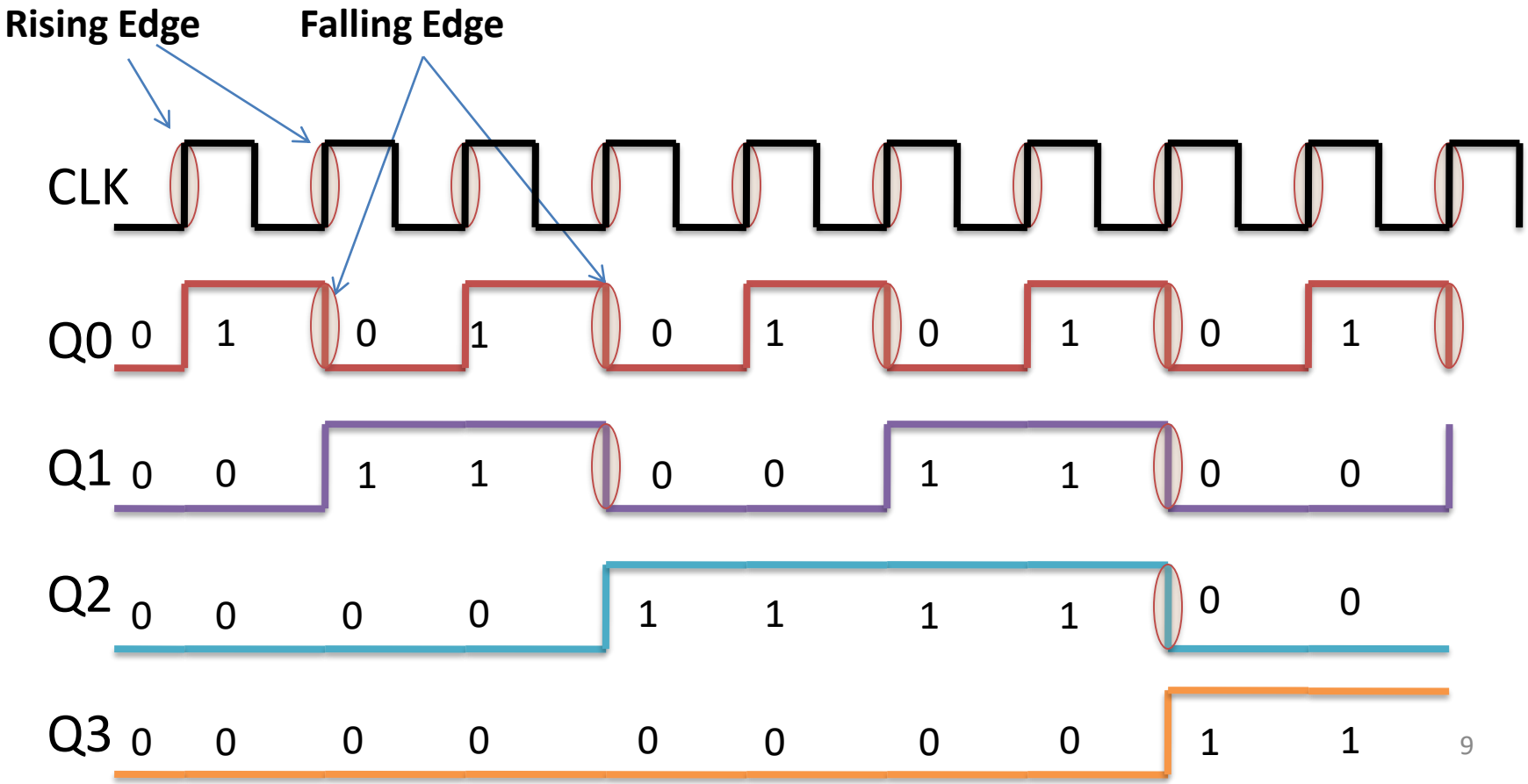
Binary Counter: using T FF



What is the problem with this?

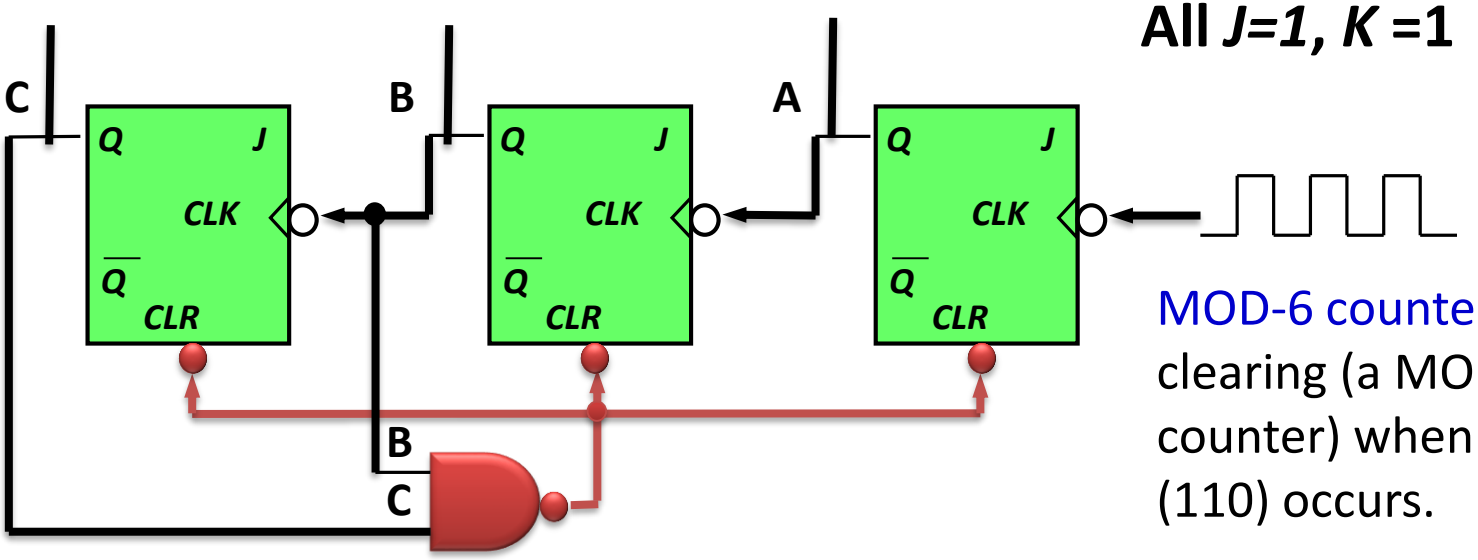
Binary Counter: using T FF



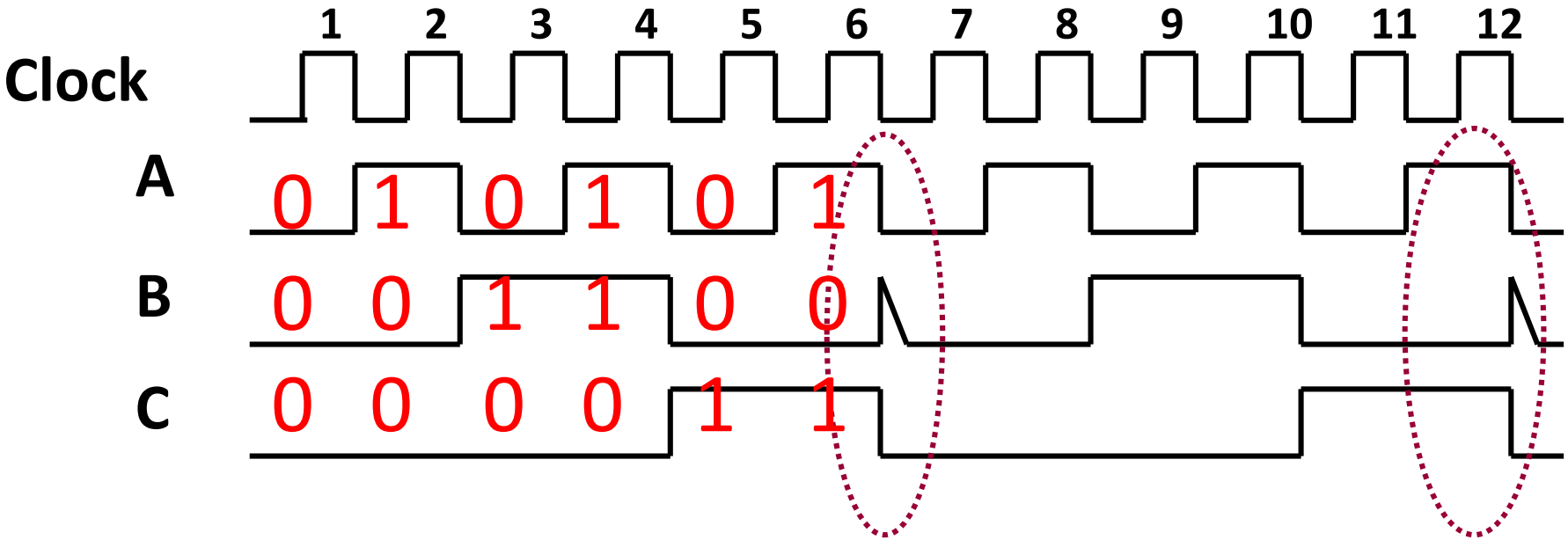


Asyn. Counters with MOD no. < 2^n

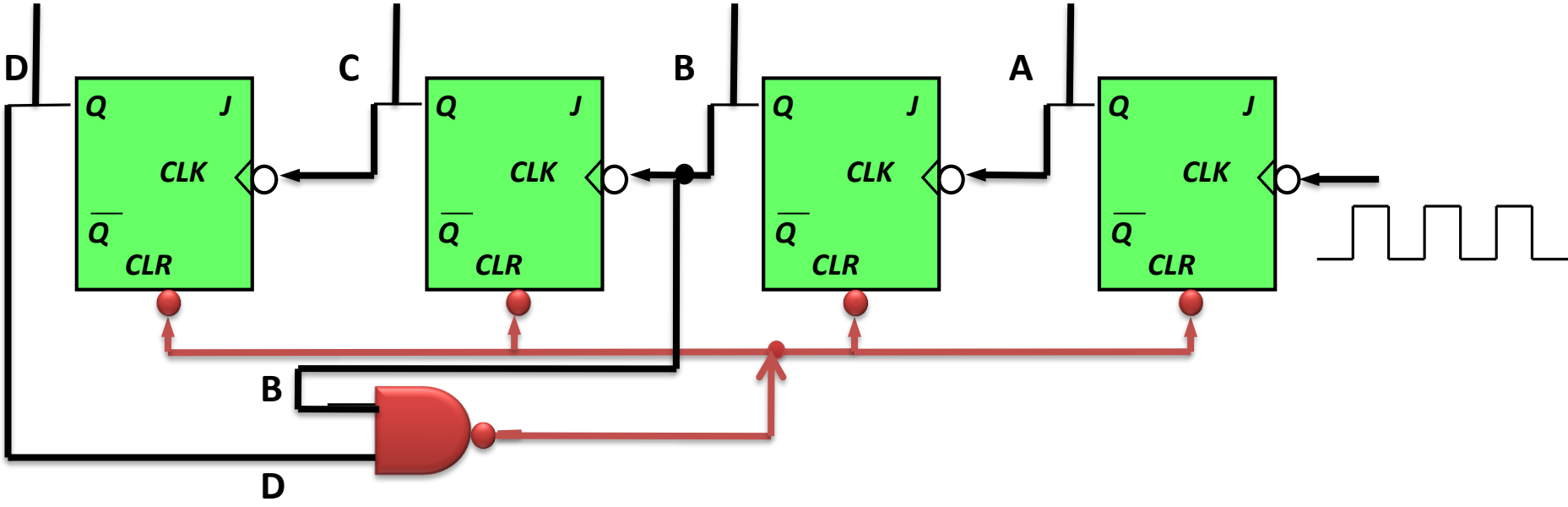
Asyn. Counters with MOD 6



MOD-6 counter produced by clearing (a MOD-8 binary counter) when count of six (110) occurs.



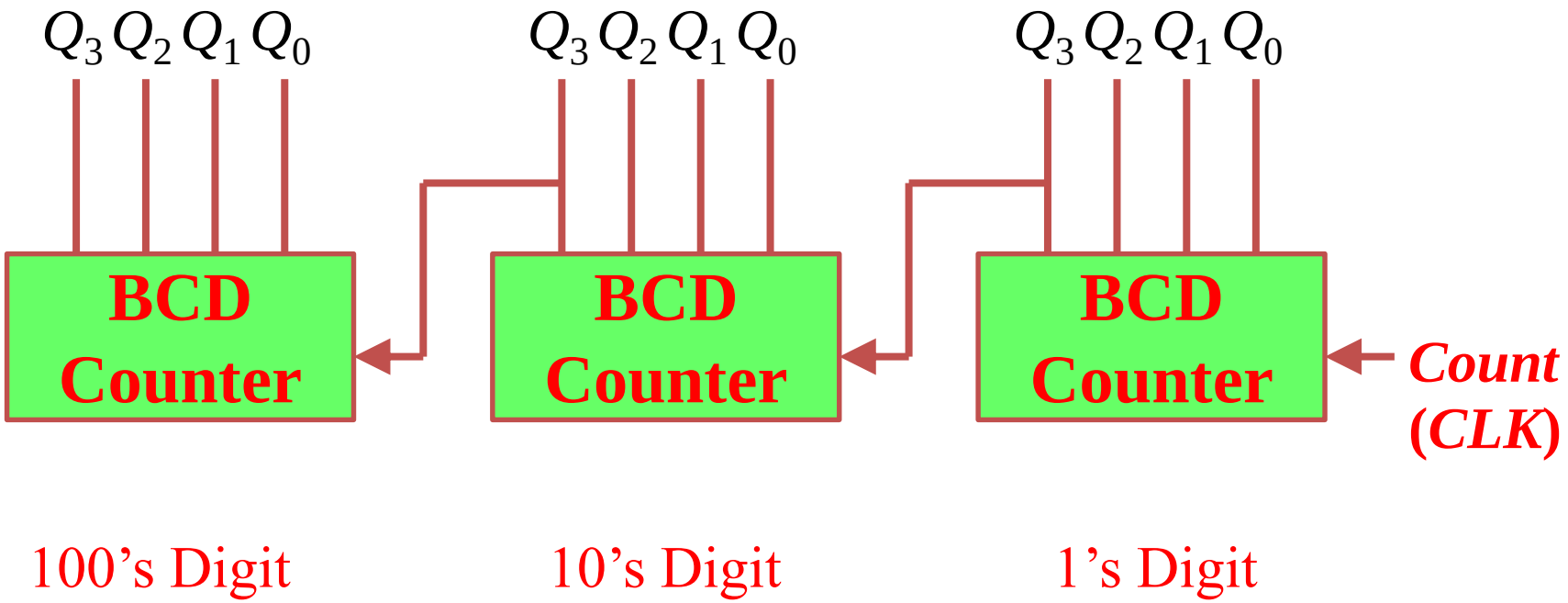
Asyn. Counters with MOD 10: BCD Ctr



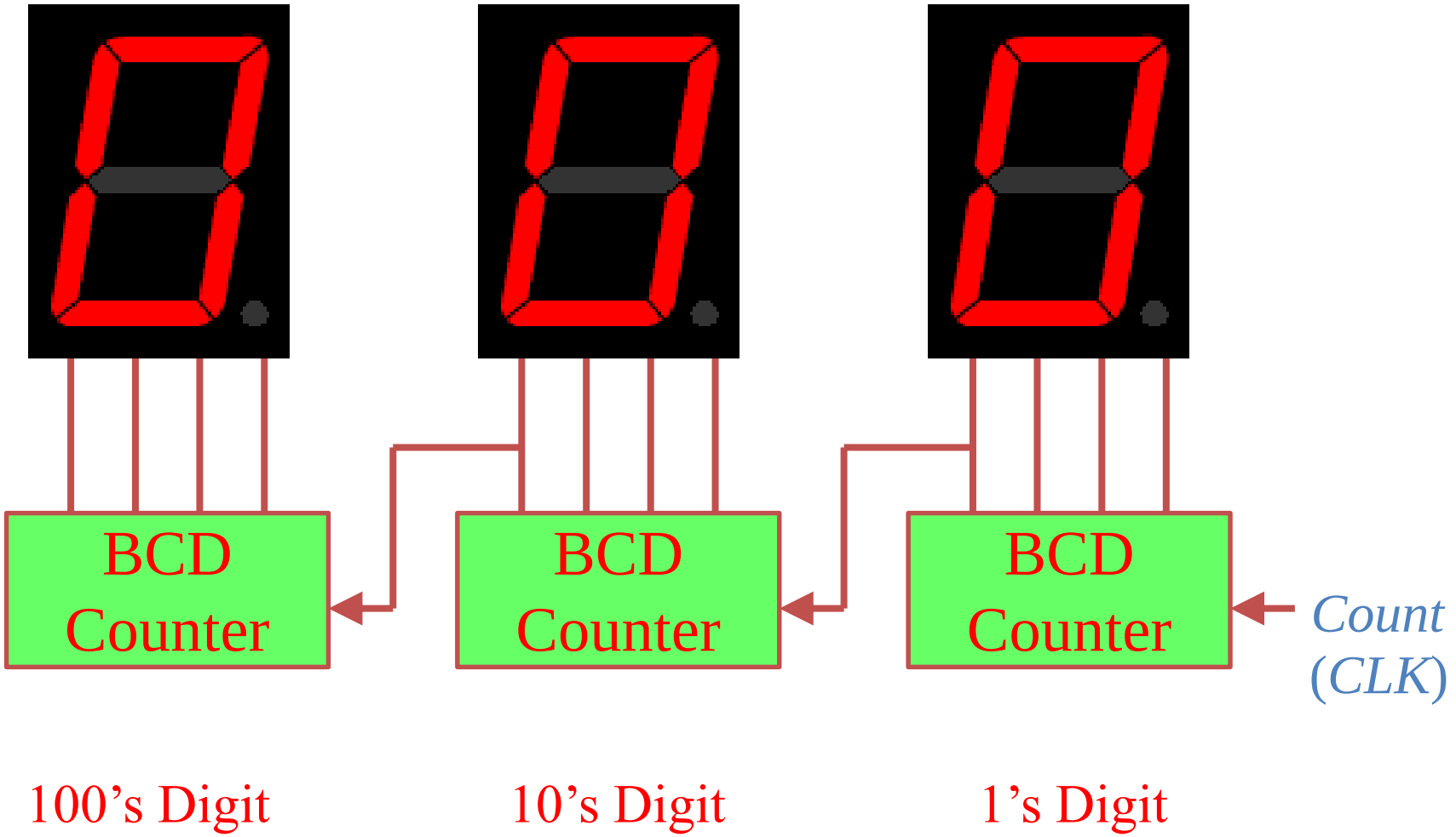
All *J=1*, *K* =1

MOD-10 counter produced by clearing (a MOD-16 binary counter) when count of six (1010) occurs.

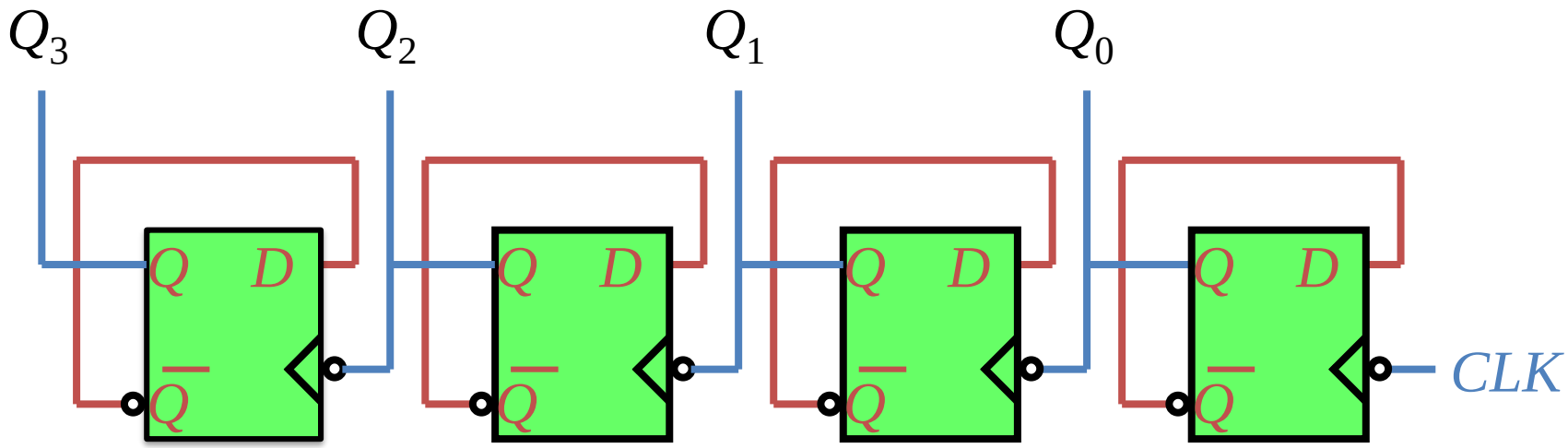
Decade Counter

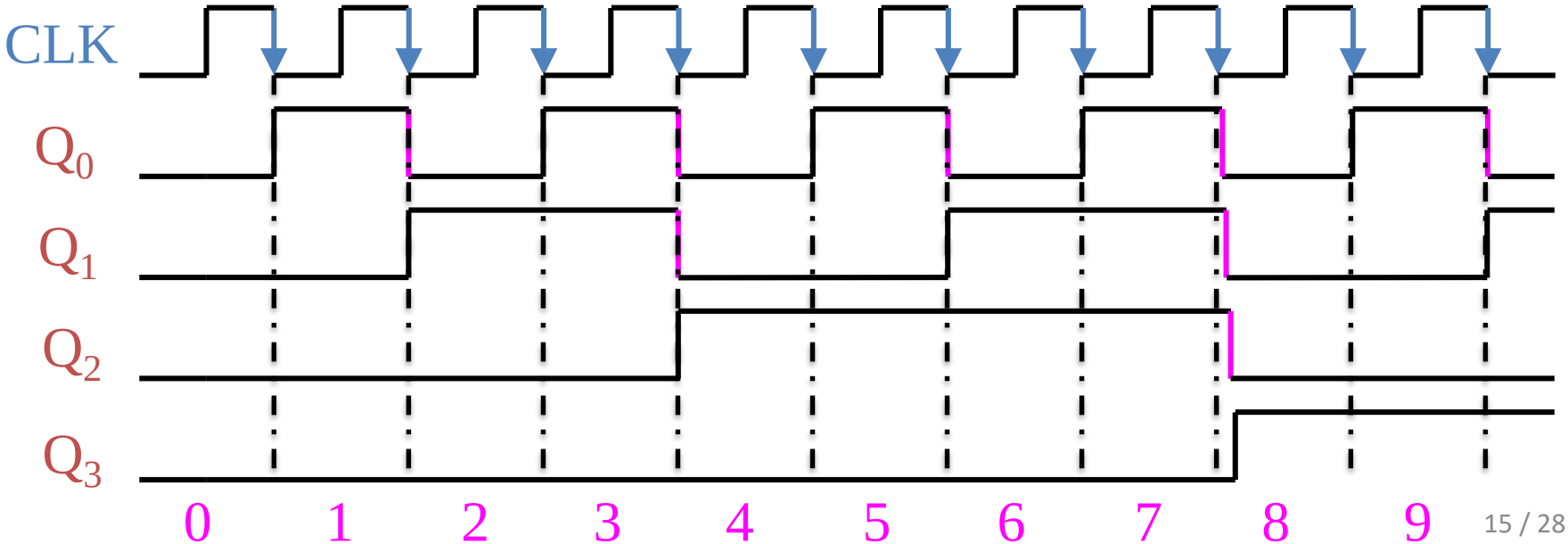


Decade Counter: Interfaced BCDto7Seg Decoder +7Seg



Ripple Counters using D-FFs





Binary Counter: using T FF

- It is very easy to design Ripple counter

Is there any Issue with this ?
If yes, what?

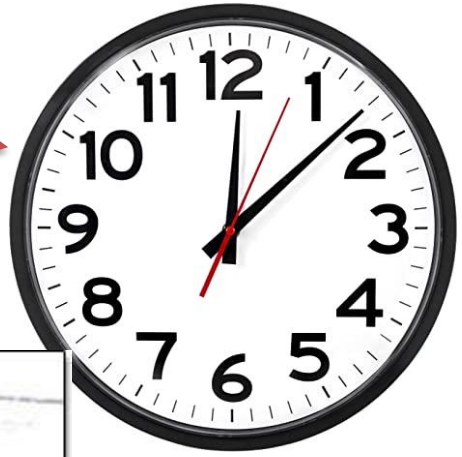
Binary Counter: using T FF

- It is very easy to design Ripple counter

First thing: we should not play **with clock** but make change to the Circuit..

Synchronized and Unsynchronized Classic Example: Clock at Railway Station

- Unsynchronized Analog
- Synchronized Digital Clock



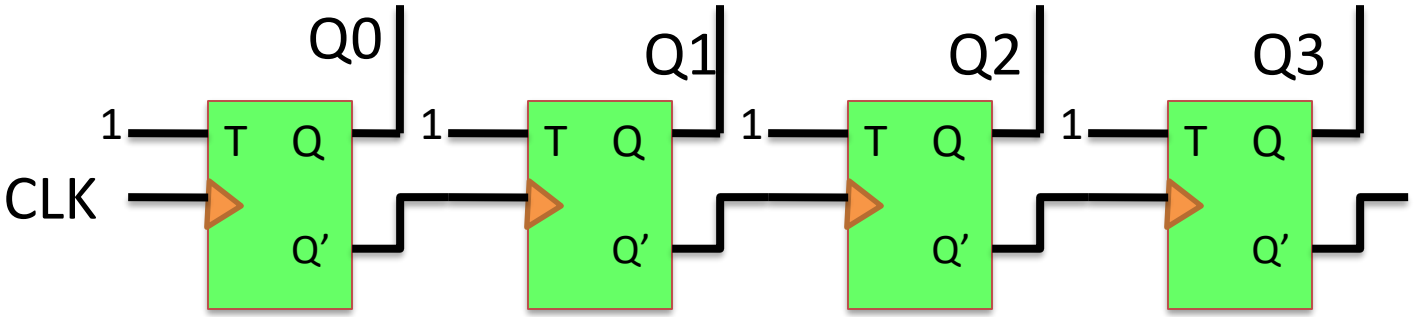
Problem with Ripple Counter

- FFs are not synchronized ☺ ☹
- Even “Wall Clocks” of our examination halls are synchronized now a days.
  - Railway clocks : Synched Clock with Network time
  - NTP : network time protocol
- You can Sync clock of “Smart Mobile” with Network Clock which is in Sync with India Clock and World Clock

Problem with Ripple Counter

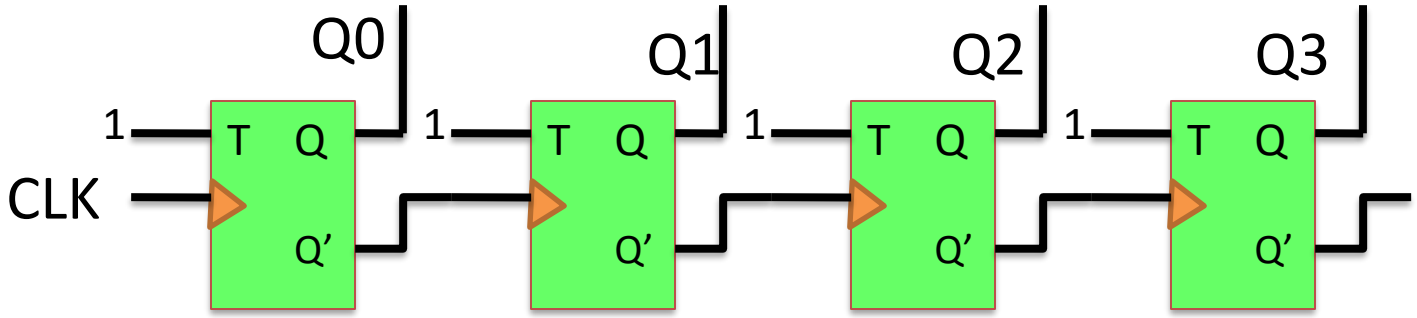
- Student A copies Solution from B with some error, C copies from B with some error and continues..
  - What will be the solution of Z. (=Sol+26*error)
  - Communication Gap
- So, all the FFs should take same clock signal

Ripple Counter : Asynchronous



- Clock is applied at FF0, it propagate through to FFn
- Change in State of Q_{i-1} is used to Toggle Q_i
- Input Clock to FF1= Skewed version of Clk of FF0
  - Clock + Propagation delay of FF

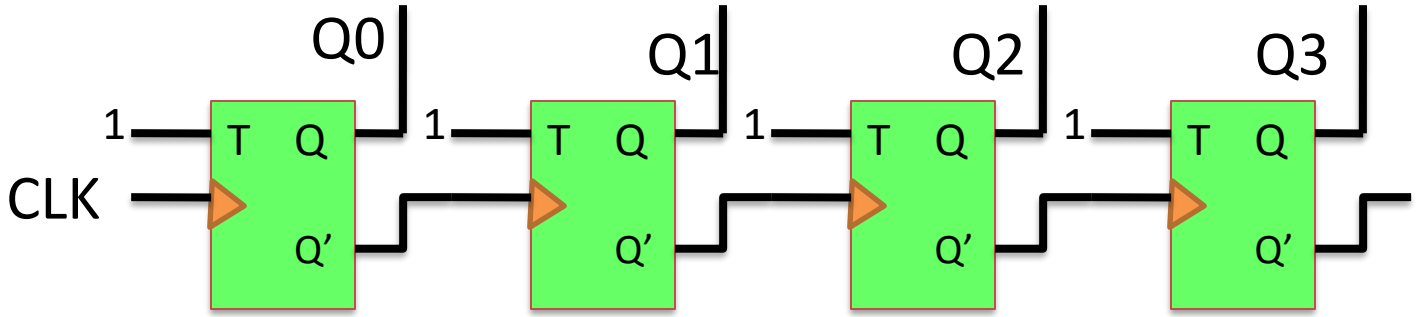
Ripple Counter : Asynchronous

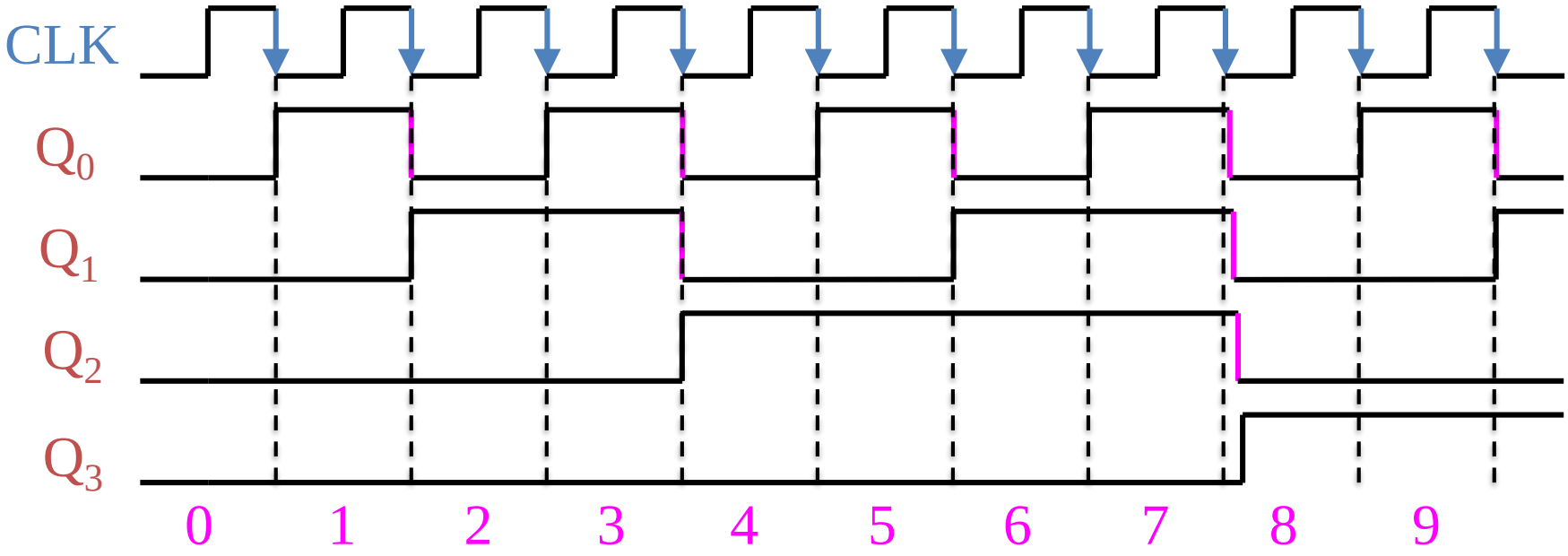


- Rippling : Overall time delay of occurrence of count pulse and when stabilized count appear at O/P
- When counter : 1111..11 to 0000..00, toggle signal must propagate through all FFs
- **Worst case Settling time: $n \times t_{pd}$**

  where t_{pd} =Propagation delay of a FF

Ripple Counter : Asynchronous





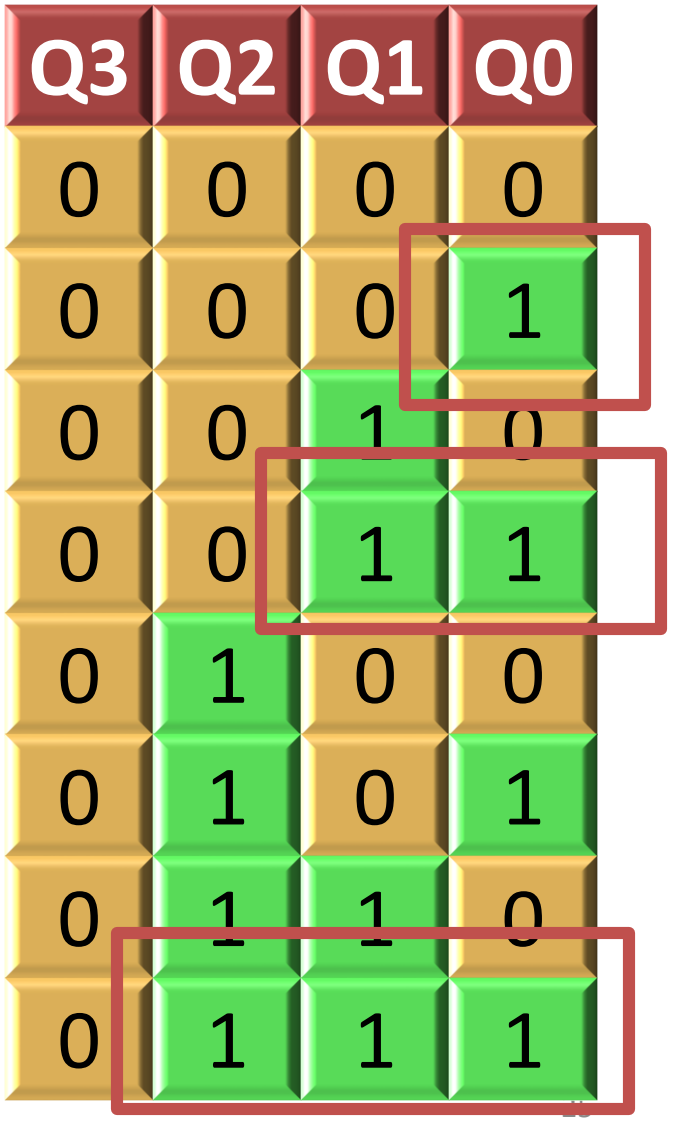
Synchronous Counter

- **Synchronous Counter**: One single clock to all the FFs of the Counter
- Need to design and add Extra Circuitry to make it synchronous

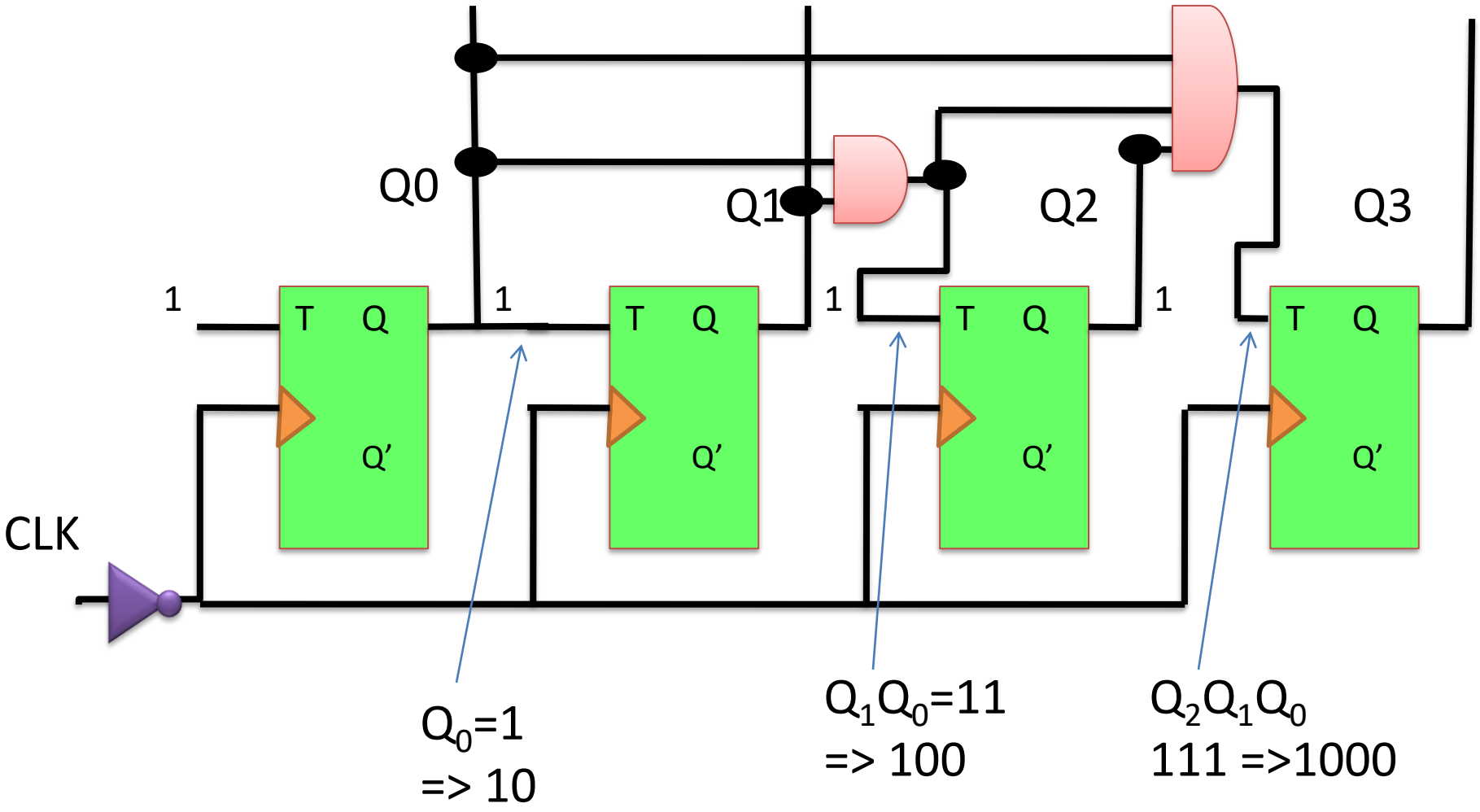
How to Design and put extra circuitry?

How to design a simple counter

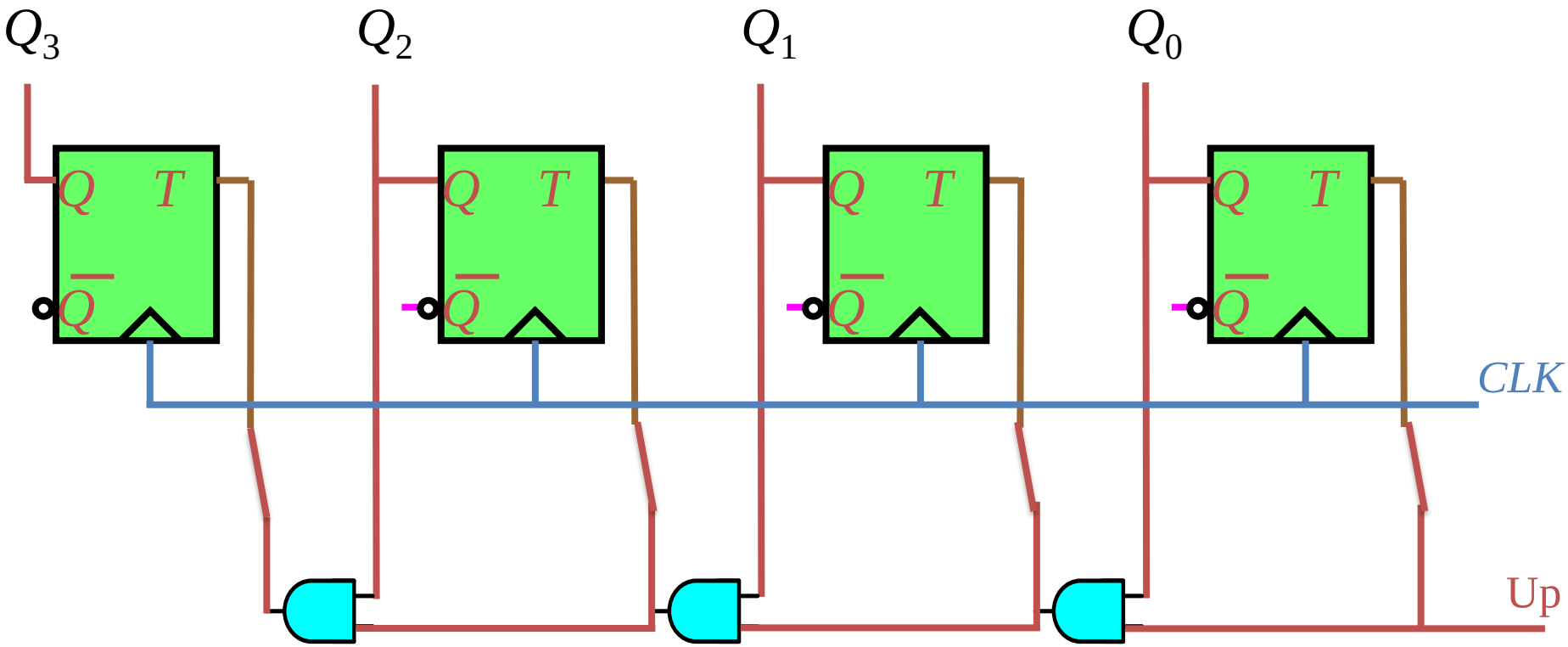
- Q0 change every time
- Q1 change when
  - Q0=1
- Q2 changes when
  - Q0=1 and Q1=1
- Q3 changes when
  - Q0=1 and Q1=1 and Q2=1



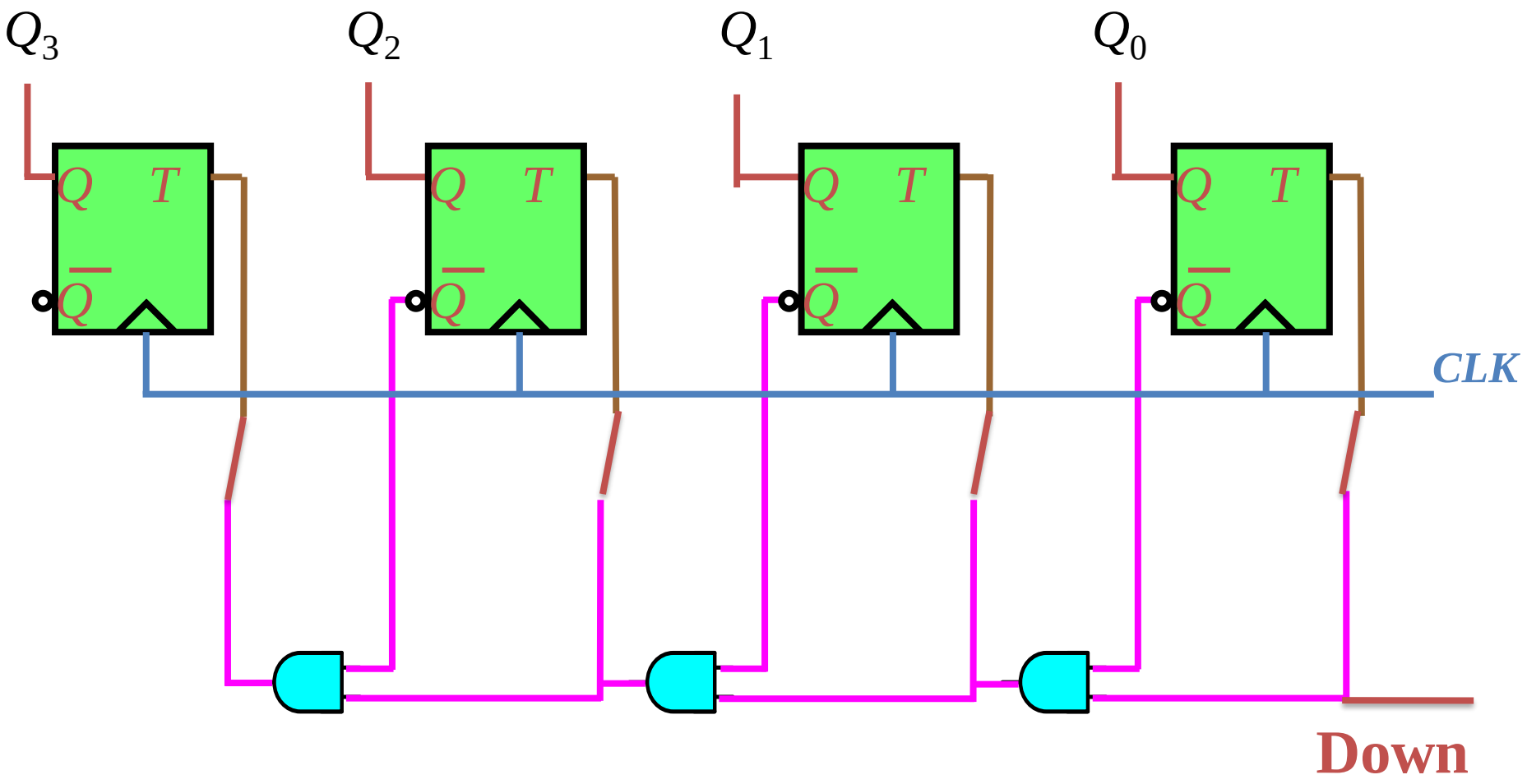
Binary Counter: Synchronous



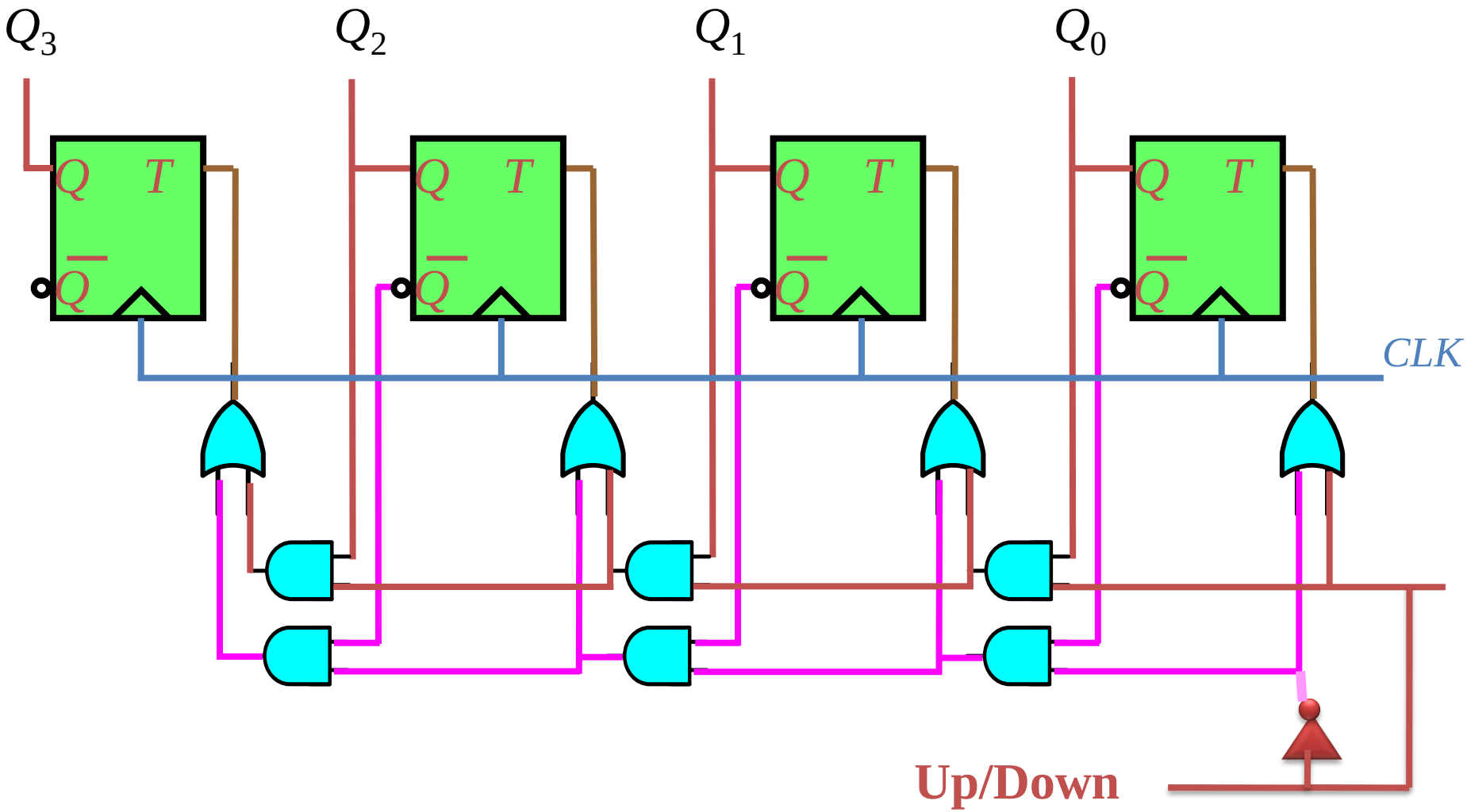
Sync: Binary UP Counter



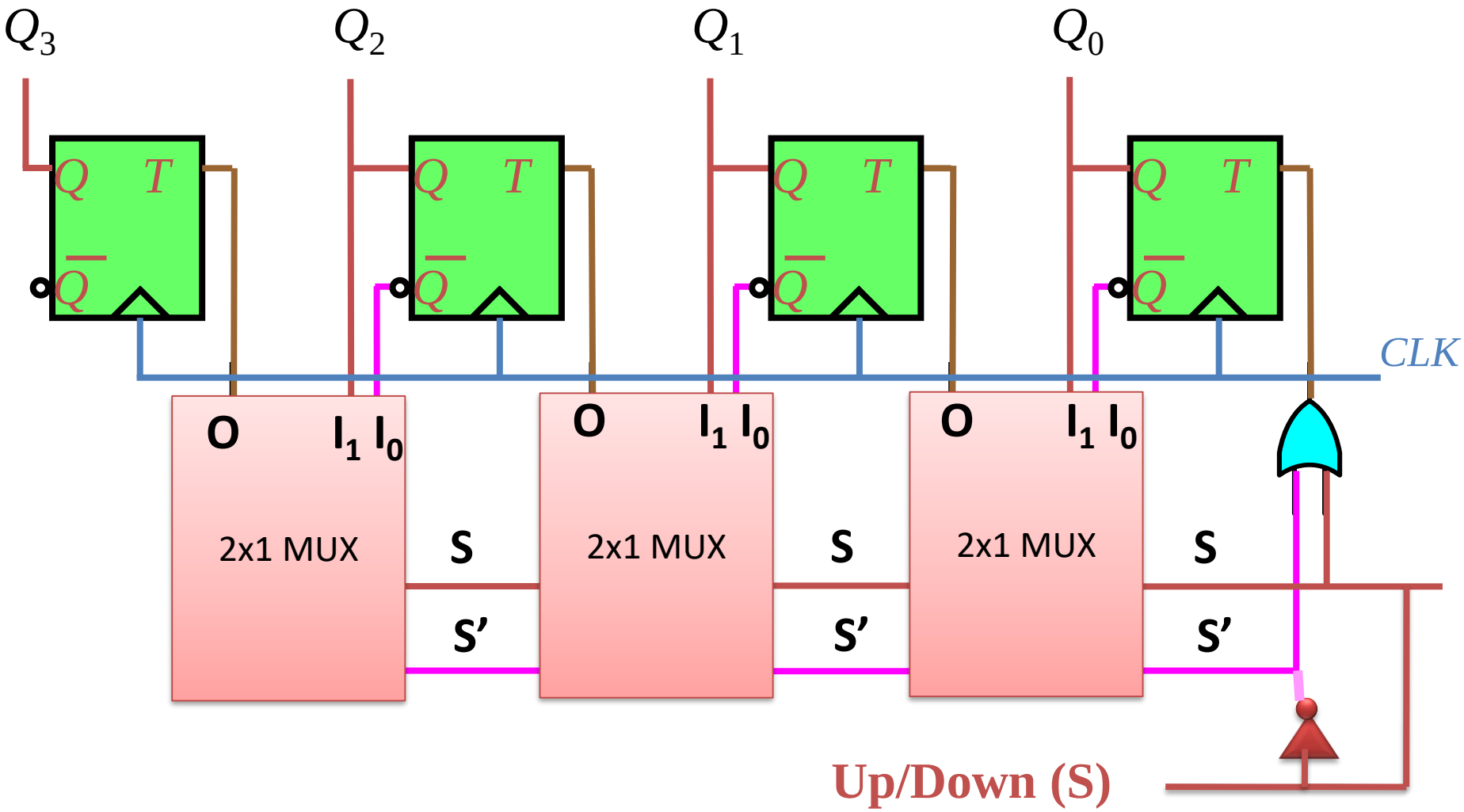
Sync: Binary Down Counter



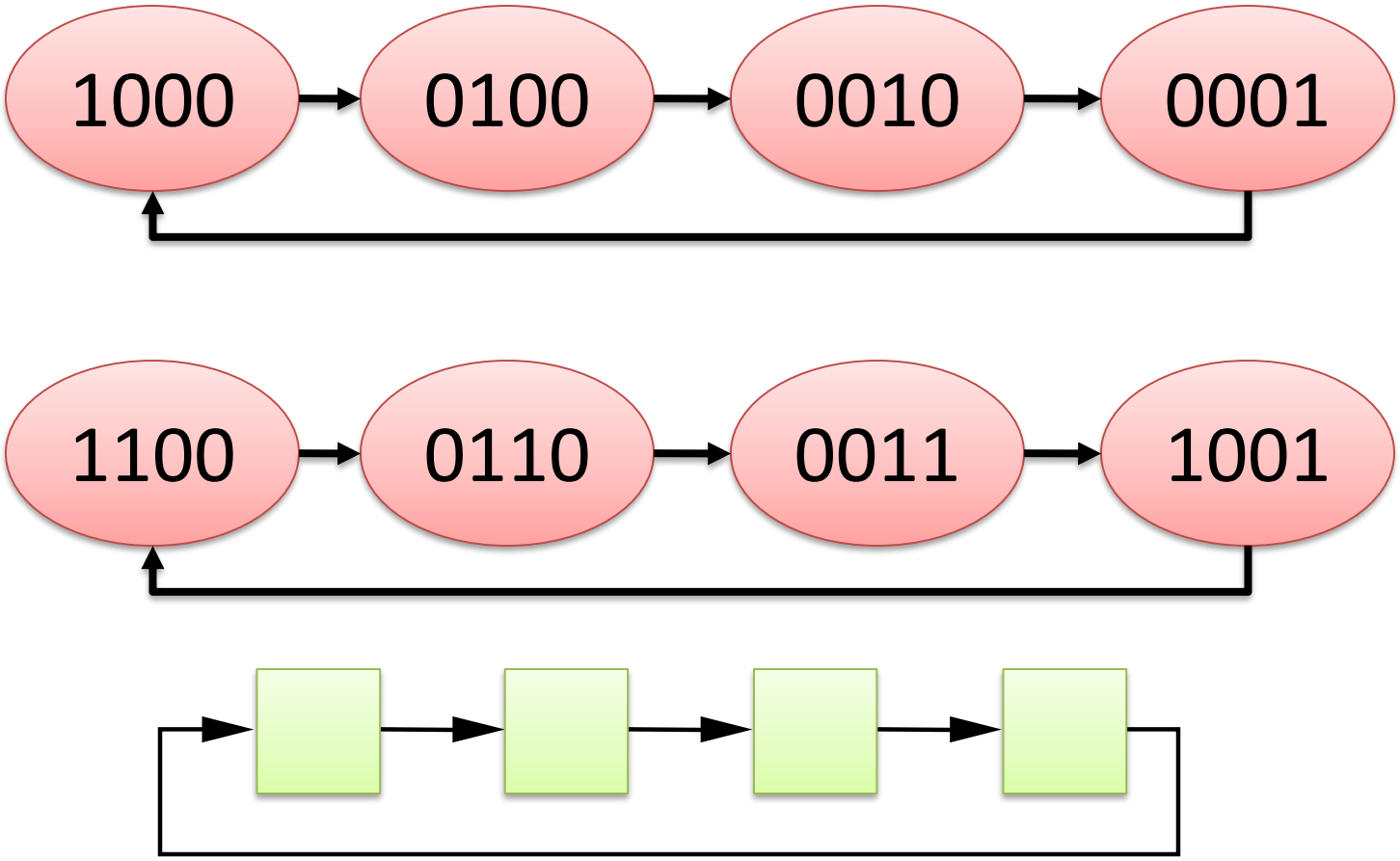
Sync: Up/Down Binary Counter



Sync: Up/Down Binary Counter



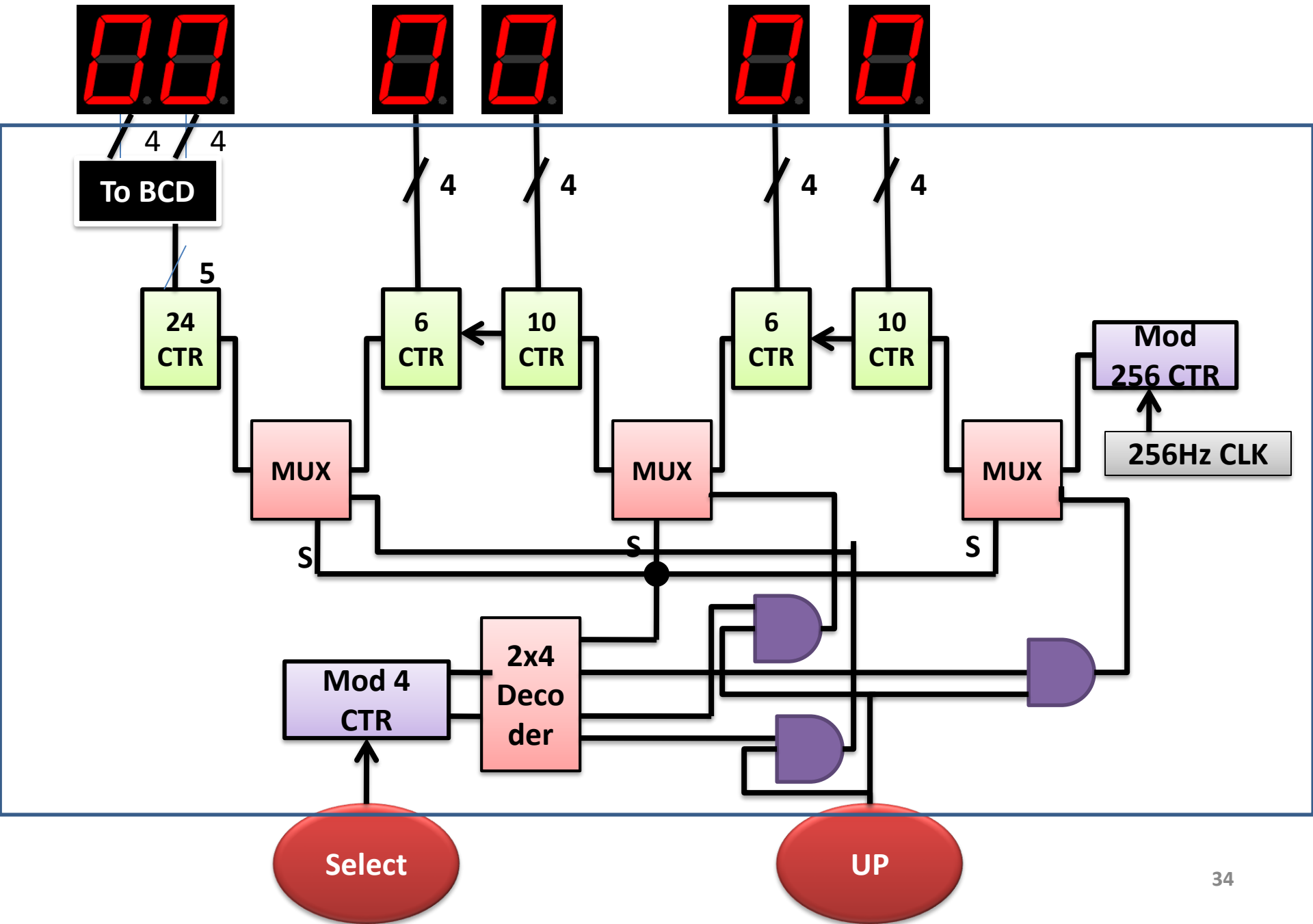
Counter Based on Shift Register

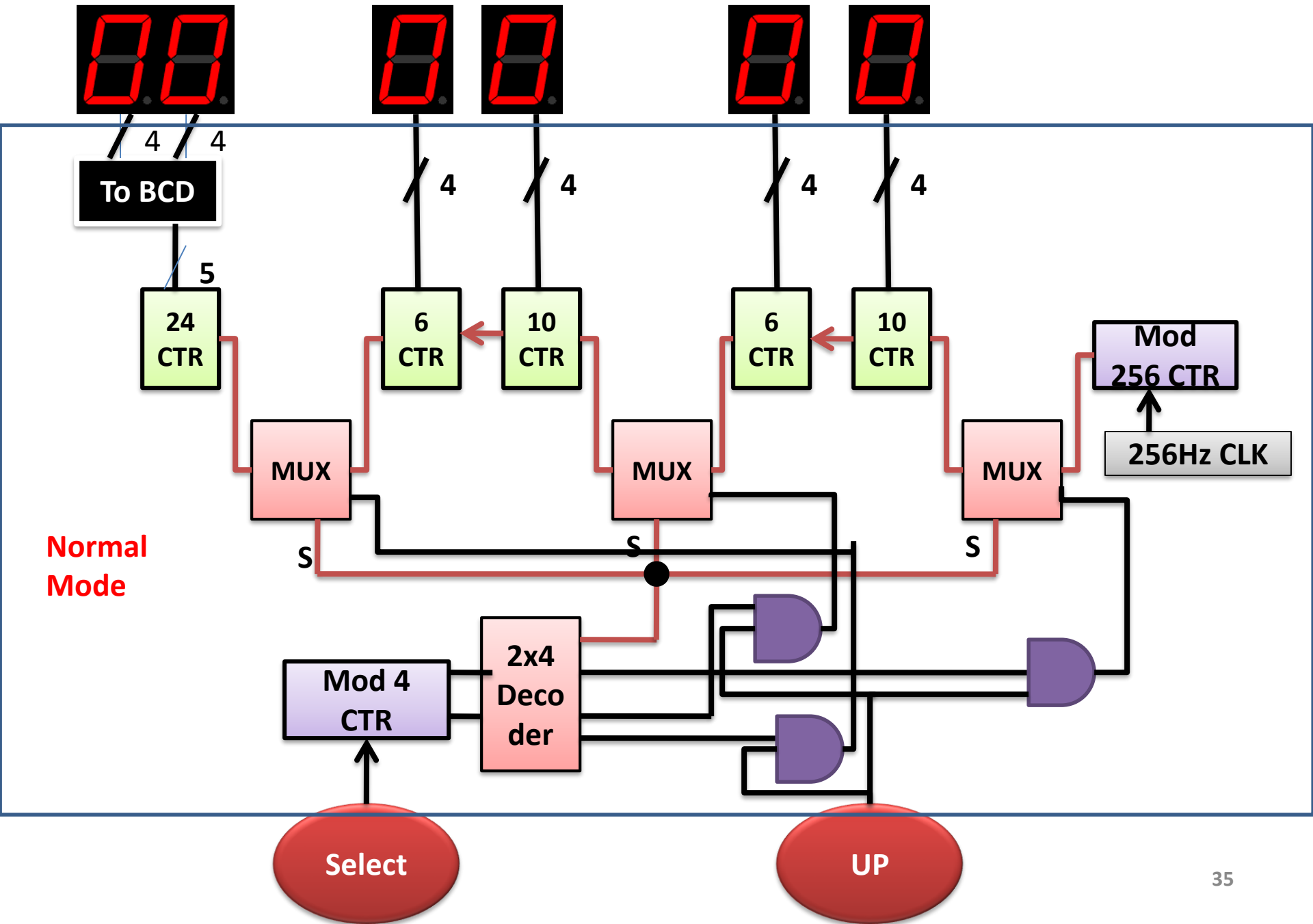


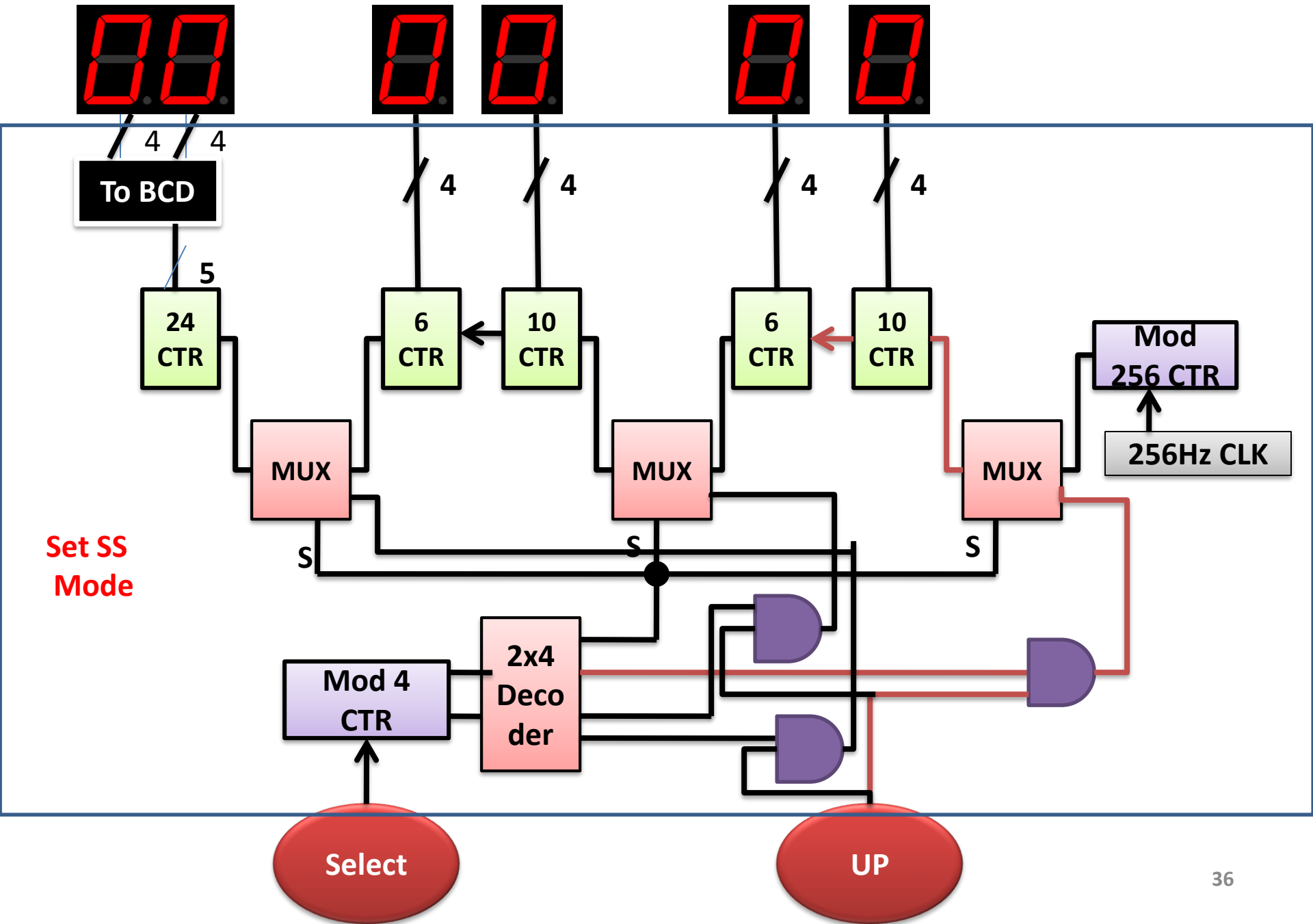
Design of Digital Wall Clock

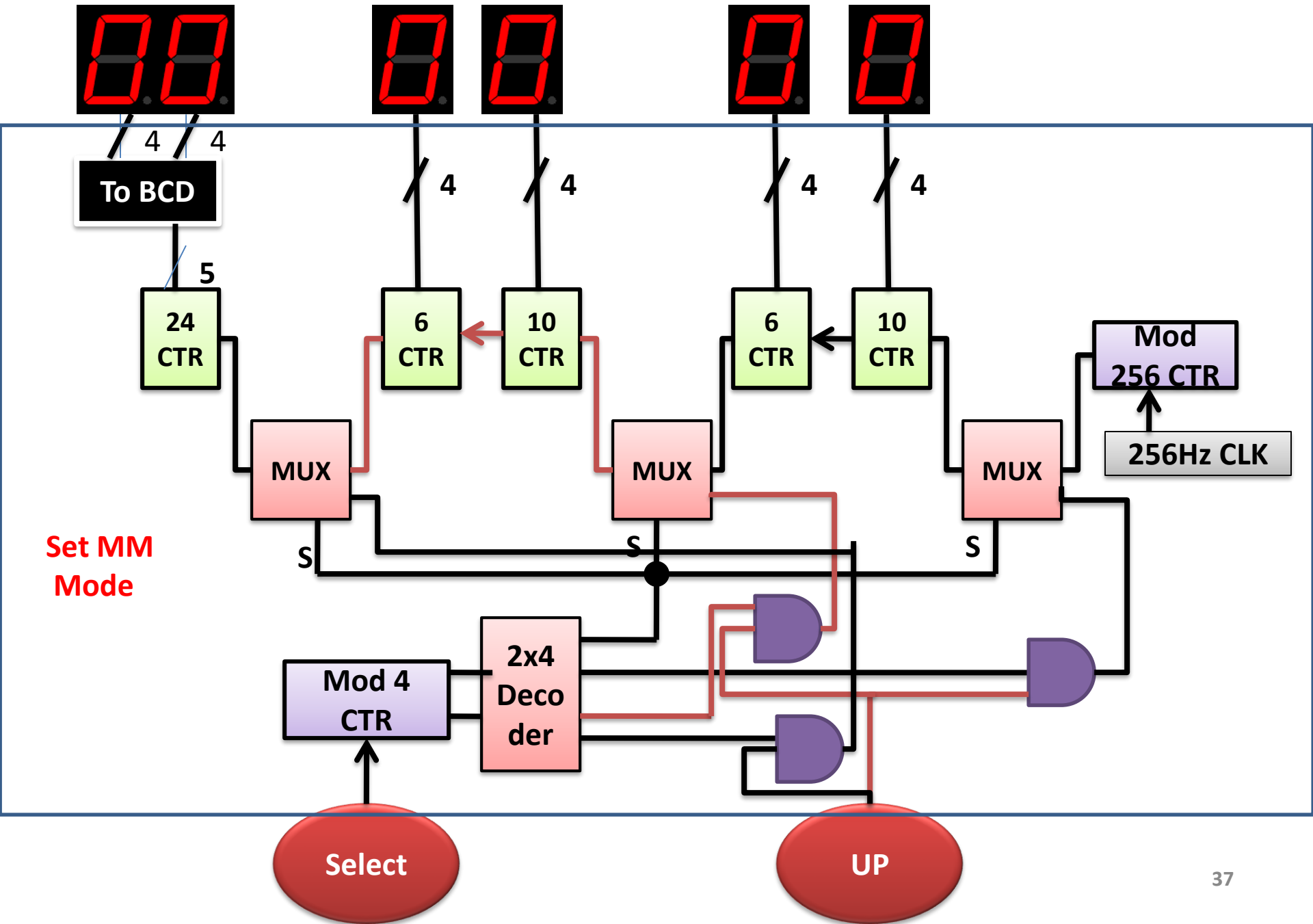
Design of Digital Wall Clock

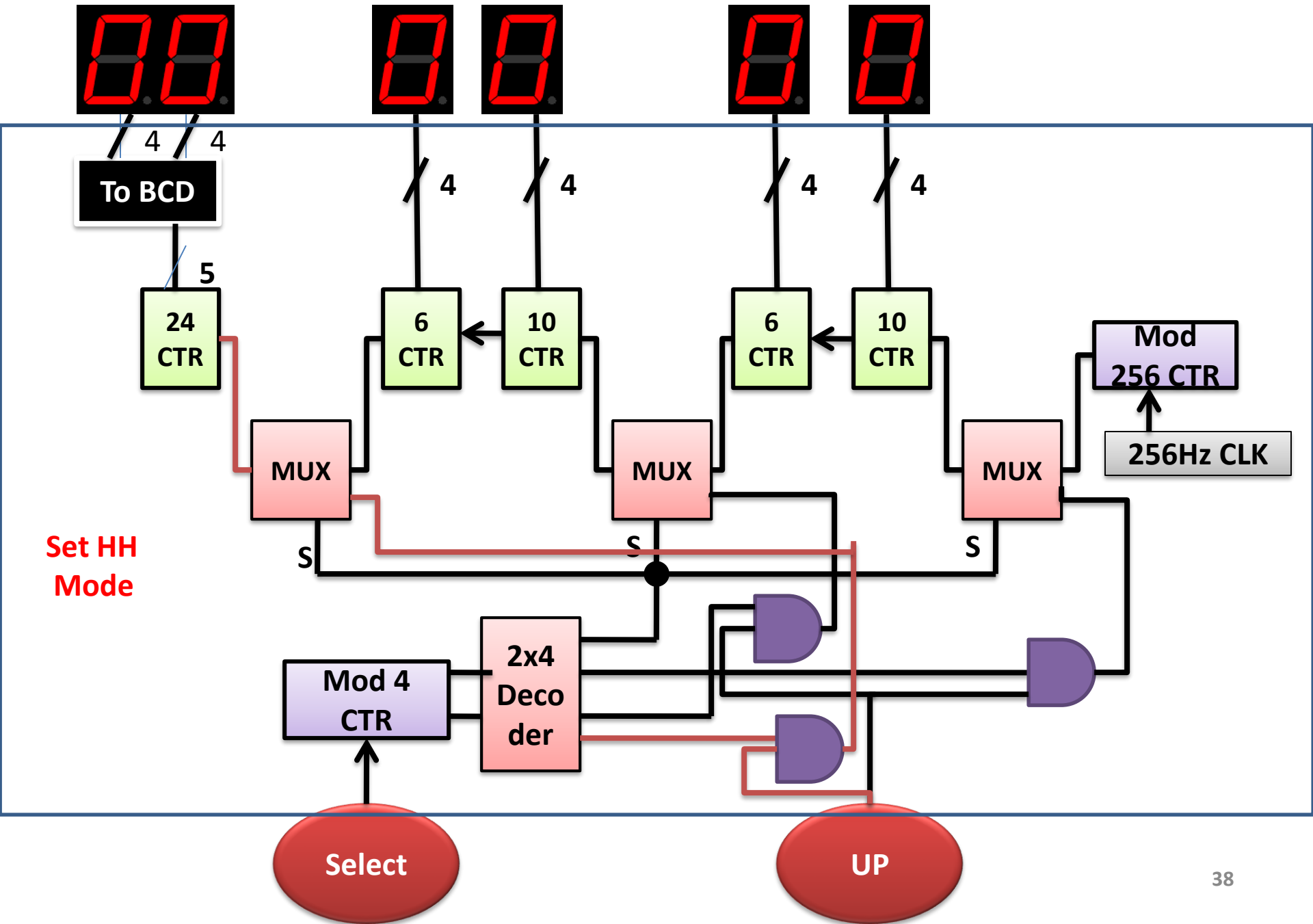
- Given 256 Hz Clock Quartz and other Digital components
- Design a Wall Clock
  - To display time : HH : MM :SS format
  - Should support Reset/Adjust of time using selectable switch
  - Button 1: for select the Mod Ctr
    - 3 for SS, 2 for MM, 1 for HH, 0 for X
  - Button 2: increasing select mod Ct


4
4
To BCD
5
4
4
4
4
24 CTR
6 CTR
10 CTR
6 CTR
10 CTR
Mod 256 CTR
256Hz CLK
MUX
MUX
MUX
S
S
S
Mod 4 CTR
2x4 Deco der
Select
UP


4
4
To BCD
5
24 CTR
4
4
6 CTR
10 CTR
4
4
6 CTR
10 CTR
Mod 256 CTR
256Hz CLK
MUX
MUX
MUX
S
S
S
Normal Mode
Mod 4 CTR
2x4 Deco der
Select
UP


4
4
To BCD
5
4
4
4
4
24 CTR
6 CTR
10 CTR
6 CTR
10 CTR
Mod 256 CTR
256Hz CLK
MUX
MUX
MUX
S
S
S
Set SS Mode
Mod 4 CTR
2x4 Deco der
Select
UP


4
4
To BCD
5
24 CTR
4
4
6 CTR
10 CTR
4
4
6 CTR
10 CTR
Mod 256 CTR
256Hz CLK
MUX
MUX
MUX
S
S
S
Set MM Mode
Mod 4 CTR
2x4 Deco der
Select
UP


4
4
To BCD
5
4
4
4
4
24 CTR
6 CTR
10 CTR
6 CTR
10 CTR
Mod 256 CTR
256Hz CLK
MUX
MUX
MUX
S
S
S
Set HH Mode
Mod 4 CTR
2x4 Deco der
Select
UP

Thanks