CS221: Digital Design

Sequential Logic Design

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Post Midsem Topics

- **Part I : Basic Sequential Design**
  - Latch and Flip Flop : Design, Characteristics Eqn, excitation Table
  - Register, Multi-Function Register, Memory Design
  - Counter Design: Basic
- **Part II: Formal Sequential Design**
  - FSM Design : Spec, Implementation
  - FSM Optimization
- **Part III : Advanced Formal Sequential Design**
  - RTL: ASM Design, ASM implementation
  - Digital System Design using FPGA and HDL

Quizzes and Exam

- Will be in RapidFire Mode on MS Teams
- Two quizzes
  - Quiz 1 : Basic Sequential Design
  - Quiz 2 : Formal Sequential Design
- End Semester have three parts
  - Part I: Advanced Sequential Design
  - Part II: Basic and Formal Sequential Design
  - Part III: Pre-mid Semester part & Post mid sem part

Books to be referred

- **ManoBook**: M. Morris Mano and M. D. Ciletti, *Digital Design*, 4/e, Pearson Education India, 2007.
- **VahidBook:** Frank Vahid, Digital Design (Preview Edition), Wiely India Edition, 2005 *[[FF and Register design]]*
- **KumarBook:** A. Anand Kumar, *Fundamentals of Digital Circuits* 3rd Edition, PHI. 2014 **((This book have a lot of examples to understand the concepts))** [[ASM Chart]]
- **KatzBook:** Randy H. Katz, G Borriello, *Contemporary Logic Design*, 2nd Edition, PHI, India, 2009 [[FSM Opt.]
- **Givone Book:** Donald D. Givone, Digital Principles and Design, McGraw-Hill, 2003 [[Counter Design]]

Announcement

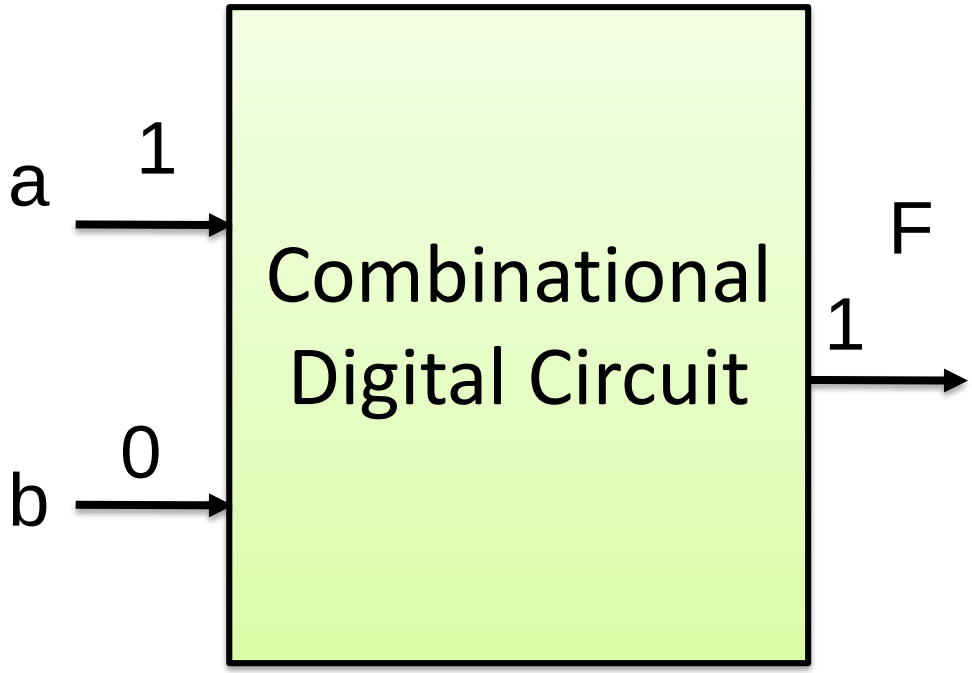
- There will be no CS221 class on 1st Oct and 3rd Oct ==> Coming Friday and Monday
- Both the Instructors will be out of town for JEE related work
- Makeup classes for 1st Oct and 3rd Oct are scheduled on 6th and 12th Oct at evening 5.30 to 6.30pm

Outline

- Combinational Vs Sequential Logic Design
- Design a **flip-flop**, that stores one bit
  - RS latch
- Stabilizing RS latch : Level Sensitive
- Clocked Latch : Flip Flop- Edge Sensitive
- D, JK, T flip flops
- Characterization Table and Equation
  - RS, D, JK and T Flip flop

Combinational Vs Sequential Logic

- Combinational circuit
  - **Output depends on present input**
  - Examples: F (A,B,C), FA, HA, Multiplier, Decoder, Multiplexor, Adder, Priority Encoder



Y = F (a,b)

Propagation delay

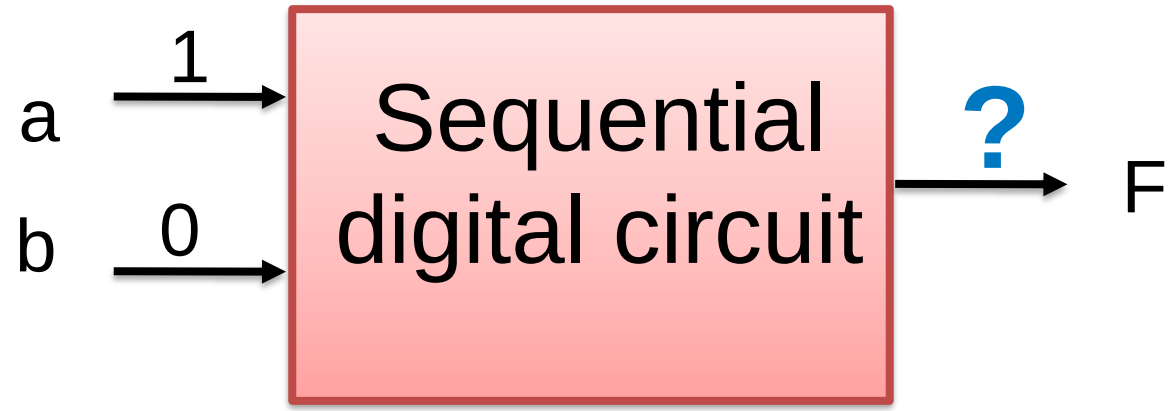
$Y(t+t_{pd})=F(a(t), b(t))$

Combinational Vs Sequential Logic

- Sequential circuit
  - Output depends not just on present inputs
  - But also on past sequence of inputs (State)
    - Stores bits, also known as having “state”

Combinational Vs Sequential Logic

- Simple example: a circuit that counts up in binary

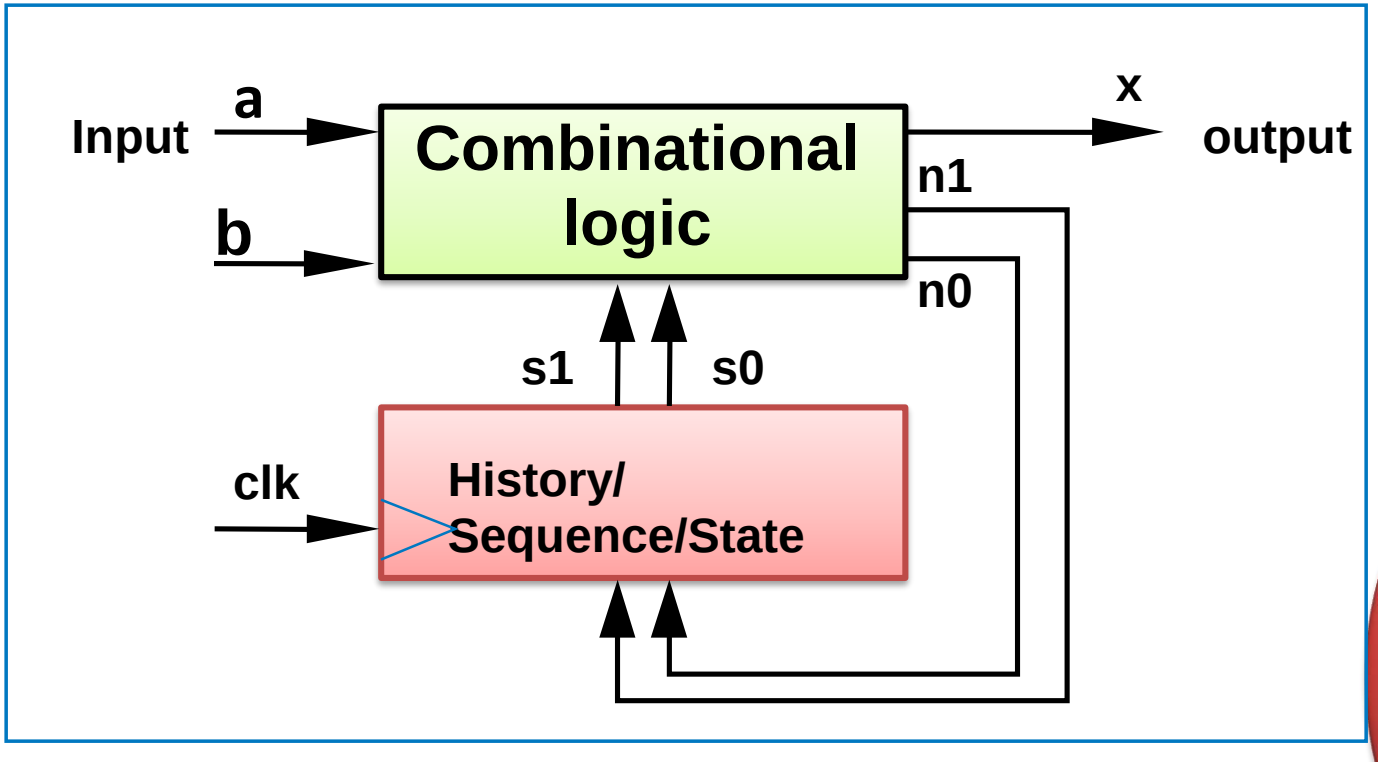


Must know sequence of past inputs to know output

Y (t) = F (a(t),b(t), H)

H is History/Sequence/State

Sequential Circuit: Generic Circuit



Where to Store this History

(Memory Element)

Y (t) = F (a(t), b(t), H)

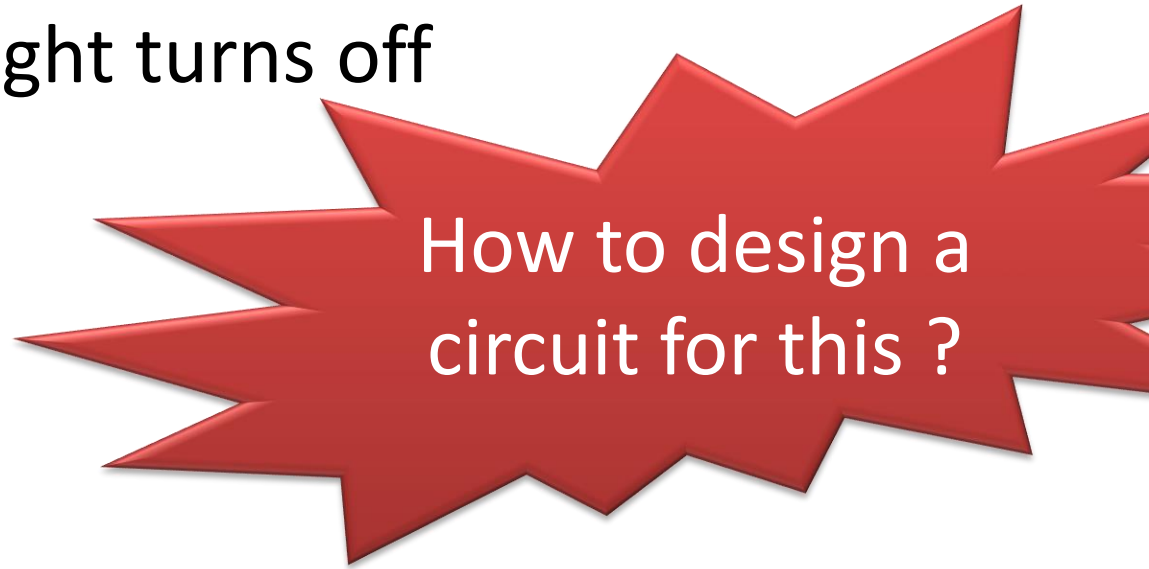
H is History/Sequence/State

Example Needing Bit Storage

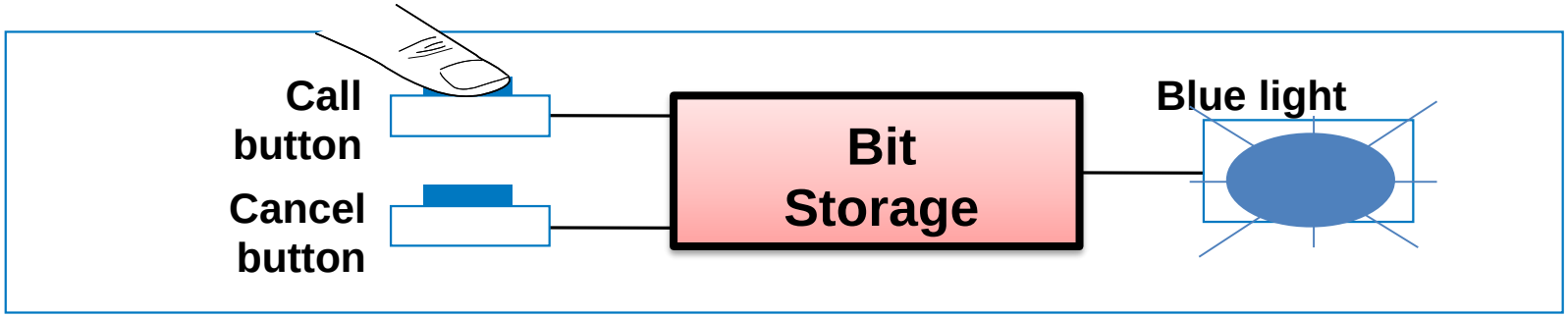
- Mechanical Example: Retractable Ball point pen
  - Push to change : on or off
  - T-FFs

Example Needing Bit Storage

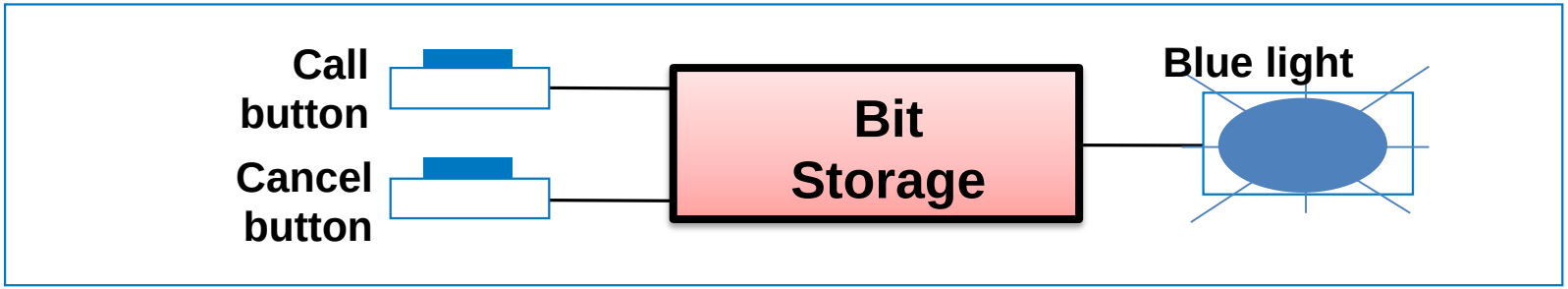
- Electronics Example: Flight attendant call button
  - Press call: light turns on
    - ***Stays on*** after button released
  - Press cancel: light turns off



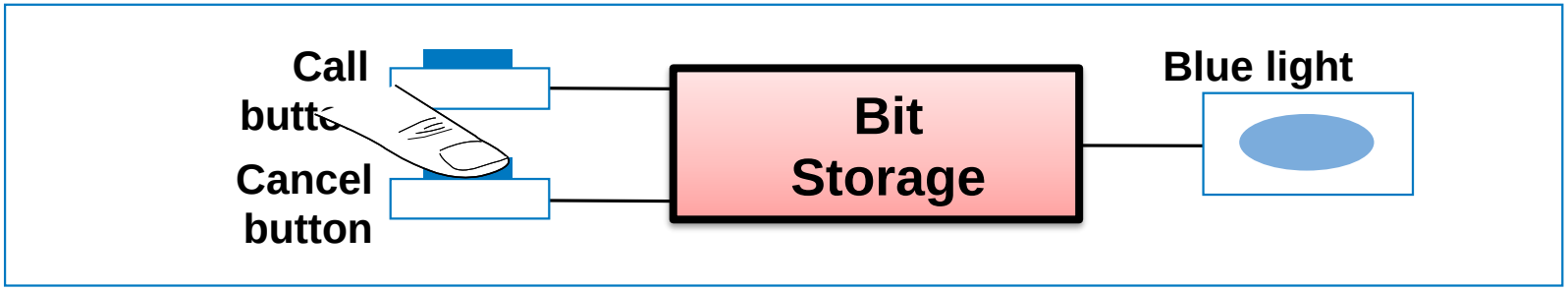
Example Needing Bit Storage



1. Call button pressed – light turns on



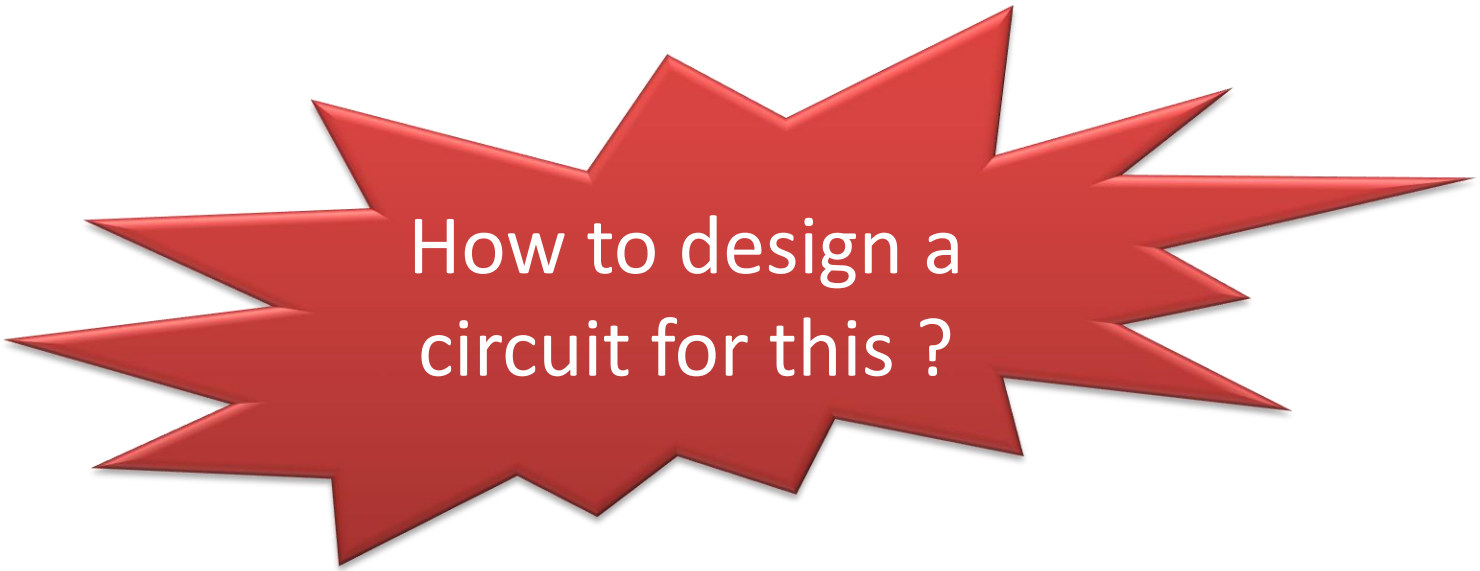
2. Call button released – light stays on



3. Cancel button pressed – light turns off

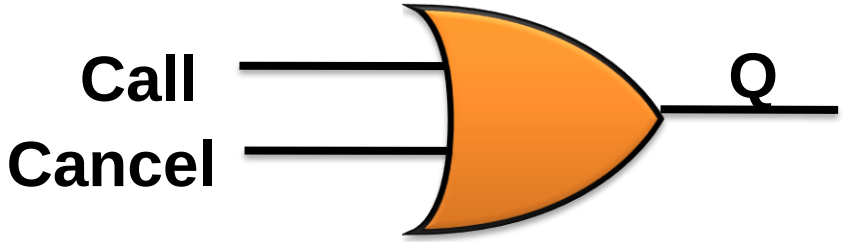
Example Needing Bit Storage

- Flight attendant call button
  - Press call: light turns on
    - ***Stays on*** after button released
  - Press cancel: light turns off



Example Needing Bit Storage

- Flight attendant call button
  - Press call: light turns on : ***Stays on*** after button released
  - Press cancel: light turns off
- Logic gate circuit to implement this?

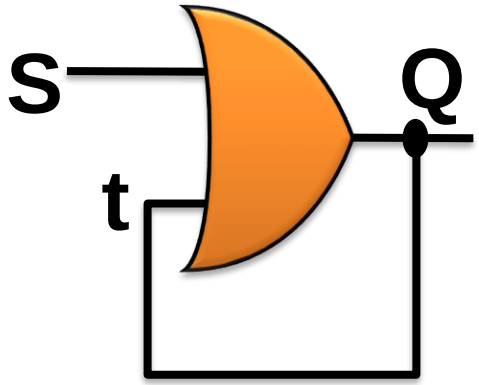


Doesn't work. Q=1 when Call=1, but doesn't stay 1 when Call returns to 0

Need some form of "feedback" in the circuit

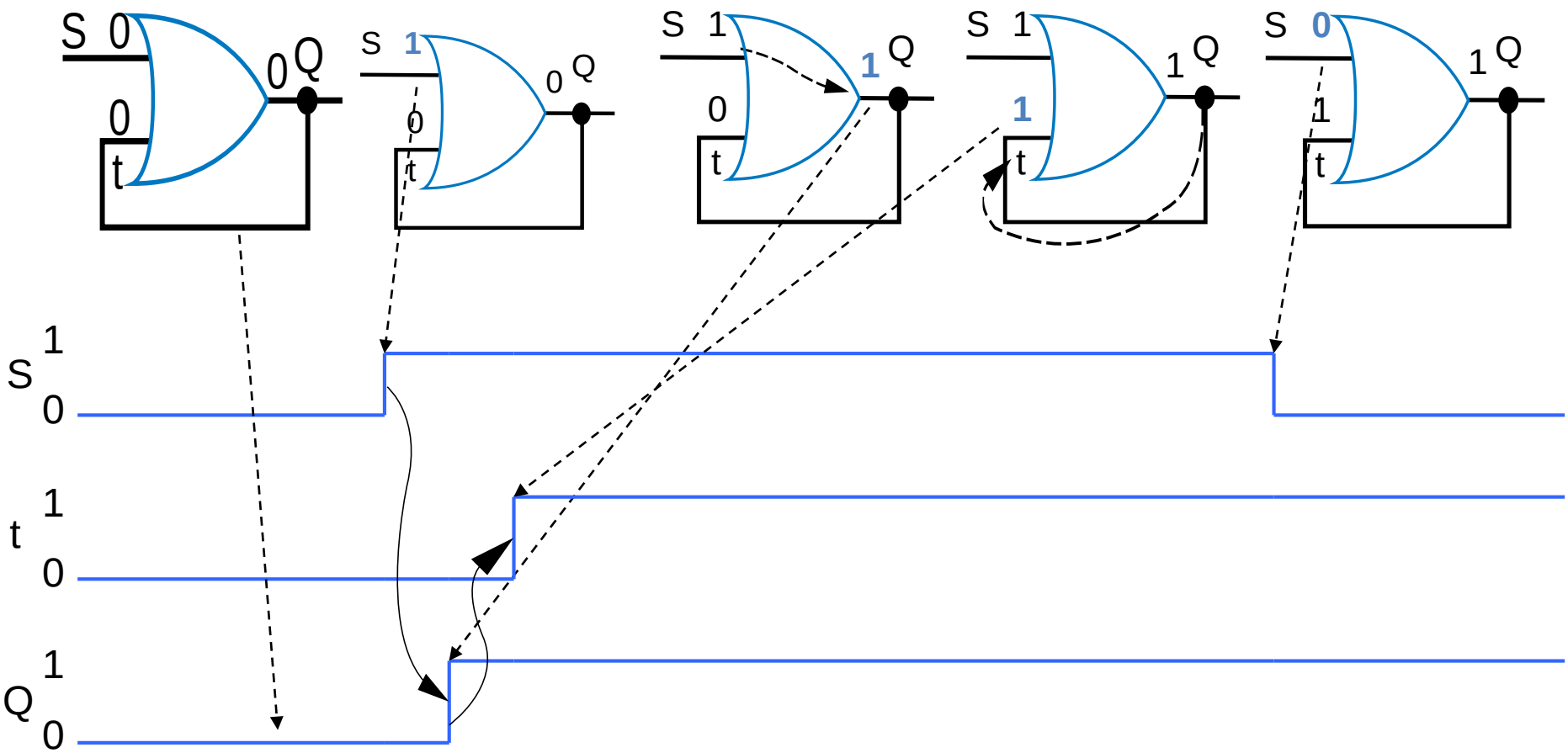
First attempt at Bit Storage

- We need some sort of feedback
  - Does circuit this circuit do what we want?



  - No: Once **Q** becomes 1 (when **S**=1), **Q** stays 1 forever – no value of **S** can bring **Q** back to 0

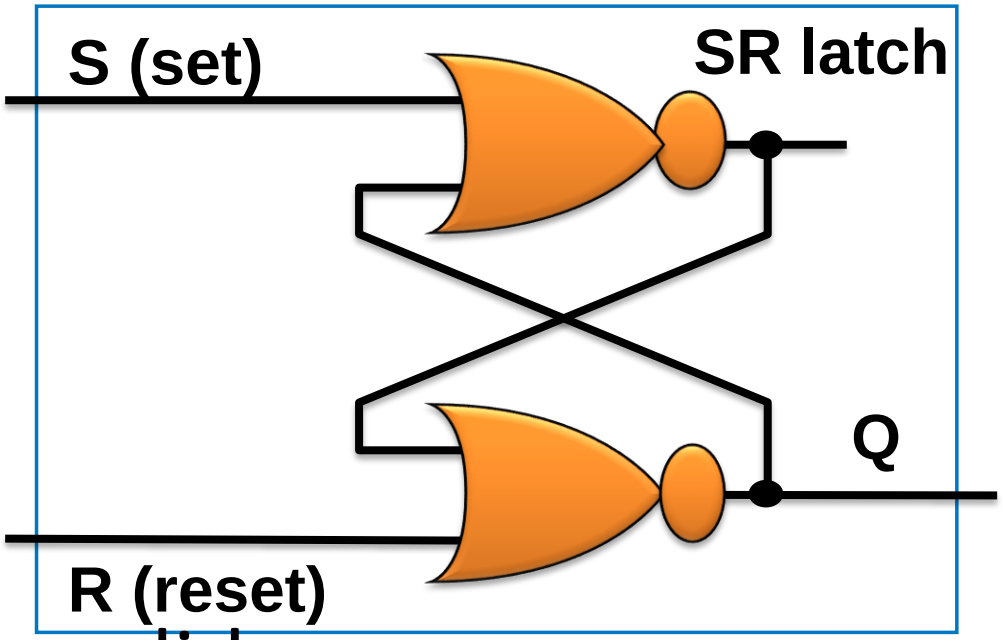
First attempt at Bit Storage



Once **Q** becomes 1 (when **S**=1), **Q** stays 1 forever – no value of **S** can bring **Q** back to 0

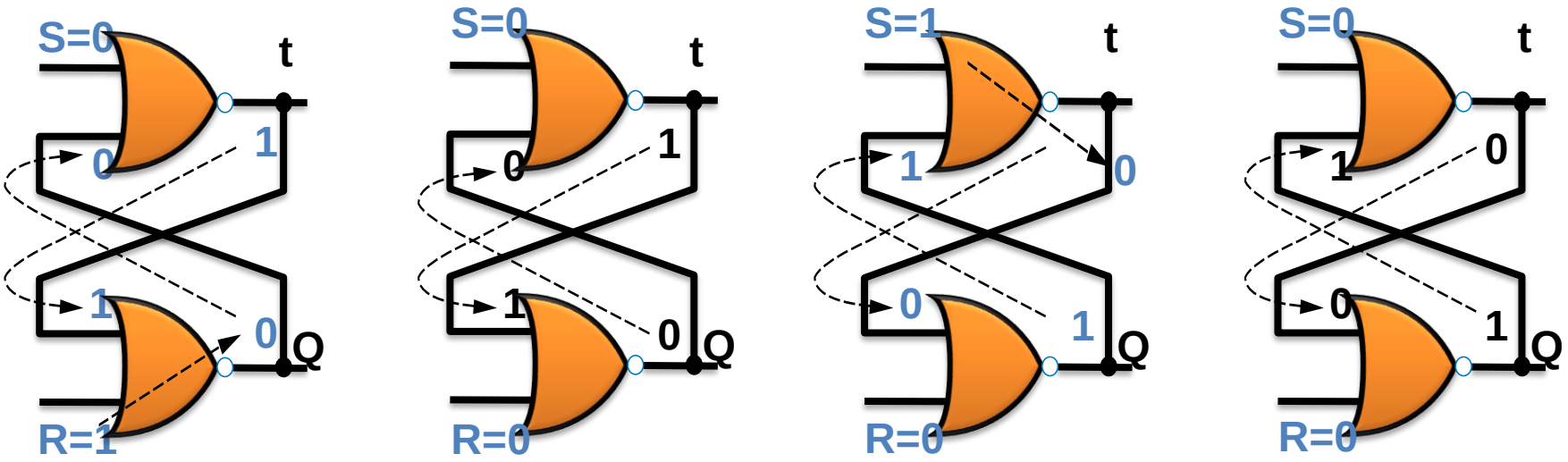
Bit Storage Using an SR Latch

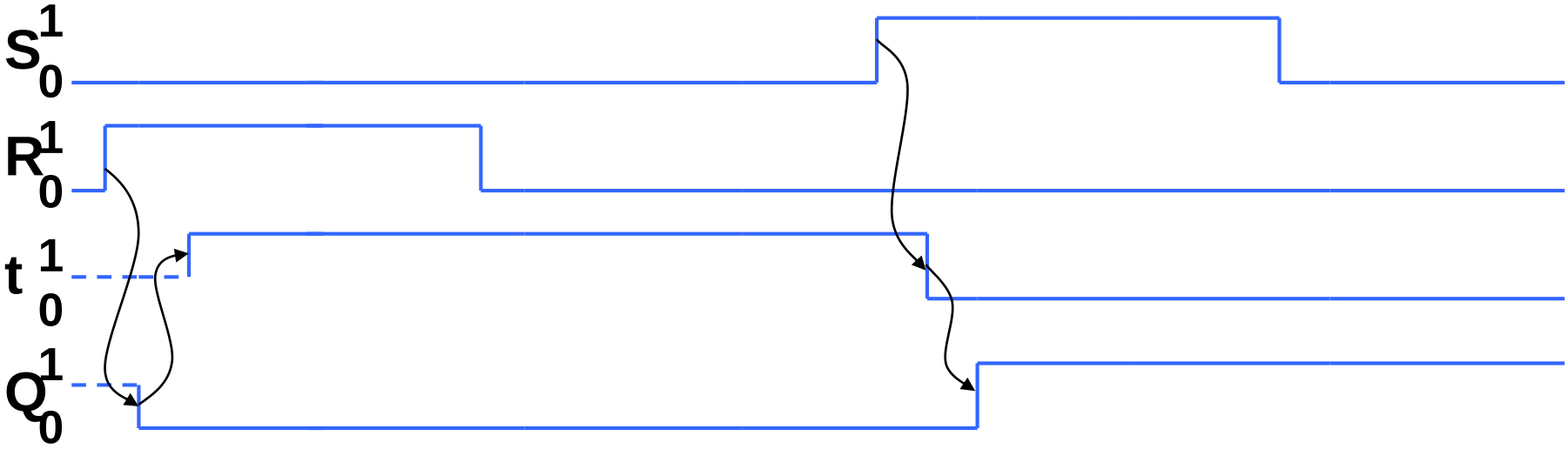
- With cross-coupled NOR gates
  - Does the circuit to the right ?
  - Do what we want?



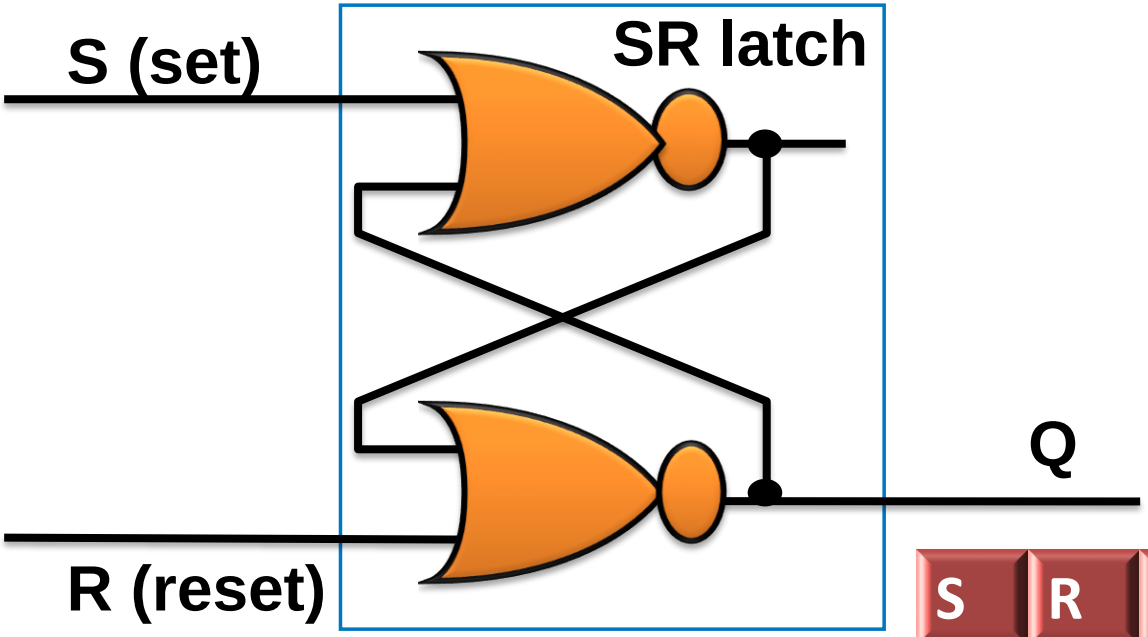
- Yes! How did someone come up with that circuit?
  - Maybe just trial and error, a bit of insight...

Bit Storage Using an SR Latch





Function Table of SR Latch

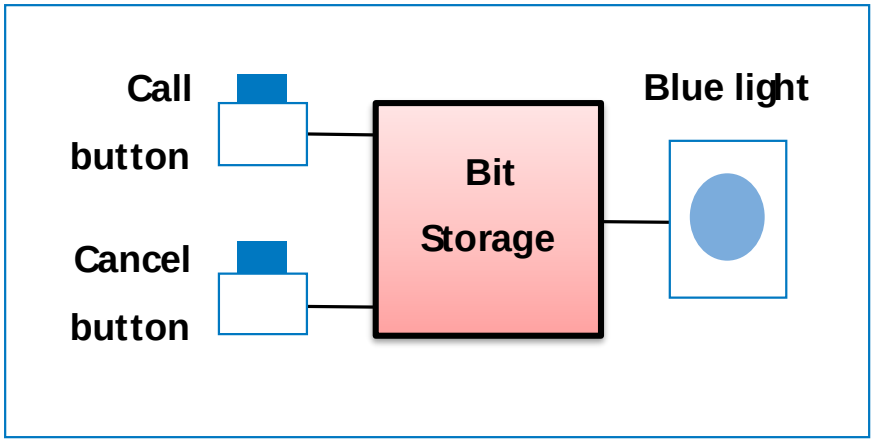


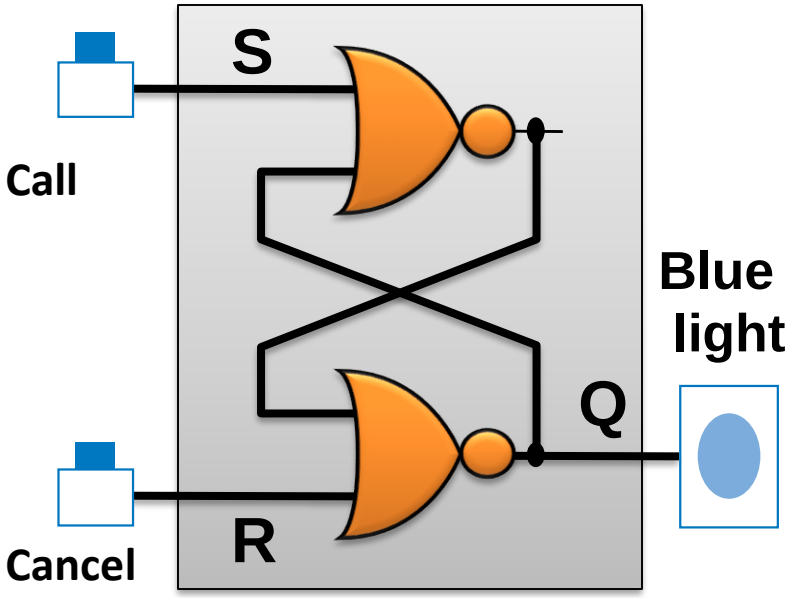
S	R	Q	Q’	
1	0	1	0	
0	0	1	0	After S=1, R=0
0	1	0	1	
0	0	0	1	After S=0, R=1
1	1	0	0	Forbidden

Set ***: make out put 1***

Reset ***: make out put 0***

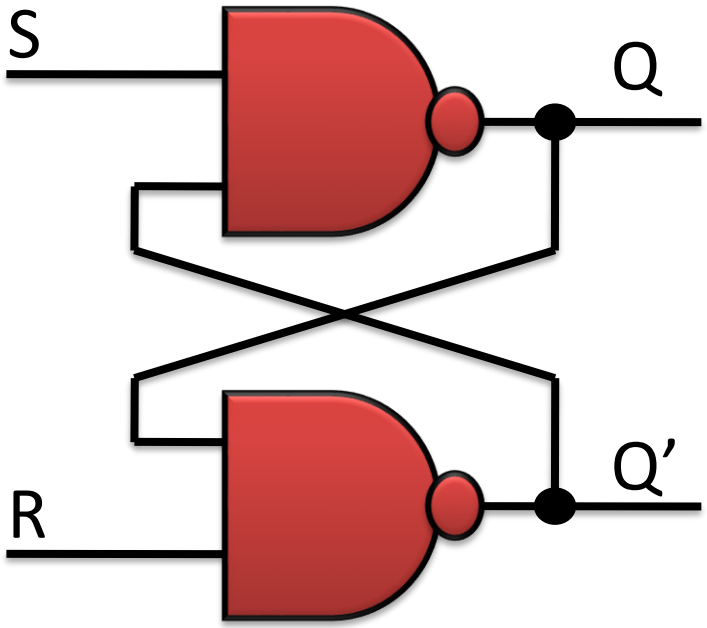
Example Using SR Latch for Bit Storage





- SR latch can serve as bit storage of flight-attendant call button : ☺ ☺ ☺ Great
  - Call=1 : sets Q to 1
    - Q stays 1 even after Call=0
  - Cancel=1 : resets Q to 0
- **But, there's a problem...**

SR Latch with NAND Gates



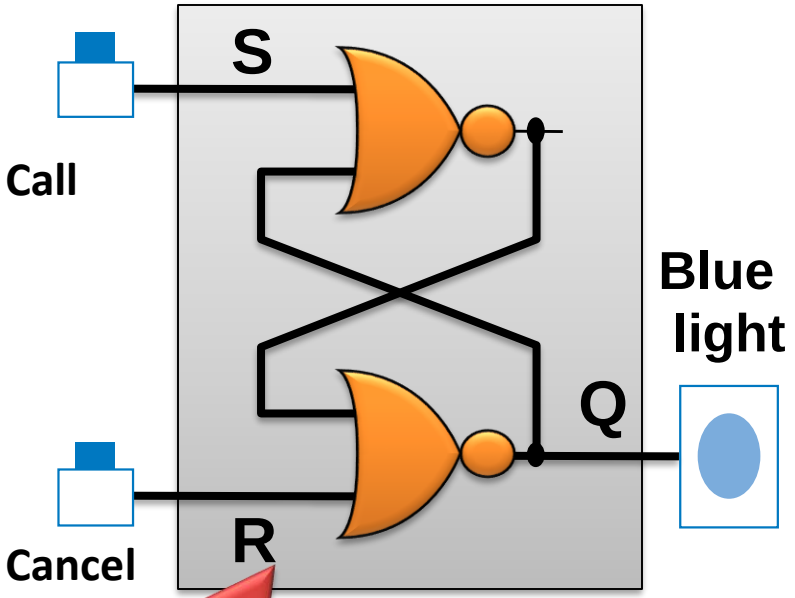
S	R	Q+
0	0	1*0* (Unpredictable)
0	1	1
1	0	0
1	1	Q

Opposite to SR Latch with NOR Gates

Set will do Q=0 and Reset will Q=1

Problem with SR Latch: SR=11

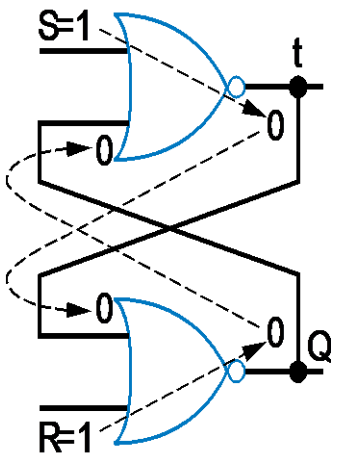
- Problem
  - If S=1 and R=1 simultaneously, we don't know what value Q will take (Unpredictable)

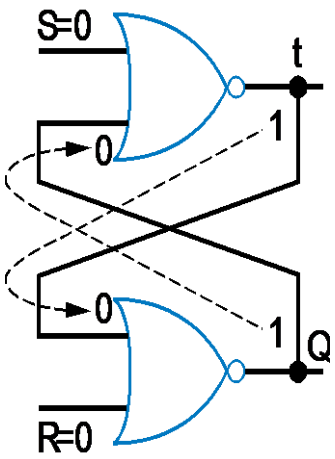


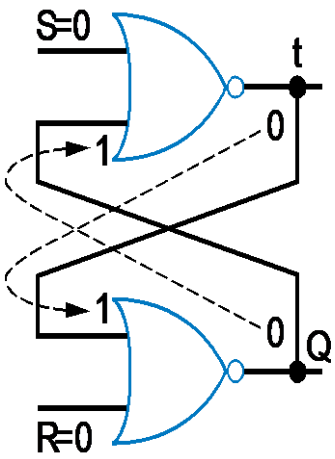
Race Condition :-

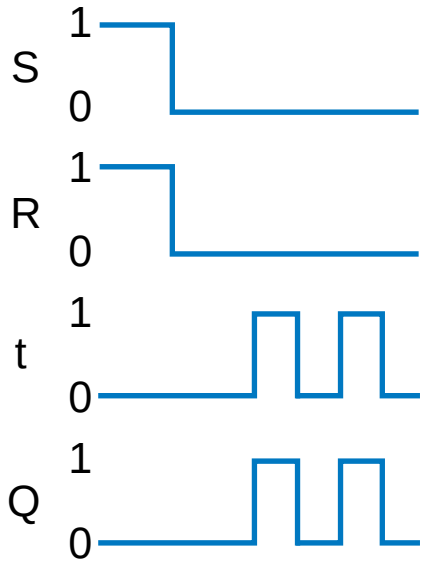
Who will win 0 or 1?
Eventually, what will be the value of Q?

Problem with SR Latch

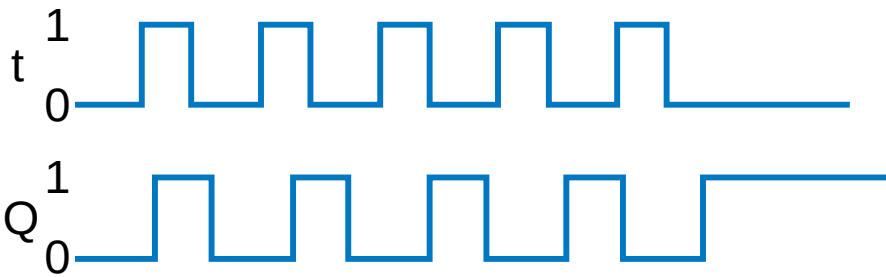






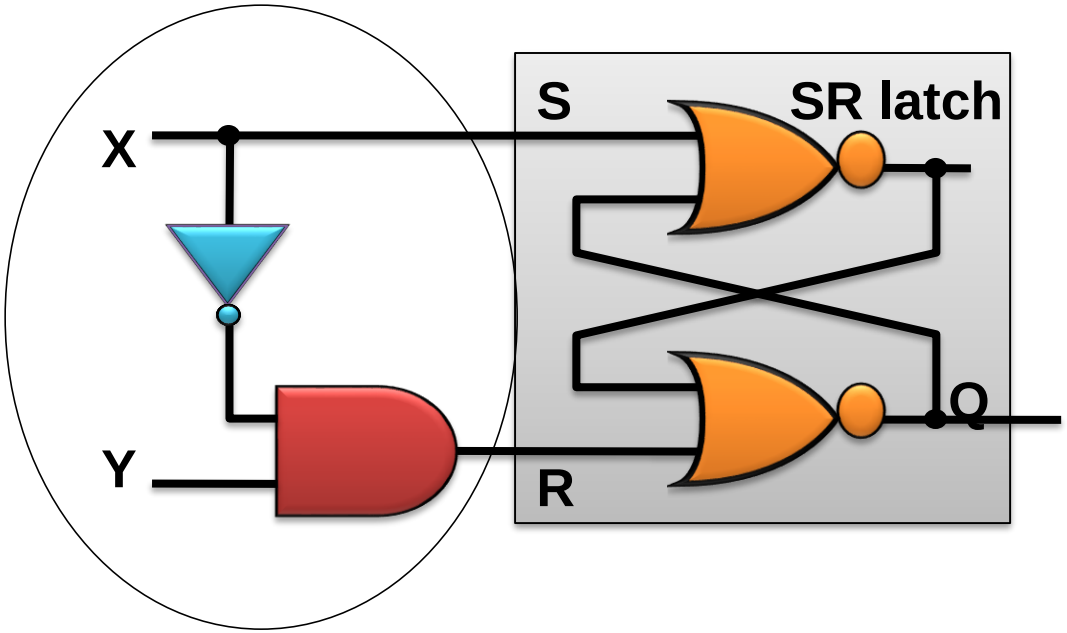


Q may oscillate. Then, because one path will be slightly longer than the other, Q will eventually settle to 1 or 0 – but we don't know which.



Solution to Race Condition

- We try to avoid S=1 and R=1 by the following circuit



- Can we ensure value S=1 and R=1 will not happen at the same time?

Reference

VahidBook: Frank Vahid, Digital Design (Preview Edition), Wiely India Edition, 2005 *[[FF and Register design]]*

Thanks