CS221: Digital Design

Finite State Machine (Examples)

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Outline

- Finite State Machine
- Formal definition
- FSM implementation
- FSM Examples

Finite State Machine

- Finite-State Machine (FSM)
  - A way to describe desired behavior of sequential circuit
  - Similar/Akin to Boolean equations for combinational behavior
  - List states, and transitions among states

Set Theoretic Description

Moore Machine is an ordered quintuple

$$\text{Moore} = (\mathbf{S}, \mathbf{I}, \mathbf{O}, \delta, \lambda)$$

where

$\mathbf{S}$ = Finite set of states $\neq \Phi, \{s_1, s_2, \cdots, s_n\}$

$\mathbf{I}$ = Finite set of inputs $\neq \Phi, \{i_1, i_2, \cdots, i_m\}$

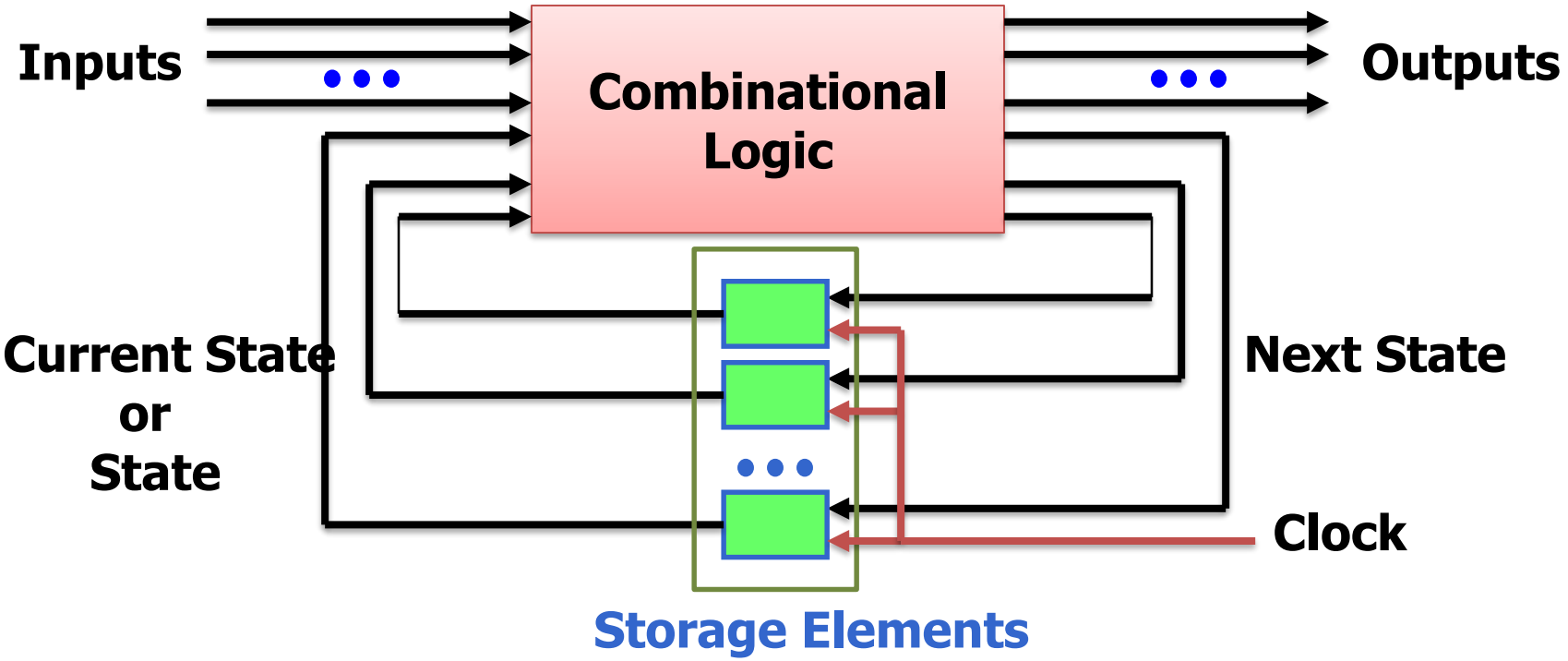
$\mathbf{O}$ = Finite set of outputs $\neq \Phi, \{o_1, o_2, \cdots, o_l\}$

δ = Next state function which maps $\mathbf{S} \times \mathbf{I} \rightarrow \mathbf{S}$

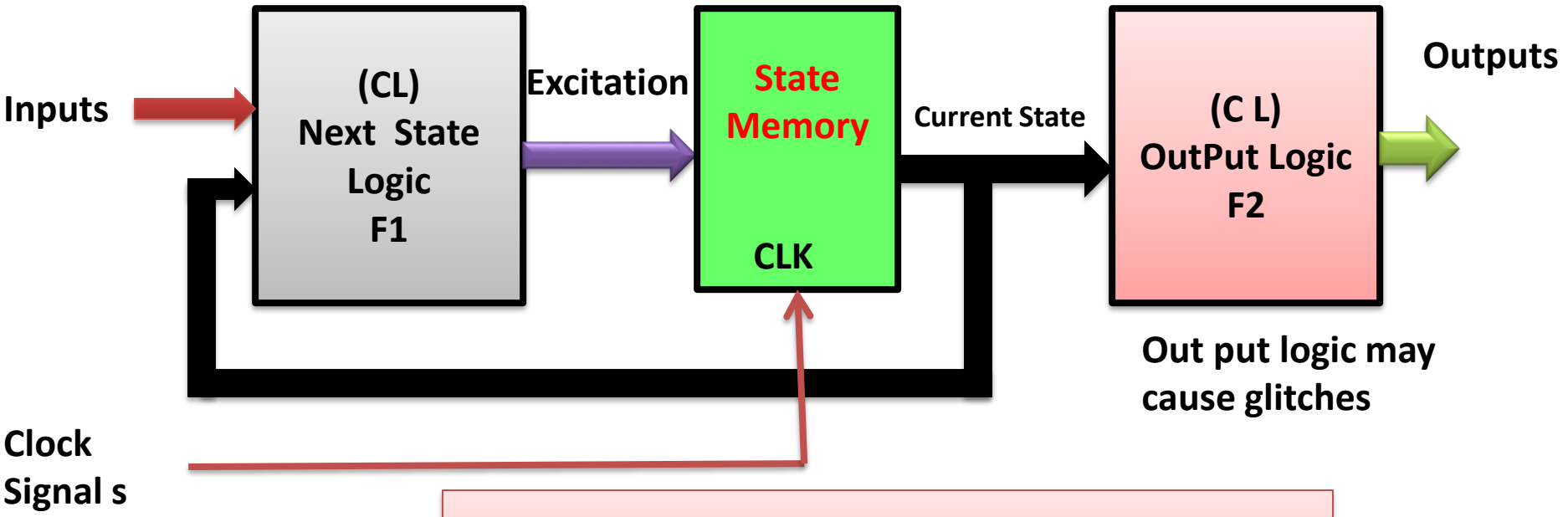
λ = Output function which maps $\mathbf{S} \rightarrow \mathbf{O}$

Clocked synchronous FSM structure

- **States**: determined by possible values in sequential storage elements
- **Transitions**: change of state
- **Clock**: controls when state can change by controlling storage elements



Moore machine



$$\text{Next state} = F_2(\text{current state, inputs})$$

$$\text{Output} = G_2(\text{current state})$$

FSM

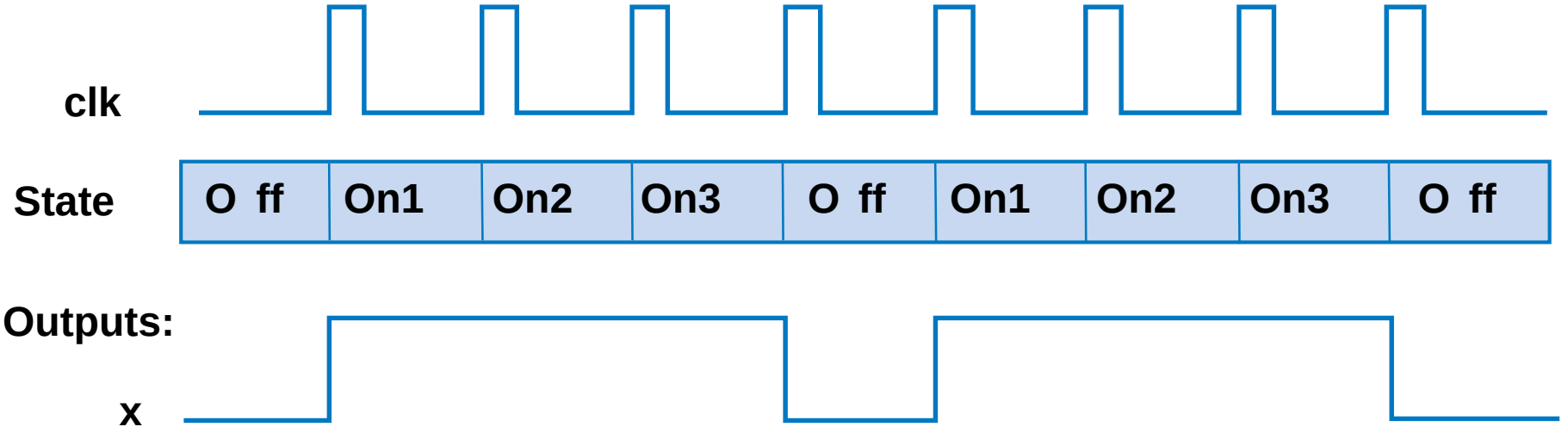
We often draw FSM graphically, known as ***state diagram***

Can also use table (state table), or textual languages

FSM Example 6:
Counter that repeat 0,1,1,1,

FSM Example: 0,1,1,1,repeat

- Want 0, 1, 1, 1, 0, 1, 1, 1, …
  - Each value for one clock cycle
- Can describe as FSM: Four states, Transition on rising clock edge to next state



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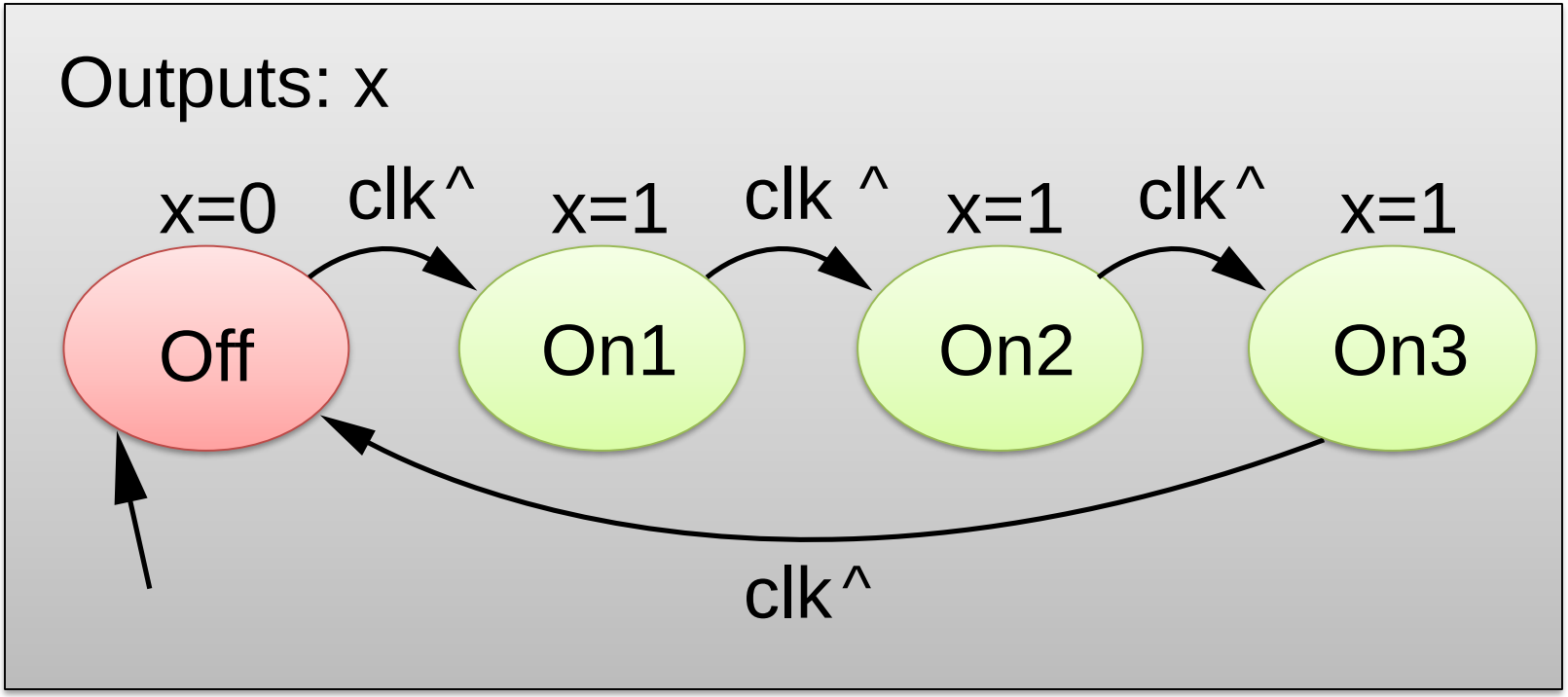

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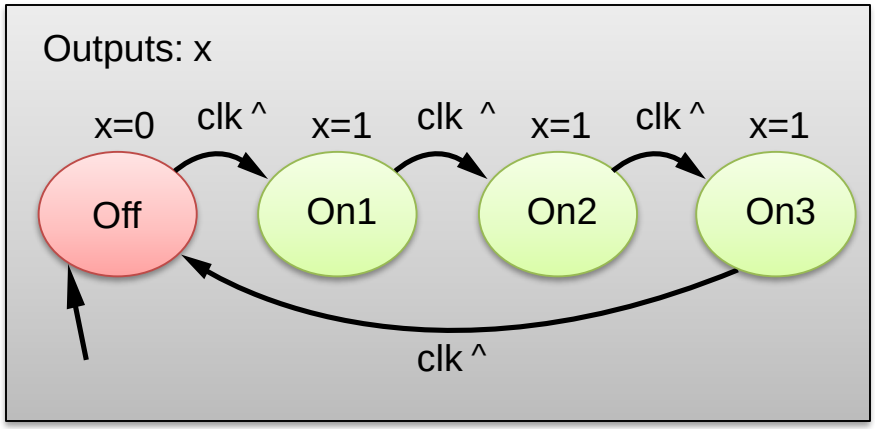


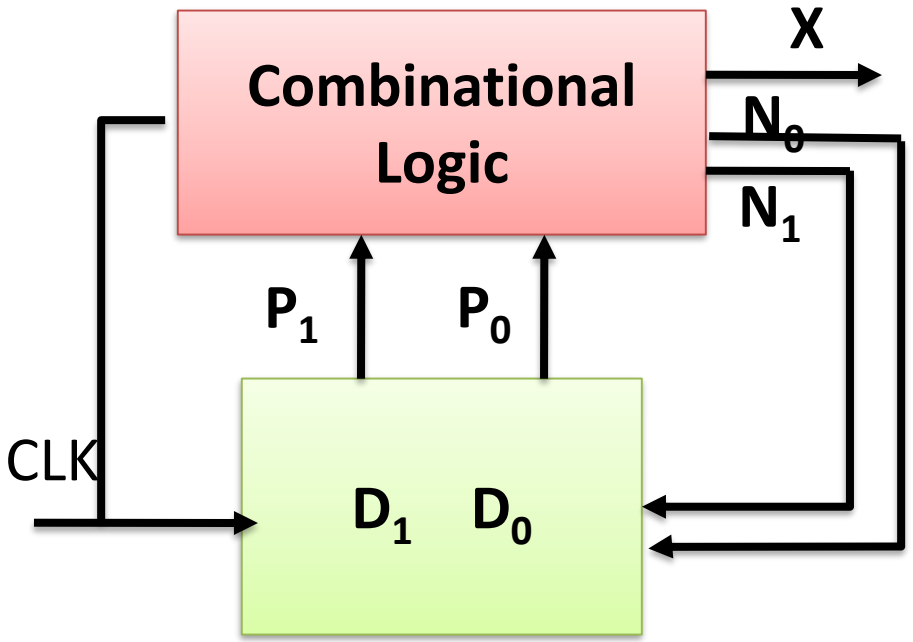
PS	NS	X
00	01	0
01	10	1
10	11	1
11	00	1

Require two FF to store states

Controller of FSM Example: 0,1,1,1,repeat

Input		Output		
CLK	PS P_1 P_0		NS N_1 N_0	X
RE 1	0 0		0 1	0
RE 1	0 1		1 0	1
RE 1	1 0		1 1	1
RE 1	1 1		0 0	1

D-FF used to store the Present state



$X=P_1+P_0$

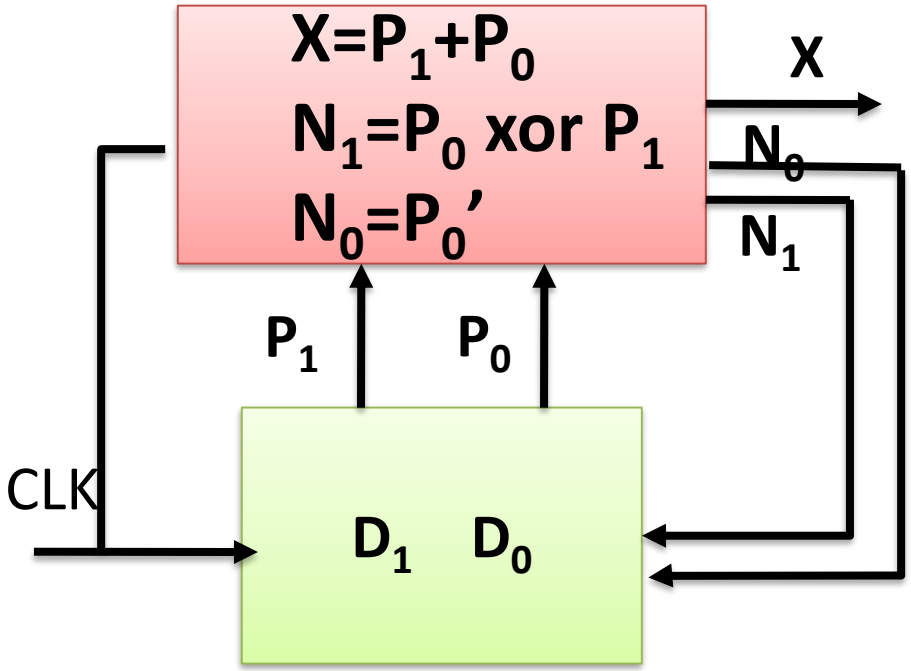
$N_1=P_0$ xor P_1

$N_0=P_0'$

Rising Edge: Clock implicit

Controller of FSM Example: 0,1,1,1,repeat

Input		Output		
CLK	PS P_1 P_0		NS N_1 N_0	X
RE 1	0	0	0 1	0
RE 1	0	1	1 0	1
RE 1	1	0	1 1	1
RE 1	1	1	0 0	1



D-FF used to store the Present state

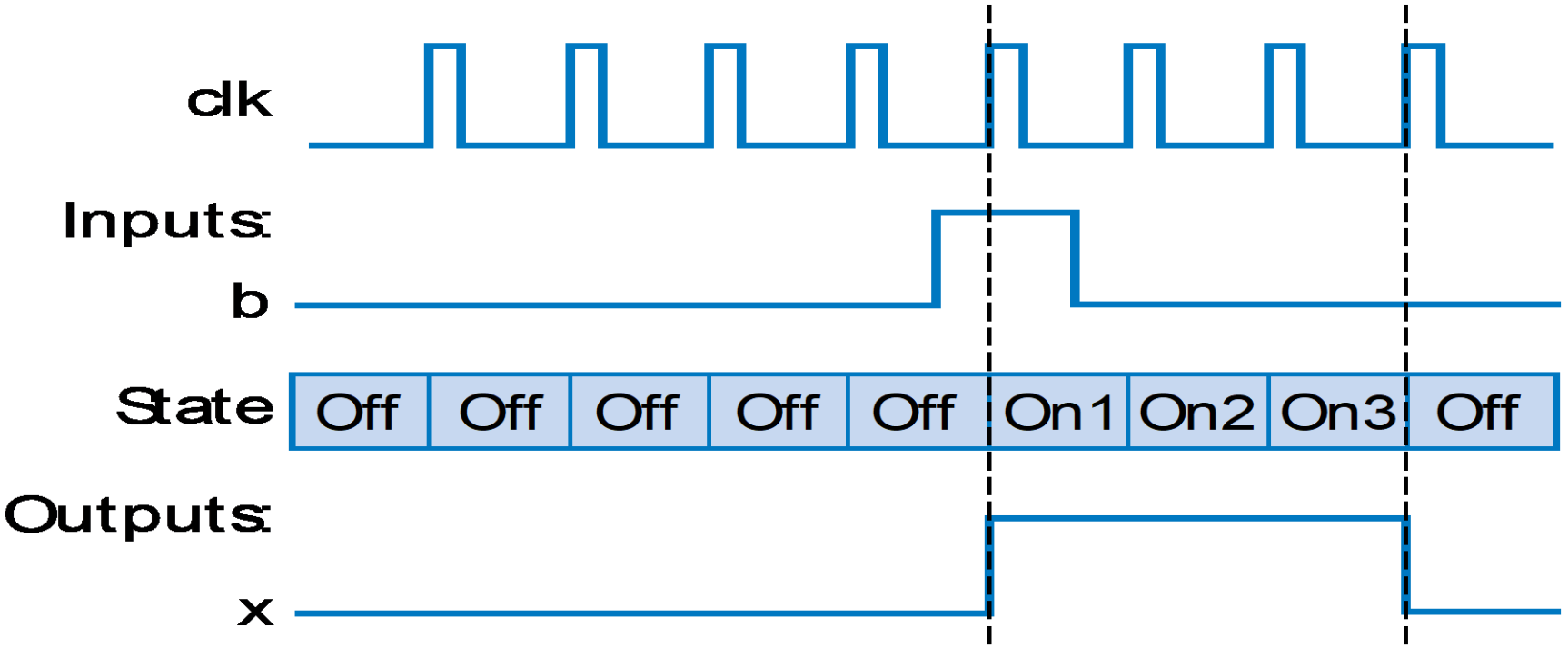
Rising Edge: Clock implicit

FSM Example 7:
Three-Cycles High Laser Timer

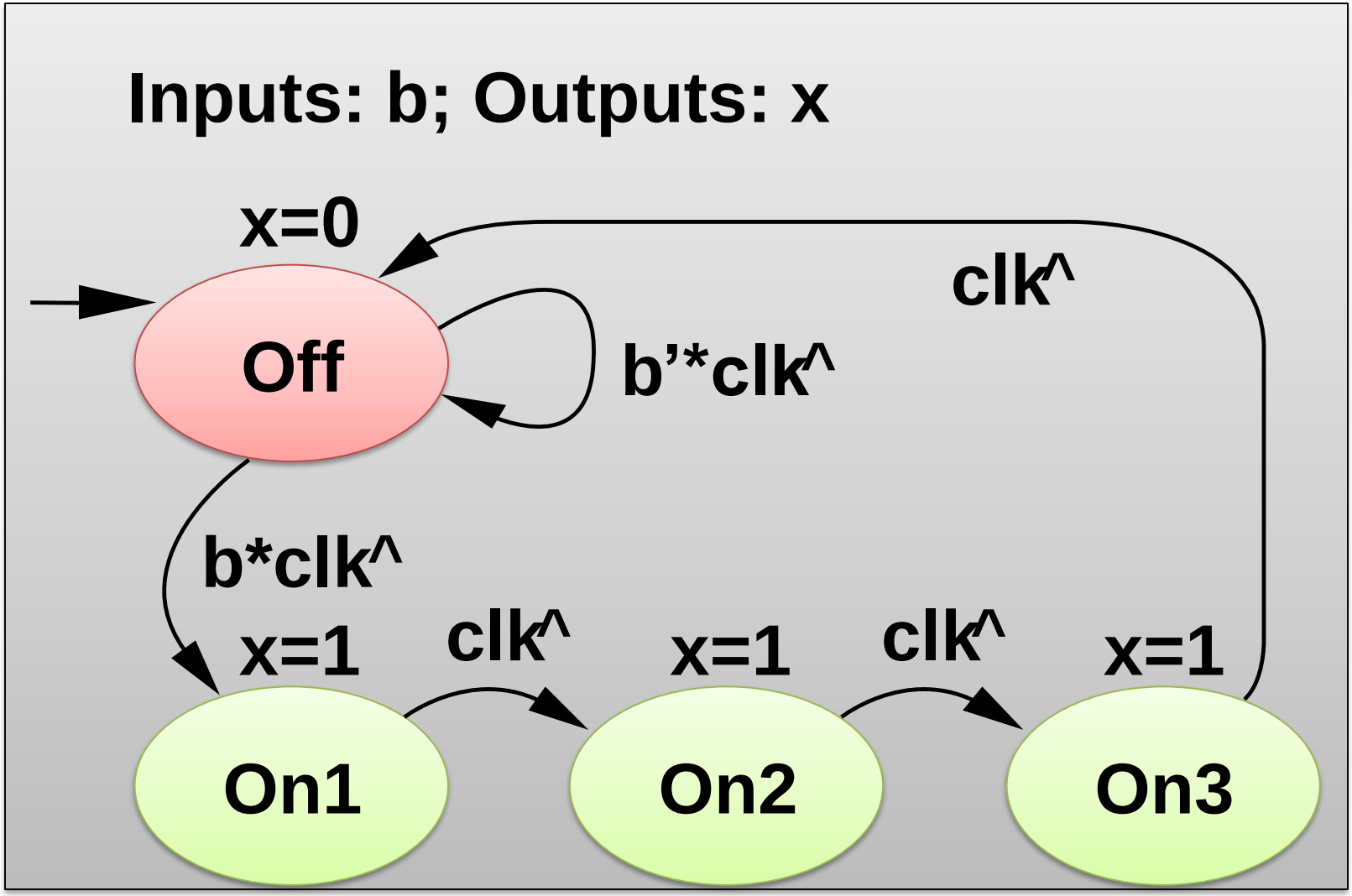
Extend FSM to Three-Cycles High Laser Timer

- Four states: Wait in “Off” state while b is 0 (b’)
- When b=1 (& rising clock edge), transition to On1
  - Sets X=1
  - On next two clock edges, transition to On2, then On3, which also set x=1
- So x=1 for three cycles after button pressed

Extend FSM to Three-Cycles High Laser Timer



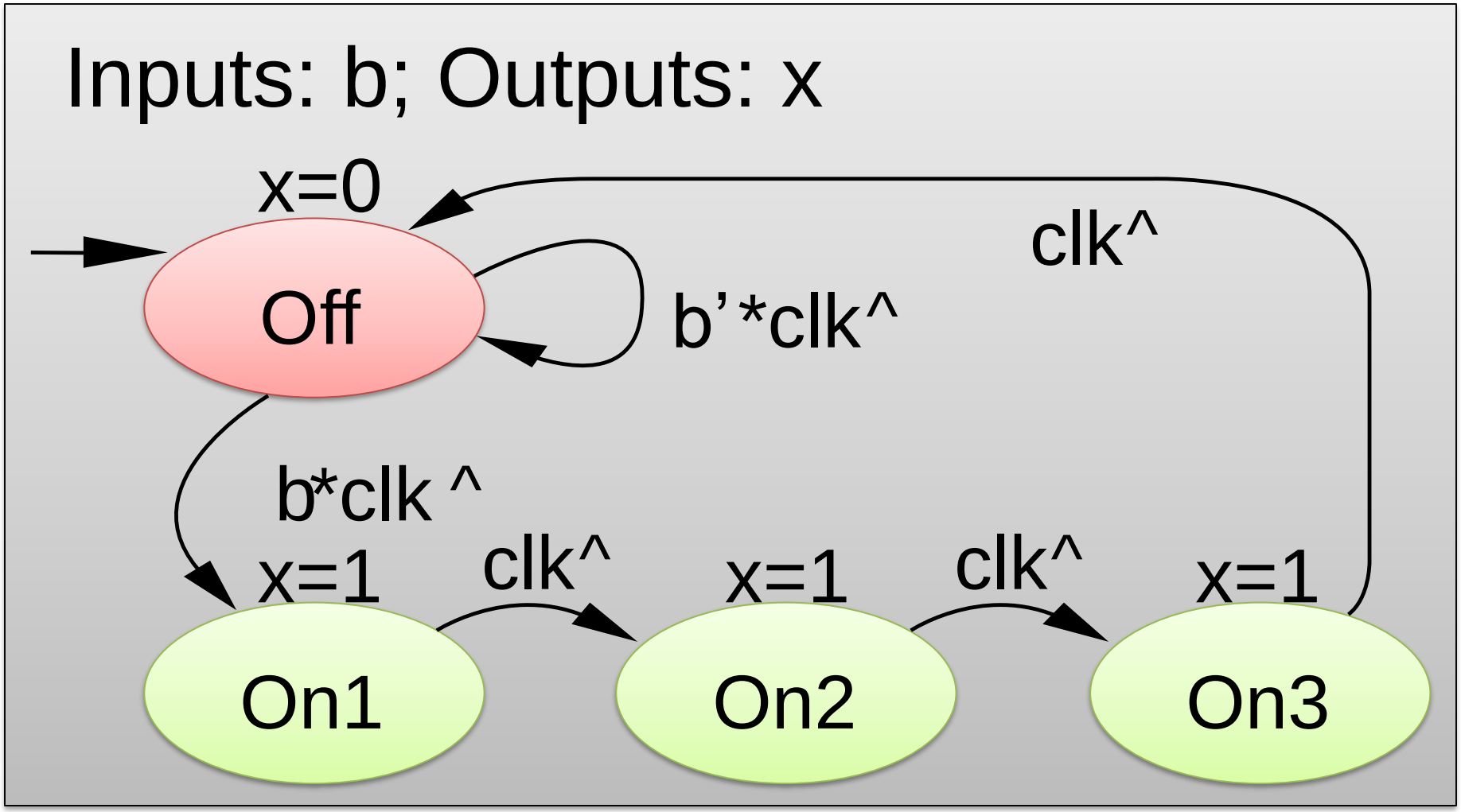
Extend FSM to Three-Cycles High Laser Timer



FSM Simplification: Rising Clock Edges Implicit

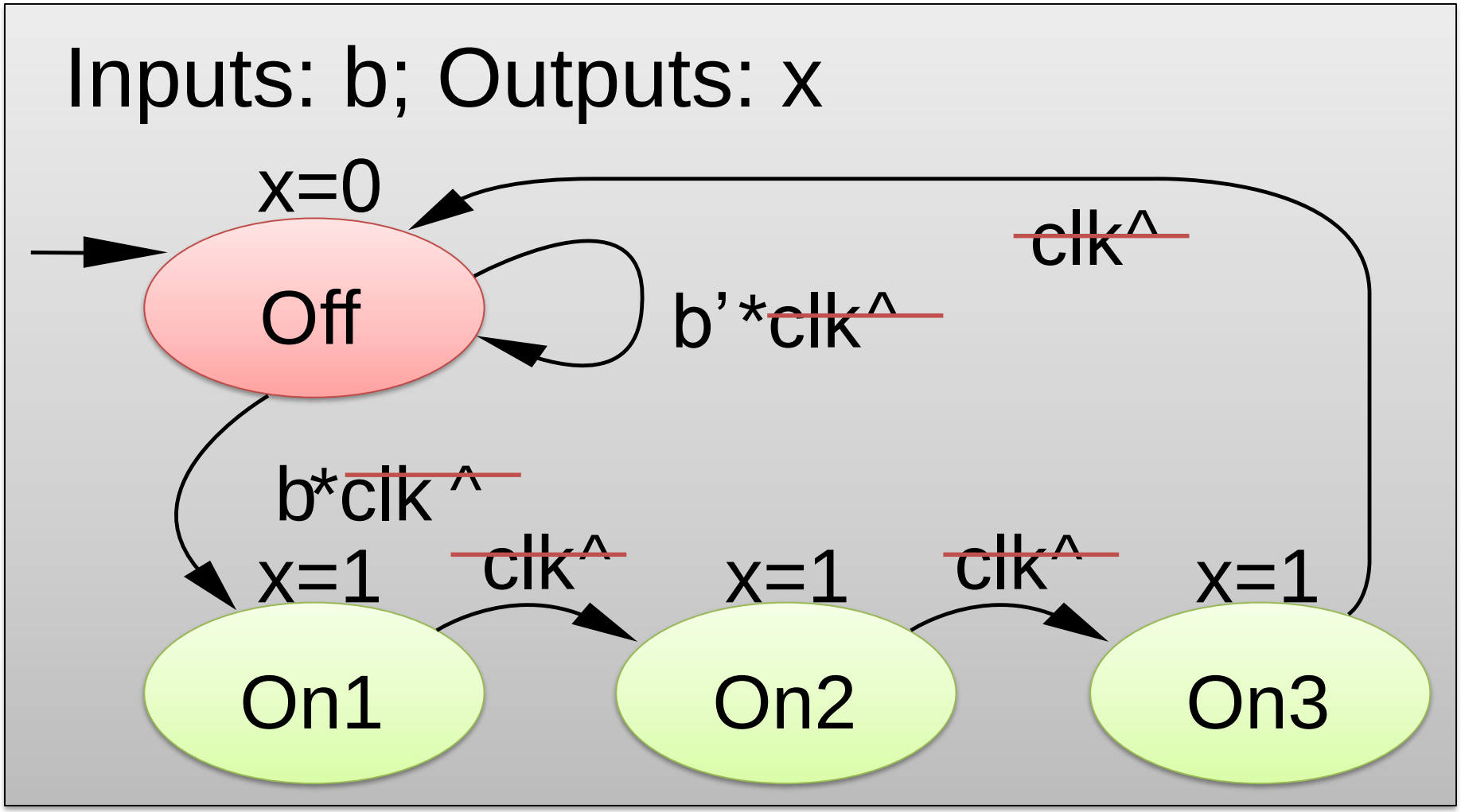
- Showing rising clock on every transition: cluttered
- Make implicit -- assume every edge has rising clock
- What if we wanted a transition *without* a rising edge
  - **Asynchronous FSMs -- less common, and advanced topic**
  - We consider ***synchronous*** FSMs
  - ***All* transition on rising edge**

FSM Simplification: Rising Clock Edges Implicit



Note: Transition with no associated condition thus transistions to next state on next clock cycle

FSM Simplification: Rising Clock Edges Implicit



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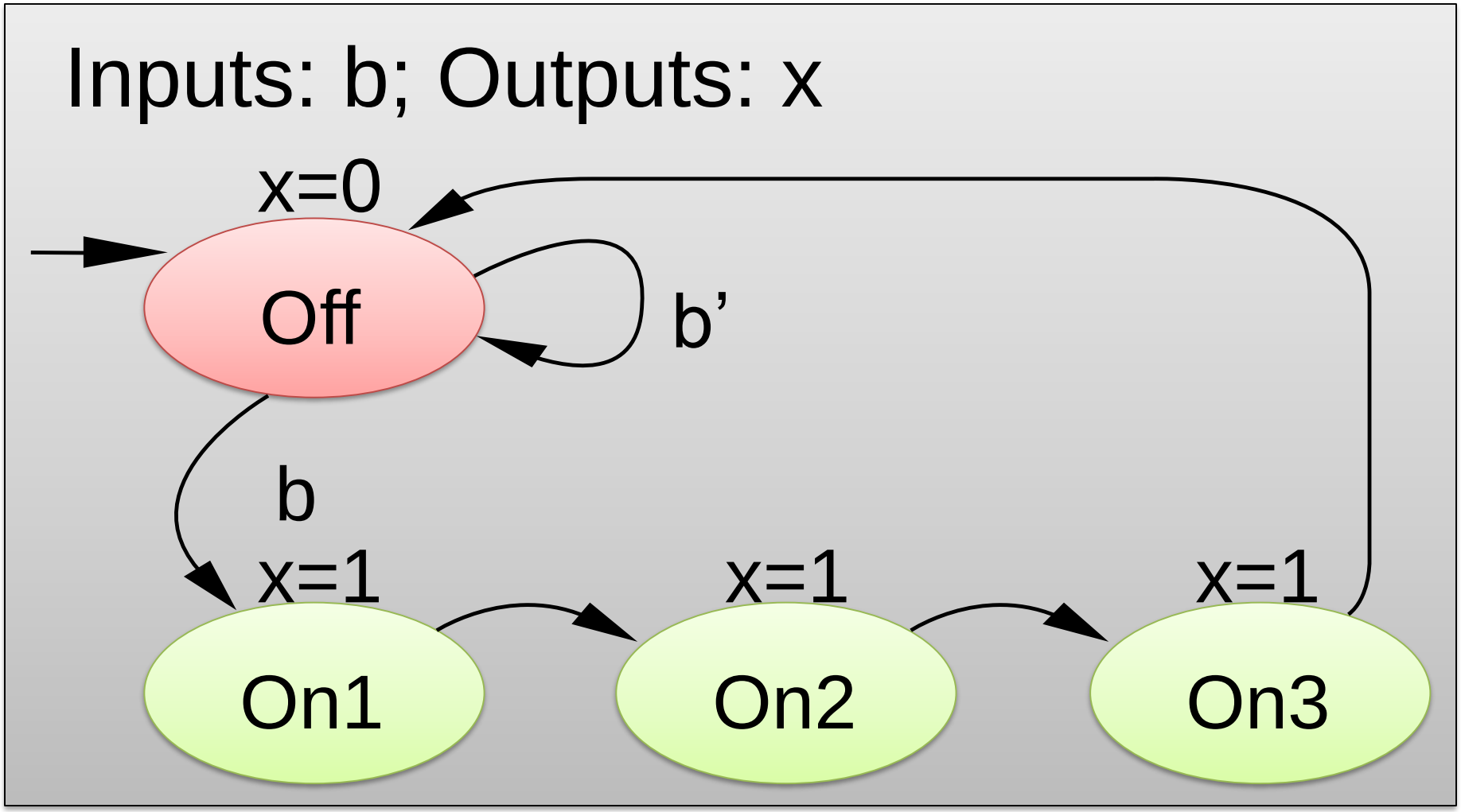
FSM Simplification: Rising Clock Edges Implicit



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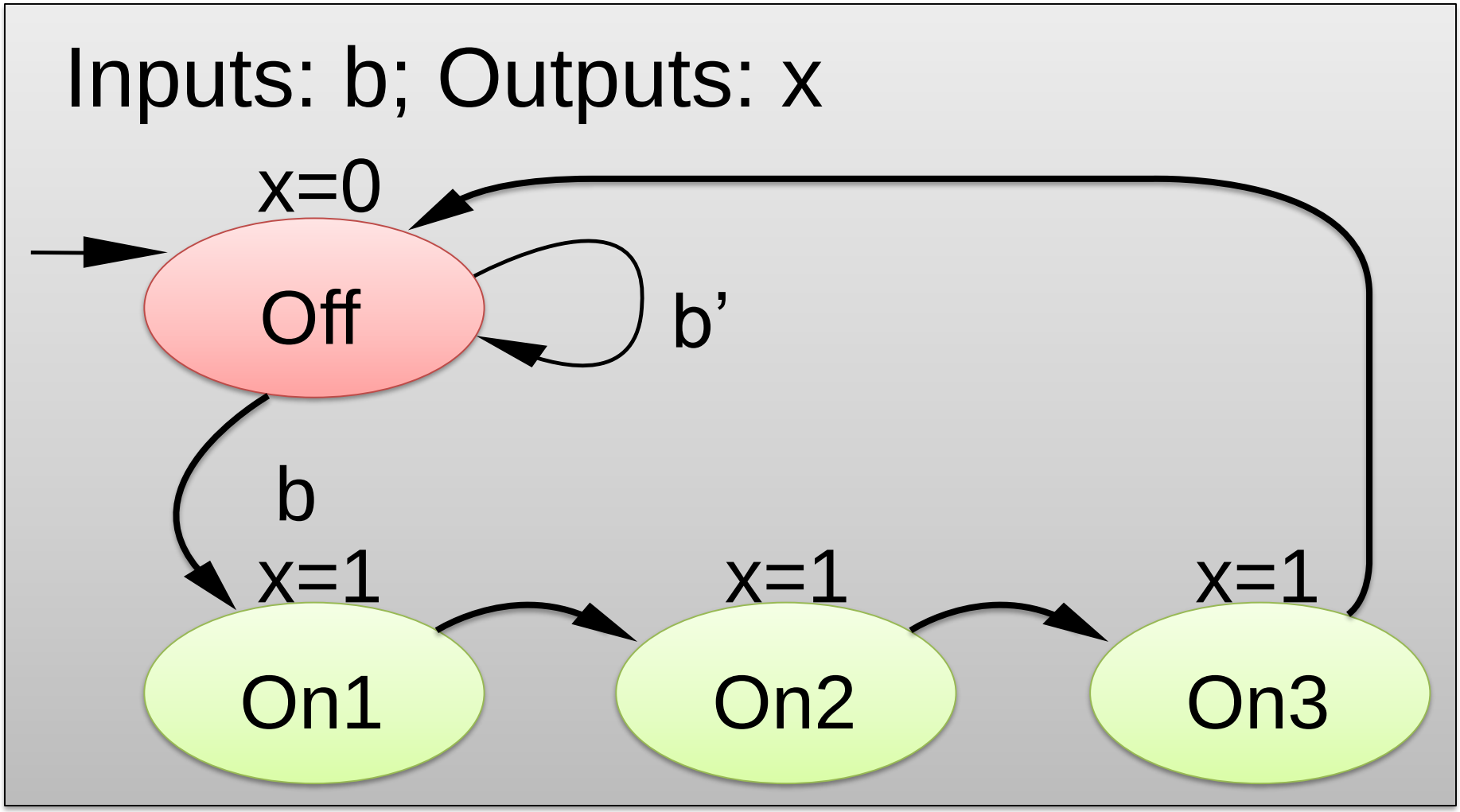
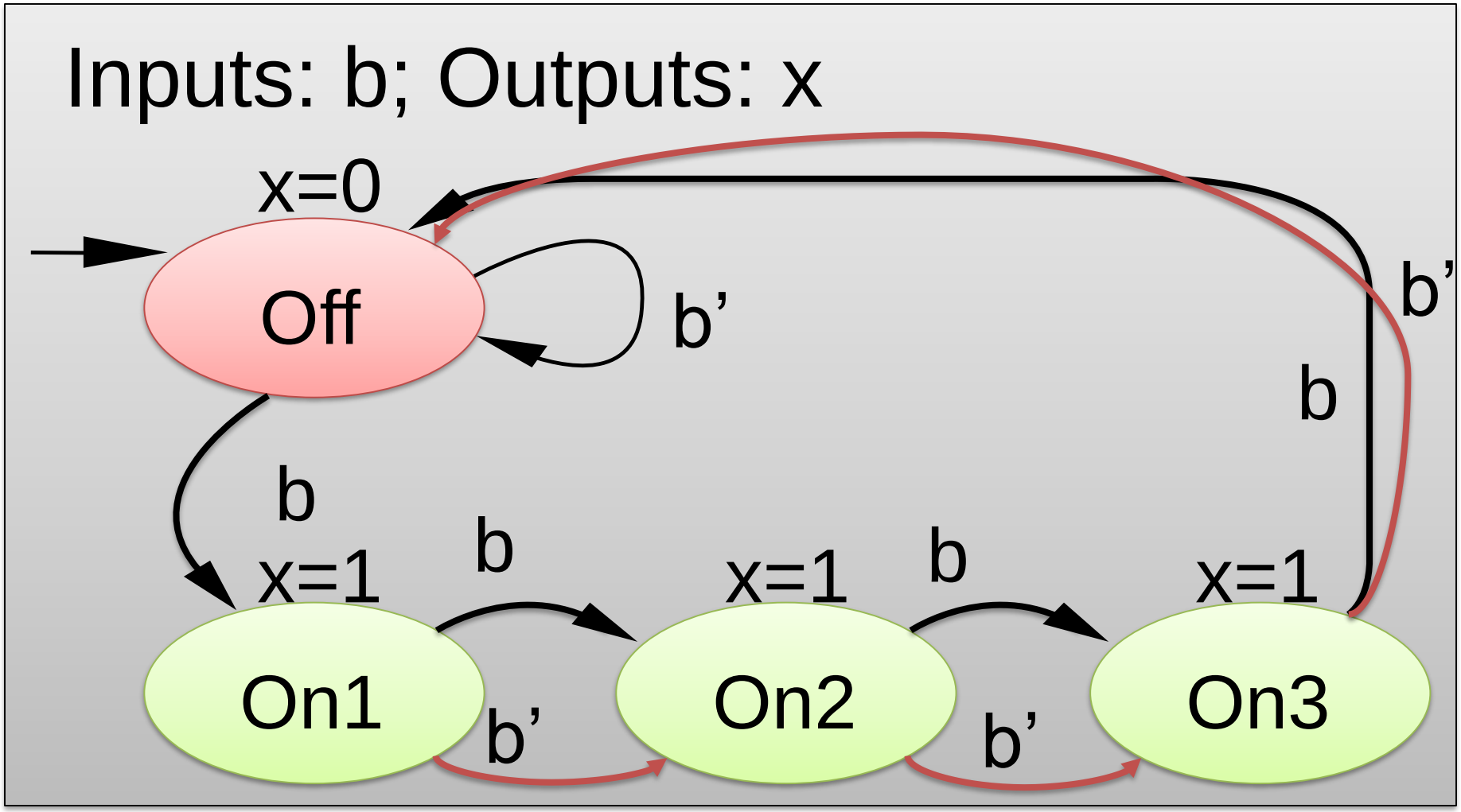


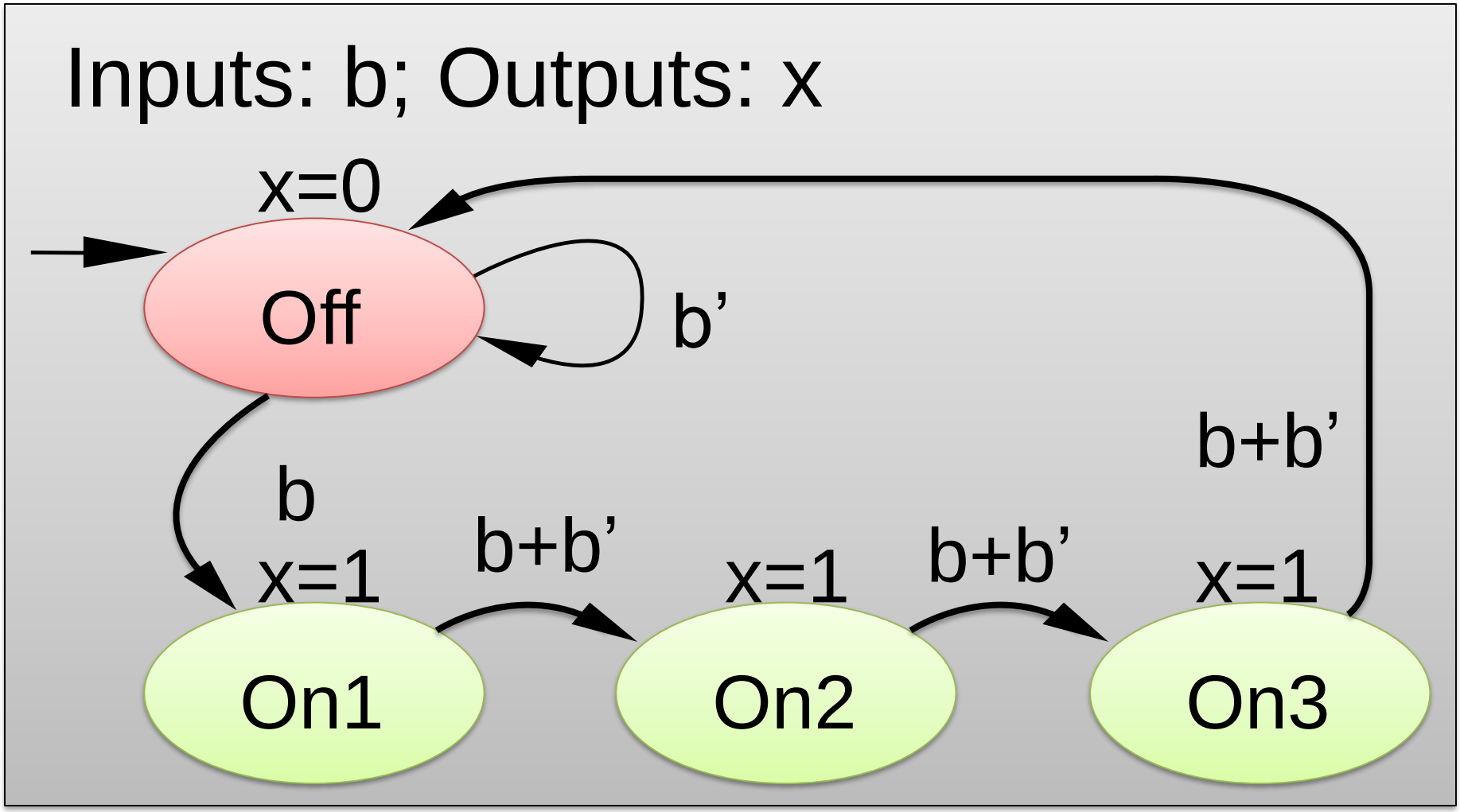
Value of b=1: 0111..repeat, ***Is this FSM is complete?***

FSM Simplification: Rising Clock Edges Implicit



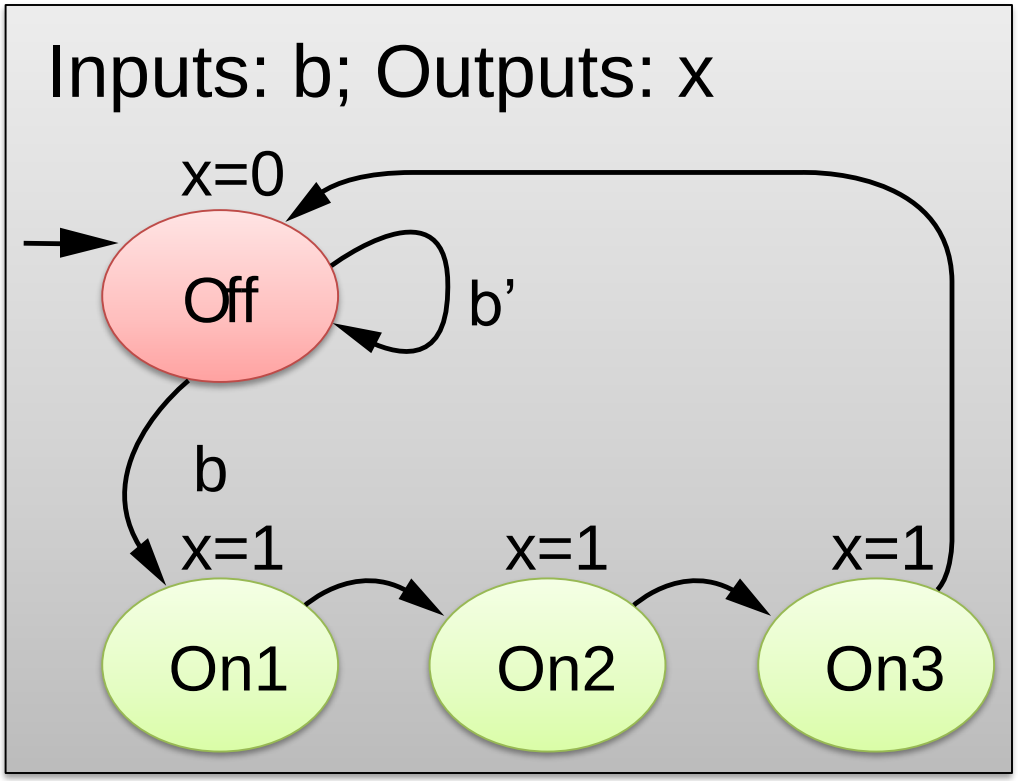
Value of b=1: 0111..repeat, ***Is this FSM is complete?***

FSM Simplification: Rising Clock Edges Implicit



Value of b=1: 0111..repeat, ***Is this FSM is complete?***

FSM Implementation : Three-Cycles High Laser Timer



PS	b	NS	X
00	0	00	0
00	1	01	0
01	x	10	1
10	x	11	1
11	x	00	1

FSM Implementation : Three-Cycles High Laser Timer

PS	b	NS	X
00	0	00	0
00	1	01	0
01	x	10	1
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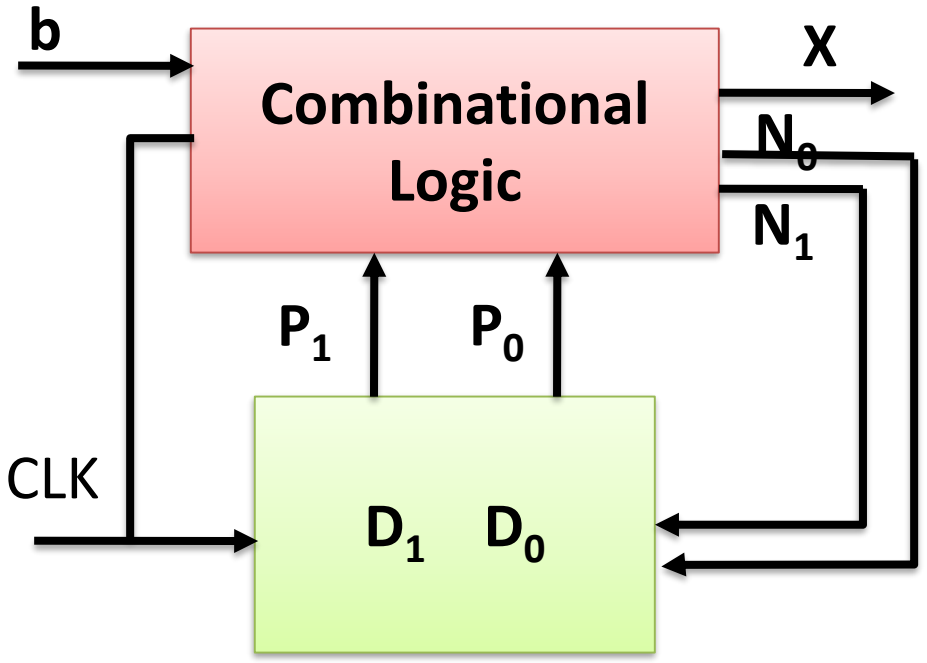
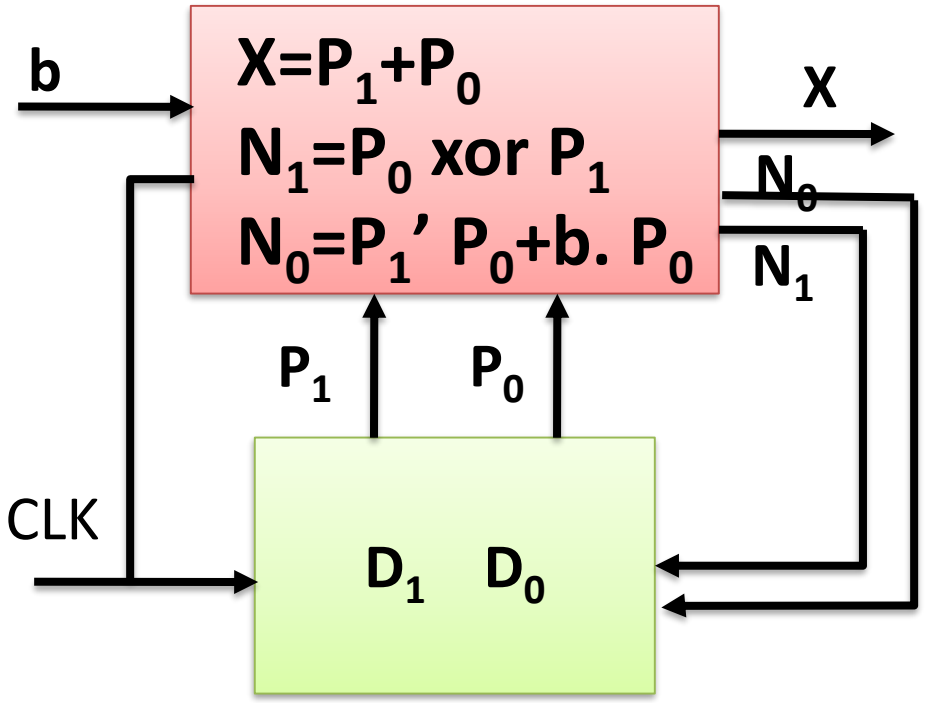


FSM Implementation : Three-Cycles High Laser Timer

PS	b	NS	X
00	0	00	0
00	1	01	0
01	x	10	1
10	x	11	1
11	x	00	1



Once we specify FSM for a problem/system

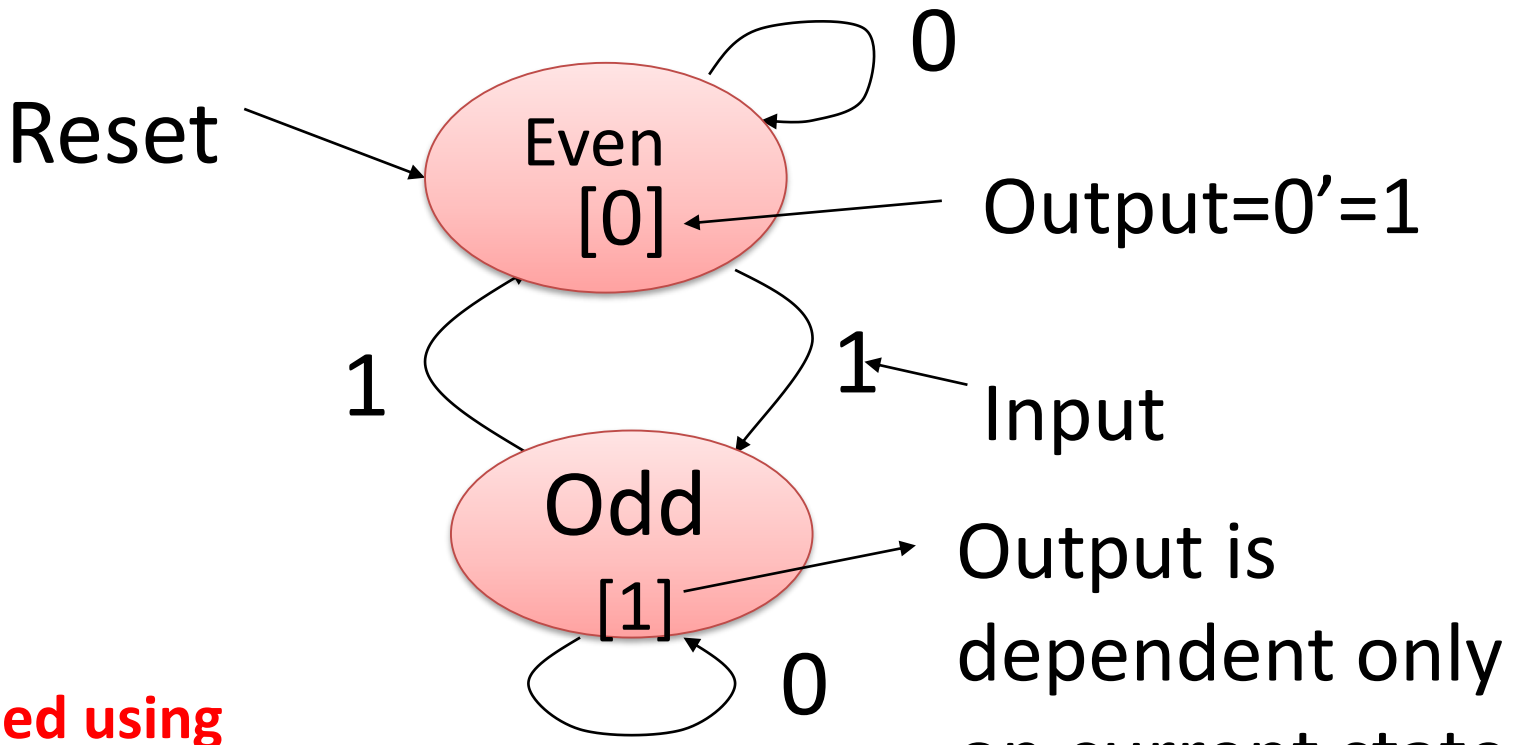
=== >

Implementation is not difficult

FSM Example 8:
Parity Encoder

FSM Example 8: Parity Encoder

- Input: 1 or 0 // entering as stream
- Out put: output a 1 when total number of 1 is even

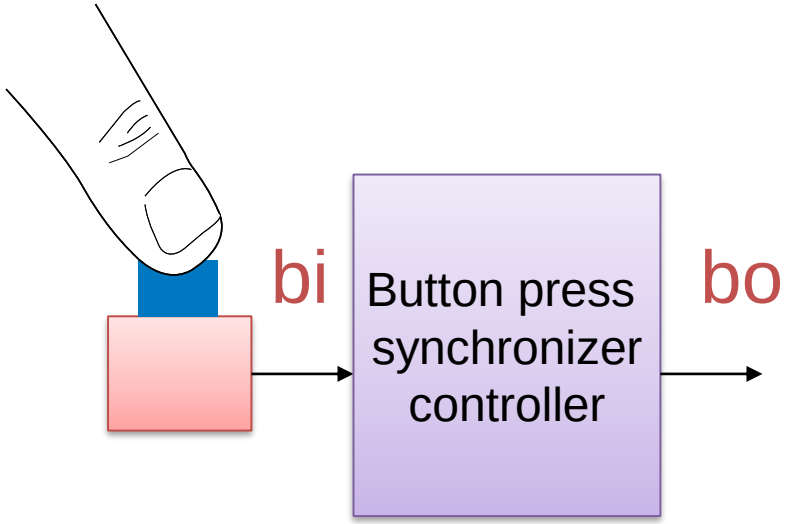


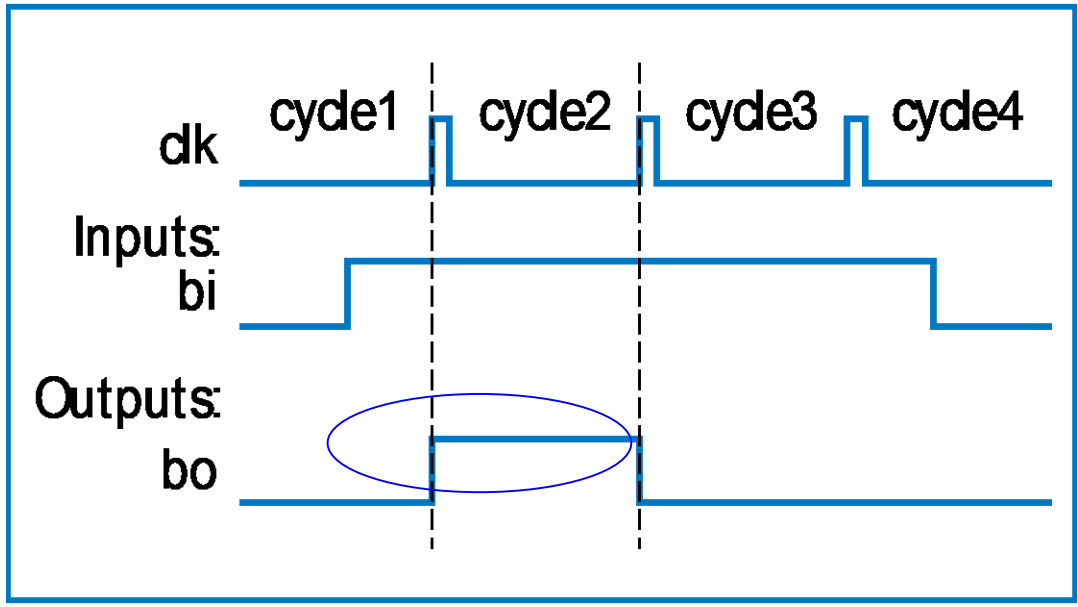
T- FF : designed using D-FF

FSM Example 9:
Button Press Synchronizer

Example 9 : Button Press Synchronizer

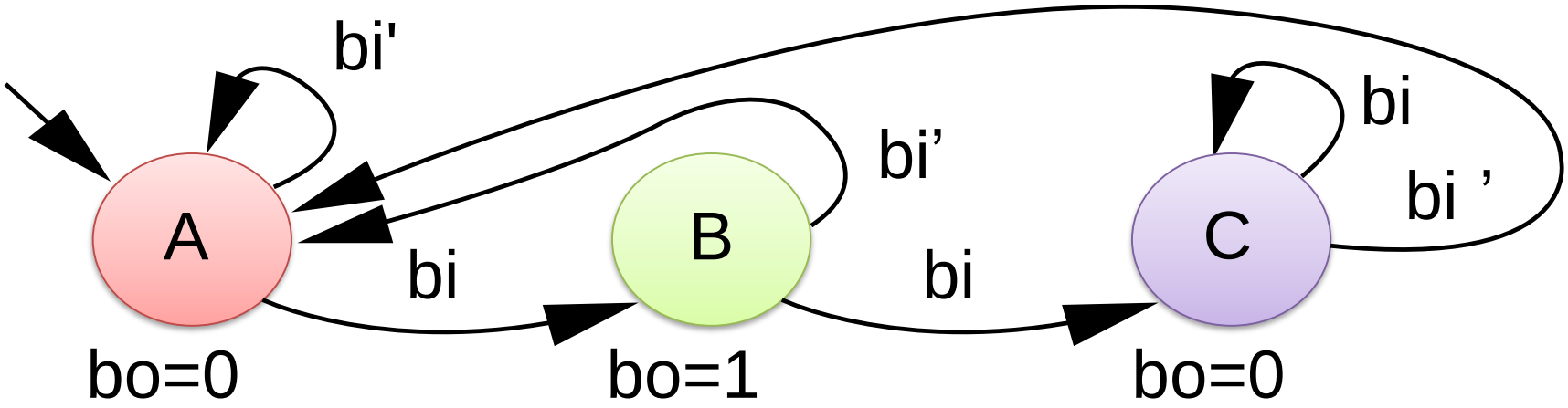
- **English Language Specification**
- **All most all the keyboards use this method**
- We want simple sequential circuit
  - Converts button press to single cycle duration
  - Regardless of length of time that button actually pressed





FSM Example 9 : Button Press Synchronizer

FSM inputs: bi; FSM outputs: bo



I am Off When B=0

I am On in First CLK and When B=1

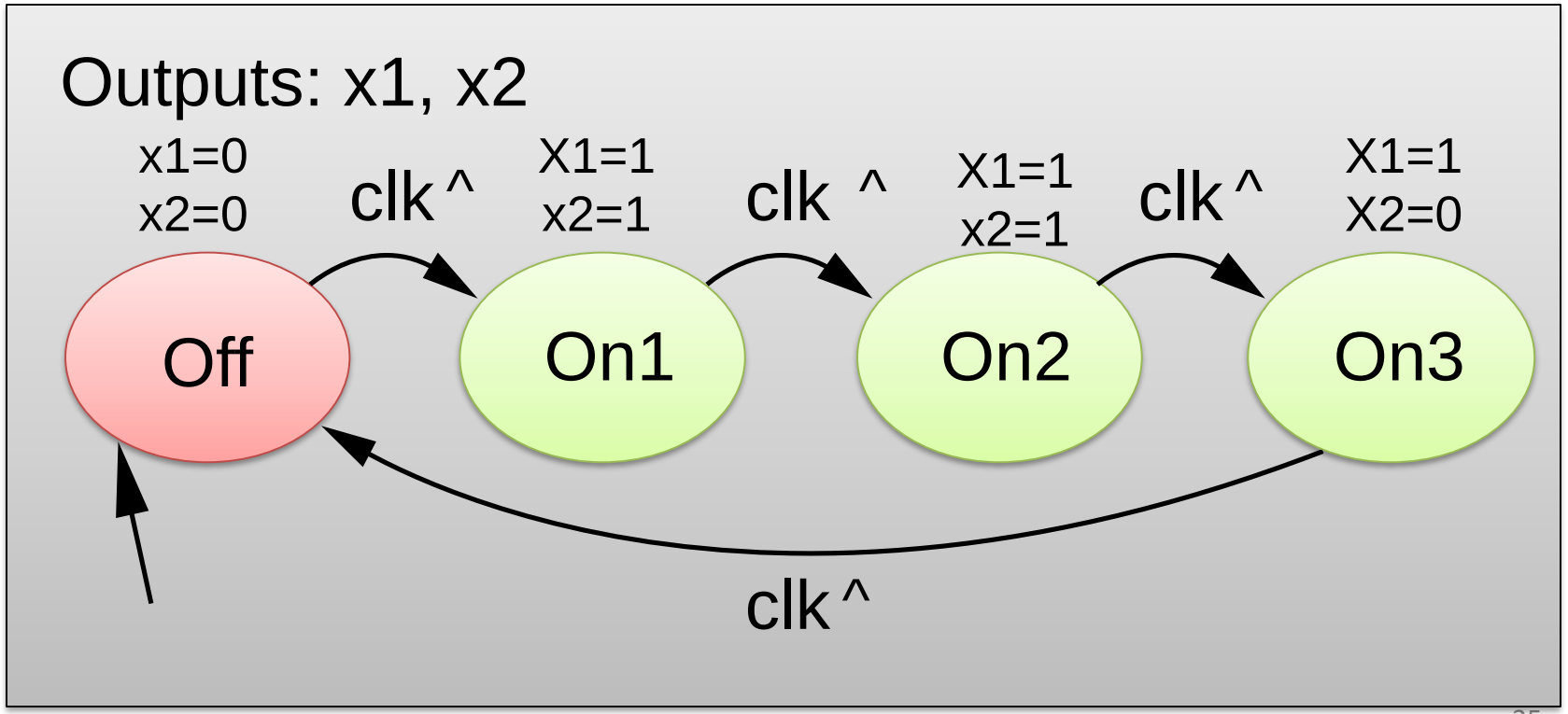
I am Off Even if B=1

Step 1: Design FSM

FSM Example 10: Sequence generator

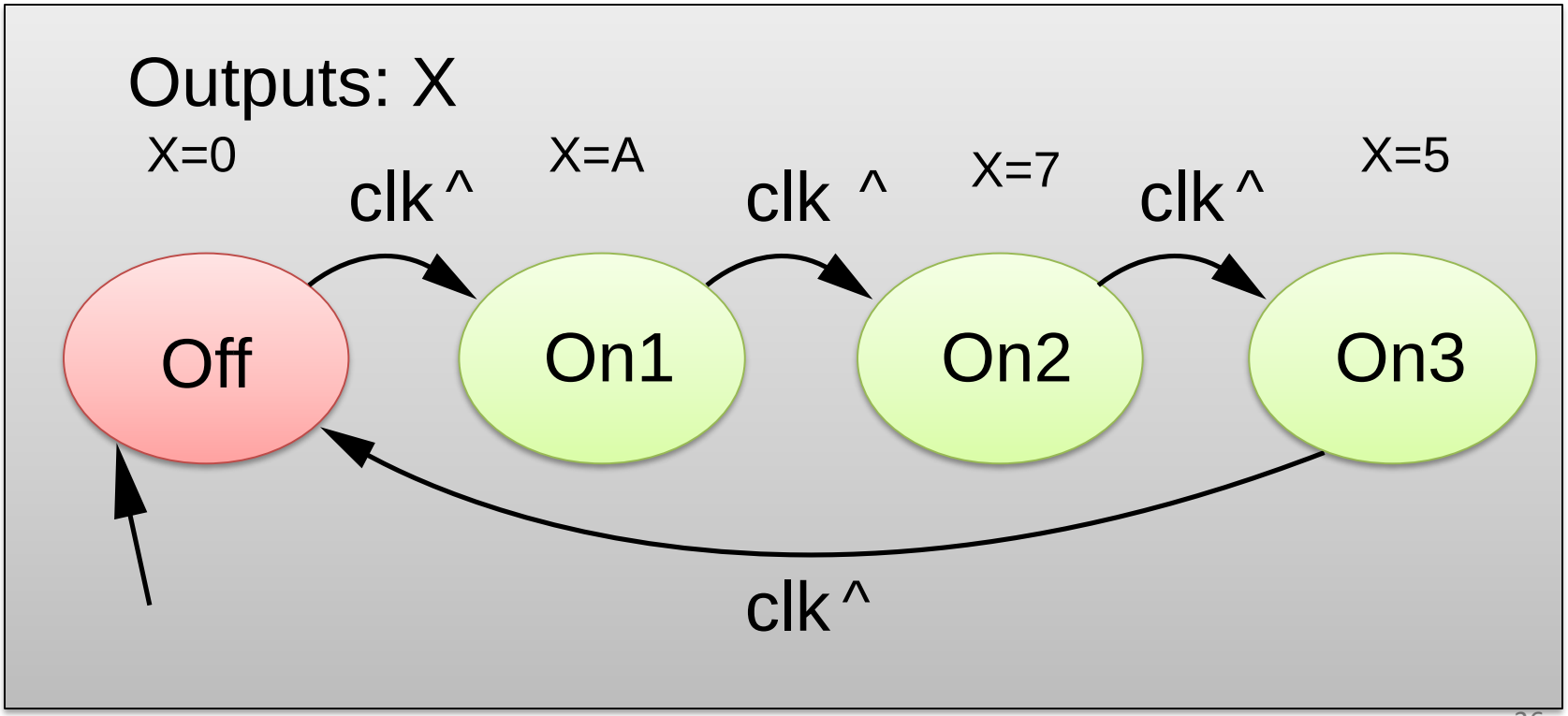
FSM Example 10: Sequence generator

- Generate two output sequence
  - X1= 0111….repeat
  - X2= 0110…repeat



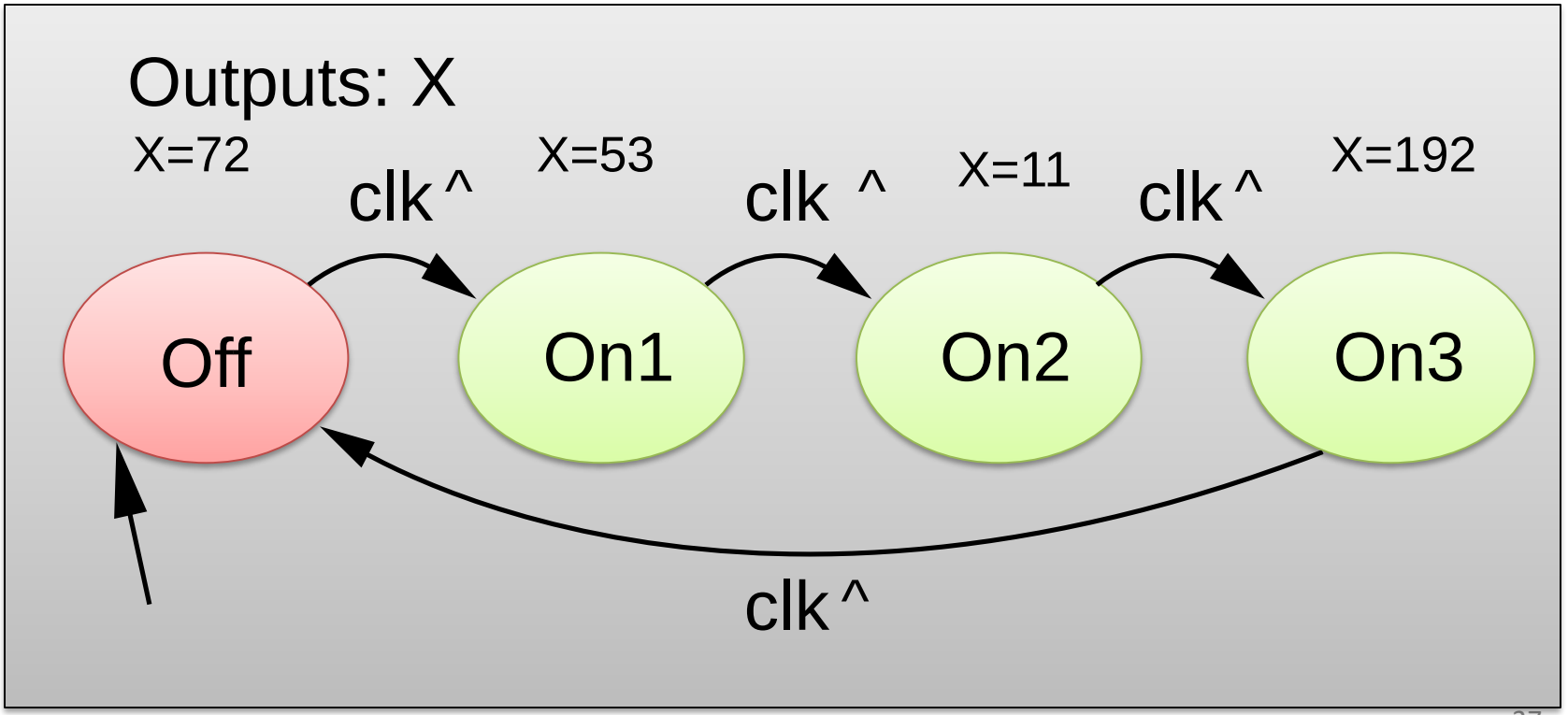
FSM Example 10-E1: Sequence generator

- Generate 4 bit integer output sequence
  - X= 0, A, 7, 5….repeat
  -



FSM Example 10-E2: Sequence generator

- Generate 8 bit integer output sequence
  - X= 72, 53, 11, 192,….repeat
  -



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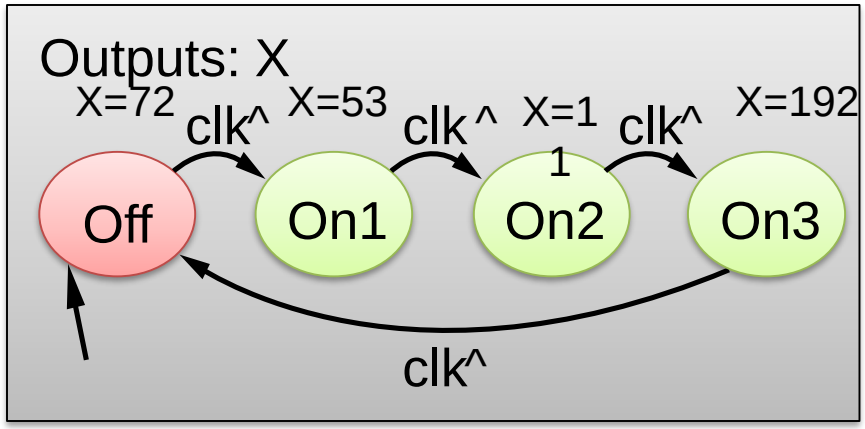

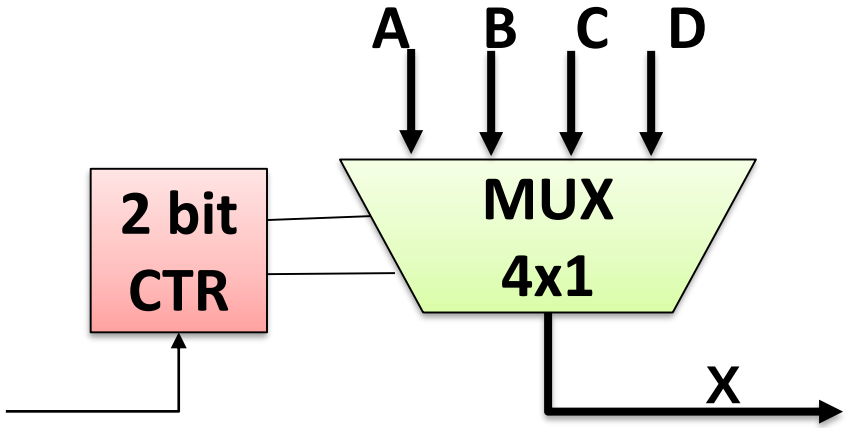

A,B,C,D values can be hardwired

FSM Example 10-E2: Sequence generator

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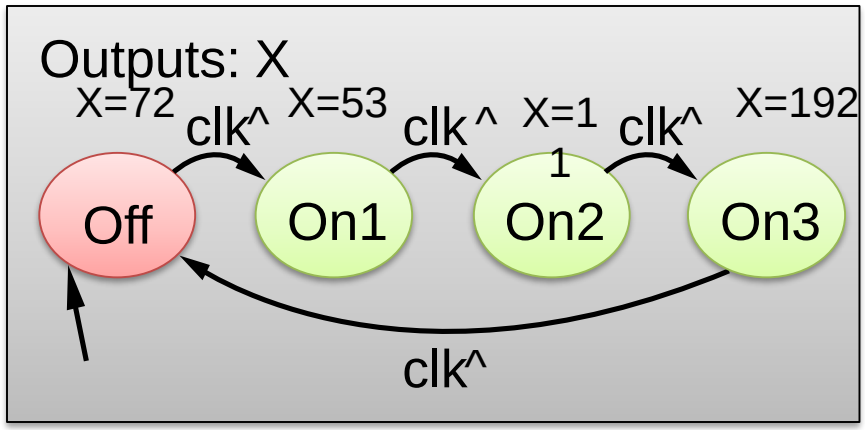
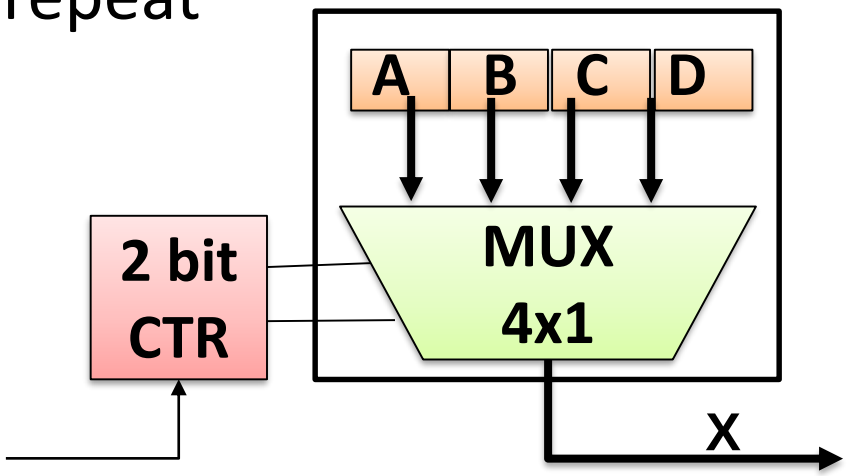
  - X= 72, 53, 11, 192,….repeat





A,B,C,D values can stored in 4 register (With Mux it act as memory)

FSM Output logic may be Simpler than Register and Mux

Simpler to Implemen Outputlogic: Eight 2 input binary function