Pranav Kumar

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RESEARCH INTERESTS

Computer Systems, Computer Architecture and Digital Electronics

EDUCATION

- **Indian Institute of Technology Kanpur, India**   Expected: June 2017
  B.Tech. in **Electrical Engineering**
  Minor in **Computer Systems** (Computer Science and Engineering)
  CGPA of **9.1/10** (**9.4/10** in major), after 6th semester
- **St. John's School, Varanasi, India**   2012
  Class XII - Indian School Certificate (ISC) - **95.2%**
- **St. John's School, Varanasi, India**   2010
  Class X - Indian Certificate of Secondary Education (ICSE) - **94.8%**

PUBLICATIONS

- **Pranav Kumar** and Lavisha Aggarwal, "An Integrated Approach to Robust Exemplar-based Object Removal", *International Conference on Advances in Signal, Image and Video Processing (SIGNAL 2017)*, Barcelona, Spain, 2017 (under peer review).

SCHOLASTIC ACHIEVEMENTS

- Awarded the **Academic Excellence Award** by IIT Kanpur for outstanding performance in the term 2013-14.
- Awarded a travel grant to **Aalborg University Copenhagen** for the Workshop in Innovation and Entrepreneurship (WOFIE) 2016
- Selected for the **Summer Research Fellowship Programme 2016** by the Indian Academy of Sciences.
- Awarded the **Ericsson Innovation Award-2015** by Ericsson, conferred to top 6 projects in India.
- Secured **A*** grade in the course **Microelectronics** for exemplary academic performance.
- Secured an **All India Rank 1** in **SCRA-2013** and **Rank 5** in **UPSEE-2012**.
- Awarded the **Indra Dhanush Donors' Scholarship** for excellence in academics and strong leadership skills for the freshmen and sophomore years.
- Secured an **All India Rank 520** in **IIT-JEE (Advanced)-2013** among 1.4 million candidates.
- Secured an **All India Rank 17** in **National Level Science Talent Search Examination-2012**.
- Secured an **International Rank 24** in the **International Mathematics Olympiad**, **128** in the **National Science Olympiad** and **201** in the **National Cyber Olympiad**, conducted by the Science Olympiad Foundation.

INTERNSHIPS

- *New York University* – **Design of a 10 GHz Class-A Power Amplifier using a Gallium Nitride Radio-Frequency Device Model**   May 2016 - July 2016
  Mentored by Prof. Shaloo Rakheja, Dept. of ECE, New York University   [Presentations]
  - Extensively reviewed literature on GaN, its behavioral nuances and associated device models.
  - Used the MIT Virtual-Source GaN RF model to design a single-stage 2.14 GHz power amplifier with a given optimum impedance for maximum power flow. Constructed the matching circuits and verified the design by running S Parameter simulations.
  - Moved on to designing a 10 GHz (SHF Microwave Spectrum) Class-A Power Amplifier. After DC Biasing and checking for small signal stability, performed Load- and Source-Pull analyses to extract the optimum impedance data. The circuit was constructed and its performance verified.
  - Studied the impact of technological parameters like Source Injection Velocity, Low-Field Mobility and Access-Region Sheet Resistance on the performance.
  - Based on this, further optimized the design to yield a 6 dBm increase in gain. Inter-Modulation Distortion and Adjacent Channel Power Rejection was also found out in case of modulated signals.
  - Apart from this, mentored a junior undergraduate in my research group and helped him understand the fundamental concepts of device physics and the various quasi-ballistic and ballistic models of nanotransistors, specifically the MIT Virtual Source Models 1 and 2.

- *New York University* – **An improved Virtual-source based transport model for quasi-ballistic transistors, MIT Virtual Source Model (MVS-2.0)**   May 2015 - July 2015
  Mentored by Prof. Shaloo Rakheja, Dept. of ECE, New York University
  - Gained an in-depth knowledge of the essential physics behind nanoscale transistors.
  - Solved coupled Schrödinger-Poisson equation for III-V High electron mobility transistors (HEMTs) and implemented quantum well InGaAs heterostructure devices to study the role of gate voltage and carrier confinement in low effective mass materials.
  - Simulated MVS 1.0.1 in Spectre, and verified it by running netlists like inverter and ring oscillators.
  - Worked on implementing a revised model in Verilog-A which took into account the dependence of carrier injection velocity on concentration, the VS charge on the non-equilibrium channel transport conditions and the non-linearity of access region resistances.
  - The revised MVS-2 model is now deployed on nanohub-U.

RESEARCH PROJECTS

- **FPGA Implementation of an 8-bit Microprocessor and Audio Monitoring System**   July 2016 - Nov 2016
  Mentored by Prof. S. Qureshi, Electrical Engineering, IIT Kanpur   [Code] [Report] [Presentation]
  - Implemented an 8-bit microprocessor on FPGA (Xilinx Virtex-II Pro using Verilog).
  - The Control Unit was modeled as a Finite State Machine, ALU as a digital circuit and Memory as a 256-word 8-bit. Each bit of the memory in an SRAM cell was implemented with an AND gate, a D-latch, and a tri-state buffer.
  - Further, the on-board analog-to-digital converter (ADC) was made use of in developing an audio monitoring system. The system raised an alarm whenever the input audio signal was deterministic.

- **Image Inpainting: Exemplar-based Object Removal from Images**   Aug 2016 - Nov 2016
  Mentored by Prof. Tanaya Guha, Dept. of Electrical Engineering, IIT Kanpur   [Report] [Presentation]
  - Reviewed literature on the existing exemplar-based image inpainting and object removal techniques.
  - Implemented Criminisi et al's algorithm which searched the source region iteratively and filled in the damaged part with the best matched patch.
  - Some modifications were added in terms of a regulariser, a variance criterion for patch selection and usage of the edge map technique for the data term.
  - Proposed and implemented a novel adaptive regularizer and an improved criterion for patch selection which yielded results better than the state-of-the-art.
  - Adjudged as the **Best Project** for the course. Work done has been submitted to **SIGNAL, 2017**.

- **Computer Vision: 3D Display and User Interface**   Dec 2014 - Oct 2015
  Mentored by Prof. K.S. Venkatesh, Dept. of Electrical Engineering, IIT Kanpur   [Presentation]
  - Developed a desktop application for visualizing the perspective view of a 3D object.
  - Performed face detection via front camera and processed these captured face coordinates in the image to determine the viewer's actual physical location relative to the screen.
  - The actual 3D view expected to be seen by the user is displayed in real-time giving an almost life-like 3D experience.
  - Selected among the top 6 projects at the **Ericsson Innovation Awards** and awarded INR 25000.
  - Featured by Mint, Silicon India, Storypick, Networked India and OnlineShop4Me.

- **Extension of NachOS**   Aug 2016 - Nov 2016
  Mentored by Prof. Mainak Chaudhuri, Dept. of Computer Science and Engineering, IIT Kanpur
  - Implemented fork, join, exec, yield, sleep and exit system calls on NachOS.
  - Programmed FIFO, SJF, Round Robin, Priority and Unix scheduling algorithms with different time quantas. Compared them on the basis of CPU utilization and average wait time.
  - Implemented and compared FIFO, LRU and LRU-clock page replacement algorithms.

- **An Improved CMOS Design for a Full Adder Circuit**   Aug 2016 - Nov 2016
  Mentored by Prof. S. Qureshi, Dept. of Electrical Engineering, IIT Kanpur   [Report] [Presentation]
  - Reviewed literature on the existing full adder circuits.
  - Subsequently proposed a 1-bit modified full adder design employing CMOS logic and implemented it on Mentor Graphics using 180nm technology.
  - The circuit functioned with lesser number of transistors and lower power consumption.

OTHER PROJECTS

- **Network Simulation** — Apr 2014 - July 2014
  Mentored by Prof. Ketan Rajawat, Dept. of Electrical Engineering, IIT Kanpur
  - Reviewed literature on the fundamentals of computer networks.
  - Studied Transmission Control Protocol, routing and multicast protocols and simulated the same on the discrete event simulator, NS2, and network animator (NAM).

- **Udghosh-2014 Website** — July 2014 - Aug 2014
  - Created the website for the Institute Inter-Collegiate Sports Festival using HTML, CSS and Javascript.

- **Google Developer Groups DevFest-2013** and **Microsoft Code.Fun.Do 2014**
  - Designed BookMyTee, a shopping website in the 24-hour coding competition GDG DevFest 2013.
  - Built a Computer vision based Windows Desktop application in Code.Fun.Do.
  - Awarded a Special Mention in DevFest 2013.

- **Working Model of a Tornado** — July 2014 - Nov 2014
  Course Project, Mentored by Prof. Shashank Shekhar, IIT Kanpur
  - Made an accurate down-scaled model of a tornado using basic metal forming techniques like casting, brazing, welding and sheet metal cutting. Awarded the **Section Best** and the **overall Runner-up**.

WORKSHOPS ATTENDED

- *Aalborg University, Copenhagen* – **Consulting Company Model for Municipality and Waste Service Suppliers** [Presentation]
  Organized under Workshop for Innovation and Entrepreneurship (WOFIE) Denmark   March 2016
  - Won a travel grant to Aalborg University Copenhagen for WOFIE 2016.
  - Designed a model of a consulting company for the Municipality and Waste Service Suppliers of Copenhagen based on sorting, reselling and recycling waste.
  - The *Pain* was a dysfunctional waste management system. Proposed the *cure* as a business model to form a network of potential buyers and partners. Our key activities would be Advising, Consulting and Mediating efforts of reselling waste to companies that could produce energy from these and contracting with SmartBin technologies for the technological optimization of waste management.

SOCIAL INITIATIVE

Quizzare *(Jun 2014 - present)* – An initiative under which we, a group of five, conduct school-level quizzes in various cities of India, in a wide range of genres. Our aim is to enhance analytical thinking and interactive learning among school students. So far, we've conducted 7 events across 4 cities.

RELEVANT COURSES

- **Computer Systems**: Analog/Digital VLSI Circuits, Computer Organization, Computer Architecture*, Operating Systems, Computer Systems Security*
- **Electronics**: Introduction to Electronics, Microelectronics, Digital Electronics, Solid State Devices, Nanoscale Transistors (nanohub-U)
- **Electrical Engineering**: Signals, Systems and Networks, Control Systems Analysis, Principles of Communication, Information Theory, Power Systems, Electromagnetic Theory, Image Processing
- **Mathematics**: Probability and Statistics, Single and Multi-Variate Calculus, Linear Algebra, Ordinary and Partial Differential Equations, Complex Analysis
- **Algorithms**: Data Structures and Algorithms, Fundamentals of Computing

* - ongoing courses

TECHNICAL SKILL SET

- **Programming Languages**: Verilog, Verilog-A, C, C++, Java, 8085, MIPS and x86 Assembly Programming
- **Softwares and Other Tools**: Xilinx ISE, Keysight ADS, Cadence, ModelSim, Mentor Graphics, GDB, MATLAB, nextnano, Spice, GNU Octave, LaTeX
- **Development Platforms**: dsPIC, Xilinx Spartan and Virtex FPGAs

TEACHING/MENTORING EXPERIENCE

- **Project Mentor**: Mentored a junior undergraduate in my internship supervisor's research group. Helped him understand the fundamental concepts of semiconductor device physics and the various quasi-ballistic and ballistic models of nanotransistors specifically the MIT Virtual Source Models 1 and 2.
- **Academic Mentor, Introduction to Electrodynamics**: Took remedial classes for the course, Introduction to Electrodynamics, and individually mentored academically deficient students.

POSITIONS OF RESPONSIBILITY

- **Secretary, Programming Club**: Helped instill a culture of programming on campus by conducting workshops and lectures for students. Guided students in the programming contests of various intra- and inter-collegiate technical festivals.
- **Member, Google Developer Groups**: Conducted institute-level lectures on various aspects of Web Development, particularly Client and Server side coding.
- **Student Guide, Counselling Service**: Organized the Orientation Programme for the freshmen batch and given the responsibility of six students to help them settle in the campus and provide them with emotional and academic help throughout.