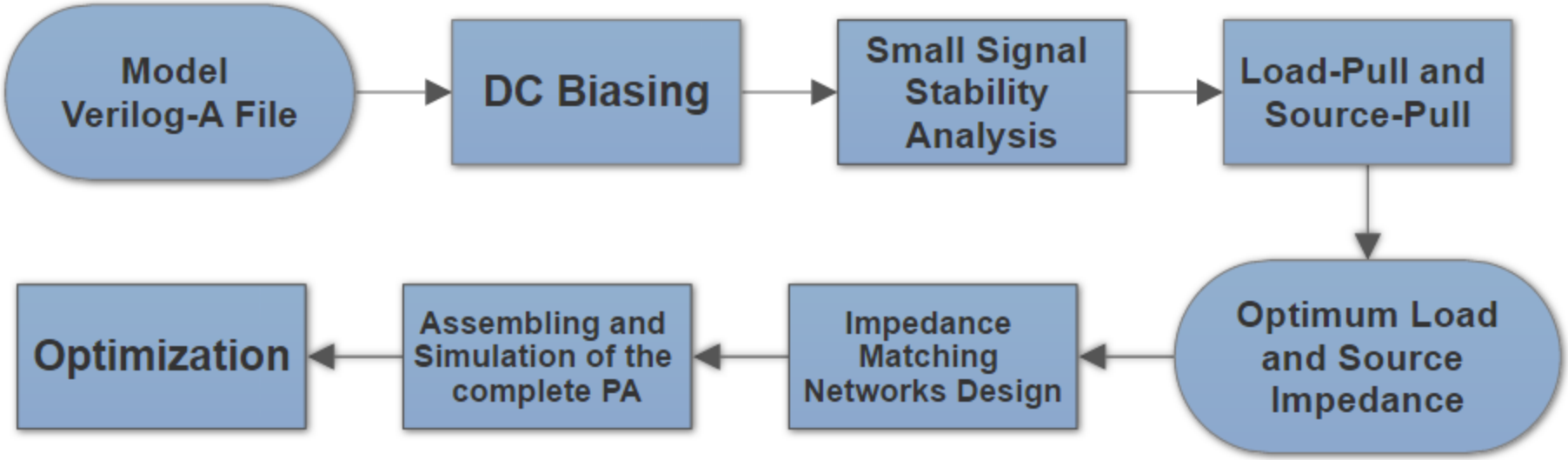
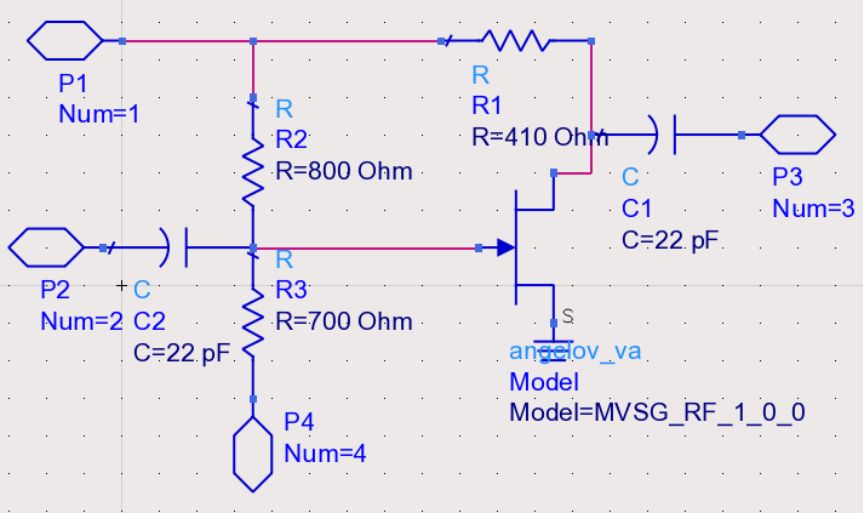
Flowchart of the Design Process

I aim to design a **10GHz Class-A Power Amplifier** using the **MVSG-RF Model**. (Ref. 1)
Following flowchart establishes the steps to be followed to do the same.



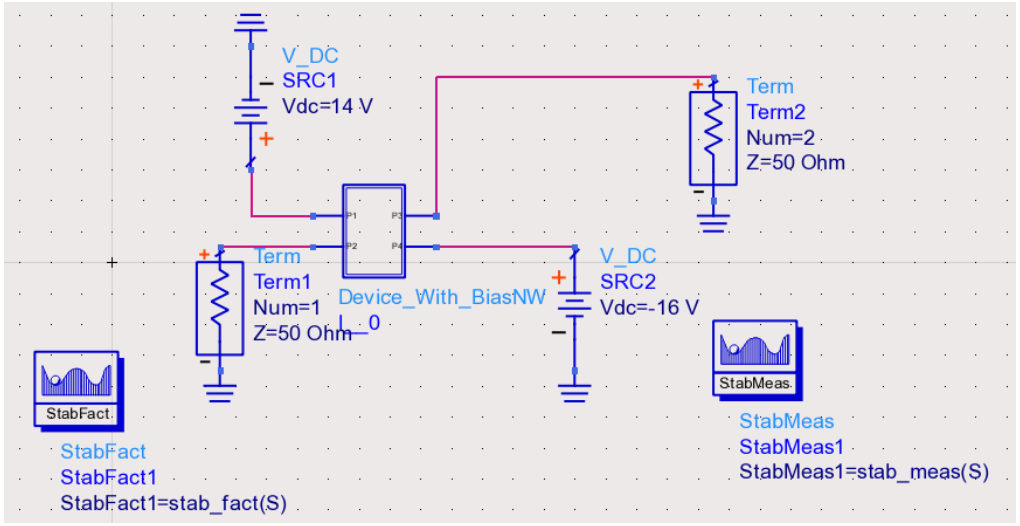
DC Biasing and Small Signal Stability Analysis



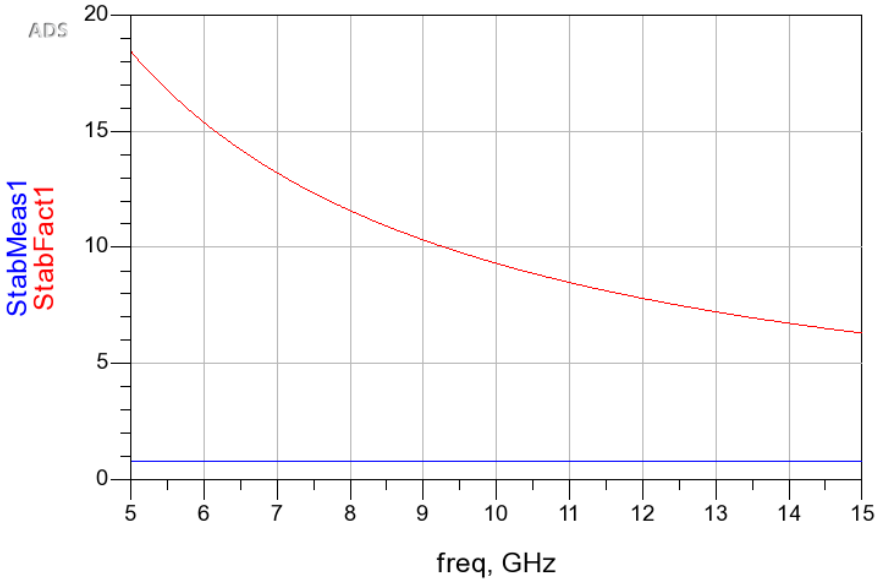
The biasing is done by applying bias voltages at pins 1 and 4. Pins 2 and 3 are for input and output. The bias point is chosen on the $I_D - V_{GS}$ graph so that the amplifier is class A.

Thus, The chosen bias point is V_{GS} = -2V, V_{DS} = 3.98V and I_D = 23.9mA by applying 14 and -16V at pins 1 & 4.

Further, the device is checked to be stable, by performing S-parameter simulations on the given circuit.
Necessary and sufficient conditions for device to be stable are:
Stability Factor (K) > 1 and
Stability Measure > 0.

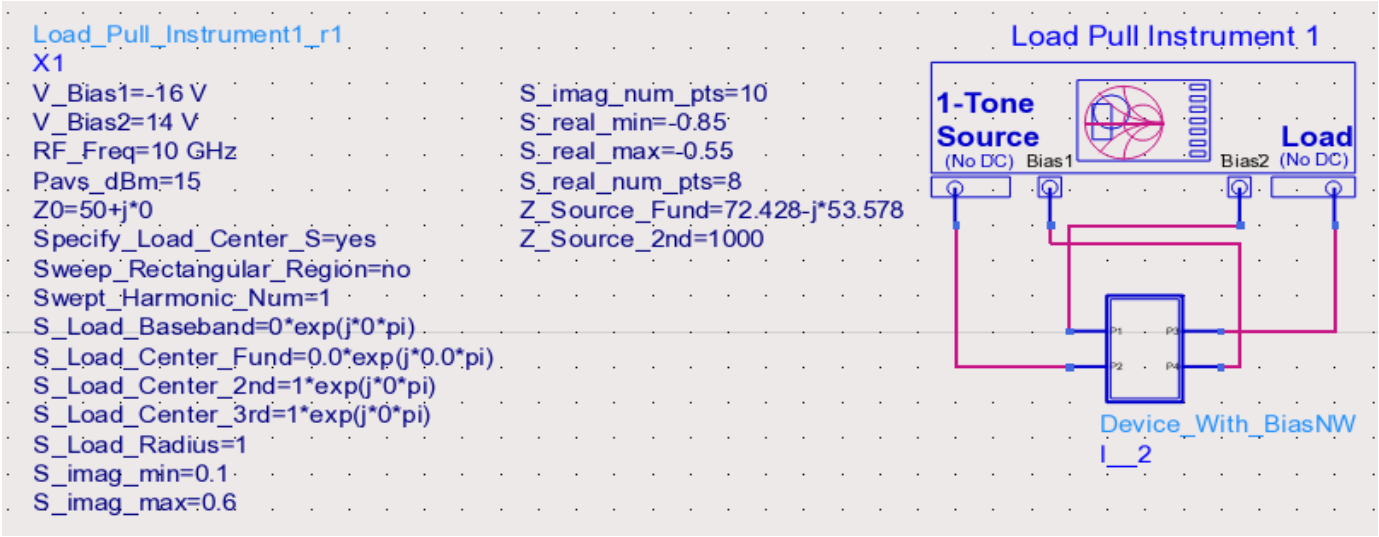


Stability Analysis Results and Load-Pull



It can be seen that Stability Factor is more than 1 and Stability Measure is greater than 0 over the entire frequency range, and hence our device is stable.

Load Pull is the technique during which we keep source impedance and source power constant and sweep impedance/reflection coefficient of load over a certain section of the smith chart to characterize Output Power. The circuit is as shown below.



Load-Pull Analysis Results

At load that gives maximum power (and gain):

BiasCurrent_at_MaxPower	Zload_at_MaxPower	MaxPowerRho
0.019	387.361 + j188.402	0.811 / 5.877

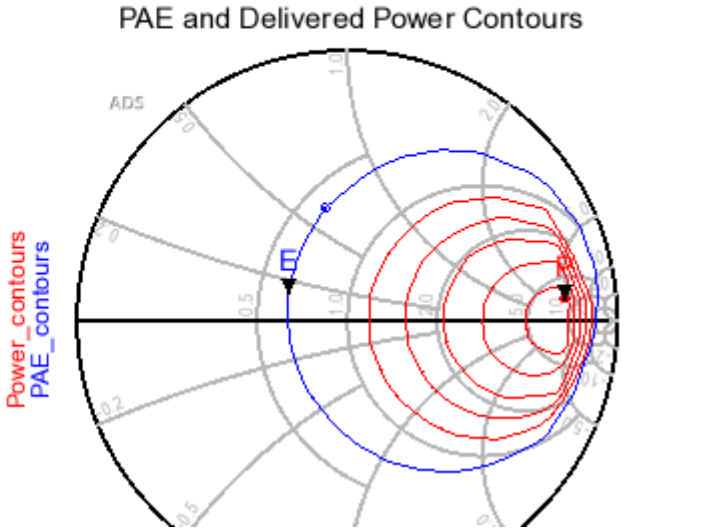
PAE_at_MaxPower
2.742

Z_In_at_MaxPower
304.161 - j208.601

Gain_at_MaxPower
0.689

Pdel_dBm_Max
15.689

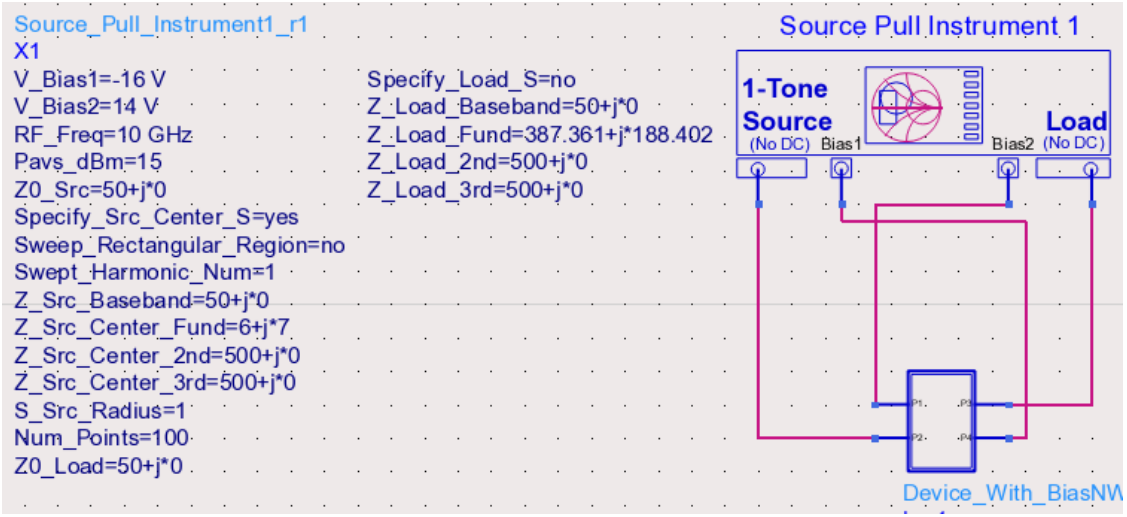
System Reference Impedance Z0: 50.000
A Rho of 0 corresponds to a load impedance of conj(Z0).



Load-Pull is performed using the *One-Tone Load Pull Simulation with constant Source Power* feature of ADS. From the analysis, **the optimum load impedance** for maximum power output comes out to be **387.361+j*188.402**. The gain is around 0.7 dBm.

Now, to find the optimum source impedance, we perform **Source-Pull**.

Source-Pull Analysis



Source-Pull is performed using the *One-Tone Source Pull Simulation with constant Source Power* feature of ADS, where we plug in the value of optimum load impedance, 387.361+j*188.402, into *Z_load_fund*. From the results, the **optimum source impedance** comes out to be **72.428+j*53.578**.

At source that gives maximum power (and gain):

BiasCurrent_at_MaxPower	Zsrc_at_MaxPower	MaxPowerRho
0.019	72.428 + j53.578	0.435 / 43.650

PAE_at_MaxPower
2.472

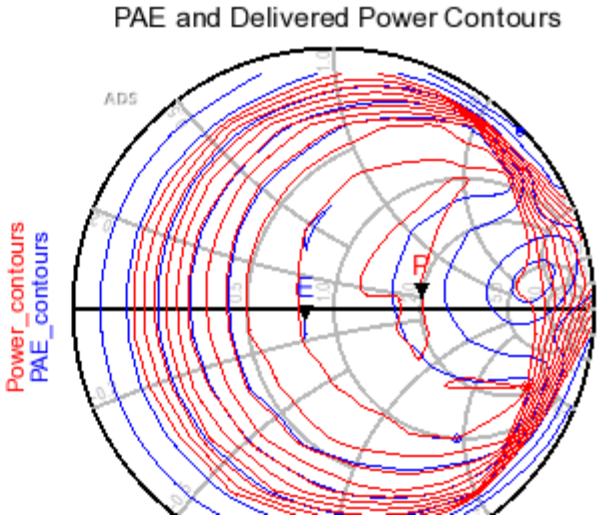
Z_In_at_MaxPower
330.325 - j218.705

Gain_at_MaxPower
0.739

Pdel_dBm_Max
15.739

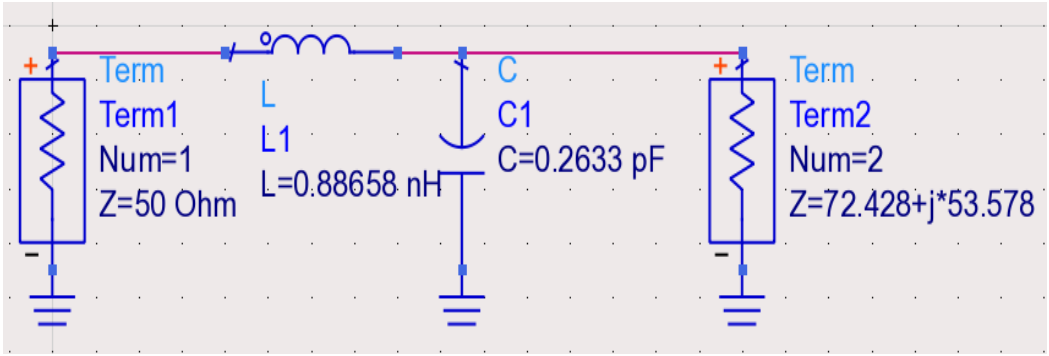
Source Reference Impedance Z0:
A Rho of 0 corresponds to a source impedance of conj(Z0).

50.000

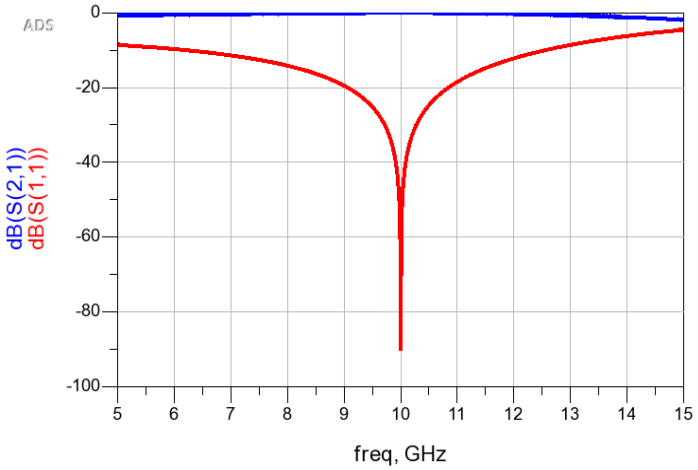


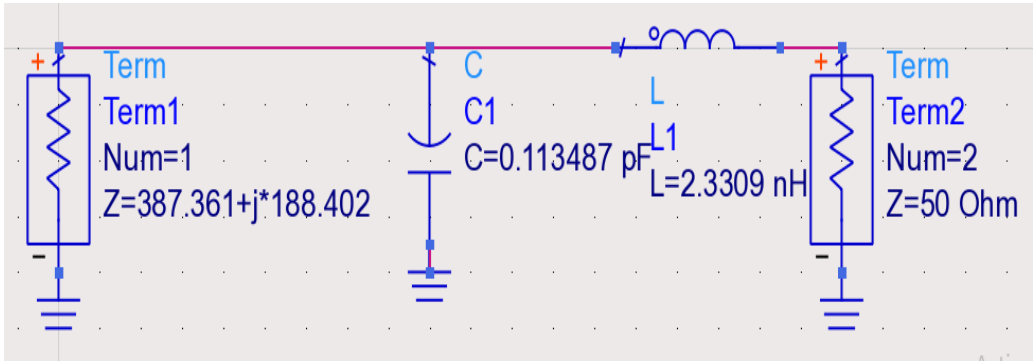
Impedance Matching Networks Design

L-matching networks for the input and output sides are designed with respect to the optimum source and load impedance. The designs are verified through S-parameter simulations.

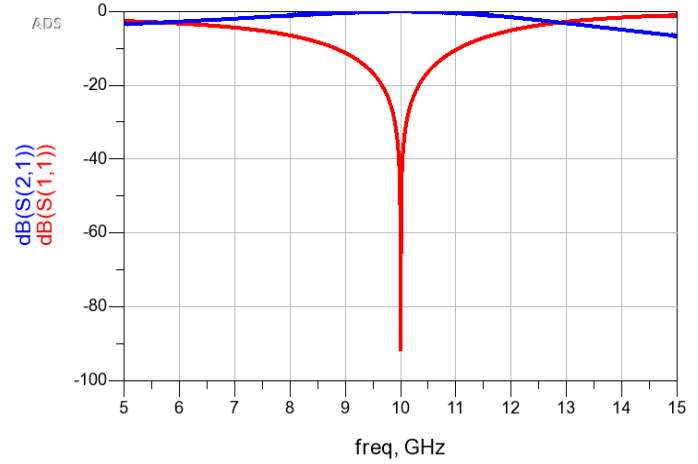


Input Matching Network Design

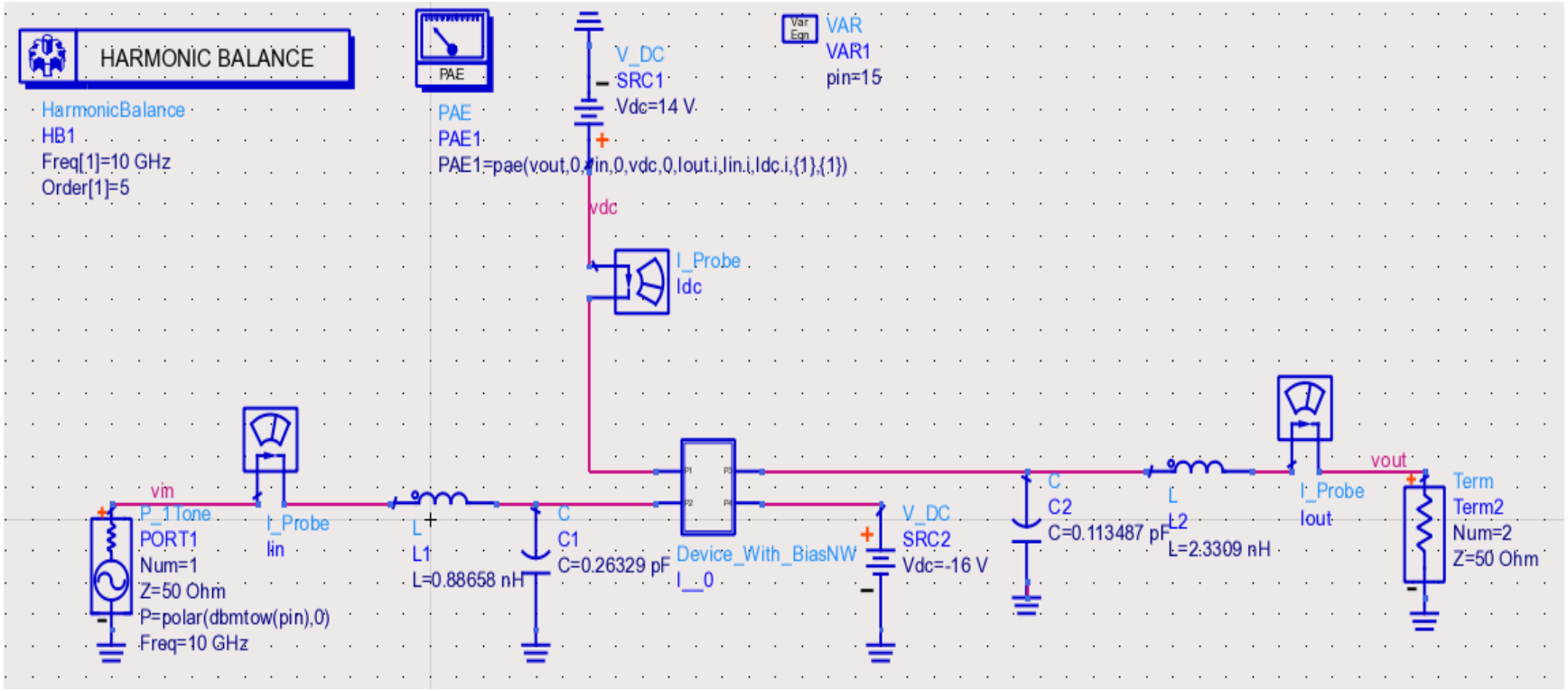




Output Matching Network Design

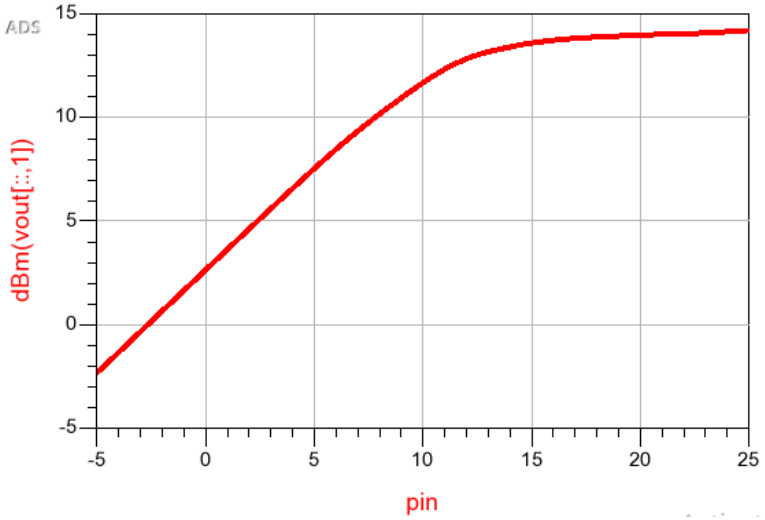


Assembling and Simulation of the complete Power Amplifier



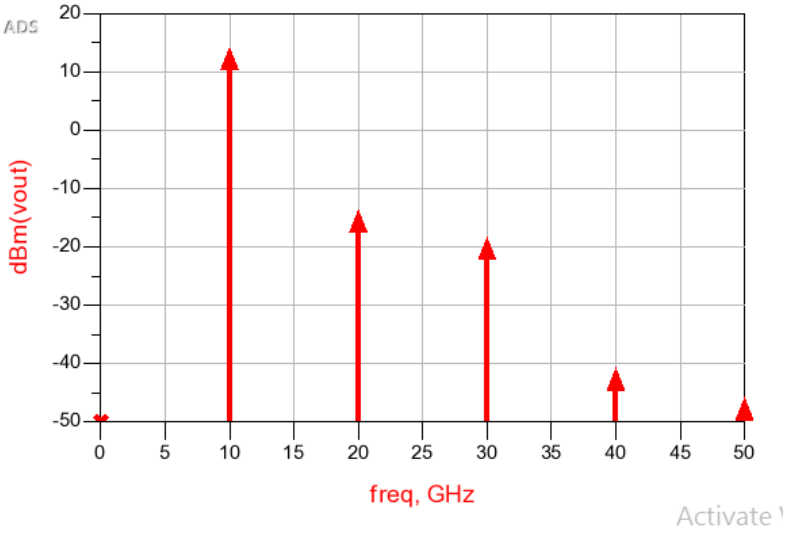
The Device with Biasing Network is assembled with both the impedance matching networks and various probe components. On performing Harmonic balance simulations, the output power in dBm of various harmonics and the P_{OUT} vs P_{IN} graphs were obtained, which are displayed on the next slide.

Performance of the Power Amplifier



The P_{OUT} vs P_{IN} graph saturates at about 13 dBm of input power and provides a gain of about 1.5 dBm at 10 dBm of input power.

From the HB Simulations, it is found that the output harmonics at 15dBm of input power are distributed as follows:
Fundamental : 14.8 dBm
2^{nd} Harmonic : -15 dBm
3^{rd} Harmonic : -19 dBm
and so on.

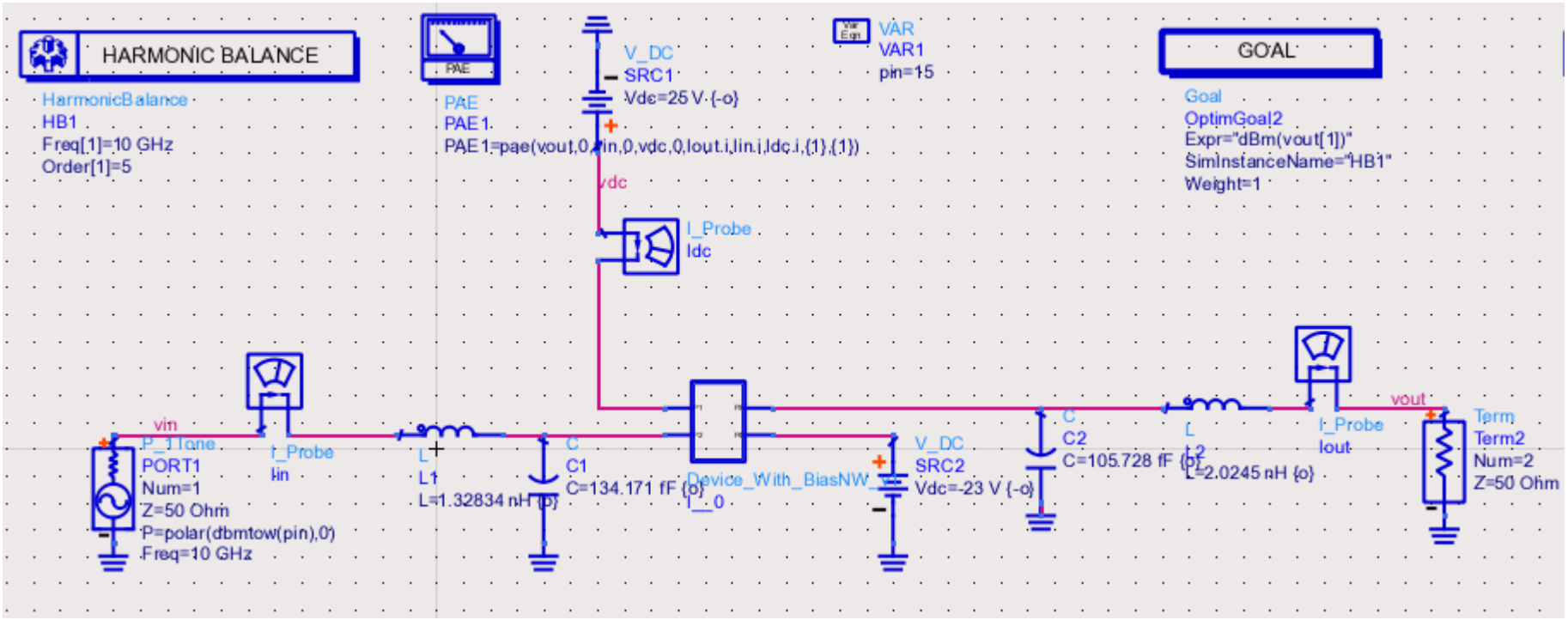


Optimization of the Performance

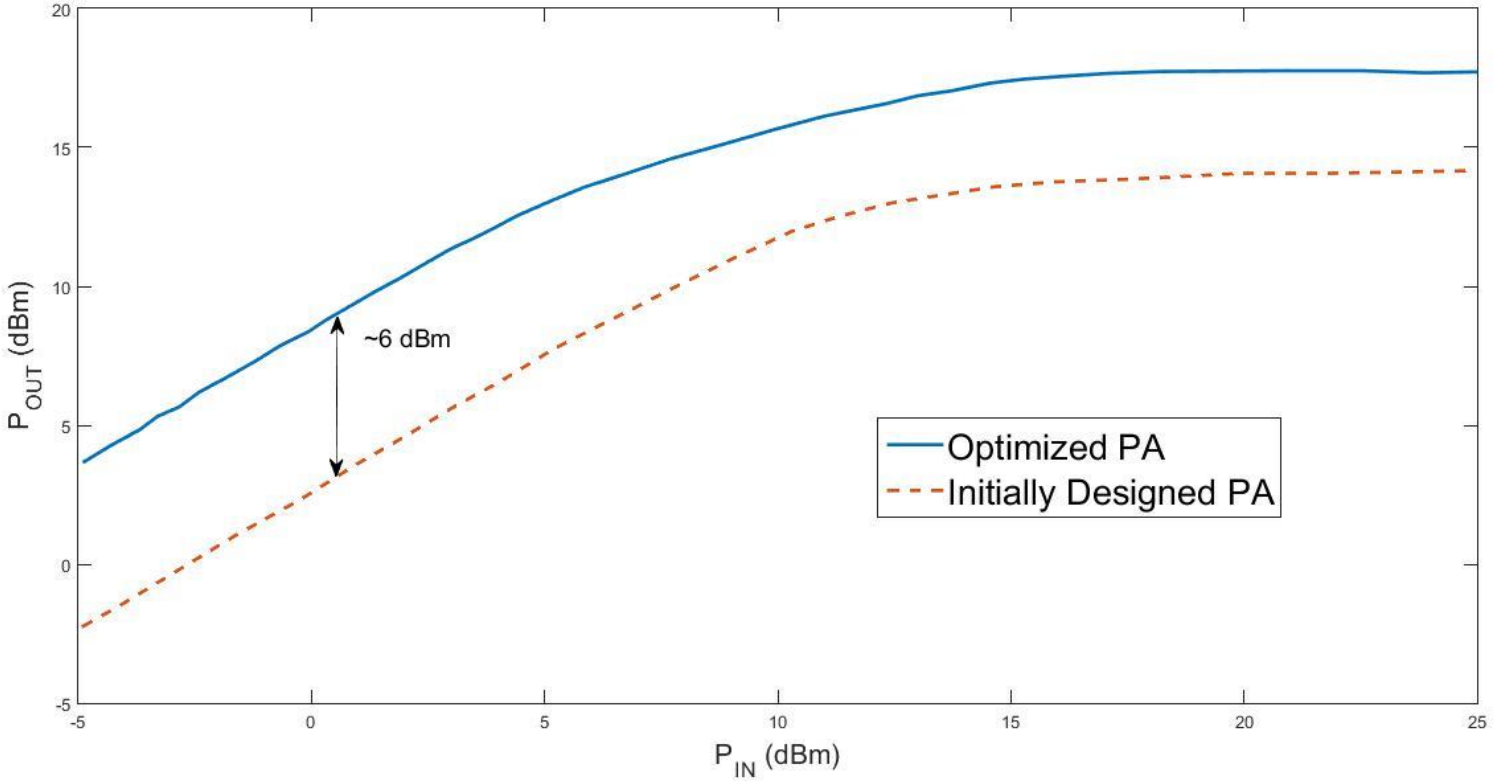
The change in performance of the Power Amplifier is investigated via two methods –

1. **Circuit Level Modifications**
2. Device Parameter Modifications

Circuit Level Modifications - The following figure illustrates the optimized design. This was done using the optimize tool of ADS by defining various circuit elements as optimizable. The goal was set at P_{OUT} = 20 dBm. After various iterations, the bias voltages were changed to 25V and -23V for better performance. Comparison with the previously designed PA is done on the next slide.



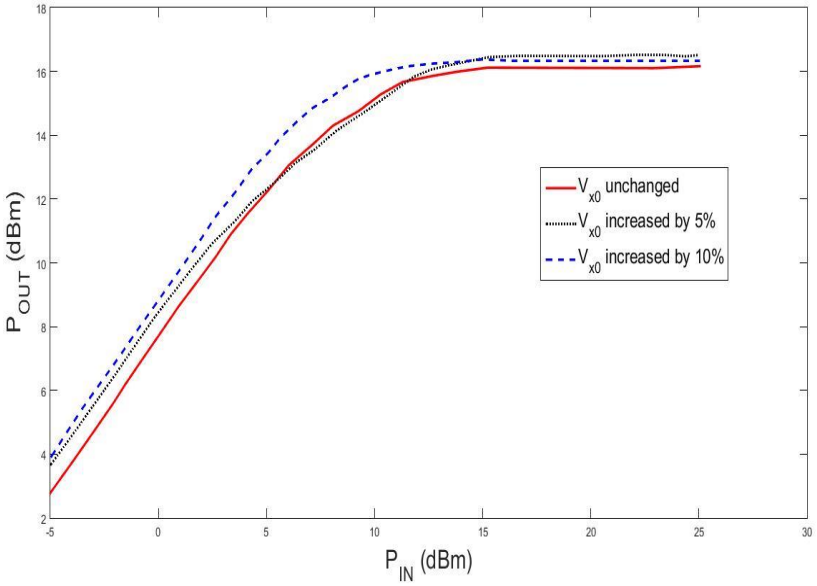
Impact of Circuit-Level Modifications

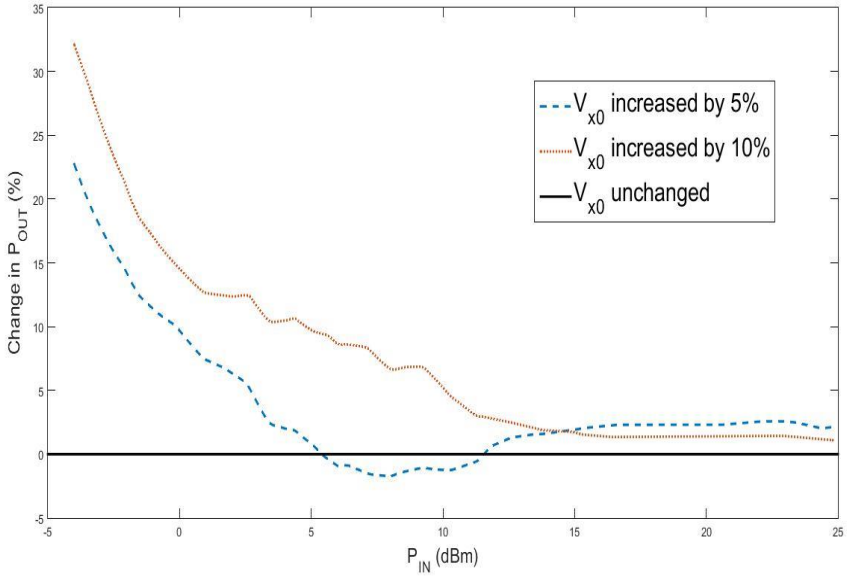


There is a significant improvement of 6 dBm in gain by optimization of the circuit. Now, **Device Parameter modifications** are carried out and their impact on performance noted.

Impact of Device Parameters Modifications

The source injection velocity, V_{xo}, was varied from its default value of 1.3e7 cm/s. The whole circuit was optimized for each change and the following graphs illustrates the Pout vs Pin characteristics and the change in P_{OUT} (%) after each such optimization. The goal was once again set at 20 dBm.





Thus, we observe that the amplifier performance is not affected much by changes in the source injection velocity, v_{xo}, as compared to circuit-level modifications.

Goals Achieved –

1. Successfully performed Load-Pull analysis on the MVSG-RF Model and designed a Power Amplifier exhibiting a high value of gain.
2. Optimized the performance of the power amplifier by circuit-level changes.
3. Investigated the change in performance by device parameter (v_{xo}) modifications.

Future Work –

1. For spectrally-efficient information transmission, highly linear PAs are required. Thus, the next step is **understanding non-linear distortion and implementing various linearization techniques** like Feedforward, Feedback and Predistortion Linearization.
2. To study the effect of Joule Heating on the performance.
3. To study the impact of change in various parameters like mobility, access region resistance on the performance of the power amplifier.
4. Compare the effects of various technology parameters by quantifying the sensitivity of gain relative to the particular parameter.

References –

1. 'Compact Transport And Charge Model For Gallium Nitride-based HEMTs For radio-Frequency applications' U. Radhakrishna, MIT, Jun.-2013.
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