RF Circuits Design

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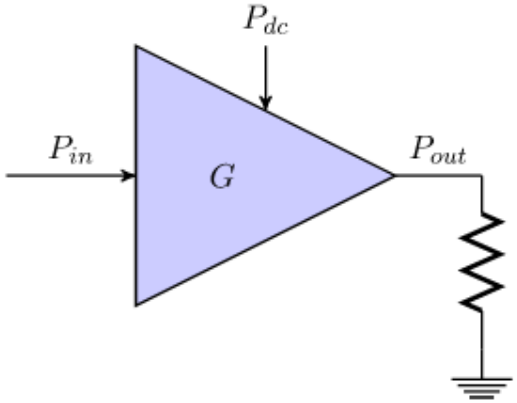
Amplifier Fundamentals

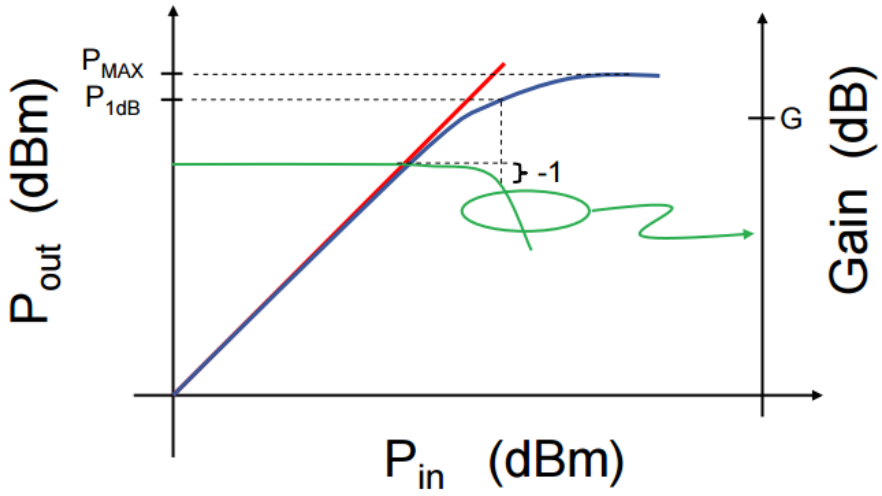
- Read up on the first chapter in the book 'RF Power Amplifiers for Wireless Communications' by Steve C. Cripps, which deals with Linear RF Amplifier theory.
- Read up on the fundamentals of small and large signal amplifiers and different classes of operation at http://www.electronics-tutorials.ws/amplifier/amp_1.html
- Understood DC biasing of an amplifier at http://www-ferp.ucsd.edu/najmabadi/CLASS/ECE60L/03-W/NOTES/BJT2.pdf
- Few points of importance are summarized in the next few slides.

RF Power Amplifiers

- A power amplifier, as the name implies, is not just intended to amplify a signal, but to also have that signal provide significant power.
- A simple amp might take a 1 mV microphone signal and make a 1 V "line" signal. It provides substantial voltage gain. Another amp might take that 1 V signal and make a 10 V signal that can drive a loudspeaker load. That is only a voltage gain of 10, but that signal has been able to provide significant output power.
- They are used in a wide variety of applications including Wireless Communication, TV transmissions, Radar, etc.

Performance Metrics

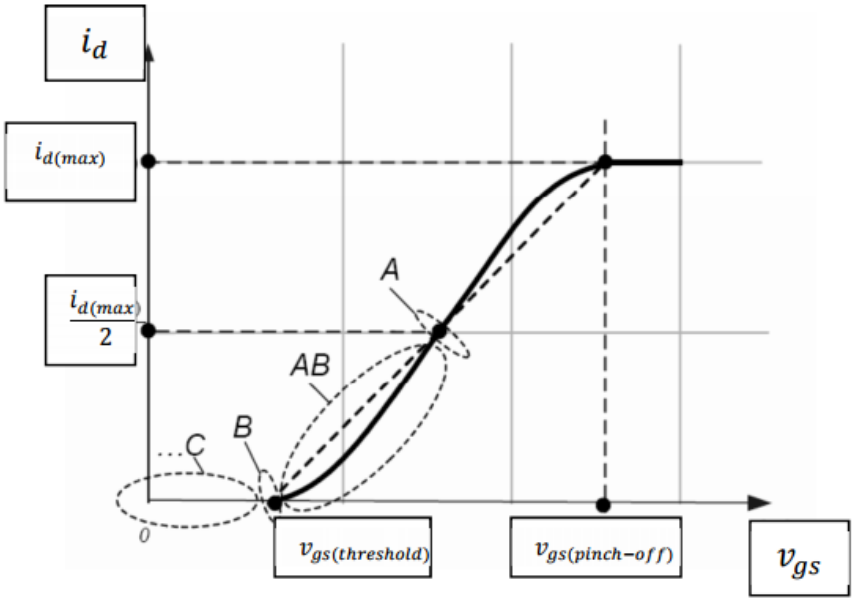




- Power Gain,
  $G = 10\log_{10}(P_{out}/P_{in})$
- Drain Efficiency , $\eta_d = P_{out}/P_{dc}$
- Power Added Efficiency, $\eta_{pae} = (P_{out} - P_{in})/P_{dc}$
- 1dB Compression Point (P_{1dB}) represents a practical limit for linear operation.

Classes of Amplifier Operation

- **Class A** : The transistor conducts through the whole RF cycle. Conduction angle is 2π.
- **Class B** : The transistor is biased at pinch off and conducts 50% of the RF cycle. Cond. angle is π.

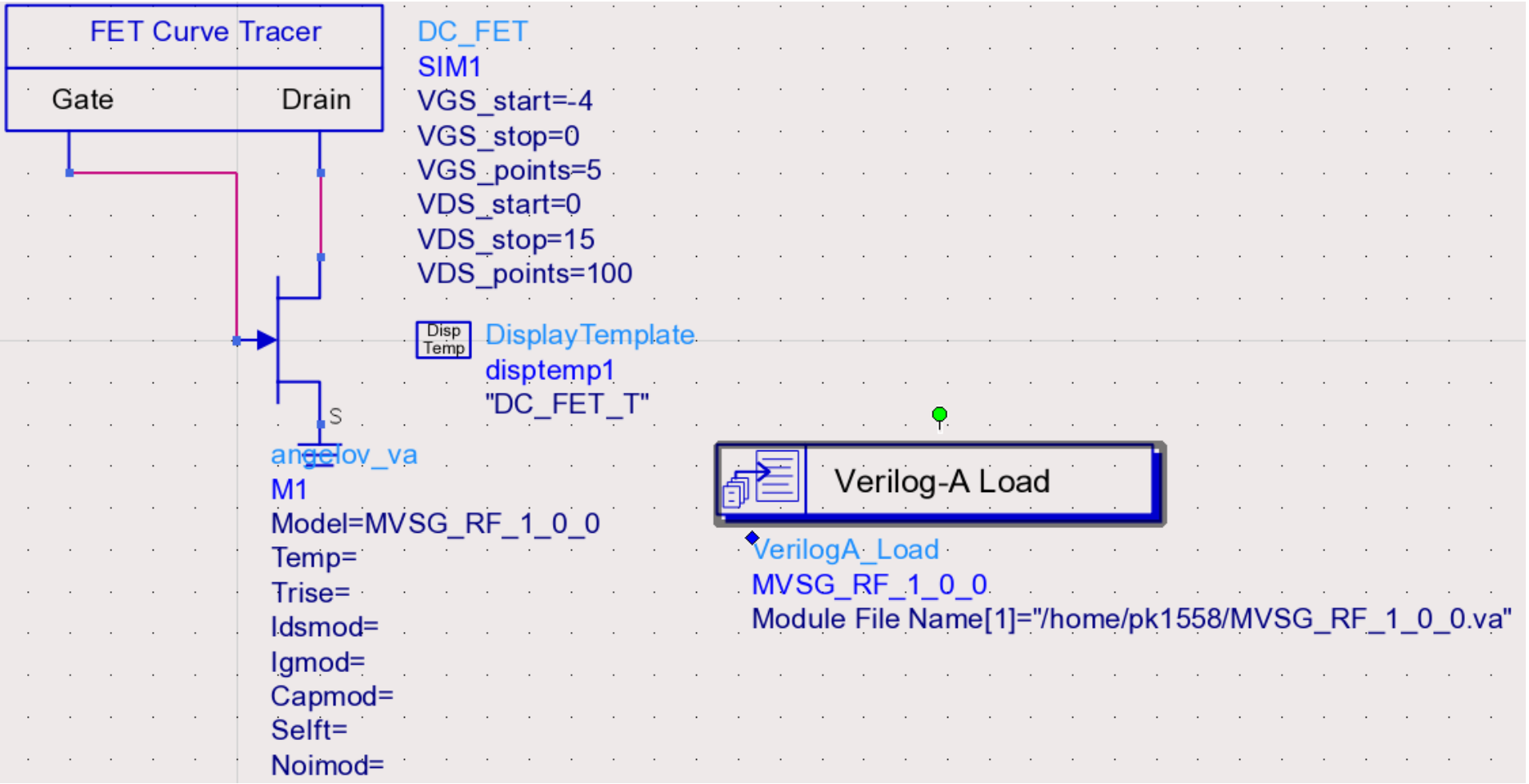


- **Class AB** : Biased somewhere in between Class A and B.
- Classes C, D, E, F, etc.

Getting started with ADS

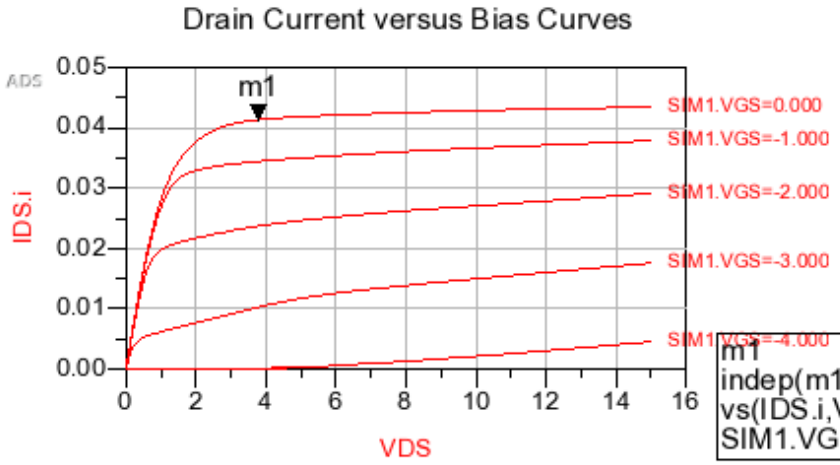
- It is an electronic design automation (EDA) software system that provides an integrated design environment to designers of RF electronic products.
- We need to bias the BJT/MOSFET/HEMT at a particular point of our choice (according to the class of operation) in the circuit. Thus, we need to first obtain the ID-VG and ID-VD graphs for our device.
- Although this can be done manually, ADS provides us with many common templates, one of which is the FET Curve Tracer. http://edadocs.software.keysight.com/pages/viewpage.action?pageId=58330051
- The gate and drain voltages can be swept and the corresponding ID-VG and ID-VD curves drawn. The example is shown in the next slide.

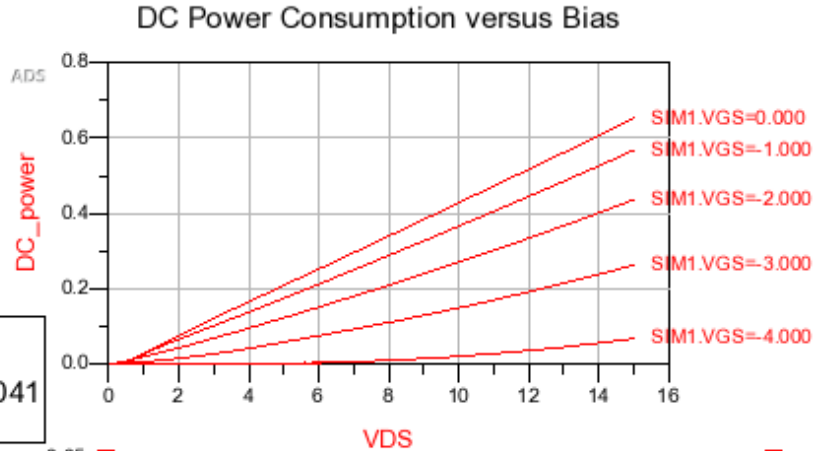
FET Tracer template with the device



- Observe that I did not use one of the predefined transistor templates rather implemented the MVSG-RF device. This can be done provided you have the model's Verilog-A code available. If you do, you may follow pages 17-22 of 'Understanding of Power Amplifiers & ADS' by Sravani Bhuma Koppula and Vikyath Goli.
- By just clicking on the Simulate icon, I get the following results.
- The ID vs VG graph can be added by adding a graph from tools and specifying the x and y-axes.

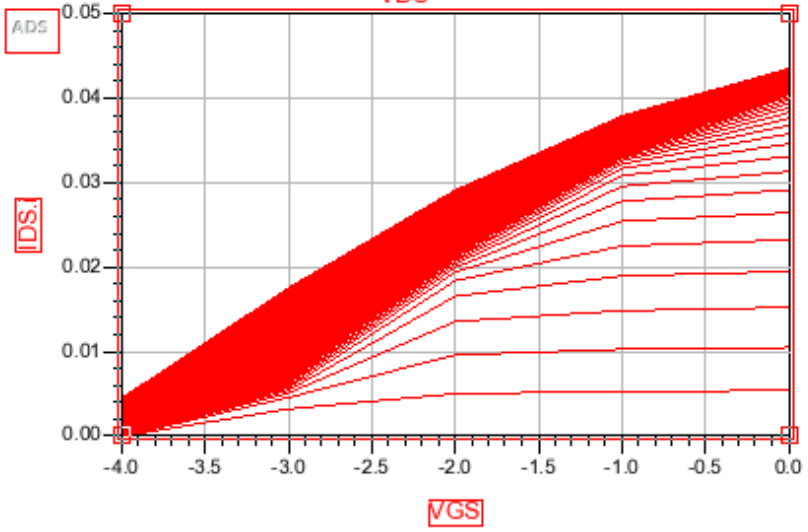
Simulation Results



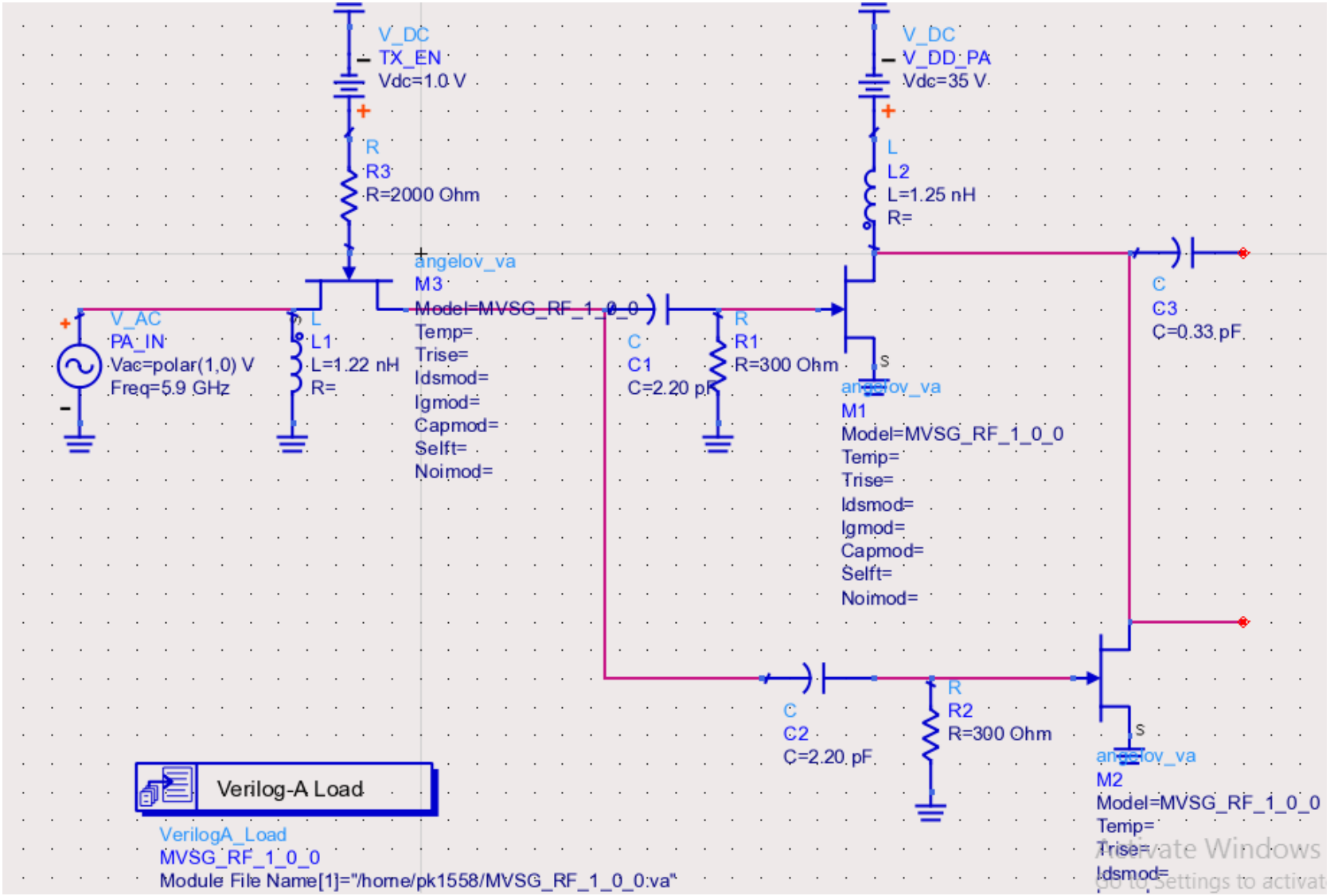


Move Marker m1 to update values below:

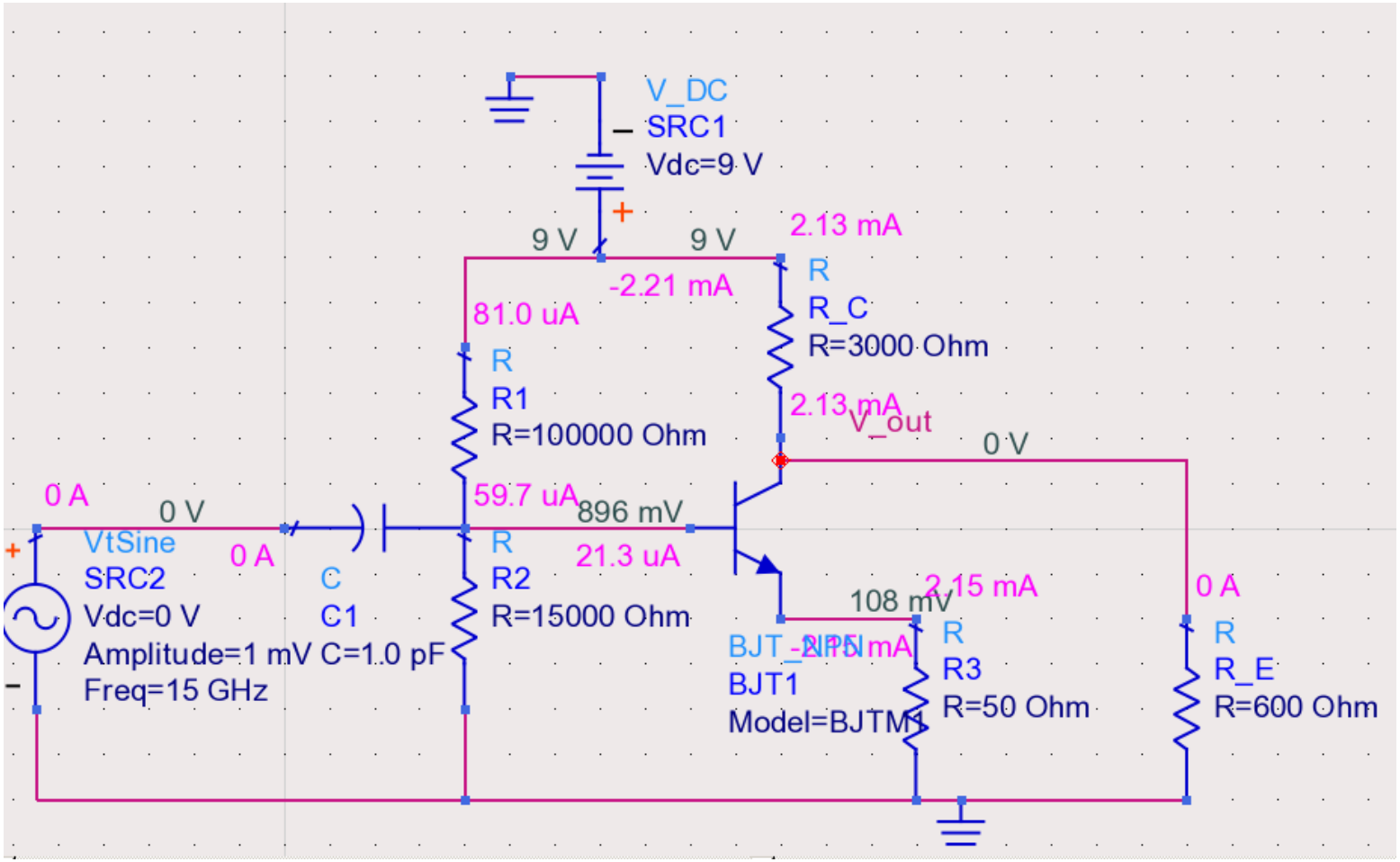
VDS	Device Power Consumption at m1 bias point, Watts
3.788	0.157



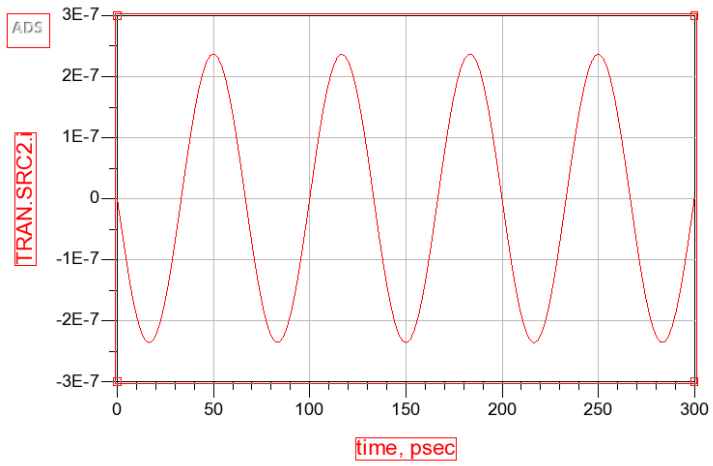
Now, you could try creating even complex circuits like the one shown below just to get acquainted with different circuit elements and how to edit theor parameters.



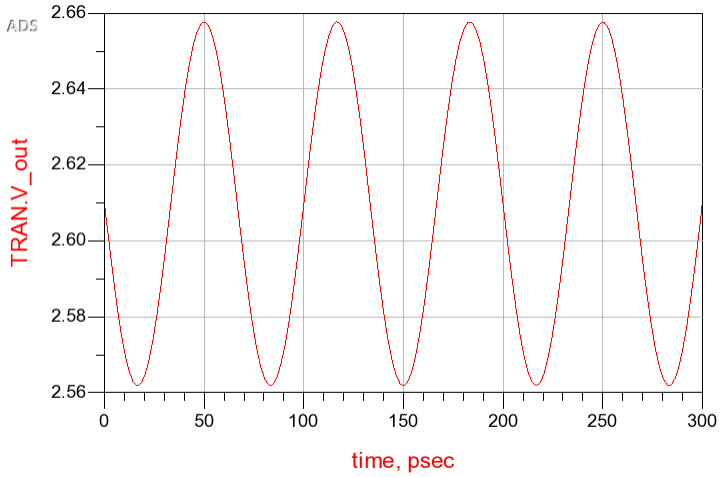
Small-signal amplifier: The biasing of the BJT is done at I_C = 2.15 mA and V_{CE} = 2.5 V and subsequently, transient simulation is carried out.



Simulation Results



INPUT



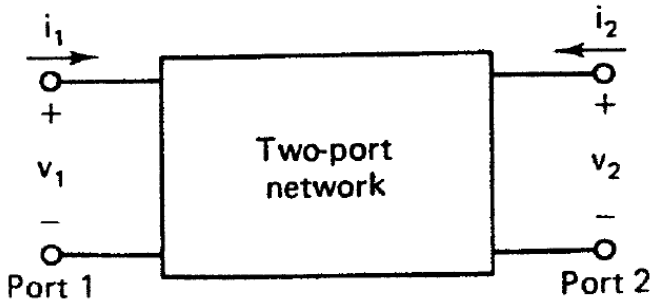
OUTPUT

- Small signal amplifier shows high-linearity due to low signal excursion over the transistor load line.
- For a Power Amplifier, this linearity is disrupted as we drive the transistor closer to its maximum output power and the excursion now occurs over a much wider range.

RF Transistor Amplifiers : Basics

- Low frequency two-port networks can be characterized by the Impedance, Admittance, Hybrid and ABCD Matrices.
- For High frequency networks, which we'll be dealing with, we require the knowledge of S parameters.
- Further for implementing a power amplifier, we would want to know about matching networks and load pull analysis, which further necessitates the knowledge of Smith Chart.
- The book to refer for all of this is 'Microwave Transistor Amplifiers, Analysis and Design' by Guillermo Gonzalez.
- I summarize the important points in the next few slides.

2-Port Network



At low frequencies, the network can be represented in various through impedance matrix (z-parameters), admittance matrix (y-parameters), the hybrid or ABCD-matrix.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \qquad \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix} \qquad \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix}$$

Calculation of z, y, h and ABCD Parameters and what happens at RF?

- Short and open circuit tests are performed.
- For example :-

$$z_{11} = \left.\frac{v_1}{i_1}\right|_{i_2=0}$$

- Over the entire RF Frequency range, located between 300 MHz and 30 GHz, short and open-circuits are very difficult to implement due to the existence of parasitic inductances and capacitances in a practical measurement set-up.
- Thus, it is difficult to characterize RF circuits in terms of voltage or current gains and input and output impedances. This problem is overcome using the Scattering parameters.
- These s-parameters are defined in terms of traveling waves and completely characterize the behavior of RF and microwave circuits.

Traveling waves and Transmission-Line Concepts

- Using the Helmholtz equations, we arrive at :

$$\frac{d^2V(x)}{dx^2} - \gamma^2 V(x) = 0 \quad \text{and} \quad \frac{d^2I(x)}{dx^2} - \gamma^2 I(x) = 0$$

- $i(x, t) =$ Re $[I(x)e^{jwt}]$ and $v(x, t) =$ Re $[V(x)e^{jwt}]$
- Here,
- Thus,

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

$$V(x) = Ae^{-\gamma x} + Be^{\gamma x}$$

$$I(x) = \frac{A}{Z_o} e^{-\gamma x} - \frac{B}{Z_o} e^{\gamma x} \qquad Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

- Thus, the voltage and current along a transmission line are a pair of waves traveling in opposite directions.

S Parameters

- Introducing the notation, $V^+(x) = Ae^{-\gamma x}$ and $V^-(x) = Be^{\gamma x}$
- where, $V(x) = V^+(x) + V^-(x)$ and

$$I(x) = I^+(x) - I^-(x) = \frac{V^+(x)}{Z_o} - \frac{V^-(x)}{Z_o}$$

- Introducing the normalized notation,

$$v(x) = \frac{V(x)}{\sqrt{Z_o}} \quad \text{and} \quad a(x) = \frac{V^+(x)}{\sqrt{Z_o}} \quad b(x) = \frac{V^-(x)}{\sqrt{Z_o}} \quad \text{where} \quad b(x) = \Gamma(x)a(x)$$

$$i(x) = \sqrt{Z_o}\, I(x)$$

- If instead of a one-port transmission line we have a two-port network with incident wave a1 and reflected wave b1 at port 1, and incident wave a2 and reflected wave b2 at port 2, we can generalize as follows :

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

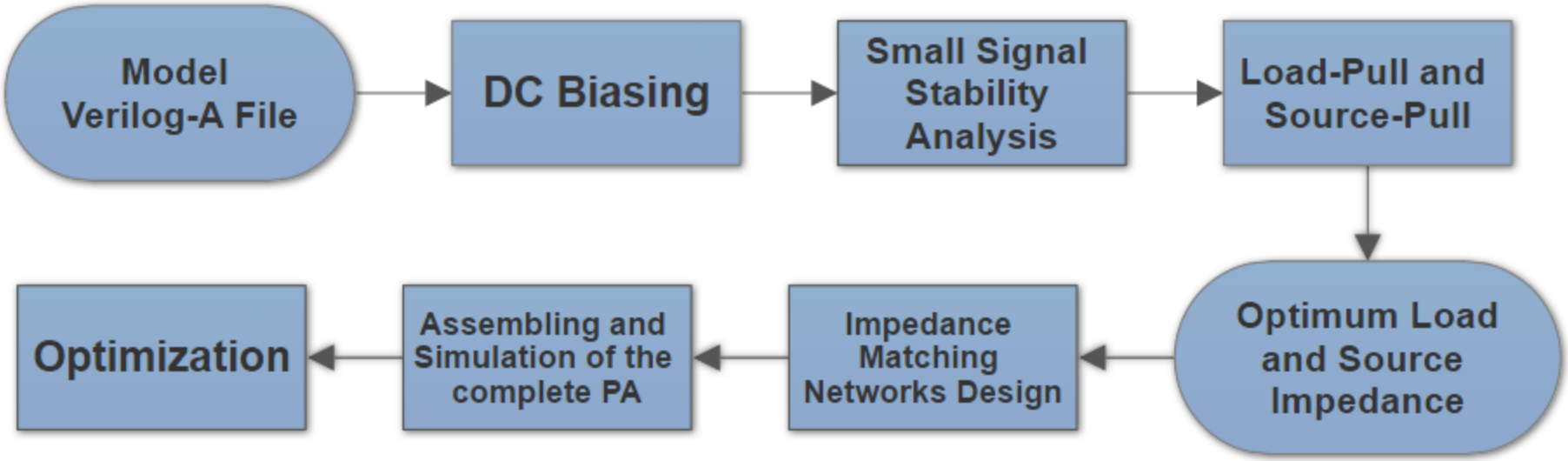
and

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

Scattering Matrix

Design of RF Power Amplifiers using the proposed model

- The device is operating under large signal conditions.
- There exists a specific source and load impedance into which the transistor can produce maximum output power.
- Because the device S parameters are no longer defined under large signal conditions, they cannot be used to determine the optimum load impedance for maximum output power.
- These impedances are determined by performing a load-pull measurement on the device.
- The complete design flow-chart is given on the next slide.


Model
Verilog-A File
DC Biasing
Small Signal
Stability
Analysis
Load-Pull and
Source-Pull
Optimum Load
and Source
Impedance
Impedance
Matching
Networks Design
Assembling and
Simulation of the
complete PA
Optimization

Design of a Single Stage Power Amplifier with Optimum Impedance Data already given

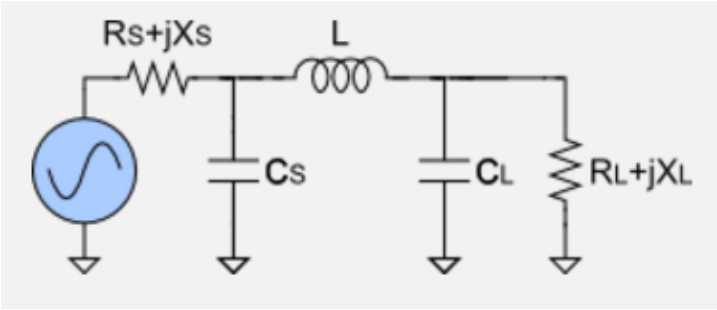
- The device being used is NPT25100.
- Gallium Nitride 28V, 125W RF Power Transistor.
- GaN-on-Silicon technology.
- The Optimum Source and Load Impedances are tabulated as follows

Frequency (MHz)	Z_S (Ω)	Z_L (Ω)
2140	12.1 - j20.0	2.6 - j2.6
2300	10.0 - j3.0	2.5 - j2.3
2400	9.5 - j3.0	2.5 - j2.5
2500	9.0 - j3.0	2.5 - j2.7
2600	8.5 - j3.0	2.5 - j3.1
2700	8.0 - j3.0	2.5 - j3.3

- I will design the power amplifier for maximum power transfer at 2.140 GHz.
- Thus for the designer, the problem reduces to a simple impedance matching exercise.

Design of the Matching Networks

- The L-matching networks are basically designed by equating $Z_S^* = Z_{IN}$.
- While it fits many applications, a more complex circuit will provide better performance or better meet desired specifications in some instances. The T-networks and π-networks will often provide the needed improvement while still matching the load to the source. Pi-networks have been used in this problem.

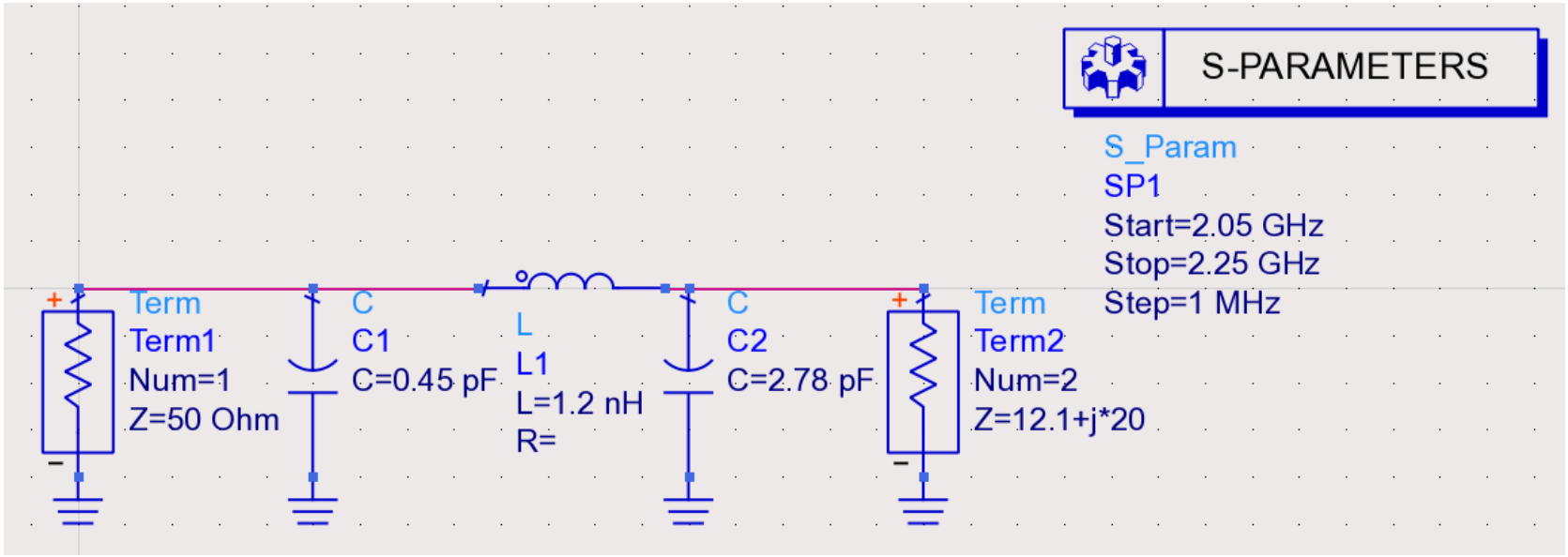


- By convention, 50 ohms source and load impedance is matched to the amplifier input and output respectively.
- All the numbers have been calculated by the Impedance Matching Utility Program in ADS using S parameter files.
- Since we do not have the model Verilog-A available, we make do with the S parameter files, as given from page 234 of '100 ADS Design Examples' by Ali Behagi.

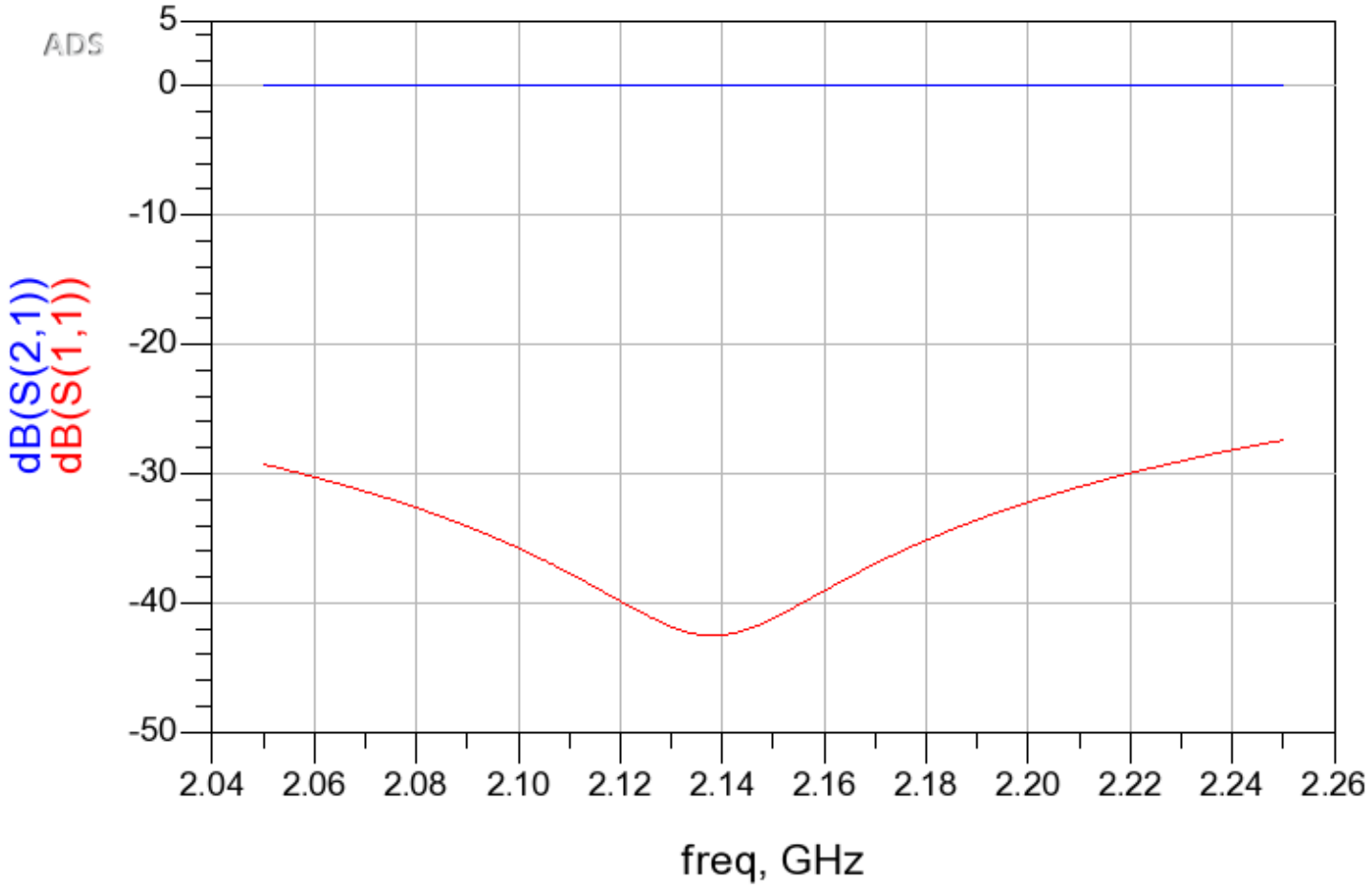
Design of the Input Matching Network

```
! Optimum Source Impedance, Zs, presented to the NPT25100
# GHz    Z         RI       R         1
! Freq   ReZ1      ImZ1
2.140    12.1      -20.0
2.300    10.0      -3.0
2.400    9.5       -3.0
2.500    9.0       -3.0
2.600    8.5       -3.0
2.700    8.0       -3.0
```

S Parameter file and the Input Matching Network



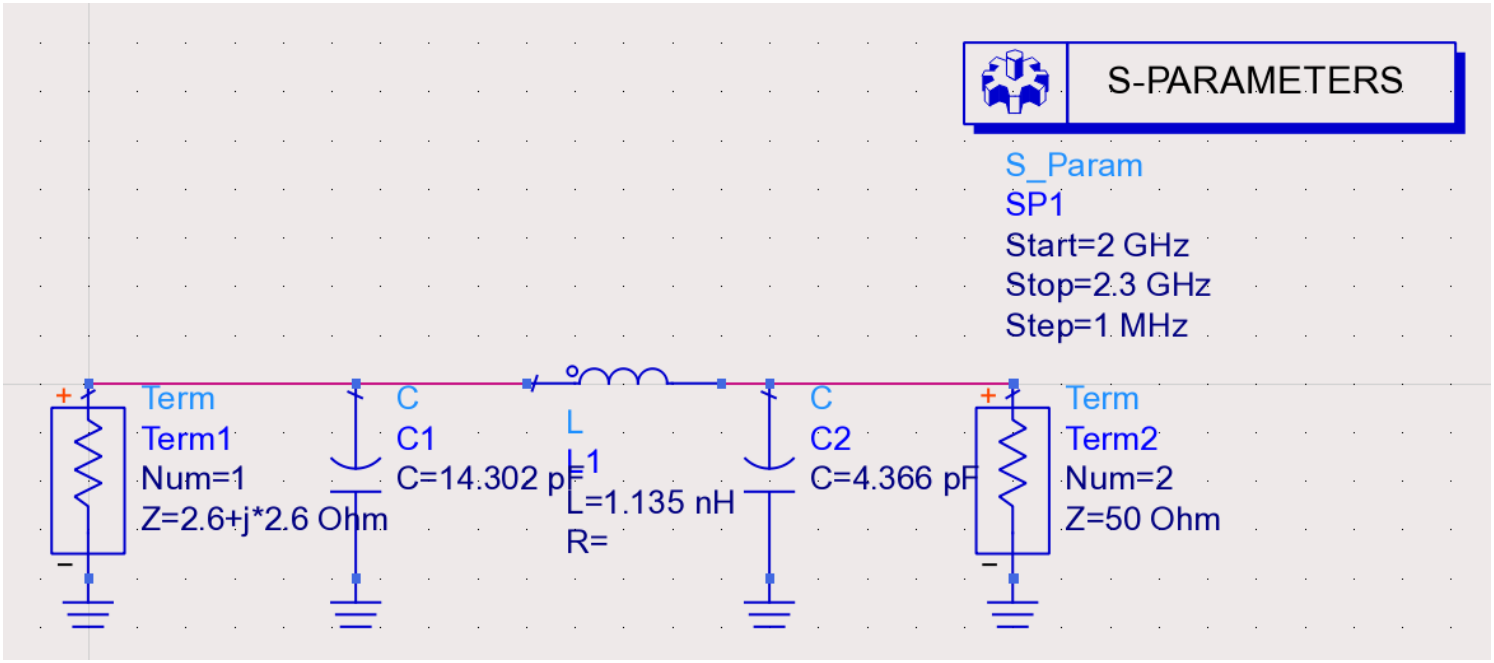
Simulation of the schematic



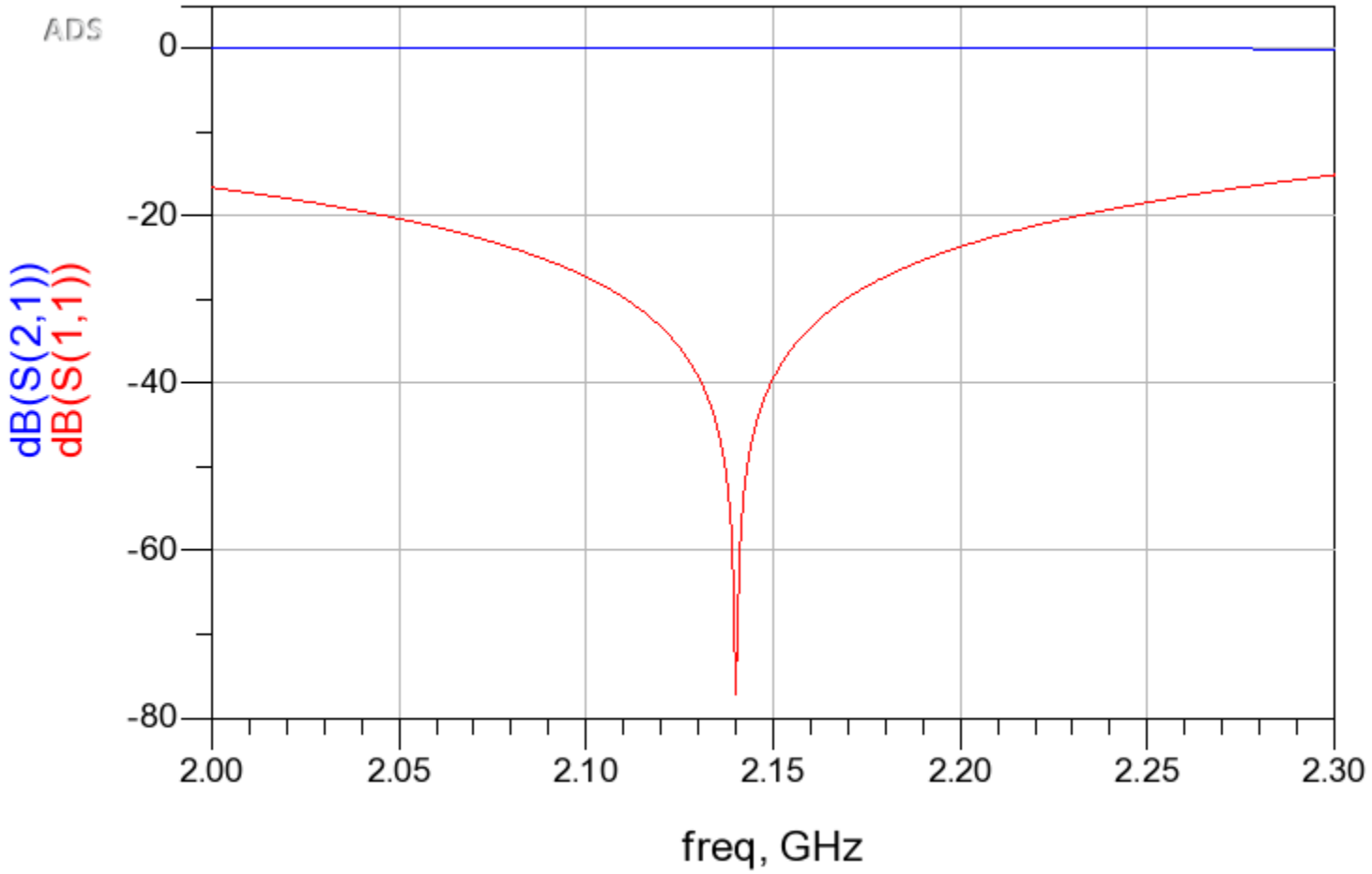
Design of the Output Matching Network

```
! NPT25100 Output Impedance
# GHz    Z        RI       R        1
!Freq    ReZ1     ImZ1
2.140    2.6      2.6
2.300    2.5      2.3
2.400    2.5      2.5
2.500    2.5      2.7
2.600    2.5      3.1
2.700    2.5      3.3
```

S Parameter file and the Output Matching Network



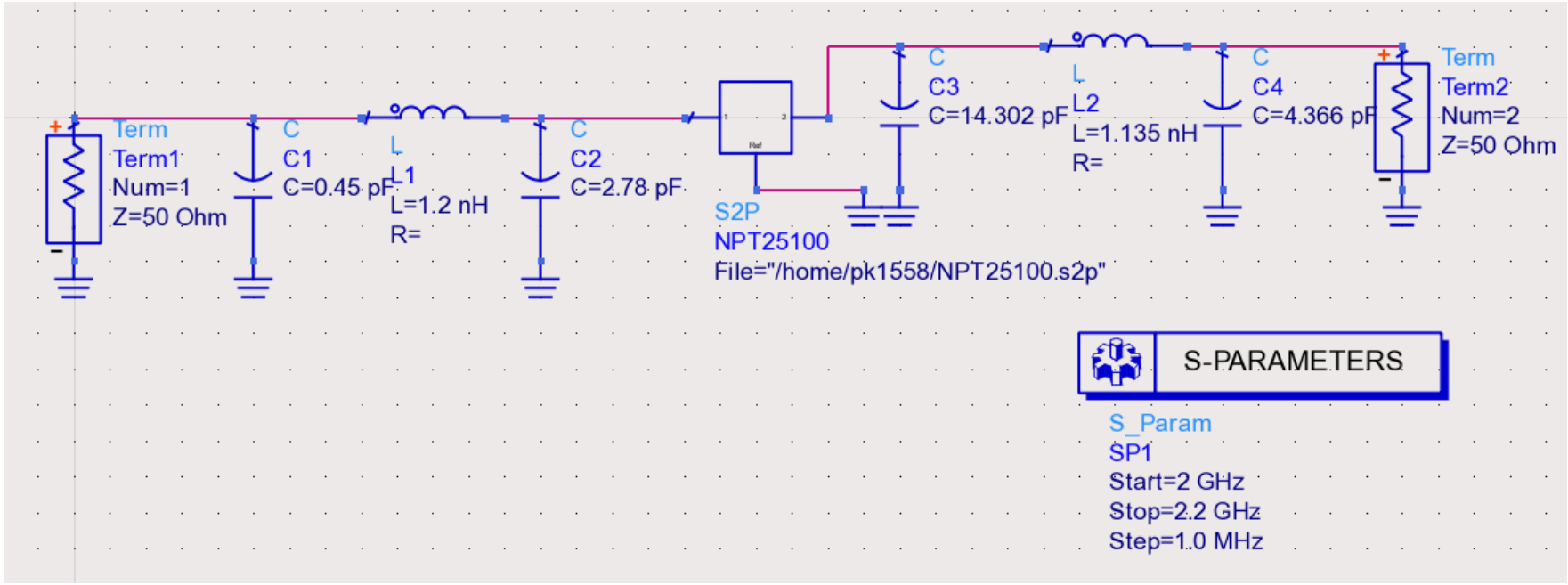
Simulation of the schematic



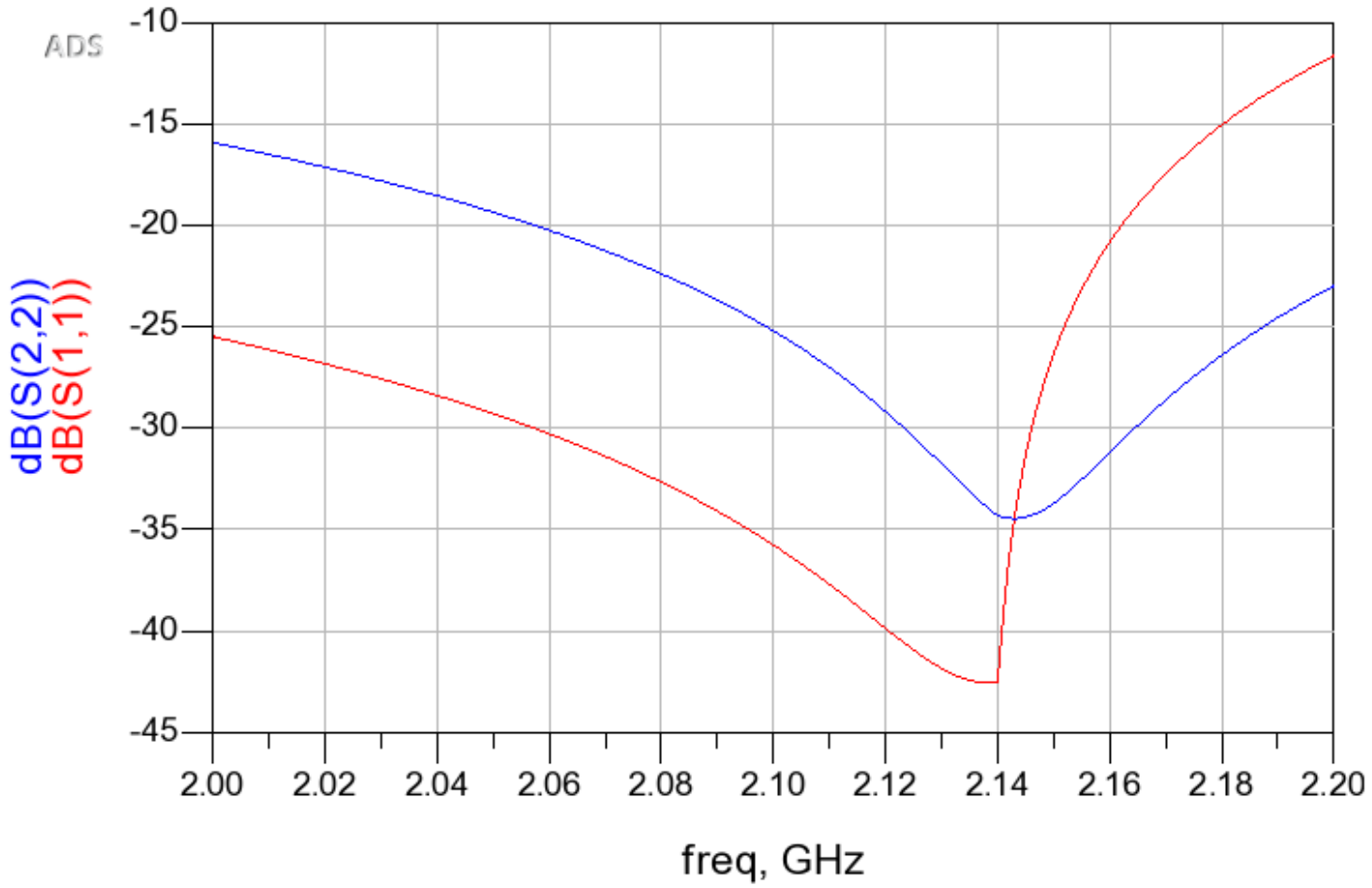
Complete Power Amplifier

```
! Large Signal Impedance of the NPT25100
# GHz Z RI R 1
! Freq ReZ1 ImZ1 M(S21) A(S21) M(S12) A(S12)    ReZ2 ImZ2
2.140 12.1 20.0 0 0     0 0 2.6 2.5
2.300 10.0 3.0 0 0 0 0 2.5 2.3
2.400 9.5 3.0 0 0 0 0 2.5 2.5
2.500 9.0 3.0 0 0 0 0 2.5 2.7
2.600 8.5 3.0 0 0 0 0 2.5 3.1
2.700 8.0 3.0 0 0 0 0 2.5 3.3
```

2-port S Parameter File and complete schematic

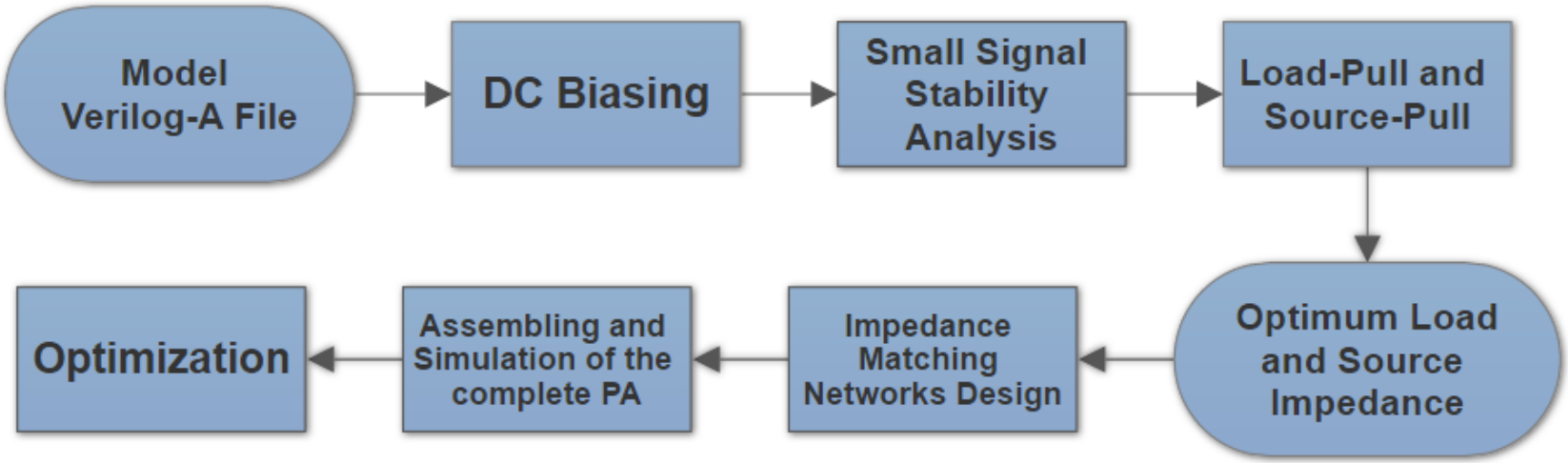


Simulation of the complete schematic



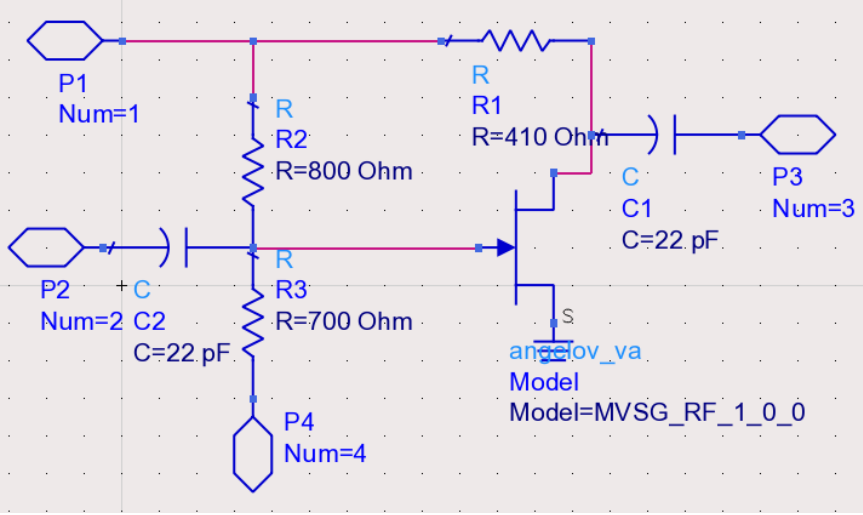
Thus, S11 and S22 have been minimized at the chosen frequency.

Design Example II - I aim to design a **10GHz Class-A Power Amplifier** using the **MVSG-RF Model**. Following flowchart re-establishes the steps to be followed.



As a tutorial, you could take a look at the ADS Design Cookbook at
http://cp.literature.agilent.com/litweb/pdf/5991-1516EN.pdf

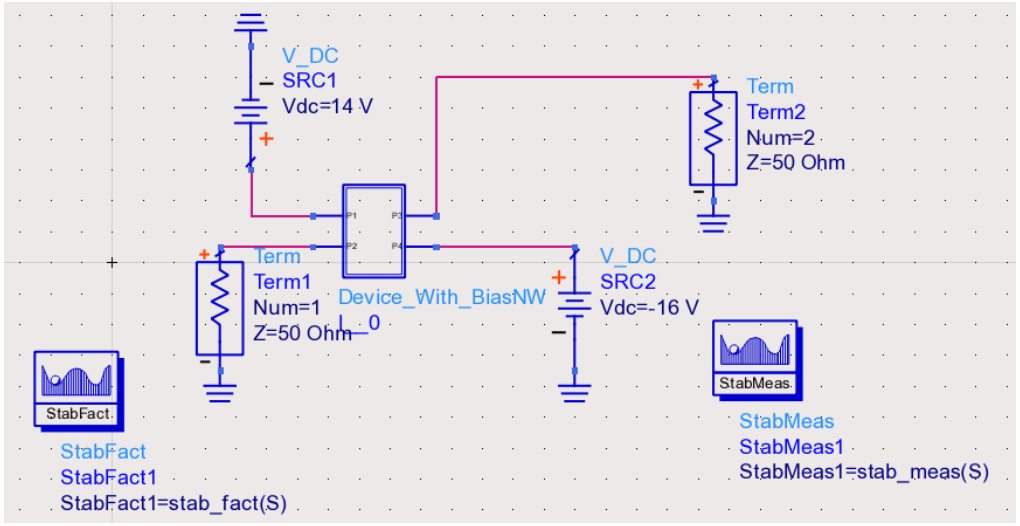
DC Biasing and Small Signal Stability Analysis



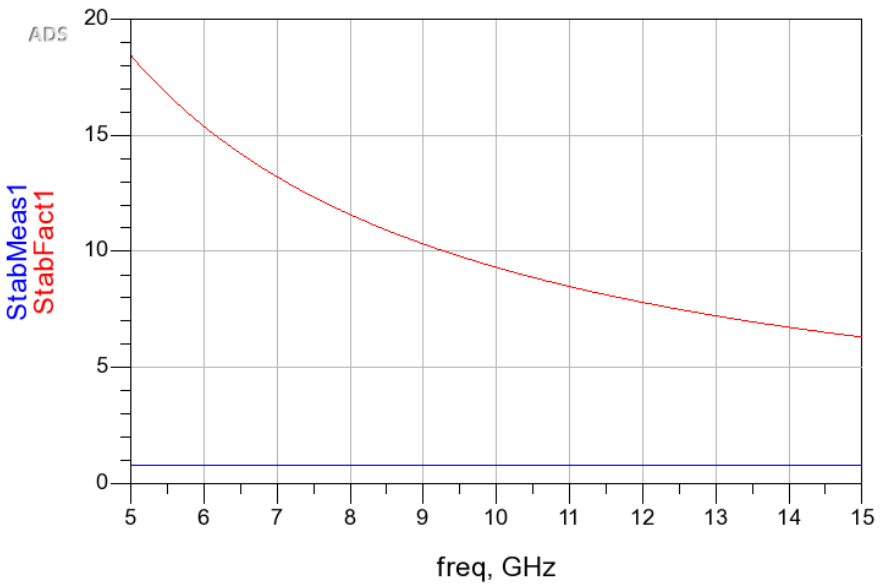
The **biasing is done** by applying bias voltages at pins 1 and 4. Pins 2 and 3 are for input and output. The bias point is chosen on the $I_D - V_{GS}$ graph so that the amplifier is class A.

Thus, The chosen bias point is V_{GS} = -2V, V_{DS} = 3.98V and I_D = 23.9mA by applying 14 and -16V at pins 1 & 4.

Further, the device is **checked to be stable**, by performing S-parameter simulations on the given circuit.
Necessary and sufficient conditions for device to be stable are:
Stability Factor (K) > 1 and
Stability Measure > 0. Refer to page 225 of the Cookbook.

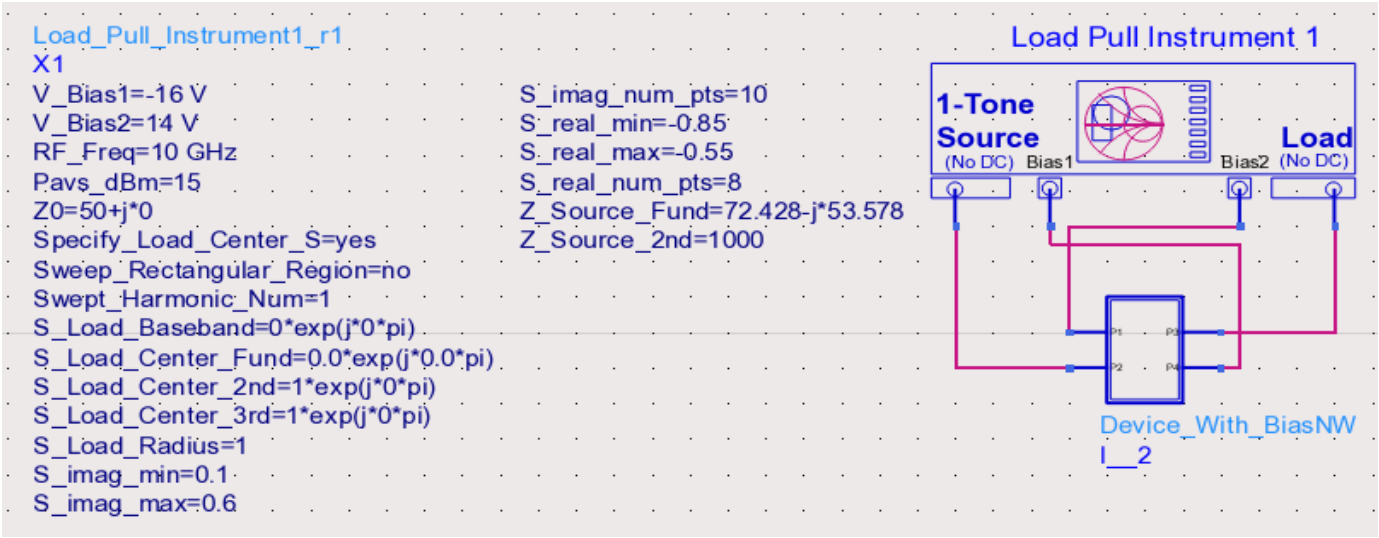


Stability Analysis Results and Load-Pull



It can be seen that Stability Factor is more than 1 and Stability Measure is greater than 0 over the entire frequency range, and hence our device is stable.

Load Pull is the technique during which we keep source impedance and source power constant and sweep impedance/reflection coefficient of load over a certain section of the smith chart to characterize Output Power. The template used is **Load Pull** from *Design Guides* and is shown below.



Load-Pull Analysis Results

At load that gives maximum power (and gain):

BiasCurrent_at_MaxPower	Zload_at_MaxPower	MaxPowerRho
0.019	387.361 + j188.402	0.811 / 5.877

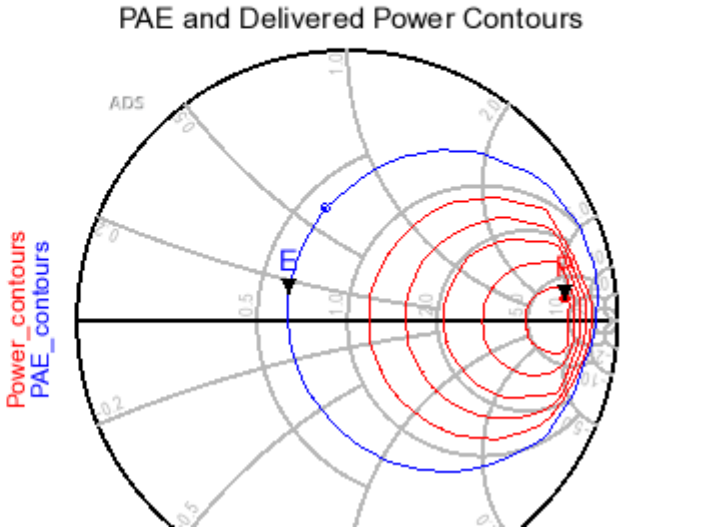
PAE_at_MaxPower
2.742

Z_In_at_MaxPower
304.161 - j208.601

Gain_at_MaxPower
0.689

Pdel_dBm_Max
15.689

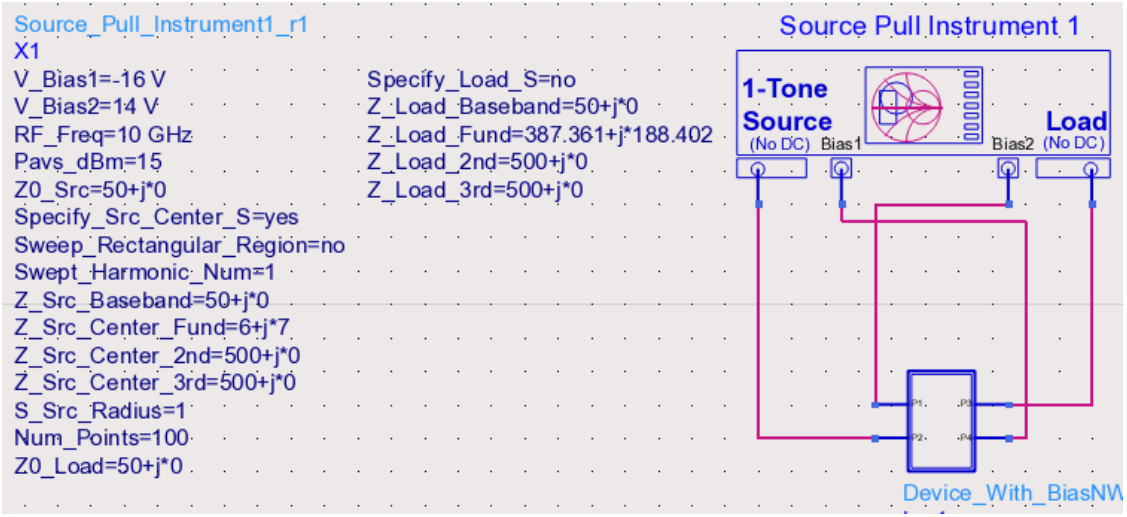
System Reference Impedance Z0: 50.000
A Rho of 0 corresponds to a load impedance of conj(Z0).



Load-Pull is performed using the *One-Tone Load Pull Simulation with constant Source Power* feature of ADS. From the analysis, **the optimum load impedance** for maximum power output comes out to be **387.361+j*188.402**. The gain is around 0.7 dBm.

Now, to find the optimum source impedance, we perform **Source-Pull**.

Source-Pull Analysis



Source-Pull is performed using the *One-Tone Source Pull Simulation with constant Source Power* feature of ADS, where we plug in the value of optimum load impedance, 387.361+j*188.402, into *Z_load_fund*. From the results, the **optimum source impedance** comes out to be **72.428+j*53.578**.

At source that gives maximum power (and gain):

BiasCurrent_at_MaxPower	Zsrc_at_MaxPower	MaxPowerRho
0.019	72.428 + j53.578	0.435 / 43.650

PAE_at_MaxPower
2.472

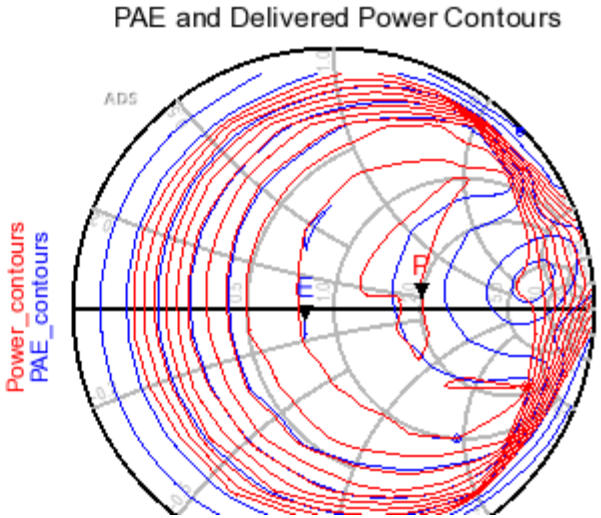
Z_In_at_MaxPower
330.325 - j218.705

Gain_at_MaxPower
0.739

Pdel_dBm_Max
15.739

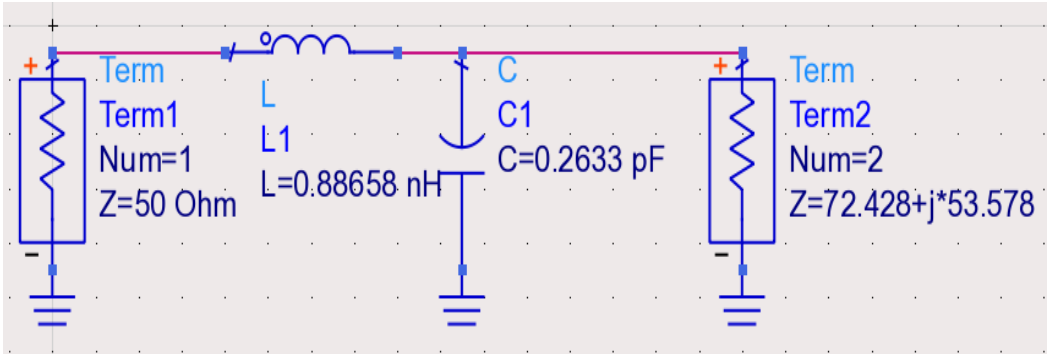
Source Reference Impedance Z0:
A Rho of 0 corresponds to a source impedance of conj(Z0).

50.000

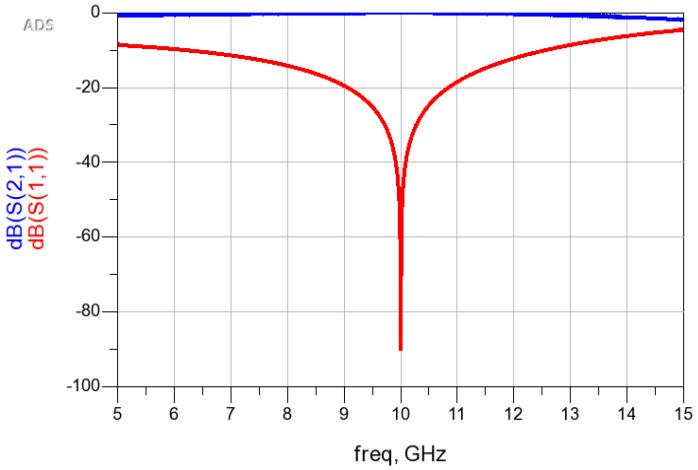


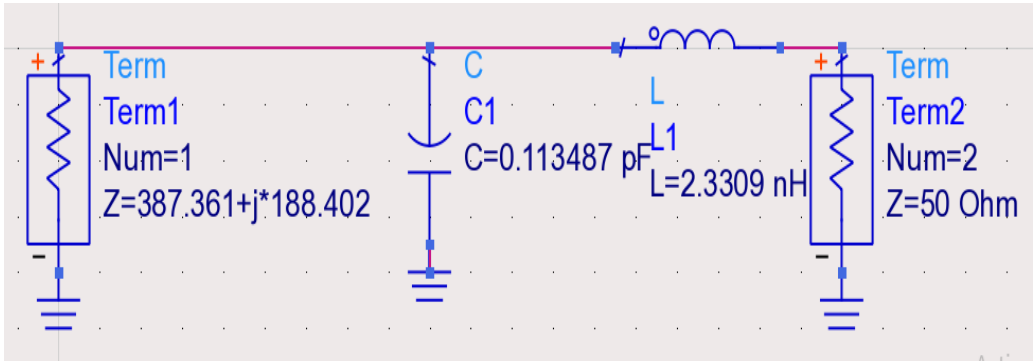
Impedance Matching Networks Design

L-matching networks for the input and output sides are designed with respect to the optimum source and load impedance. The designs are verified through S-parameter simulations.

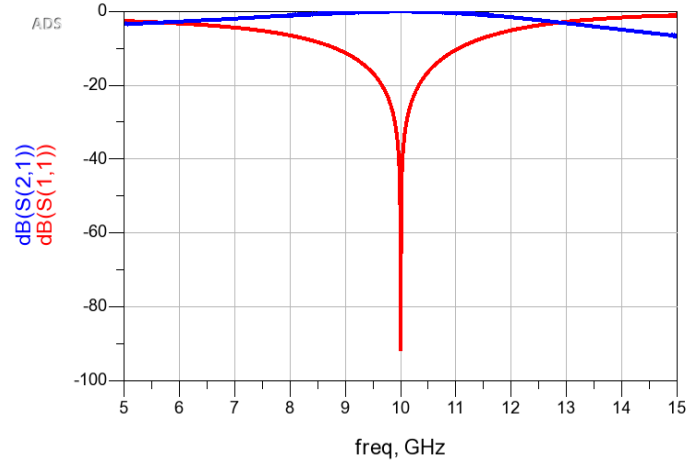


Input Matching Network Design

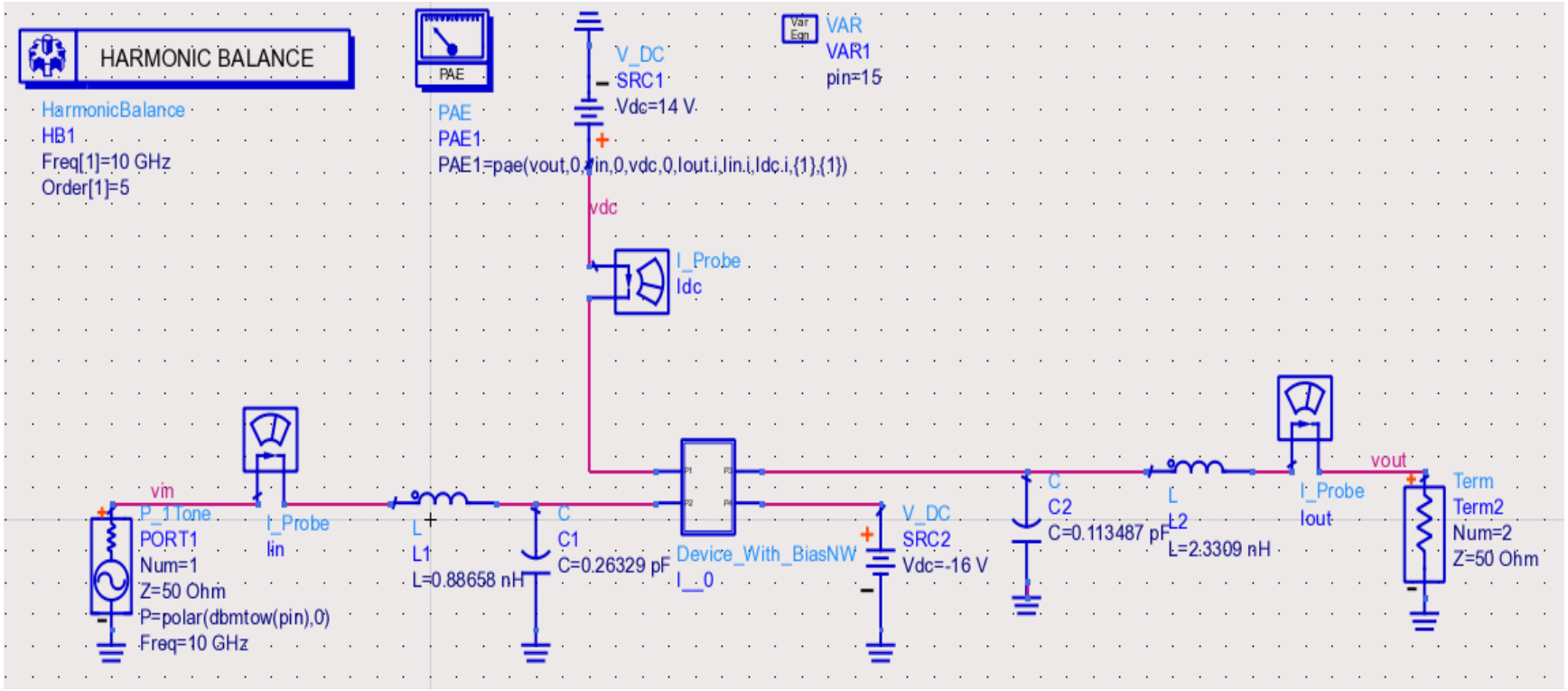




Output Matching Network Design

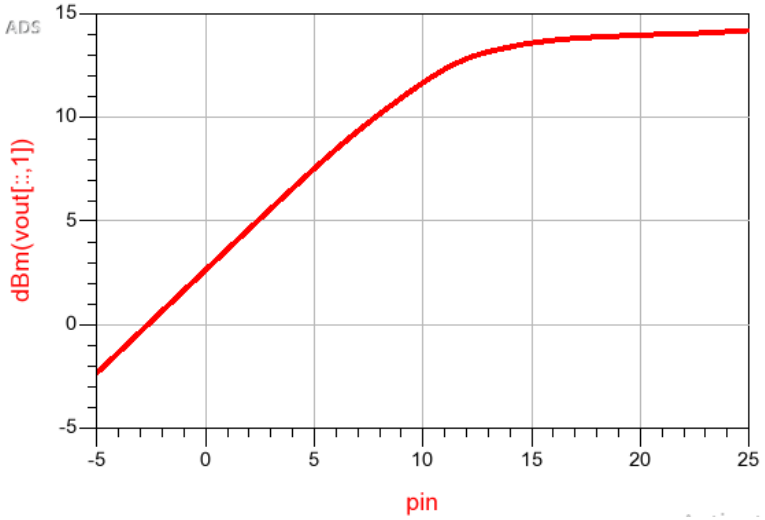


Assembling and Simulation of the complete Power Amplifier



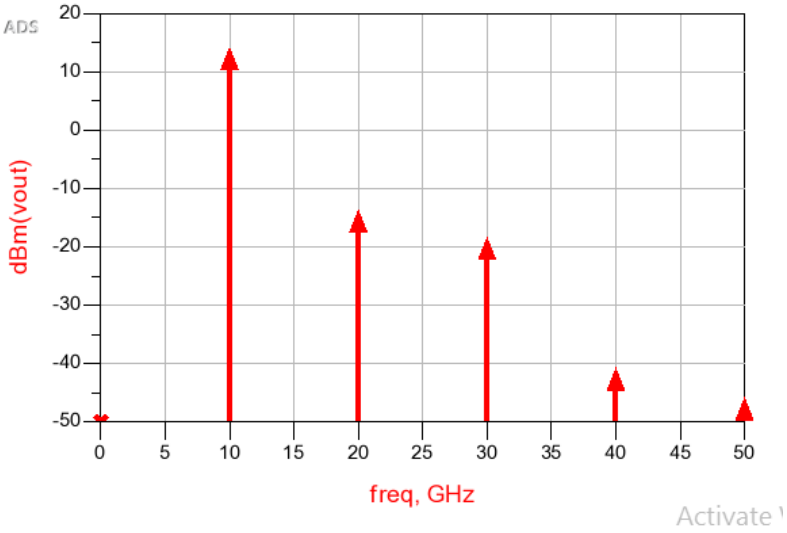
The Device with Biasing Network is assembled with both the impedance matching networks and various probe components. On performing Harmonic balance simulations, the output power in dBm of various harmonics and the P_{OUT} vs P_{IN} graphs were obtained, which are displayed on the next slide.

Performance of the Power Amplifier



The P_{OUT} vs P_{IN} graph saturates at about 13 dBm of input power and provides a gain of about 1.5 dBm at 10 dBm of input power.

From the HB Simulations, it is found that the output harmonics at 15dBm of input power are distributed as follows:
Fundamental : 14.8 dBm
2^{nd} Harmonic : -15 dBm
3^{rd} Harmonic : -19 dBm
and so on.

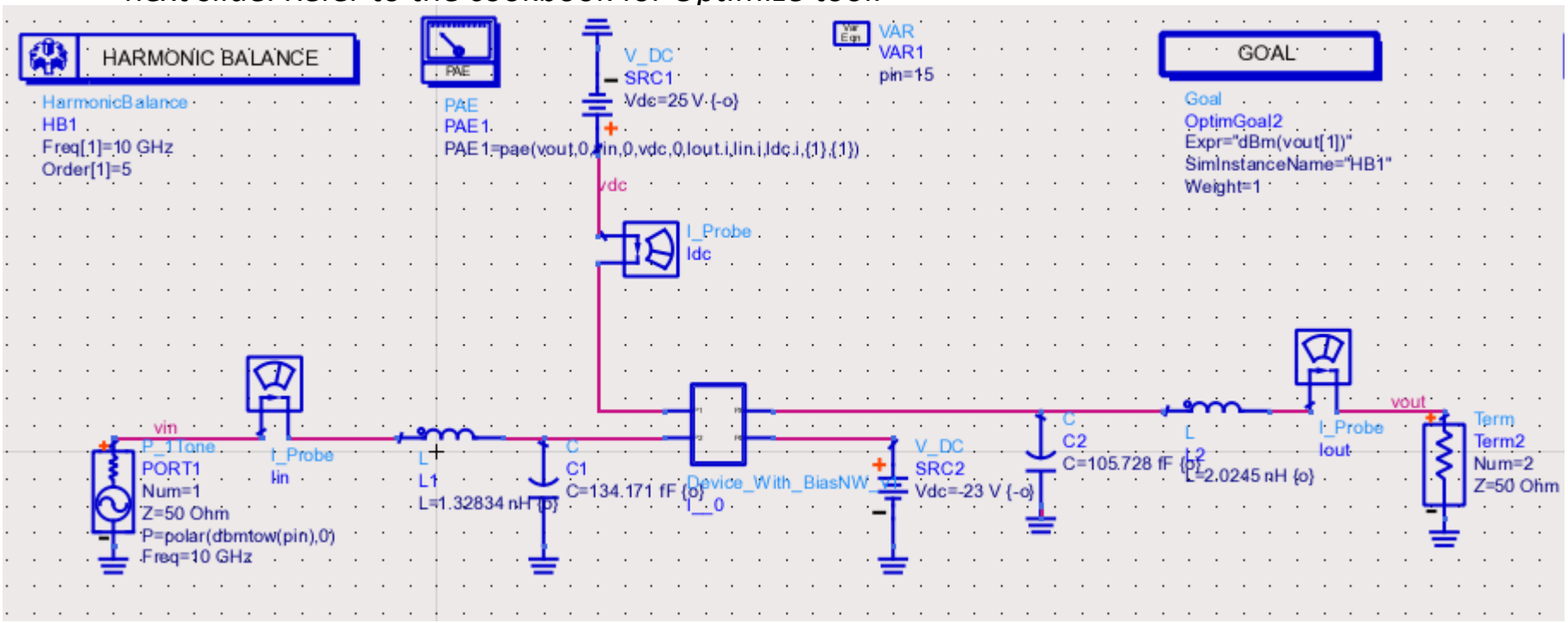


Optimization of the Performance

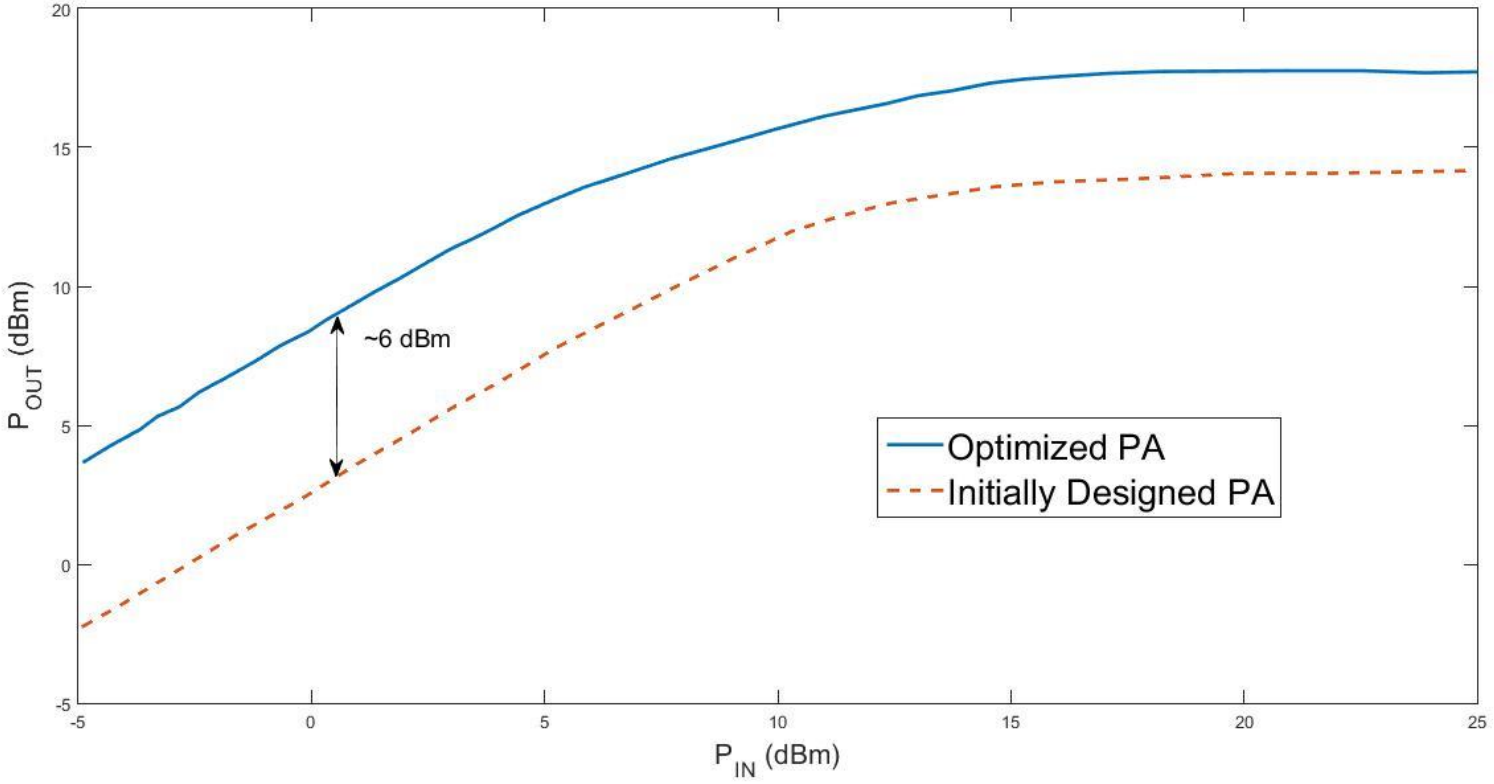
The change in performance of the Power Amplifier is investigated via two methods –

1. **Circuit Level Modifications**
2. Device Parameter Modifications

Circuit Level Modifications - The following figure illustrates the optimized design. This was done using the optimize tool of ADS by defining various circuit elements as optimizable. The goal was set at P_{OUT} = 20 dBm. After various iterations, the bias voltages were changed to 25V and -23V for better performance. Comparison with the previously designed PA is done on the next slide. Refer to the cookbook for *Optimize* tool.



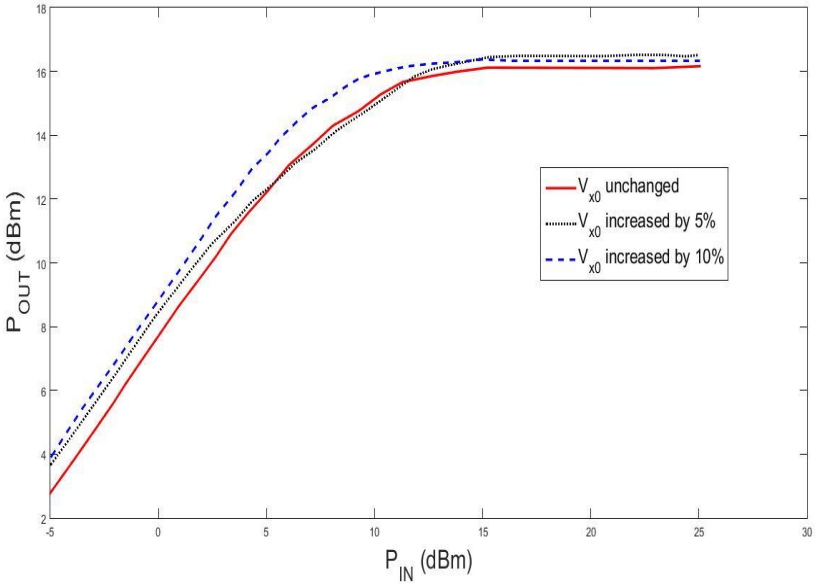
Impact of Circuit-Level Modifications

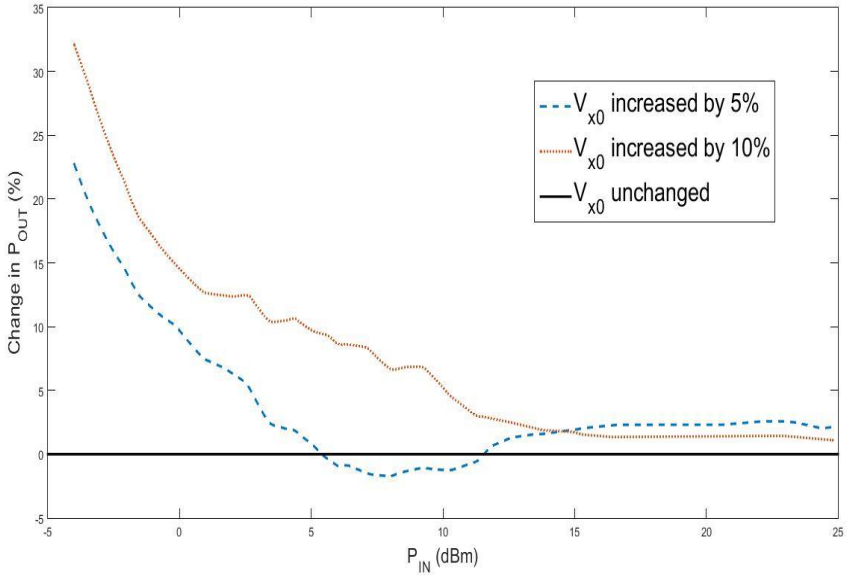


There is a significant improvement of 6 dBm in gain by optimization of the circuit. Now, **Device Parameter modifications** are carried out and their impact on performance noted.

Impact of Device Parameters Modifications

The source injection velocity, V_{xo}, was varied from its default value of 1.3e7 cm/s. The whole circuit was optimized for each change and the following graphs illustrates the Pout vs Pin characteristics and the change in P_{OUT} (%) after each such optimization. The goal was once again set at 20 dBm.





Thus, we observe that the amplifier performance is not affected much by changes in the source injection velocity, v_{xo}, as compared to circuit-level modifications.

Goals Achieved –

1. Successfully performed Load-Pull analysis on the MVSG-RF Model and designed a Power Amplifier exhibiting a high value of gain.
2. Optimized the performance of the power amplifier by circuit-level changes.
3. Investigated the change in performance by device parameter (v_{xo}) modifications.

Future Work –

1. For spectrally-efficient information transmission, highly linear PAs are required. Thus, the next step is **understanding non-linear distortion and implementing various linearization techniques** like Feedforward, Feedback and Predistortion Linearization.
2. To study the effect of Joule Heating on the performance.
3. To study the impact of change in various parameters like mobility, access region resistance on the performance of the power amplifier.
4. Compare the effects of various technology parameters by quantifying the sensitivity of gain relative to the particular parameter.

References –

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