Implementation of an 8-bit Microprocessor and Signal Monitoring System

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Outline I

Outline II

Introduction

- Embedded microprocessors, today, are used in a variety of electronic products.
- The Central Processing Unit is the core of the computer.
- In Part I of this project, I have implemented an FPGA-based 8-bit microprocessor which does basic 8085-level ALU and memory operations.
- It is designed in Verilog and mainly consists of 8 8-bit registers in a Register File, 256-word memory with 16-bit words, a Control Unit and a Function Unit implementing ALU operations.

- An Analog-to-Digital Converter is of prime importance whenever real-world signals come into play.
- This is used in the second part, where a custom microprocessor is realized.
- The XADC (Analog-to-Digital Converter) is interfaced to convert an incoming real-world analog signal to digital form. This data is validated and further checked to determine if it is noise or contains a signal.

Motivation and Relevance

- The 8085 is regarded as the father of all CPU designs and all later microprocessors were an enhancement of it.
- Thus, I would gain a good idea about basic computer architecture by implementing the same from scratch.
- Part II of this project (Signal Monitoring System) has great applications in the monitoring of illicit activities in forests.
- Forests are troubled by the increase of deforestation and poaching of endangered wildlife.
- For that, an ASIC based on my FPGA-prototype of an Audio (Analog Signal) Monitoring System will help in surveillance. The chip will detect any out-of-the-ordinary sounds in the surroundings and communicate a warning to the base station.

Part I - Microprocessor Implementation

- Microprocessors are the devices in a computer that make things happen.
- An 8-bit microprocessor can read/write 1 byte at a time and can directly access 256 bytes.
- In this part, I implement a general purpose RISC (reduced instruction set computing) microprocessor with a clock rate of 50 MHz (on-board oscillator).
- The implementation is done in a modular fashion and the descriptions of the various modules follow.

Instruction Set Architecture

The processor is designed to input 16-bit set of instructions. The format is as follows.

15 14 13 12	11	10	9	8 7 6	5 4 3	2 1 0
FS	MD	RW	MB	DA	AA	BA

Here AA, BA and DA are the A, B and Destination addresses i.e. one register out of R0 to R7. The control word further contains MB (Mux B select), FS (Function select), MD (Mux D select) and RW (Register Write). The control word is held by the Instruction Register module and fed into the datapath.

Datapath

Datapath is a set of functional units that carry out data processing operations. It is comprised of a register file, a function unit and two multiplexers.

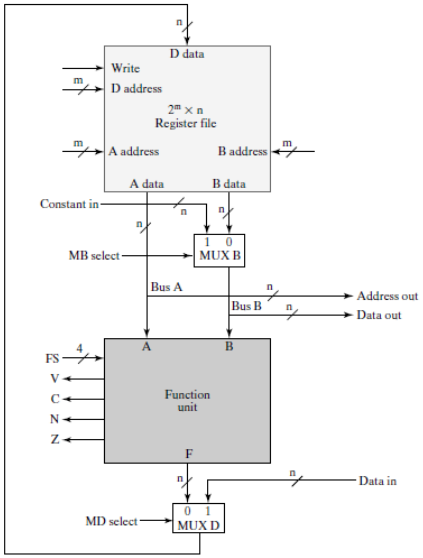

Figure 1: The Datapath

Register File

A simpler 4-register Register File with n-bit data storage is shown in figure 2.

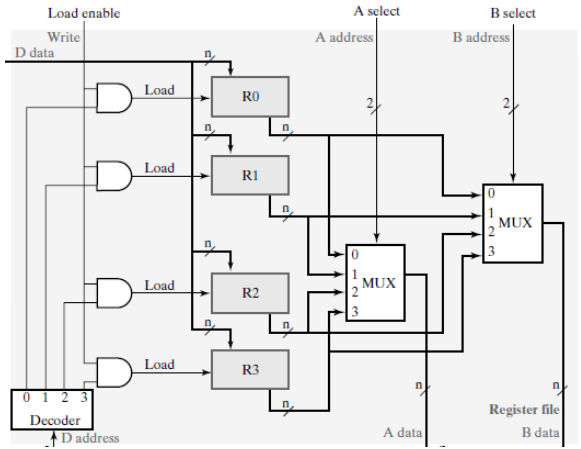

Figure 2: A simple 4*n register file

The operands for and the result of ALU operations is stored in the registers in the register file and could be re-used in a subsequent operation or saved into memory.

Function Select Bits

Function Select	Operation	Function
0000	F = A	Transfer A
0001	F = A + 1	Increment A
0010	F = A + B	Addition
0011	F = A + B + 1	Add with carry input of 1
0100	F = A + $\tilde{B}$	A plus 1s complement of B
0101	F = A + $\tilde{B}$ + 1	Subtraction
0110	F = A - 1	Decrement A
0111	F = A	Transfer A
1000	F = A AND B	AND
1001	F = A OR B	OR
1010	F = A XOR B	XOR
1011	F = $\tilde{A}$	NOT
1100	F = B	Transfer B
1101	F = B >>1	Right Shift by 1
111X	F = B <<1	Left shift by 1

Memory

The memory has 256 words and each word is comprised of 16 bits. An 8-bit address specifies the memory location which is being written to or read from.

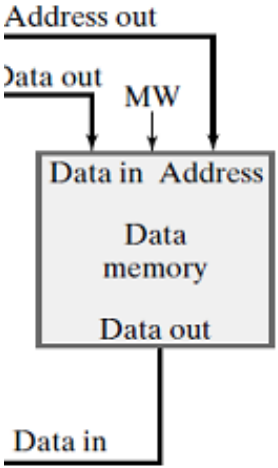

Figure 3: Memory

Bits of the control word

The function of various bits in the Control Word are as follows.

AA, BA, DA	Register select
000	Select R0
001	Select R1
010	Select R2
011	Select R3
100	Select R4
101	Select R5
110	Select R7
111	Select R7

Table 2: AA, BA and DA bits

MD	Operation
0	Bus D is fed with the ALU output
1	Bus D is fed with an external data input

Table 3: Mux D select bit

MB	Operation
0	BDATA from the register file is fed into the ALU
1	An external data input is fed into the ALU

Table 4: Mux B select bit

RW	Operation
0	No writing to memory
1	Writing to memory

Table 5: RW bit

The operations of the Function Select (FS) bits have already been tabulated in Table 1.

Part I - Microprocessor Results

The code is provided in Appendix A of the report and the results follow. The testbenches for the codes are given at `home.iitk.ac.in/~pranavk/ugp3/tbs`

- Multiplexer

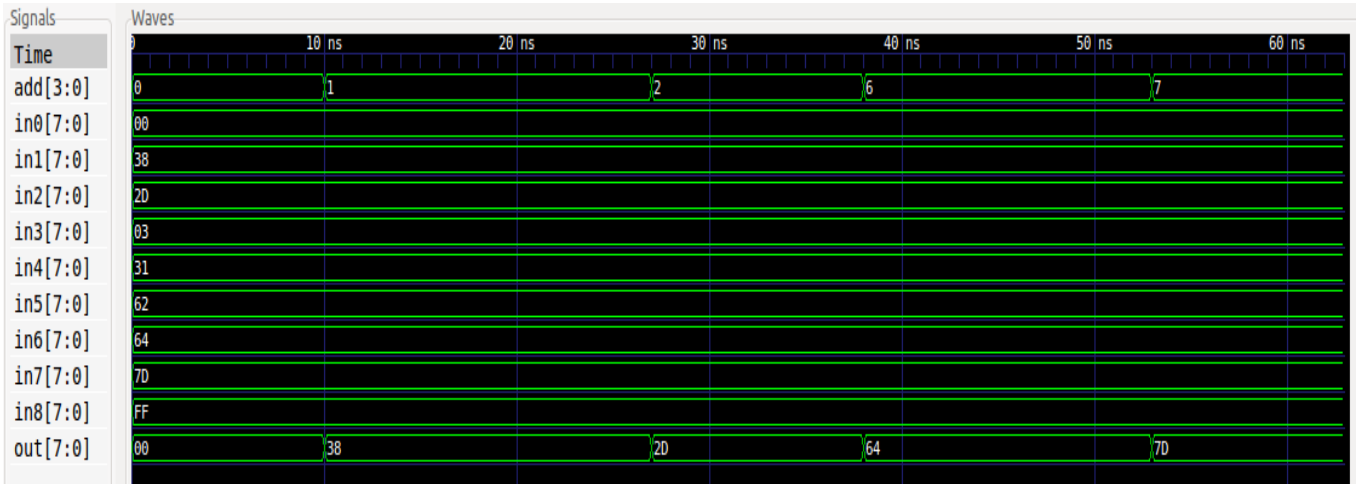

Figure 4: Multiplexer Results

- Decoder

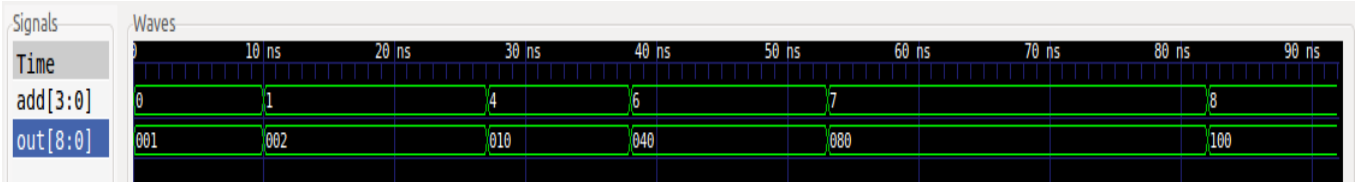

Figure 5: Decoder Results

- Register

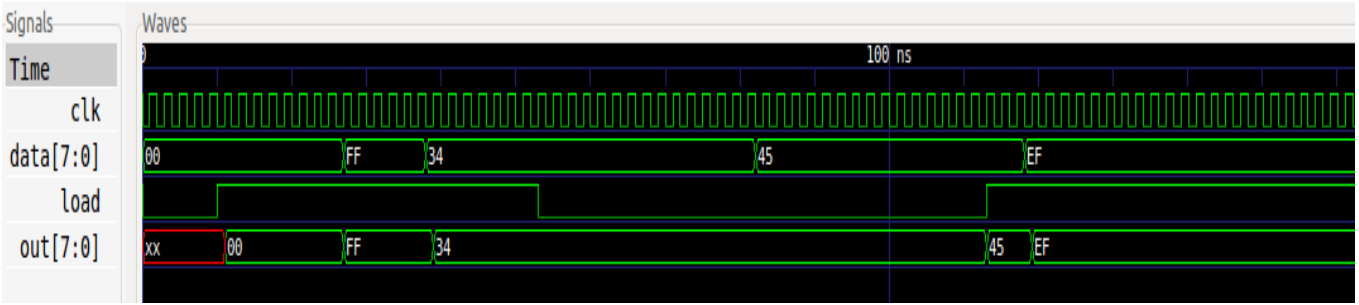

Figure 6: Register Results

- Register File

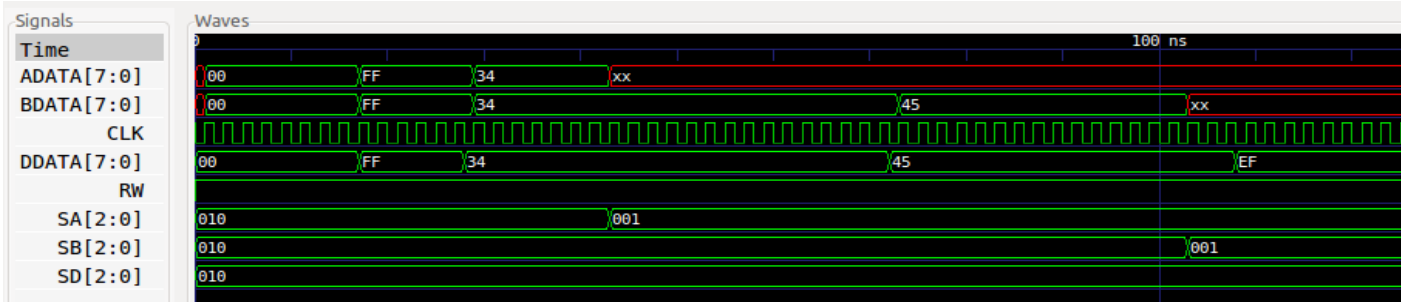

Figure 7: Register File Results

- Memory

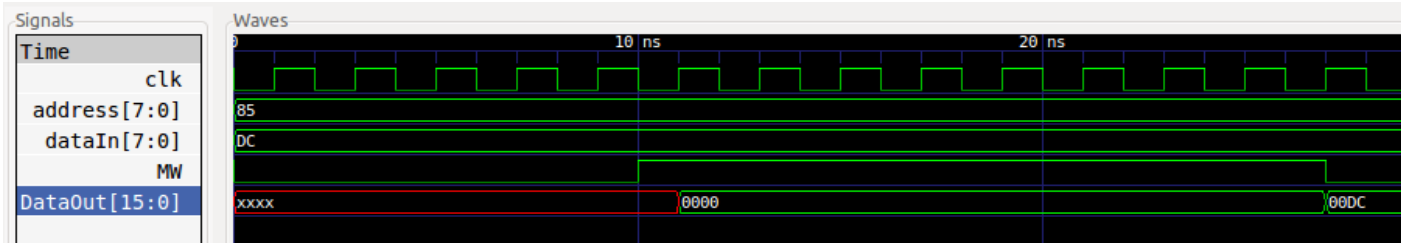

Figure 8: Memory Results

- Microprocessor

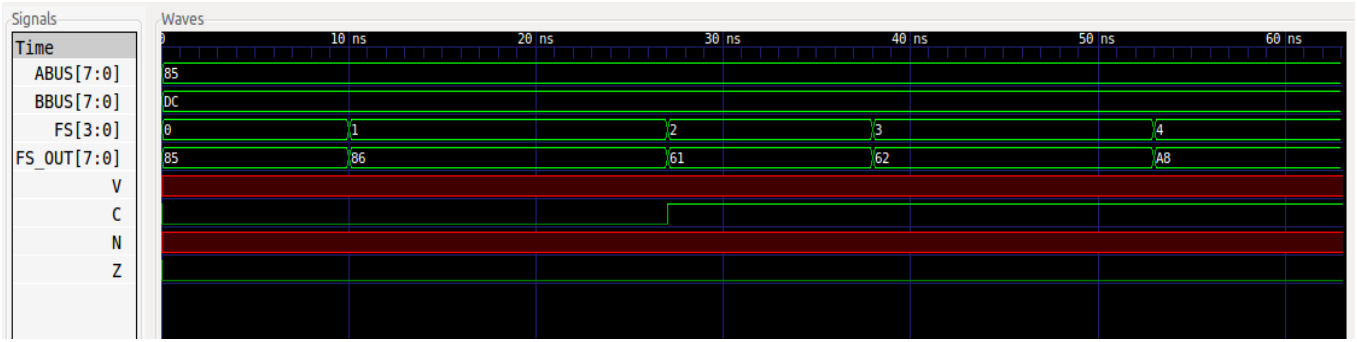

Figure 9: Microprocessor Results - I

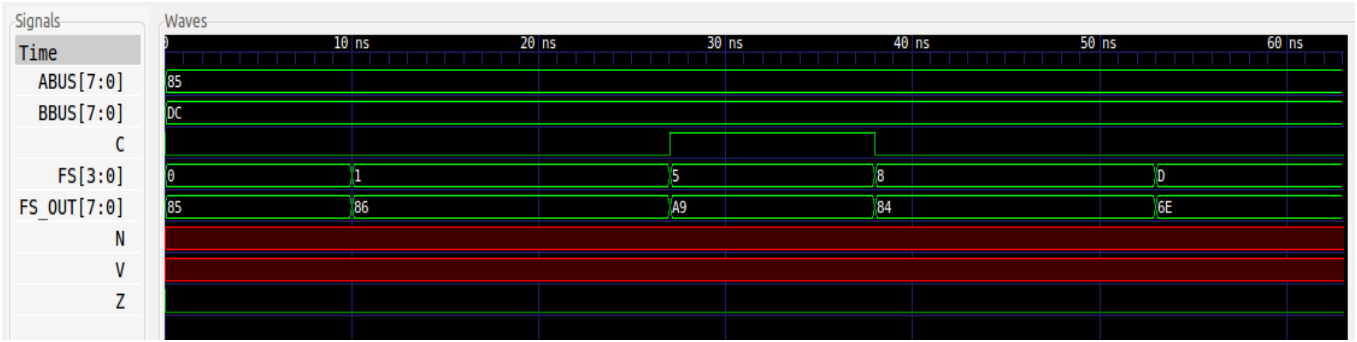

Figure 10: Microprocessor Results - II

Part II - Signal Monitoring System Implementation - XADC Functionality

- This part of the project makes use of an XADC (Analog-to-Digital Converter) on the Basys3 FPGA Board to firstly digitize an incoming analog signal.
- Further, it is checked if the signal is deterministic or random noise.
- If it is deterministic, an alarm is raised for an indefinite time until it is reset manually.

XADC Description

- The XADC includes a dual channel 12-bit, 1 Mega sample per second (MSPS) ADC and on-chip sensors.
- The dual ADCs support a range of operating modes and various analog input signal types.

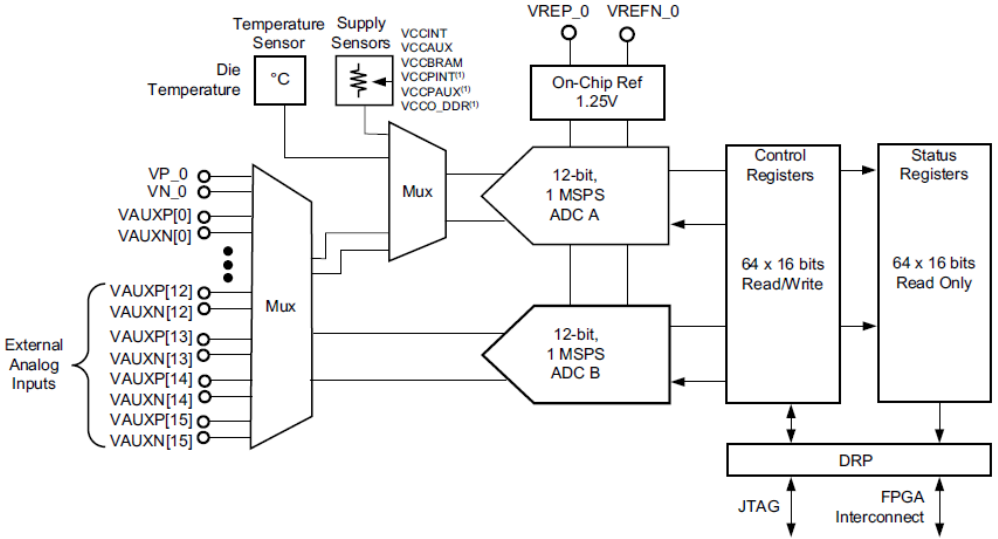

Figure 11: XADC Block Diagram

XADC Operating Modes and Input Signal Types

The XADC includes several operating modes like -

- default
- Single Channel Mode
- Simultaneous Sampling Mode.

The external analog input channels can be configured to operate in unipolar or bipolar mode -

- Unipolar Mode - Input range to the ADC is 0V to 1V. The ADC produces 000h when 0V is present and FFFh when 1V is present on the input.
- Bipolar Mode - Input range is -0.5V to 0.5V in this mode. The ADC produces a two's complement output code, that is, 000h for 0V, 7FFh for 0.5V and 800h for -0.5V.

As I am dealing with real-world signals, I'll be operating in the bipolar mode.

Status Registers

The status registers contain the results of an analog-to-digital conversion of the on-chip sensors and external analog channels. Each such measurement is mapped to a unique address.

Name	Address	Measurements of
Temperature	00h	On-chip temperature sensor
VCCINT	01h	Power Supply Sensor
VCCAUX	02h	Power Supply Sensor
VCCBRAM	06h	Power Supply Sensor
VP/VN	03h	Dedicated analog input
VAUXP/N[15:0]	10h to 1Fh	External analog inputs

Table 6: Status Registers (Read-Only)

Control Registers

These registers are used to configure the XADC operation.

Name	Address	Software Attribute	Description
Config Reg 0	40h	INIT40	To configure XADC
Config Reg 1	41h	INIT41	To configure XADC
Confi Reg 2	42h	INIT42	To configure XADC
Test Regs 0-4	43h-47h	INIT43-INIT47	Default value = 0000h

Table 7: XADC Control Registers

Instantiating and initializing the XADC

- To allow access to the status registers, the XADC must be instantiated. This refers to initialization of the control registers.
- Once the XADC has been instantiated, the different ports of it can be made use of.

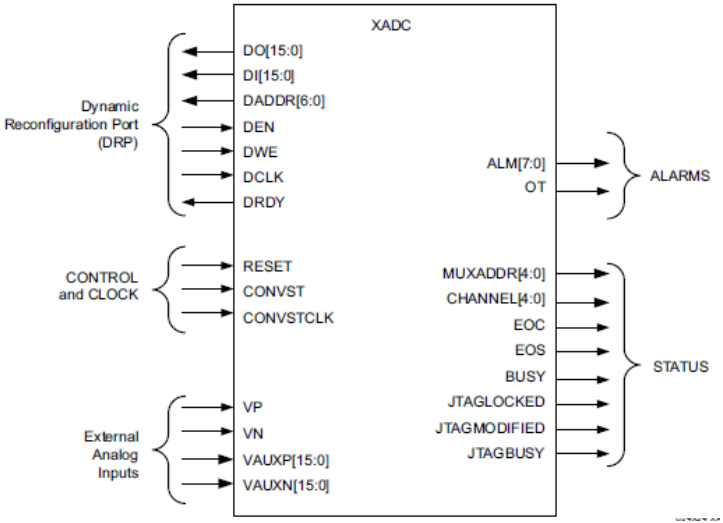

Figure 12: XADC Ports

The table below lists the functionality of the used ports.

Port	I/O	Description
DI[15:0]	Inputs	Input data bus
DO[15:0]	Outputs	Output data bus
DADDR[6:0]	Input	Address bus
DEN	Input	Enable signal
DWE	Input	Write enable signal
DCLK	Input	Clock input for the DRP = 50MHz
DRDY	Output	Data ready signal for the DRP
RESET	Input	Asynchronous ADC Reset signal
CONVST	Input	Convert Start Input
CONVSTCLK	Input	Convert Start Clock Input
VP, VN	Input	Dedicated Analog Input Pair
VAUXP/N[15:0]	Inputs	Sixteen external analog input pairs
EOC	Output	End of conversion signal
EOS	Output	End of sequence signal
Busy	Output	ADC Busy signal

Table 8: XADC Port Descriptions

- The external input is averaged over 32 samples so as to reduce the error. On averaging over N samples, the standard deviation of the error reduces to one-$\sqrt{N}$th of the original.
- Once error is reduced, the averaged digitized value is checked with a threshold (0.1V).
- If it is above it, I claim it to be a deterministic signal and raise an indefinite alarm.
- The second analog signal is the external Reset signal. If it goes above a certain value (0.5V), the alarm is reset.

TIME	VAUXP[0]	VAUXN[0]	VAUXP[1]	VAUXN[1]
00000	0.000	0.0	0.1	0.0
50000	0.2	0.0	0.0	0.0
90000	0.5	0.0	0.0	0.0
121000	0.0	0.0	0.6	0.0

Table 9: Input 1

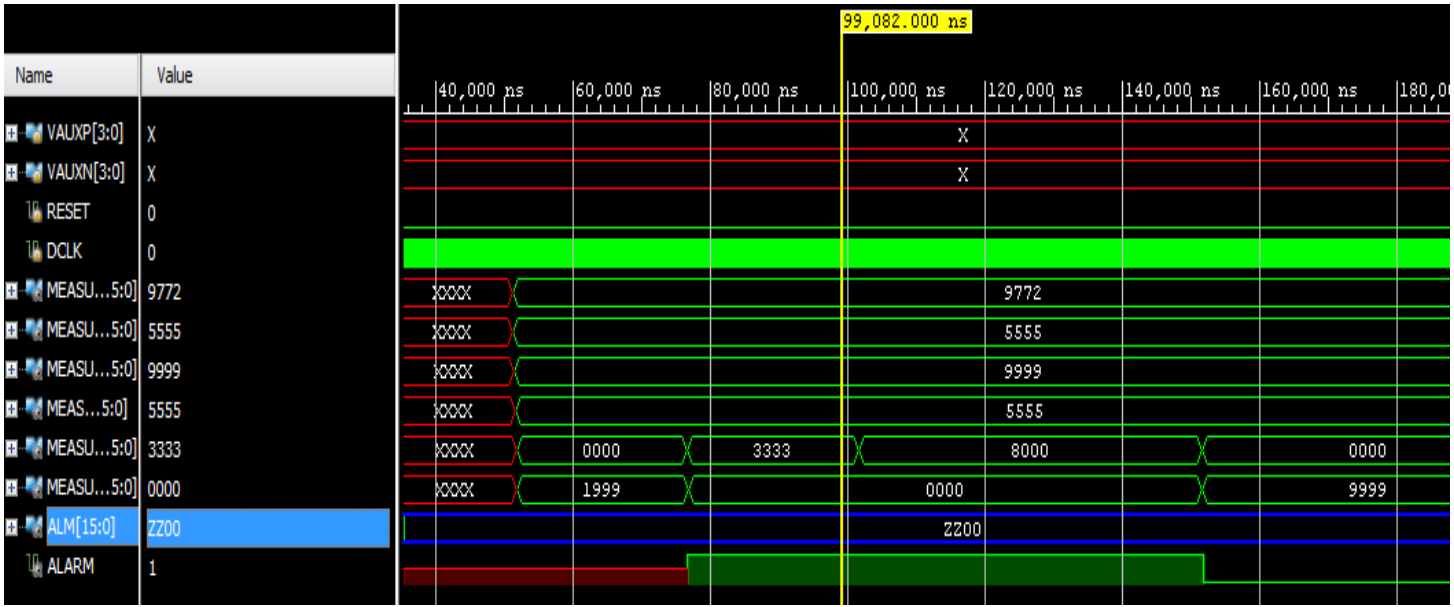

Figure 13: Results 1

The ALARM bit is set whenever the average of the last 32 samples of MEASUREDAUX0 goes above 0.1V and is reset whenever the average of the last 32 samples of MEASUREDAUX1 goes above 0.5V.

TIME	VAUXP[0]	VAUXN[0]	VAUXP[1]	VAUXN[1]
00000	0.000	0.0	0.1	0.0
10000	0.1	0	0.15	0
20000	0.15	0	0.1	0
30000	0.13	0	0.65	0
40000	0.08	0	0.15	0
50000	0.2	0.0	0.0	0.0
60000	0.3	0	0.15	0
65000	0.35	0	0.15	0
70000	0.1	0	0.15	0
80000	0	0	0.15	0
85000	0.05	0	0.65	0
90000	0.5	0.0	0.0	0.0
100000	0.0	0	0.15	0
110000	0.5	0	0.15	0
121000	0.0	0.0	0.6	0.0

Table 10: Input 2

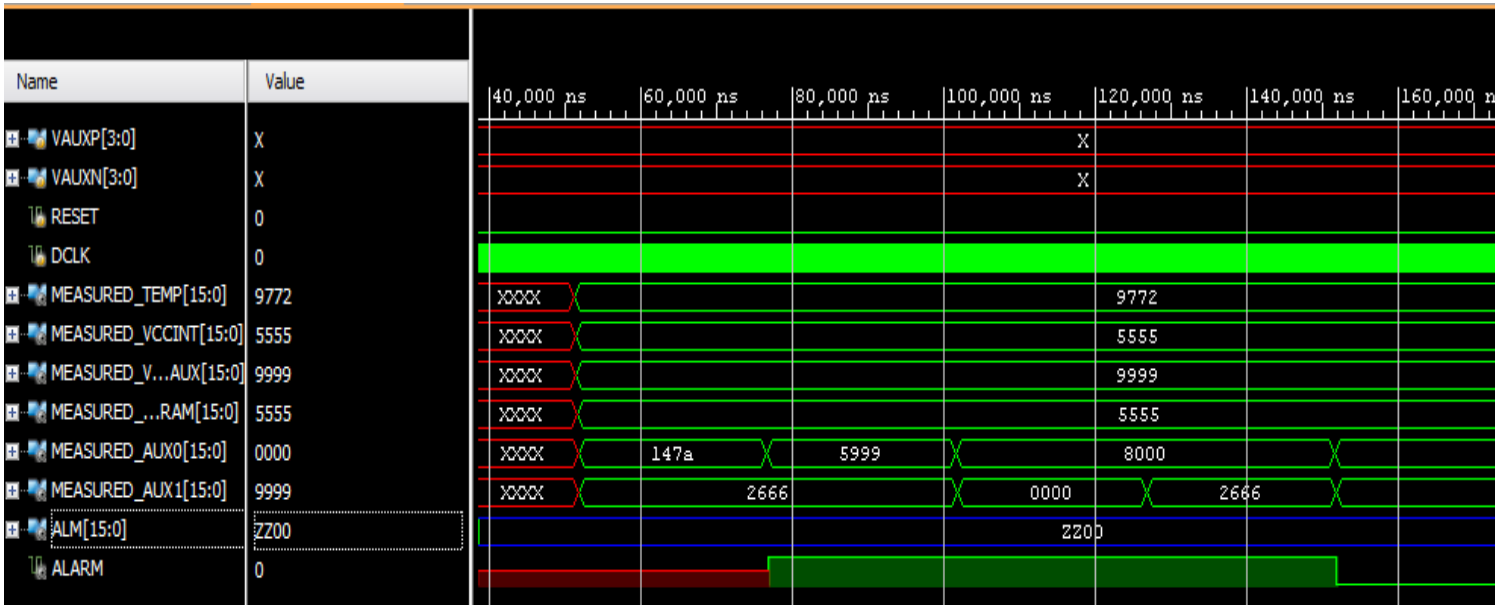

Figure 14: Results 2

The averaging is evident in Result 2 as the measured value doesn't change every 10000 ns as in the analog stimulus file, rather it changes every 32 samples (= 32000 ns) to a value equal to the average of the previous 32 samples.

Future Work

- The Signal Monitoring System can be extended and built as a System-on-chip for forest surveillance purposes.
- It would efficiently determine any out-of-the-ordinary sounds (analog signals) in the forest and any anomalous situation would be immediately reported to the base station via an alarm.
- Once the situation has been checked on and resolved, the alarm may be stopped by an external electromagnetic reset signal to the ASIC.

References

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