An Improved CMOS Design For A Full Adder Circuit

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EE610A

November 11, 2016

Outline

Introduction

- Many VLSI applications like DSP, Image Processing and Microprocessors use logic gates and perform arithmetic and logical operations.
- A full adder is an important part and is extensively used in arithmetic circuits.
- A full adder can add two inputs and a bit carried over from another addition as well.
- Improving the performance of the full adder is desirable as it will enhance the overall circuit performance as well.
- The aim of this project is to implement an improved CMOS design of a full adder.

Abstract

- In this project, a 1-bit modified full adder design employing complementary metal– oxide–semiconductor (CMOS) logic is implemented.
- The circuit is implemented using Mentor Graphics tools 180nm technology.
- The total power dissipation and the number of transistors are finally compared with the traditional CMOS designs.

Full Adder Description

The full adder has three one-bit binary inputs and two one-bit binary outputs. The first two inputs are A and B and the third input is an input carry designated as C_{IN}. It outputs a SUM and carry out, C_{OUT}. The block diagram and truth table is shown in figure 1 and table 1 respectively.

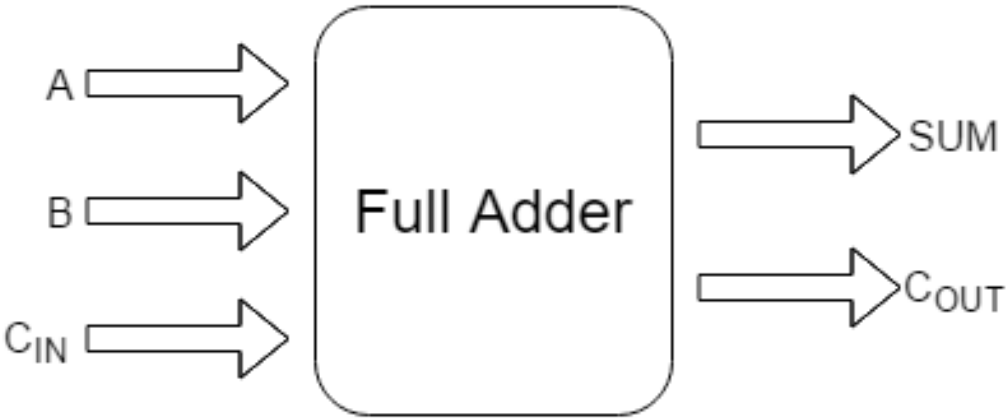

Figure 1: Full Adder Block Diagram

Full Adder Truth Table

A	B	C_{IN}	C_{OUT}	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1: Full Adder Truth Table

Full Adder Logic Description

From the above truth table, the full adder logic is derived. It is easily seen that SUM is the XOR of A, B and C_{IN}. For C_{OUT},

$$\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

$$C(\overline{A}B + A\overline{B}) + AB(\overline{C} + C)$$

$$C.A \oplus B + A.B$$

Thus,

$$S = A \oplus B \oplus C$$

$$C_{OUT} = C.(A \oplus B) + A.B$$

Implementation via logic gates

Figure 2 shows the logic gate implementation of a full adder. Total MOSFETs = 36. Thus, highly undesirable due to high parasitics and power requirement.

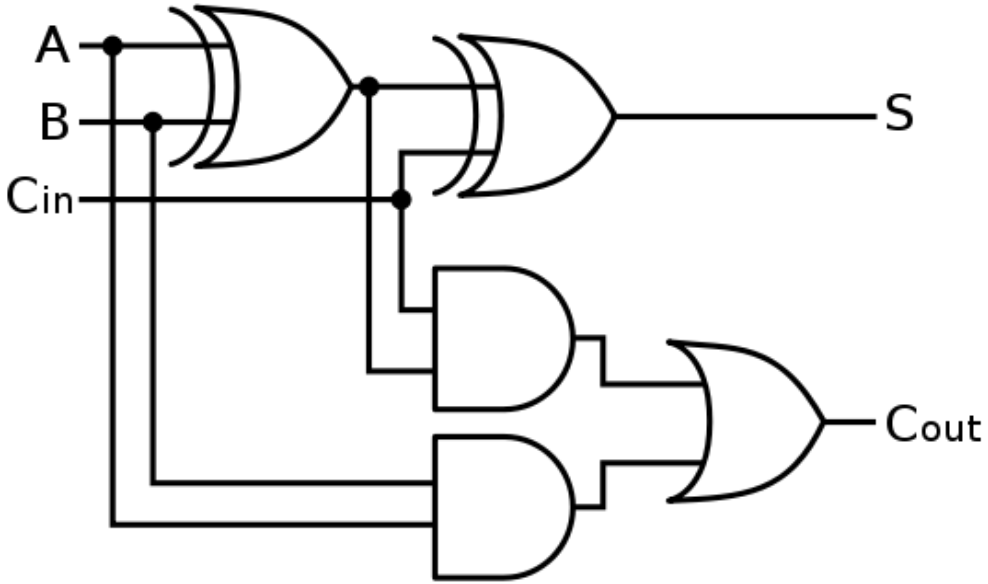

Figure 2: Logic Gate Implementation

Our implementation

We implement the design given at `http://www.cmosvlsi.com/lect11.pdf`. In this we factor SUM in terms of C_{OUT} as

$$SUM = ABC + (A + B + C).\overline{C_{OUT}}$$

The technology used is 180nm (that is L = 180nm) and the ratio W/L was same for all the MOSFETs. Therefore, we chose a few values of W/L (0.5, 1, 2, 4, 6) and finalize on W/L = 4 because comparatively it gives the best output

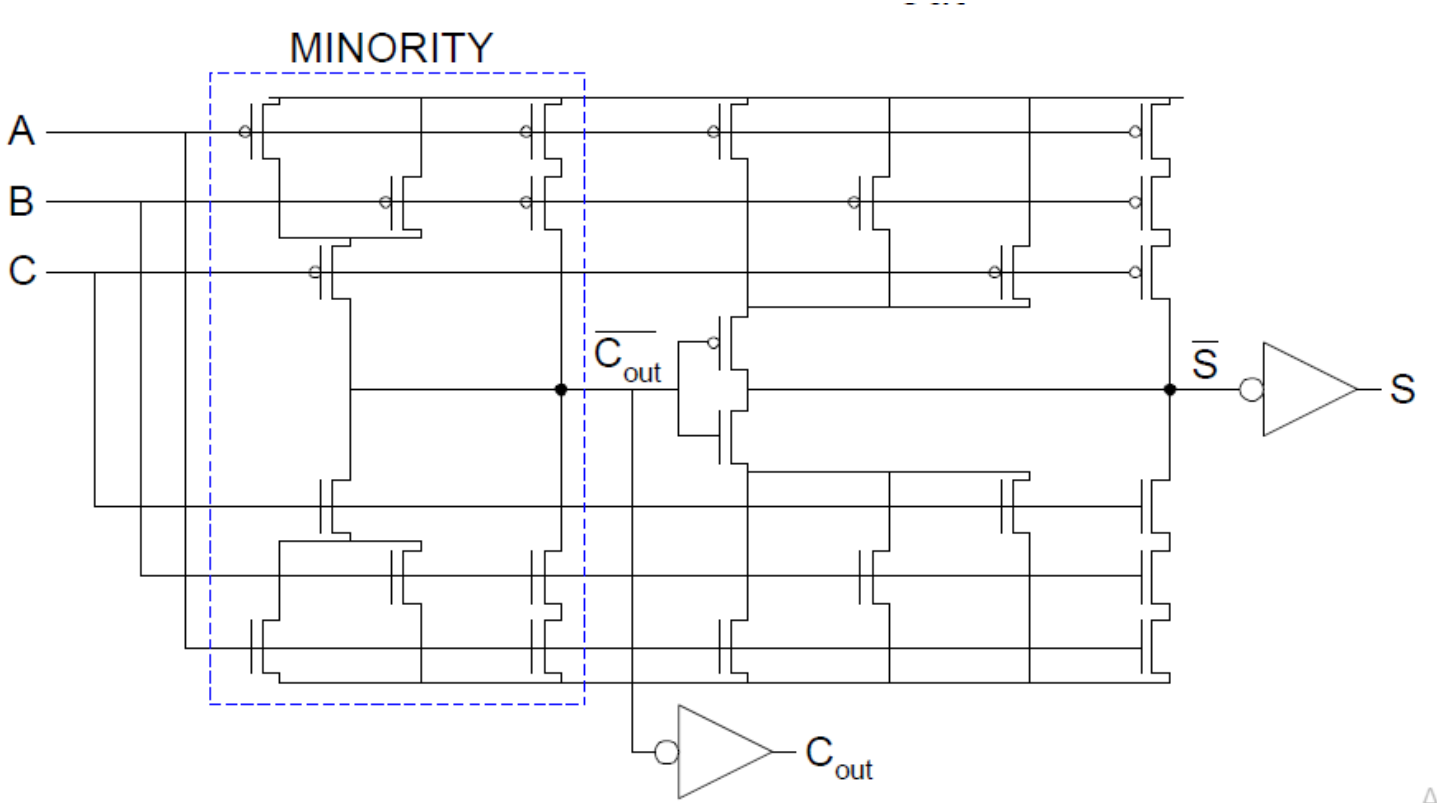

Figure 3: Improved Full Adder Circuit

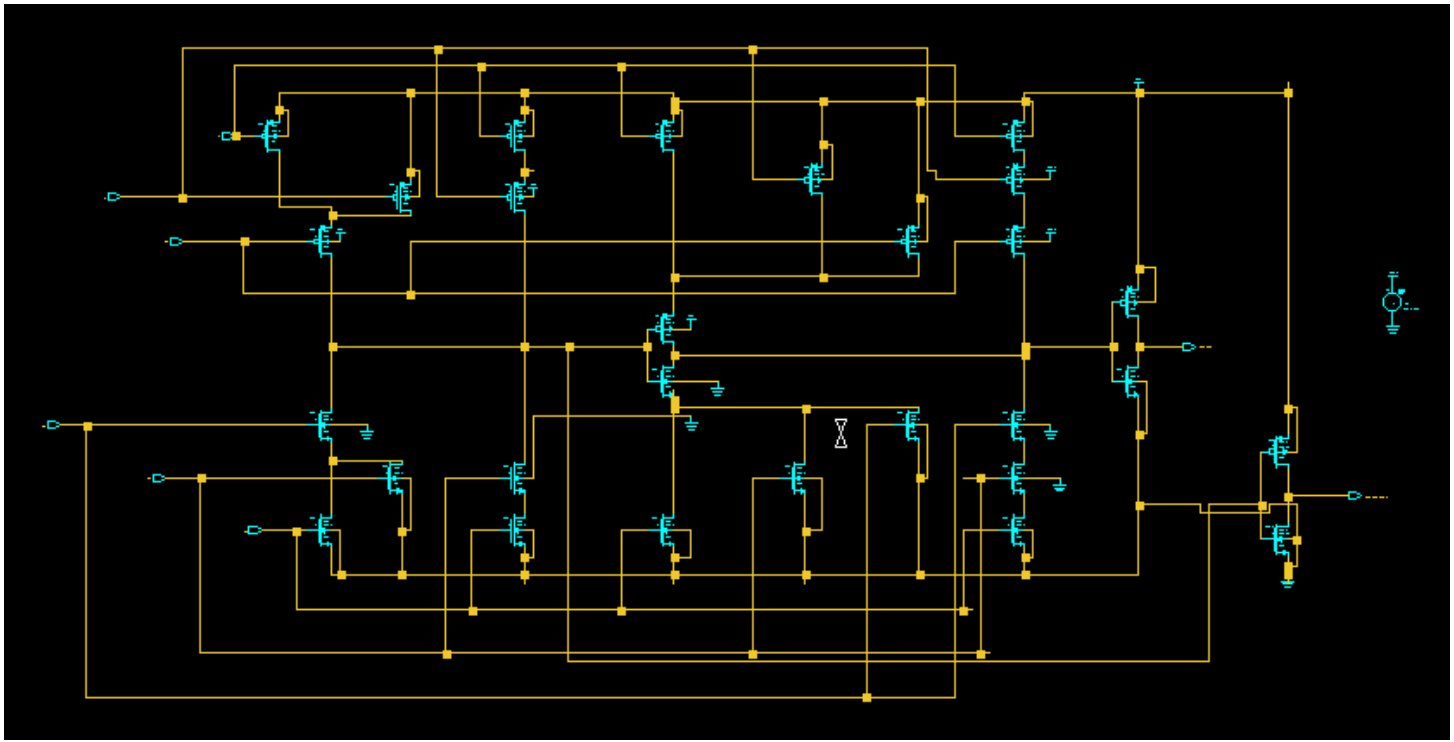

Figure 4: Implemented schematic

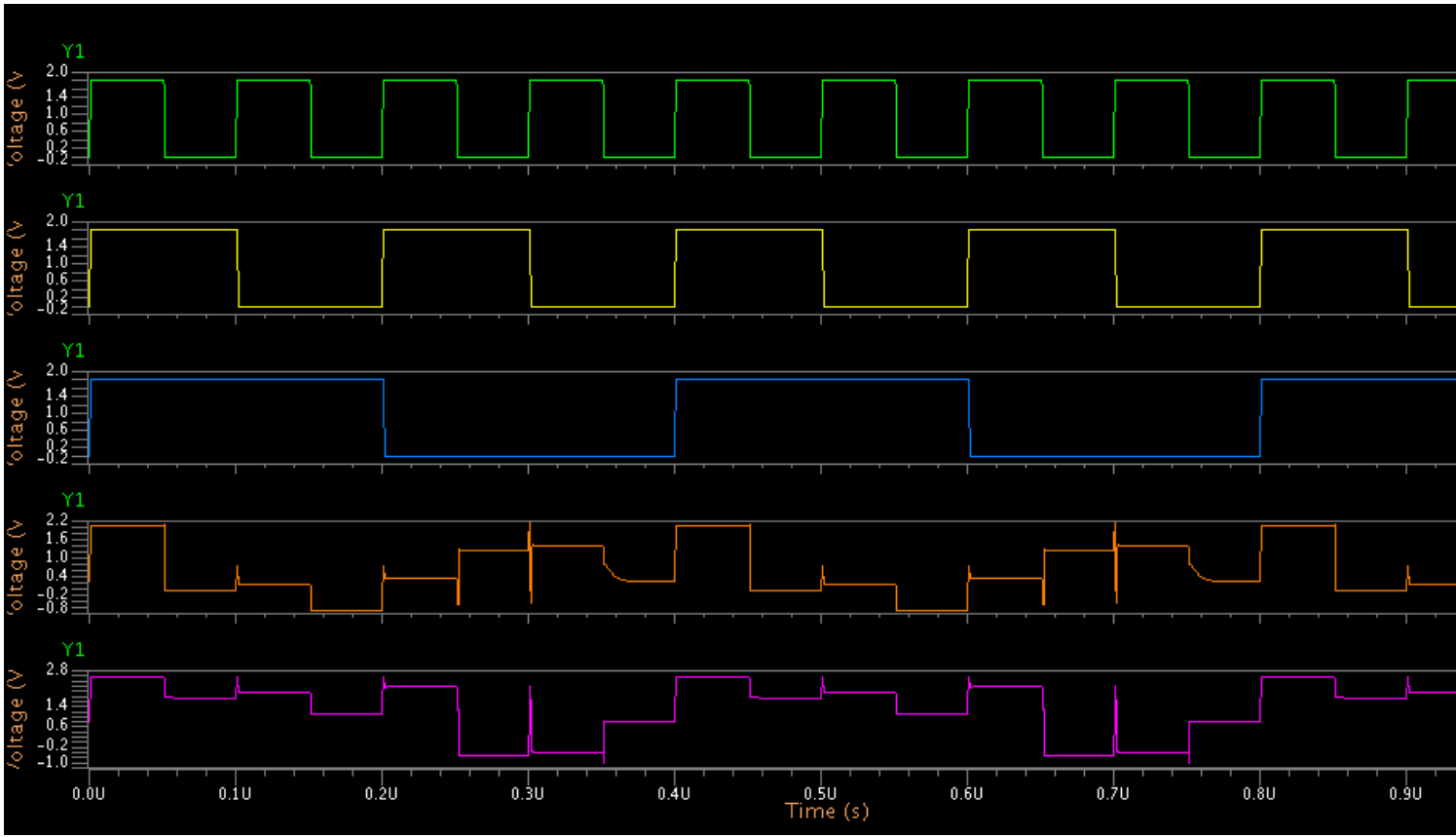

Figure 5: Results

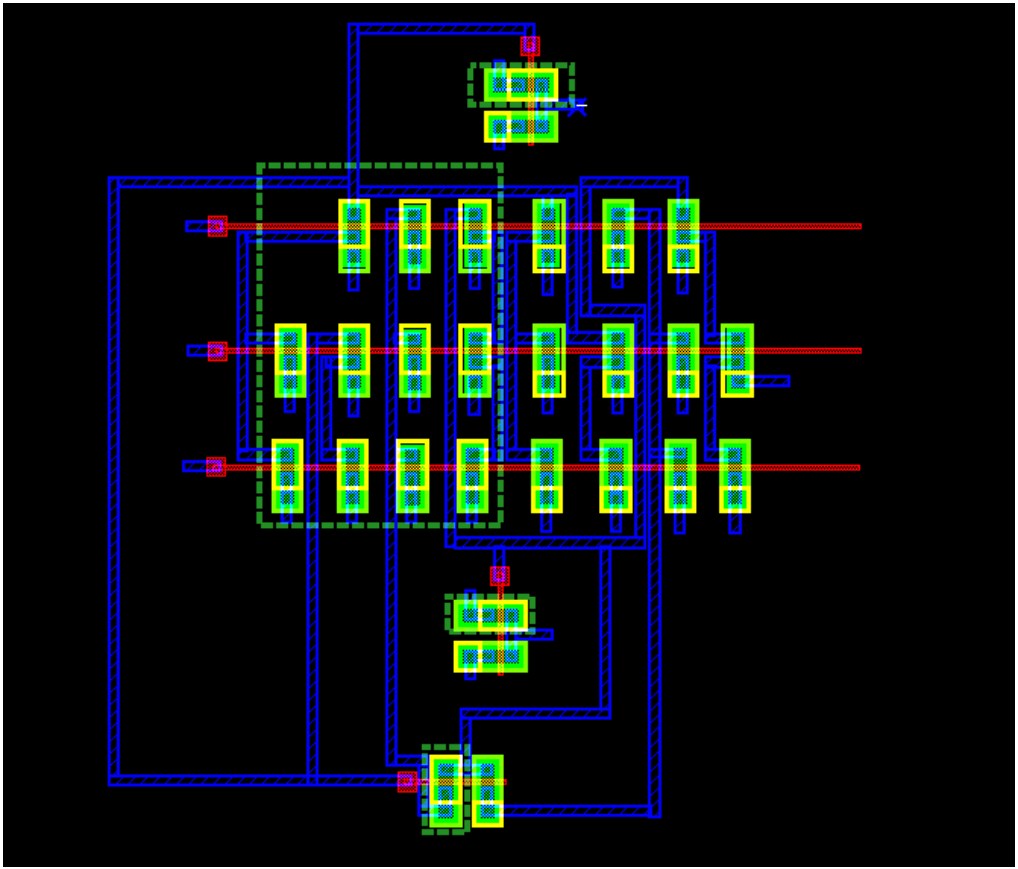

Figure 6: Layout

Conclusions and Future Work

Conclusions

- In comparison to the logic gate implementation (36), the design that we implemented employs lesser transistors (28) and thus, lesser silicon area.

Future Work

- The layout is showing some errors on simulation right now. We are working further to debug them and running the layout.

References

- David Harris. Lec 11 - Adders.[PDF Document] Harvey Mudd College. Spring 2004.
- P. Kirankumar et al. Design of Low Power High Speed Hybrid Full Adder. International Journal of Electronics and Communication Technology, Dec 2015.
- "Full Adder." Wikipedia: The Free Encyclopedia. Wikimedia Foundation, Inc. 22 July 2004. Web. 10 Aug. 2004.