Pranav Kumar

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Education

- **University of Texas at Austin** — Austin, TX
  M.S. in ECE (Architecture, Computer Systems and Embedded Systems track); GPA: 4.00 — *July 2017 – present*
- **Indian Institute of Technology Kanpur** — Kanpur, India
  B.Tech. in Electrical Engineering, Minor in Computer Systems; GPA: 9.0/10.0 (Major: 9.3) — *July 2013 – May 2017*

Skills

- **Languages**: C, C++, Java, Python, Verilog, x86 assembly
- **Software and Tools**: gem5, Xilinx ISE/Vivado, ModelSim, Mentor Graphics, Cadence, ADS, MATLAB, Spice, Tensorflow, git, PAPI, perf, PINTool
- **Development Platforms**: dsPIC, Xilinx Spartan and Virtex FPGAs

Experience

- **Spark Research Lab, UT Austin** — Austin, TX
  Graduate Research Assistant, Advisor: Prof. Mohit Tiwari — *July 2017 – present*
  - **Hardware-based Malware Detection (ISCA'18 submission)**: Designed a behavioral anomaly detector that modeled advanced malware as computational anomalies. Evaluated against memory exploits; side, covert, timing channels; code-reuse attacks, cache timing attacks and ransomware.
  - **RISC-V**: Embedding security primitives into the architecture. Porting attacks like Spectre and ROP to RISC-V.
- **VLSI EDA Lab**: IIT Kanpur
  - **Microprocessor**: Implemented an 8-bit microprocessor and sound monitoring system on FPGA.
- **Computer Systems Projects**:
  - **Architecture**: Dynamic instrumentation using PIN, prediction mechanisms implementation and pipelining MIPS.
  - **Operating Systems**: Implemented system calls, scheduling and page replacement algorithms on NachOS.
  - **Software Security**: SEED labs, finding buffer overflow vulnerabilities, writing stack-smashing and return-2-libc exploits, mounting side-channel attacks on MySQL queries.
  - **Web Security**: Server access control using SELinux, mounting XSS, CSRF and side-channel attacks on server. Implementing privilege separation.
  - **Cryptography**: Addition of RSA and AES instruction support on RISC-V, DPA attack to obtain AES key.
- **Quantum Nanoelectronics Lab, New York University** — New York City, NY
  Summer Intern, Advisor: Prof. Shaloo Rakheja — *Summer 2015 and 2016*
  - **Transistor Compact Modeling**: Implemented an improved virtual-source based transport model for quasi-ballistic transistors. Designed a 10GHz power amplifier using a GaN RF device model.

Projects

- **Improved Adder Circuit**: CMOS-based full adder circuit employing fewer transistors and lower power consumption.
- **Machine Learning**: Projects on PCA, ICA, learning human movement using Gaussian processes, implementing Pac-Man via reinforcement learning and CNN applied on MNIST.
- **3D Display**: Real-time 3D viewing based on face position on your laptop. Top 5 at Ericsson Innovation Awards India.
- **Image Inpainting**: Object removal from images. Awarded best course project.

Presentations

- **7th RISC-V Workshop (Milpitas, CA) Nov'17**: Poster on *Detecting Advanced Malware as Instruction and Microarchitectural Anomalies*
- **C-FAR Research Review (University of Michigan) Aug'17** ***and*** **3rd Annual SARC Technology Forum (Samsung Austin Research Center) Oct'17**: Poster on *Hardware-based Malware Detection on x86 Systems*

Courses

- **Computer Systems**: Computer Architecture, Computer Systems Security, Performance Evaluation and Benchmarking, Operating Systems, Computer Organization, Digital Electronics, Microelectronics
- **Mathematics and Algorithms**: Probability, Machine Learning, Data Structures and Algorithms