Birla Institute of Technology and Science, Pilani, Goa Campus

Hardware Components

SMART LIGHTING SYSTEM

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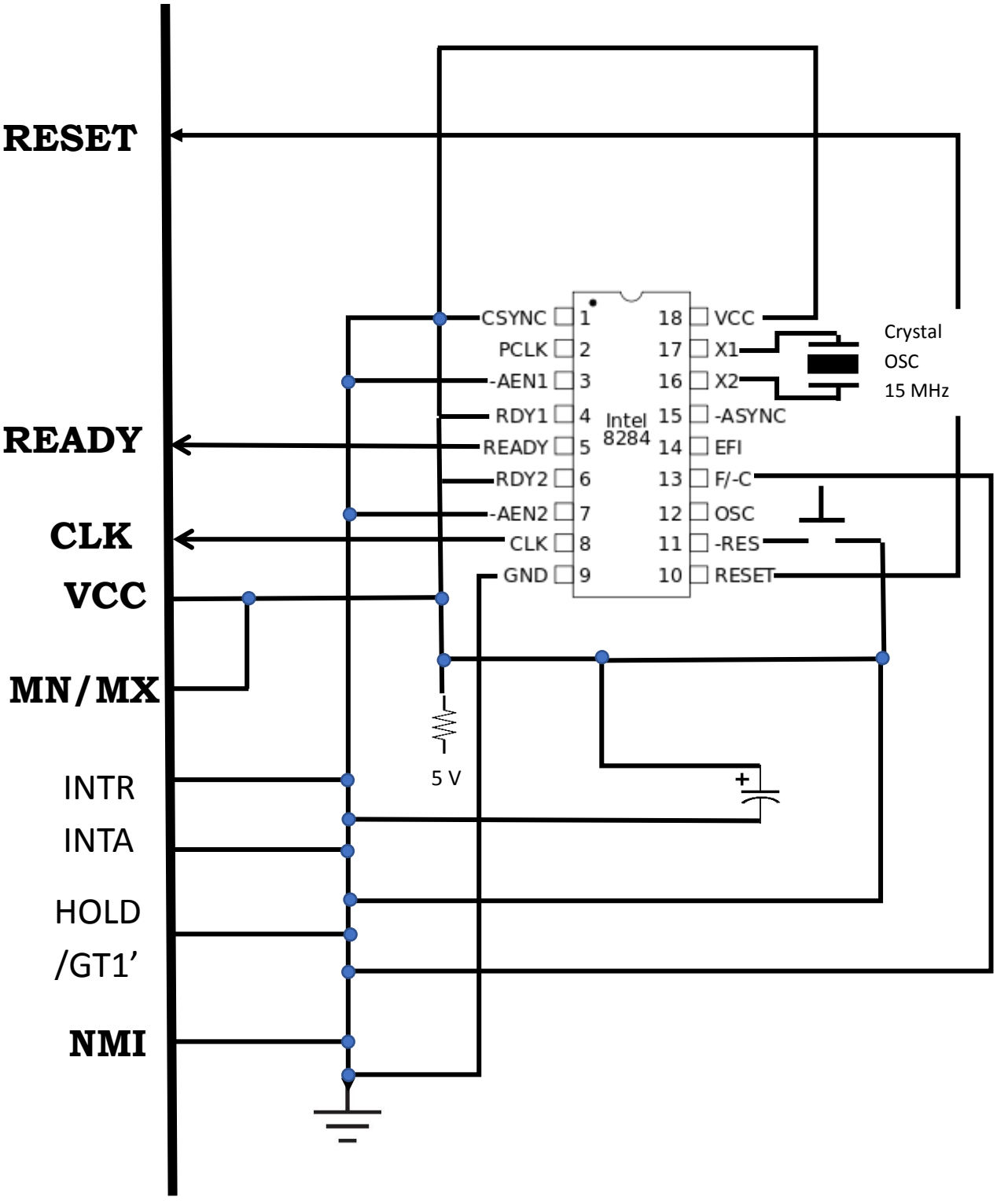
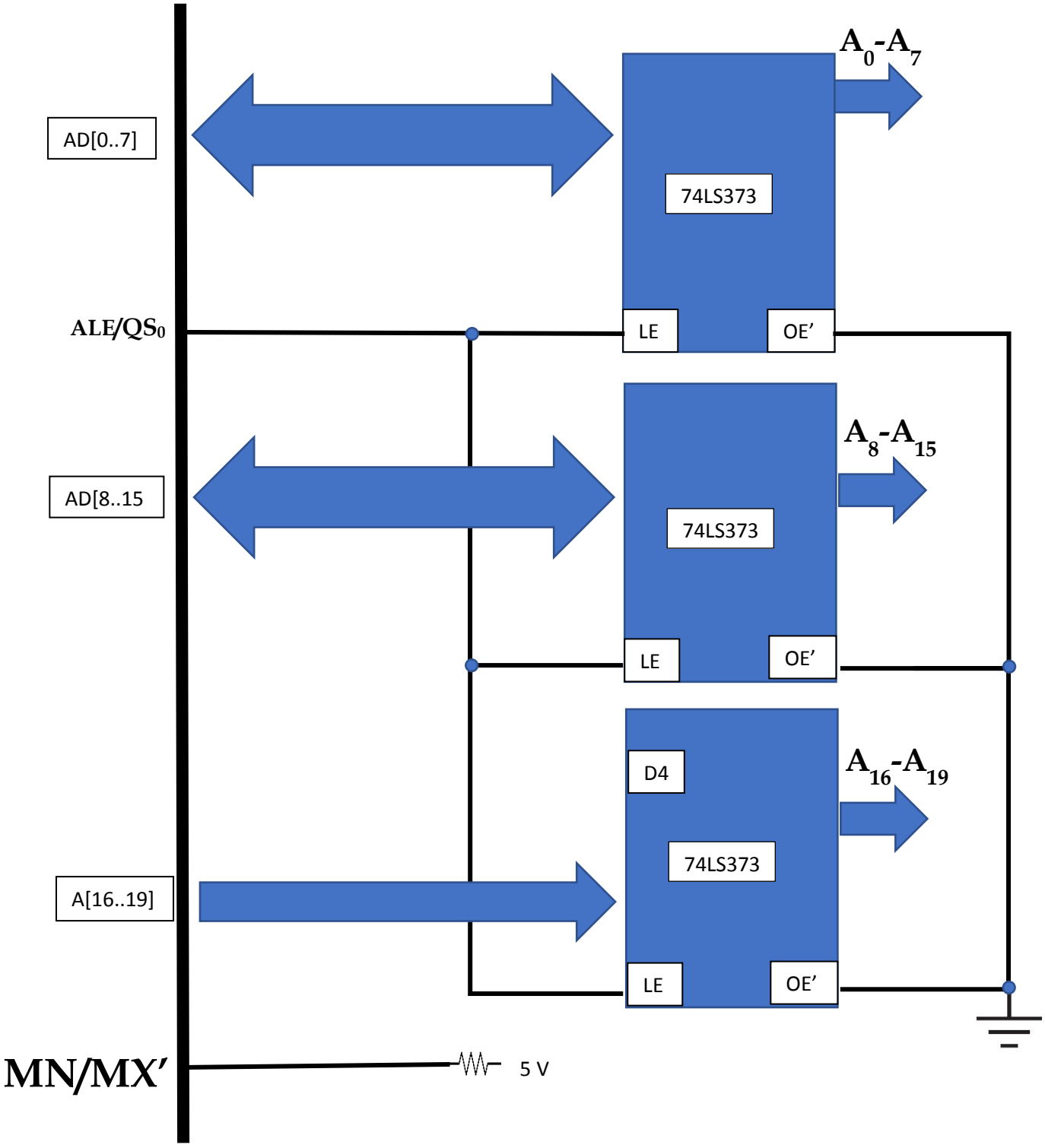
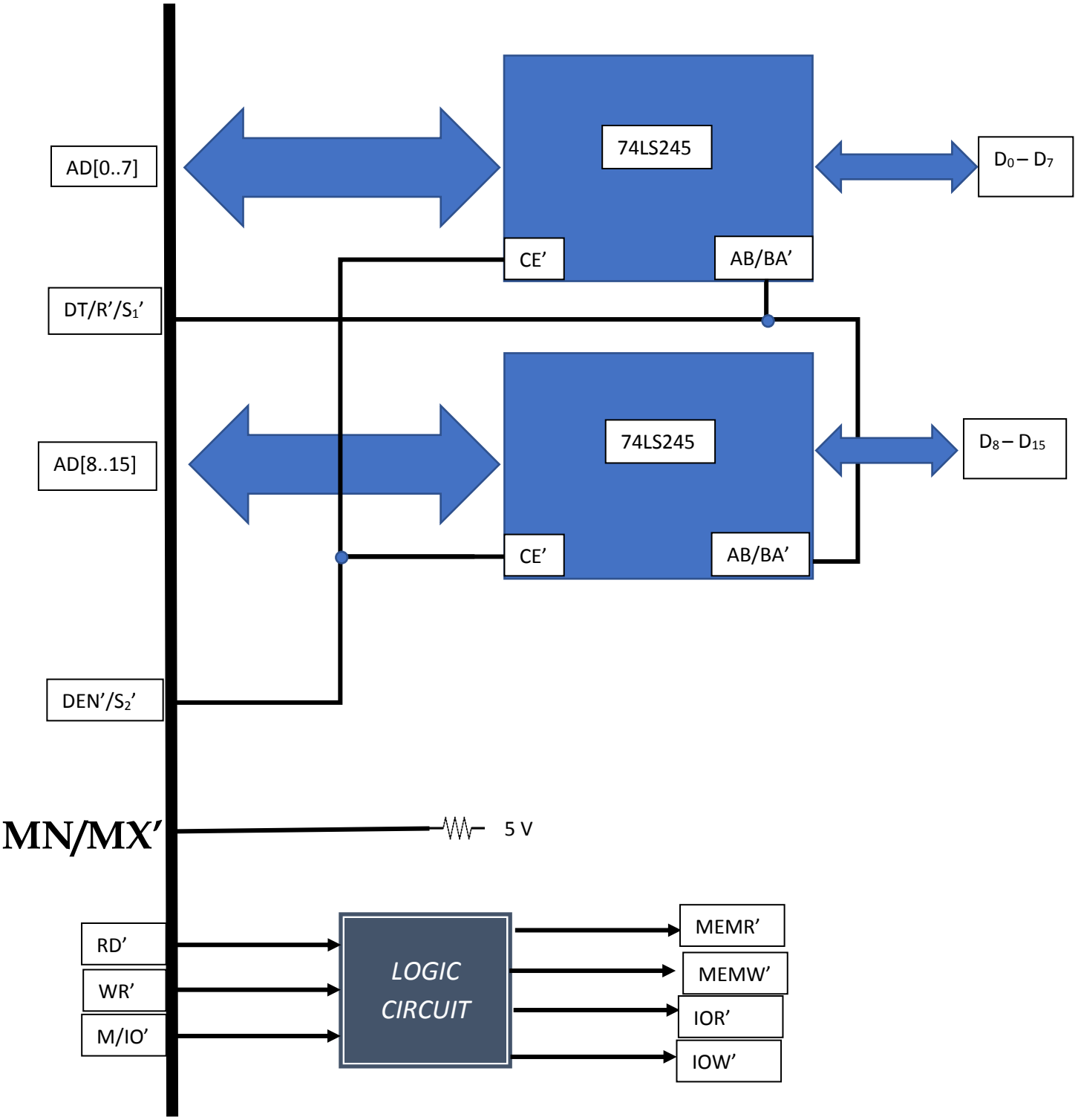
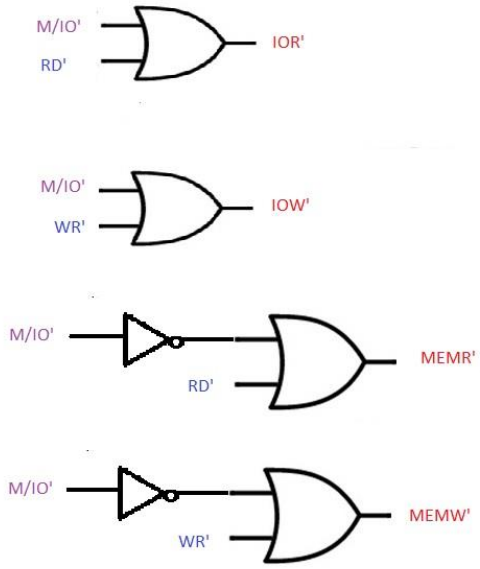
2018A7PS0535G Saubhagya Shukla

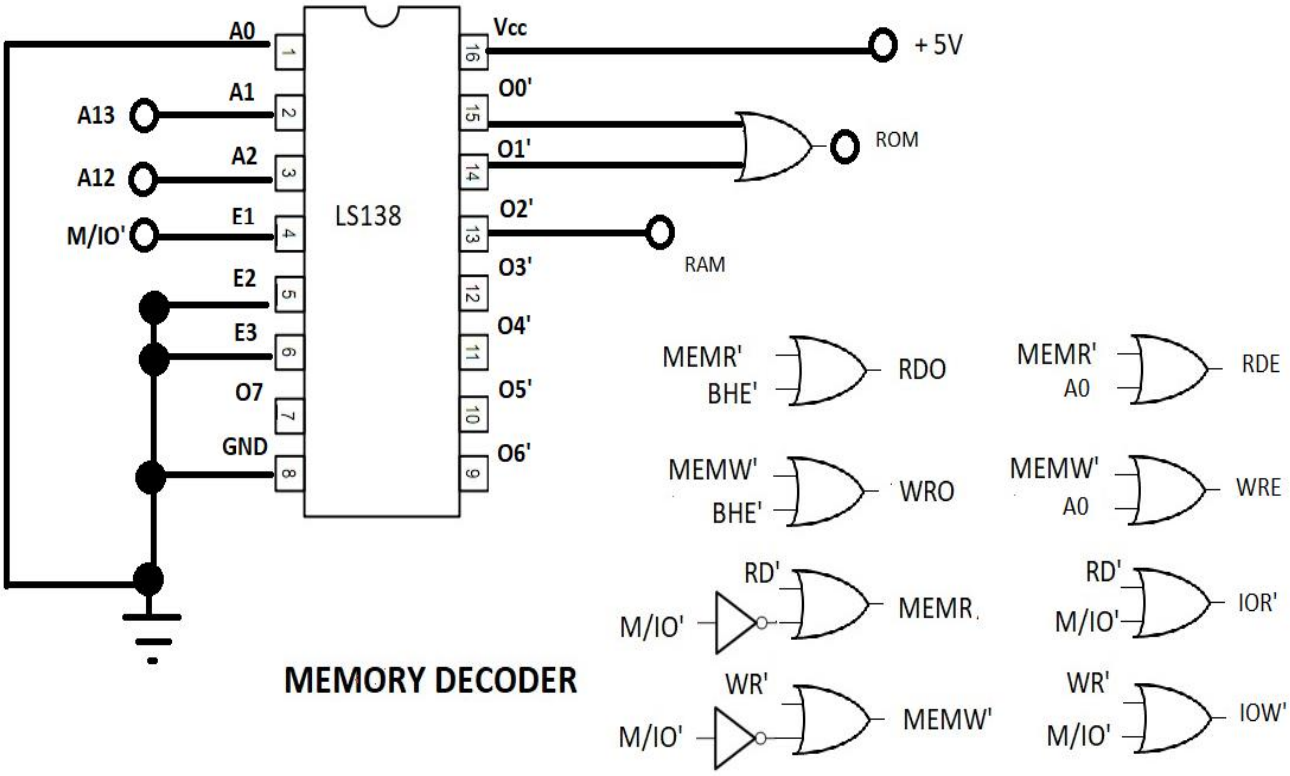

RESET
READY
CLK
VCC
MN/MX
INTR
INTA
HOLD
/GT1'
NMI
CSYNC 1
PCLK 2
-AEN1 3
RDY1 4
READY 5
RDY2 6
-AEN2 7
CLK 8
GND 9
18 VCC
17 X1
16 X2
15 -ASYNC
14 EFI
13 F/-C
12 OSC
11 -RES
10 RESET
Intel 8284
Crystal OSC 15 MHz
5 V


AD[0..7]
ALE/QS0
AD[8..15
A[16..19]
MN/MX'
74LS373
LE
OE'
A0-A7
74LS373
LE
OE'
A8-A15
D4
74LS373
LE
OE'
A16-A19
5 V

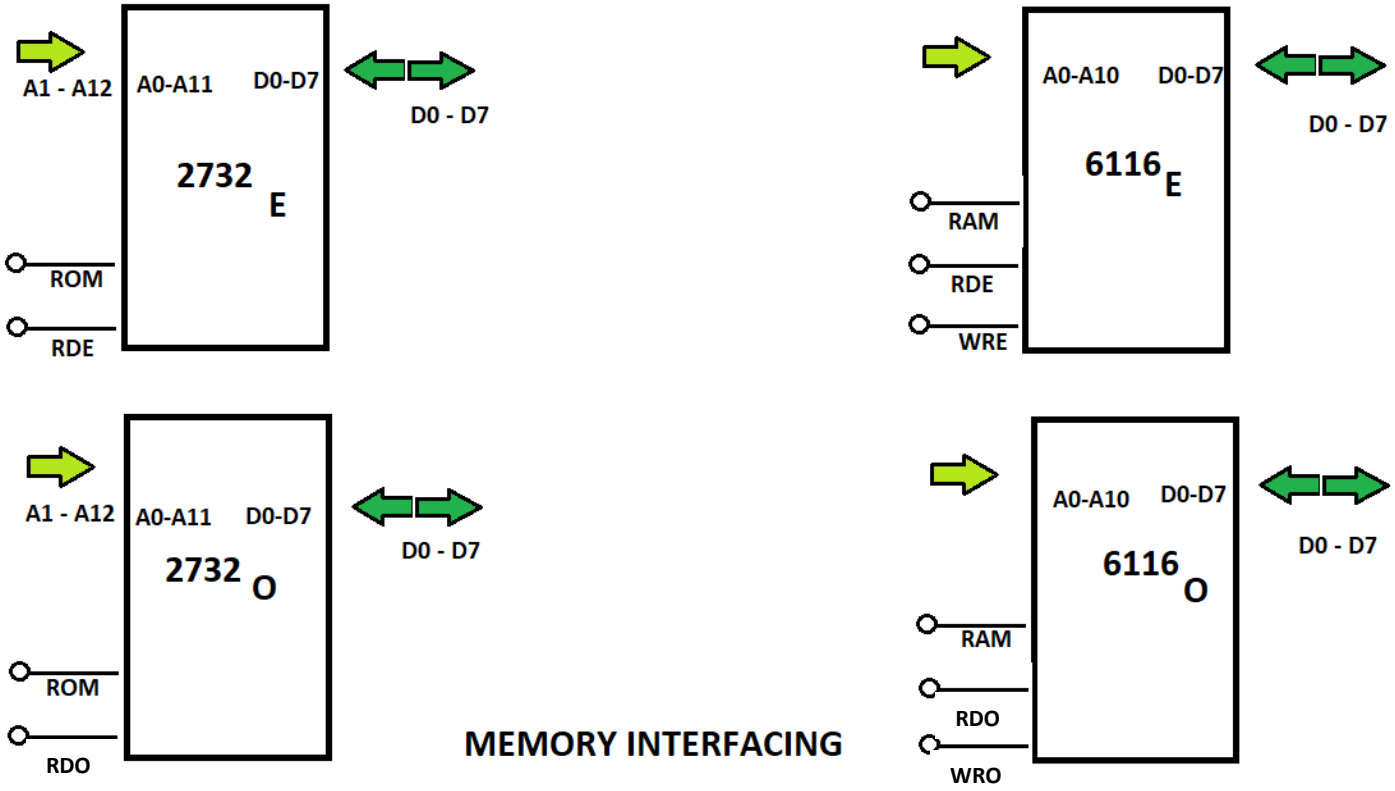

AD[0..7]
74LS245
$D_0 - D_7$
CE'
AB/BA'
DT/R'/S_1'
AD[8..15]
74LS245
$D_8 - D_{15}$
CE'
AB/BA'
DEN'/S_2'
MN/MX'
5 V
RD'
WR'
M/IO'
LOGIC CIRCUIT
MEMR'
MEMW'
IOR'
IOW'



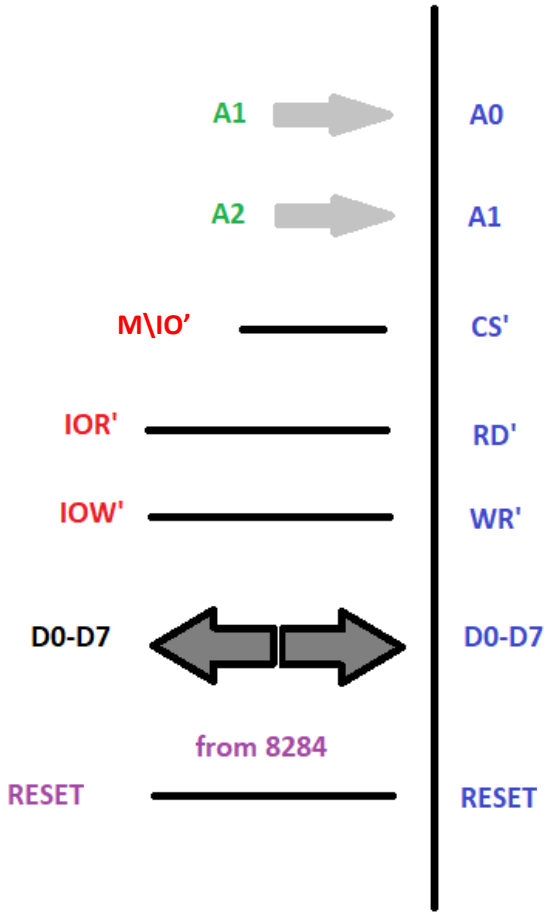
M/IO'	RD'	WR'	BUS CYCLE
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

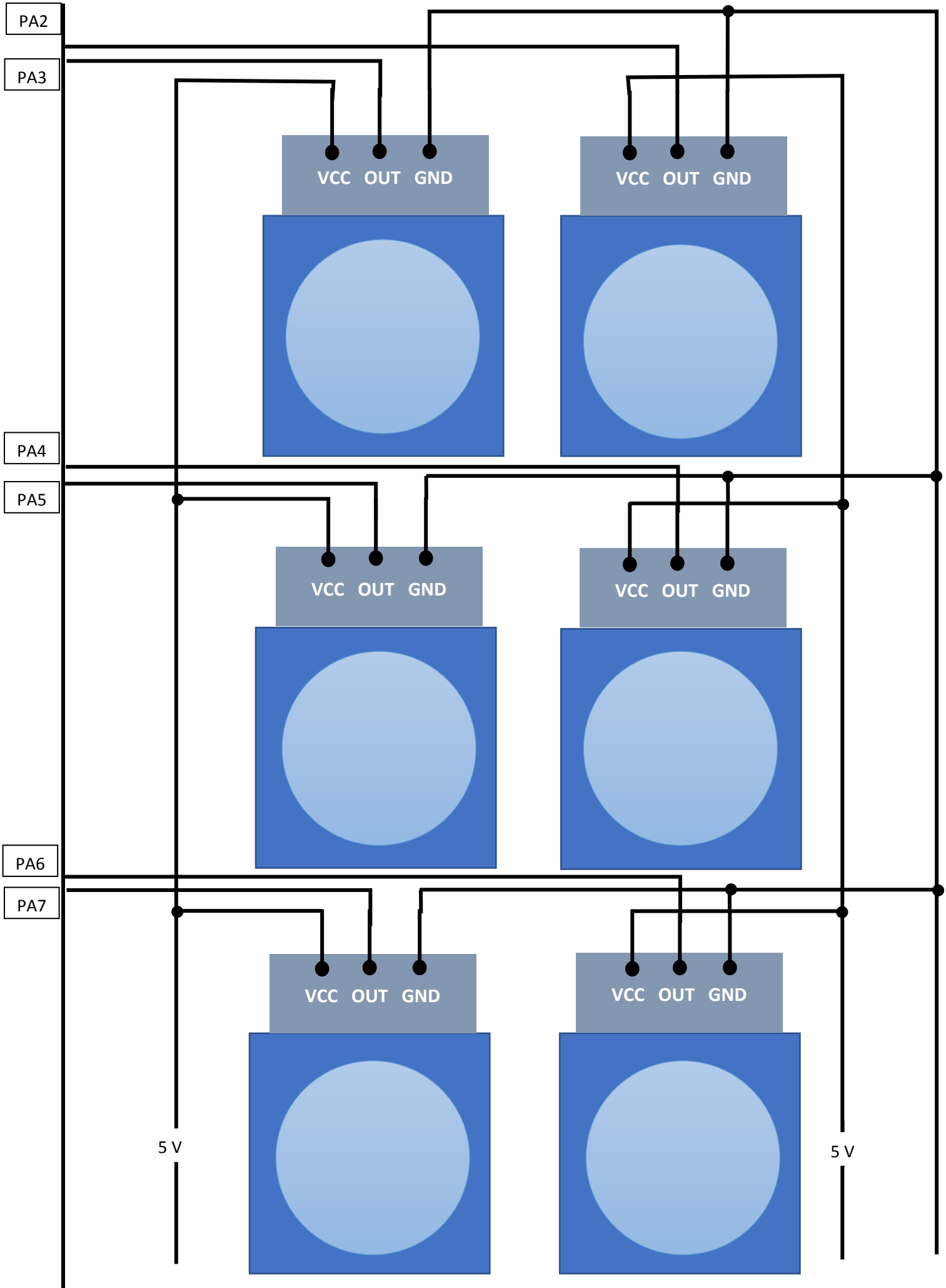


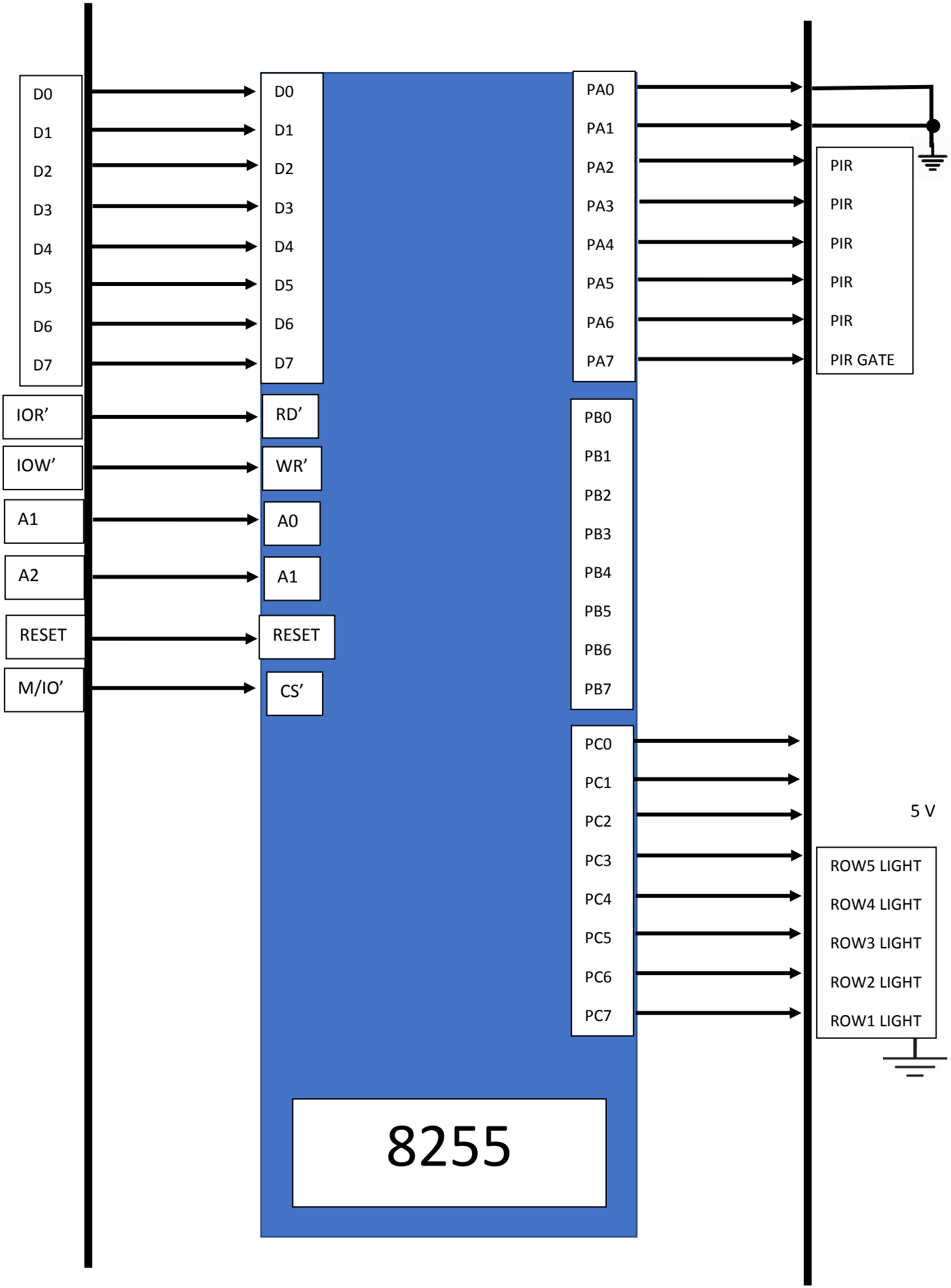
MEMORY DECODER

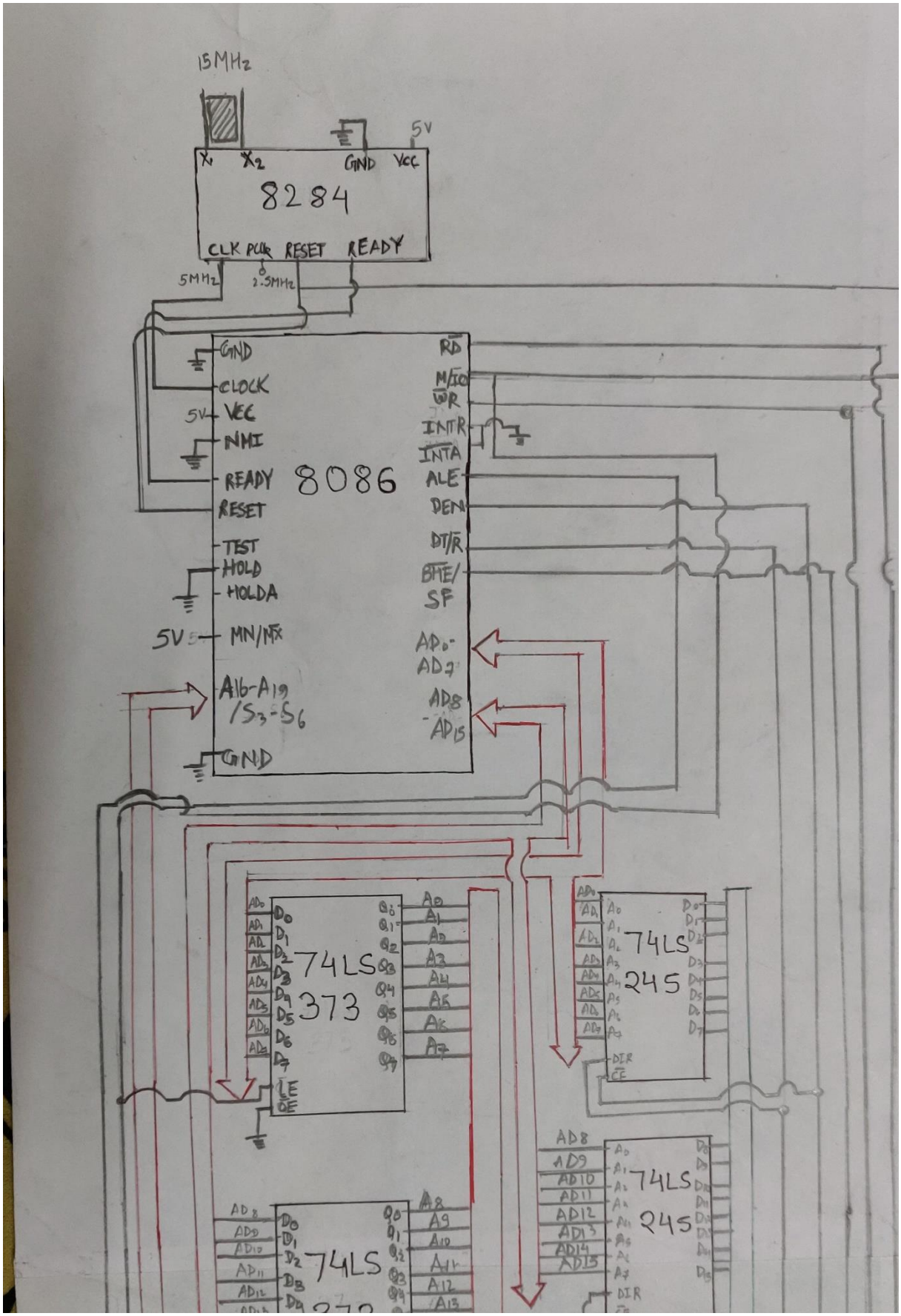


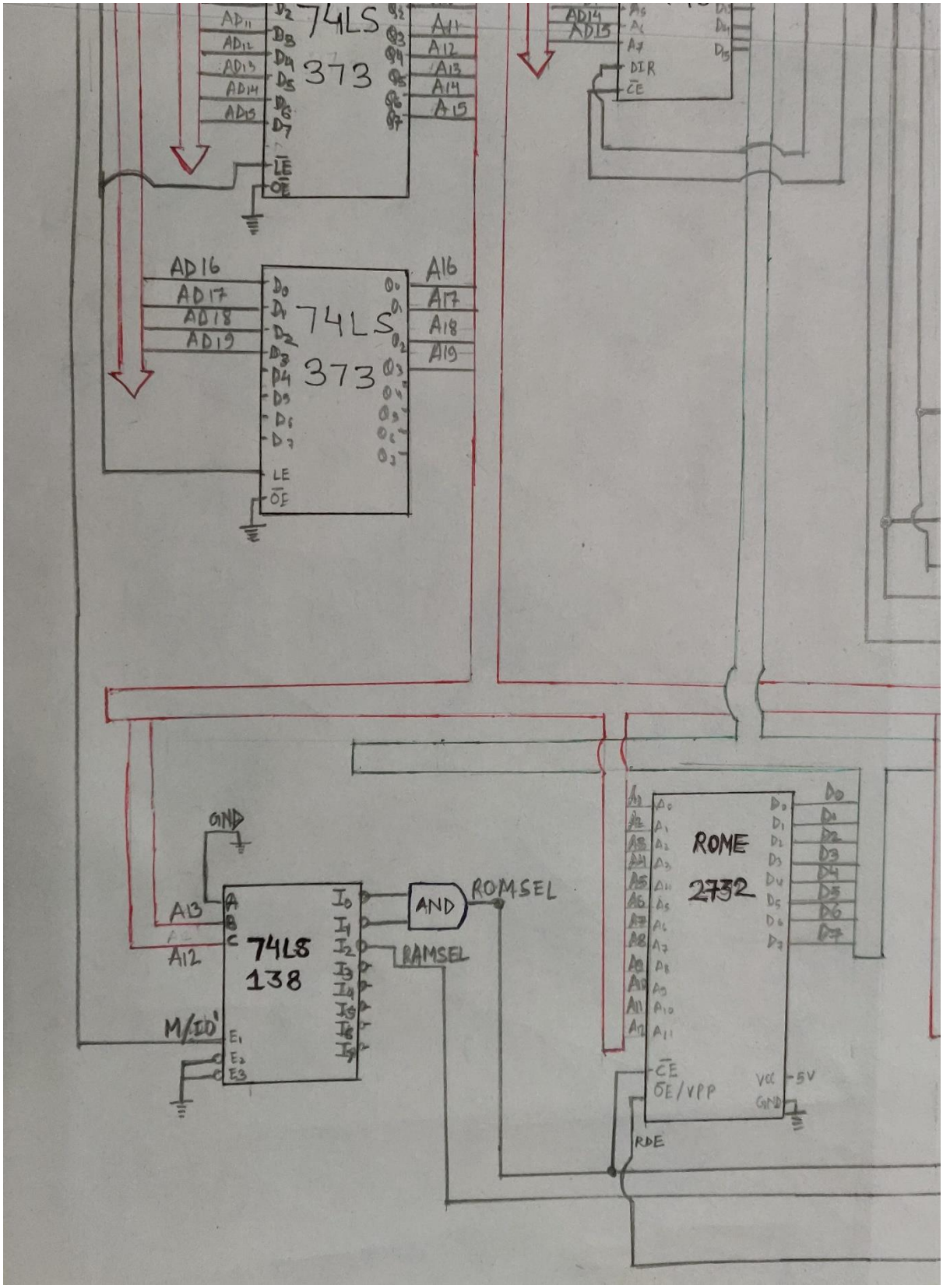
8255 Interface to the processor

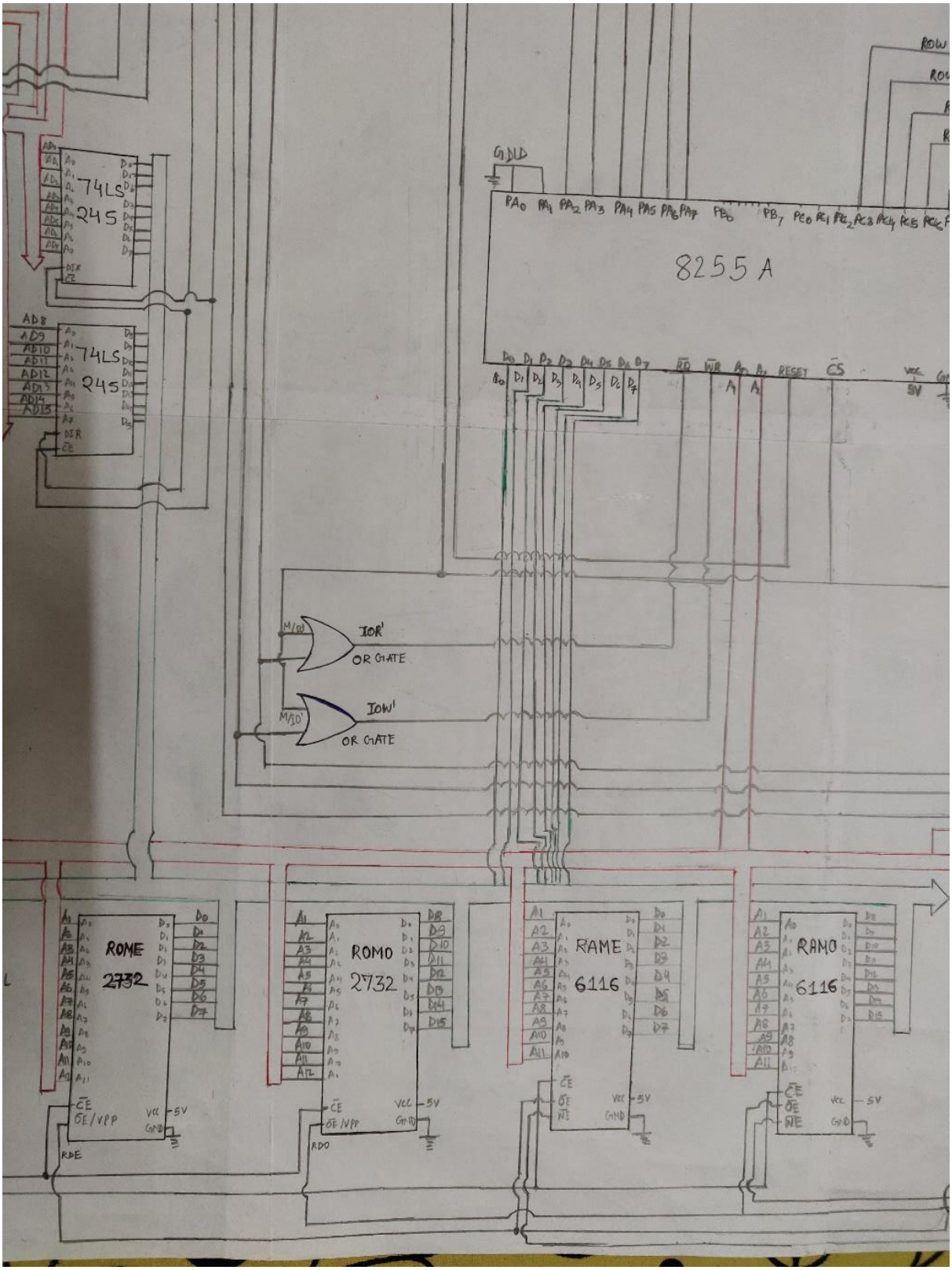


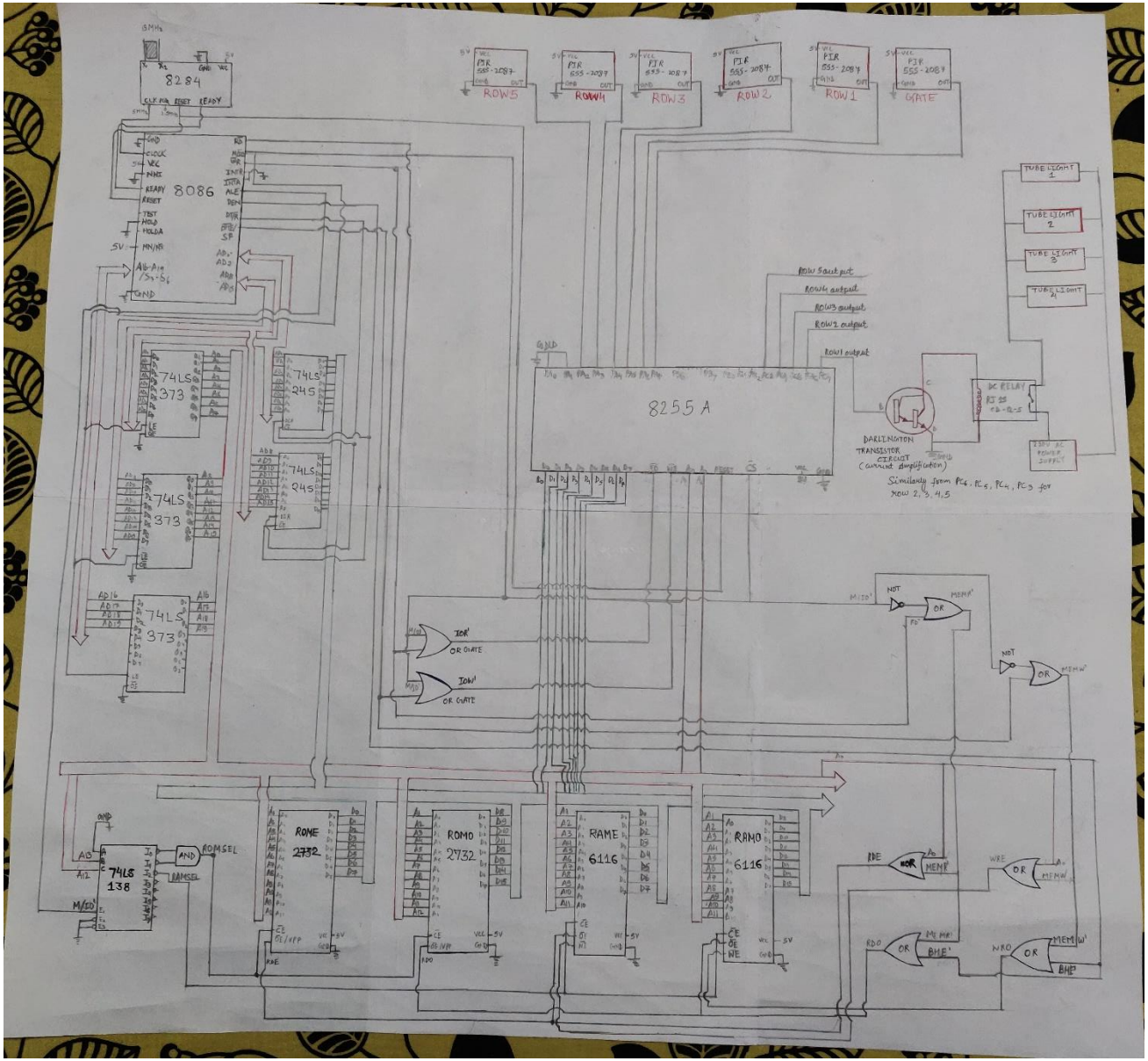

PA2
PA3
PA4
PA5
PA6
PA7
VCC OUT GND
VCC OUT GND
VCC OUT GND
VCC OUT GND
VCC OUT GND
VCC OUT GND
5 V
5 V

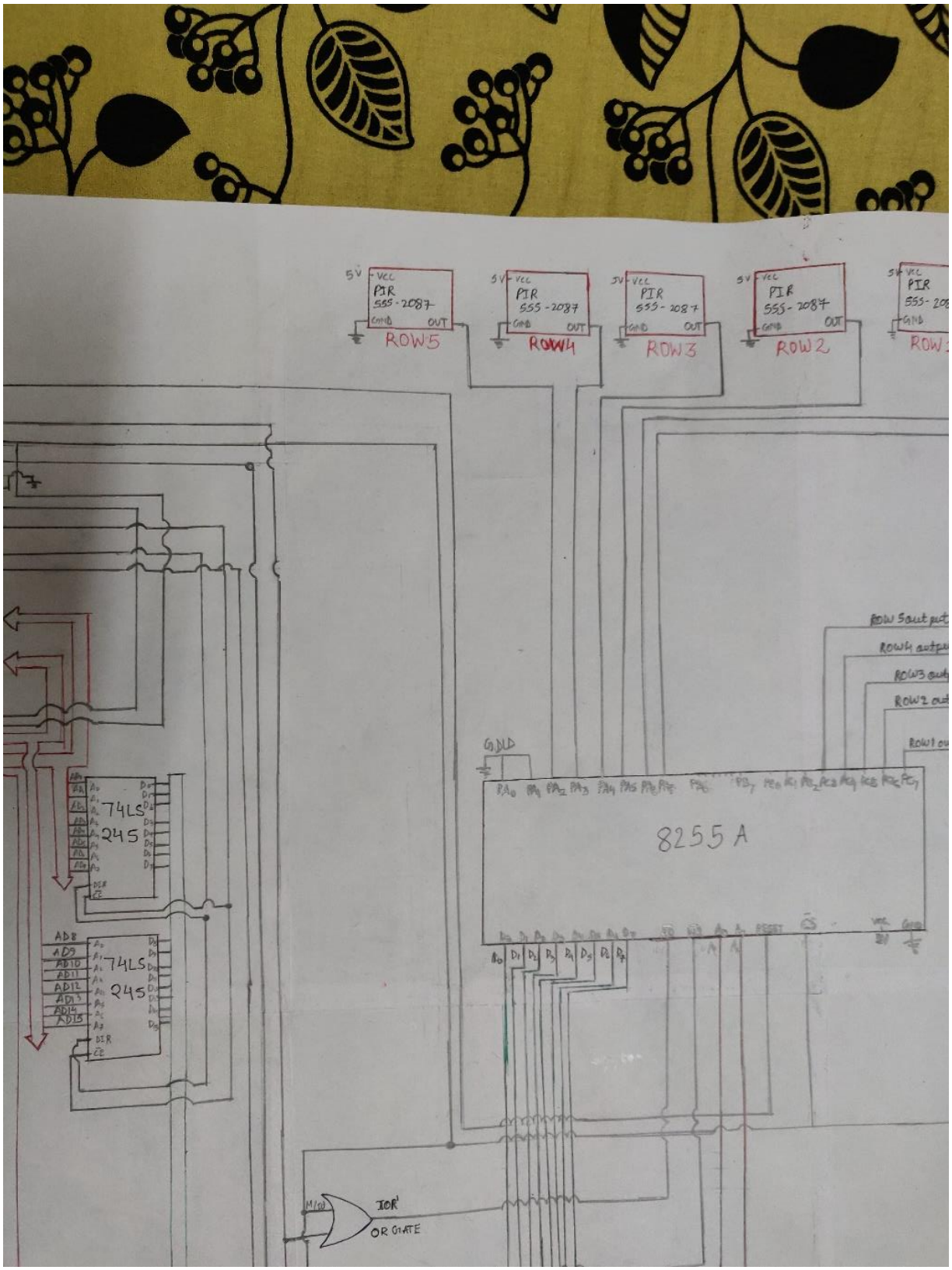

D0
D1
D2
D3
D4
D5
D6
D7
IOR'
IOW'
A1
A2
RESET
M/IO'
D0
D1
D2
D3
D4
D5
D6
D7
RD'
WR'
A0
A1
RESET
CS'
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PIR
PIR
PIR
PIR
PIR
PIR GATE
5 V
ROW5 LIGHT
ROW4 LIGHT
ROW3 LIGHT
ROW2 LIGHT
ROW1 LIGHT
8255

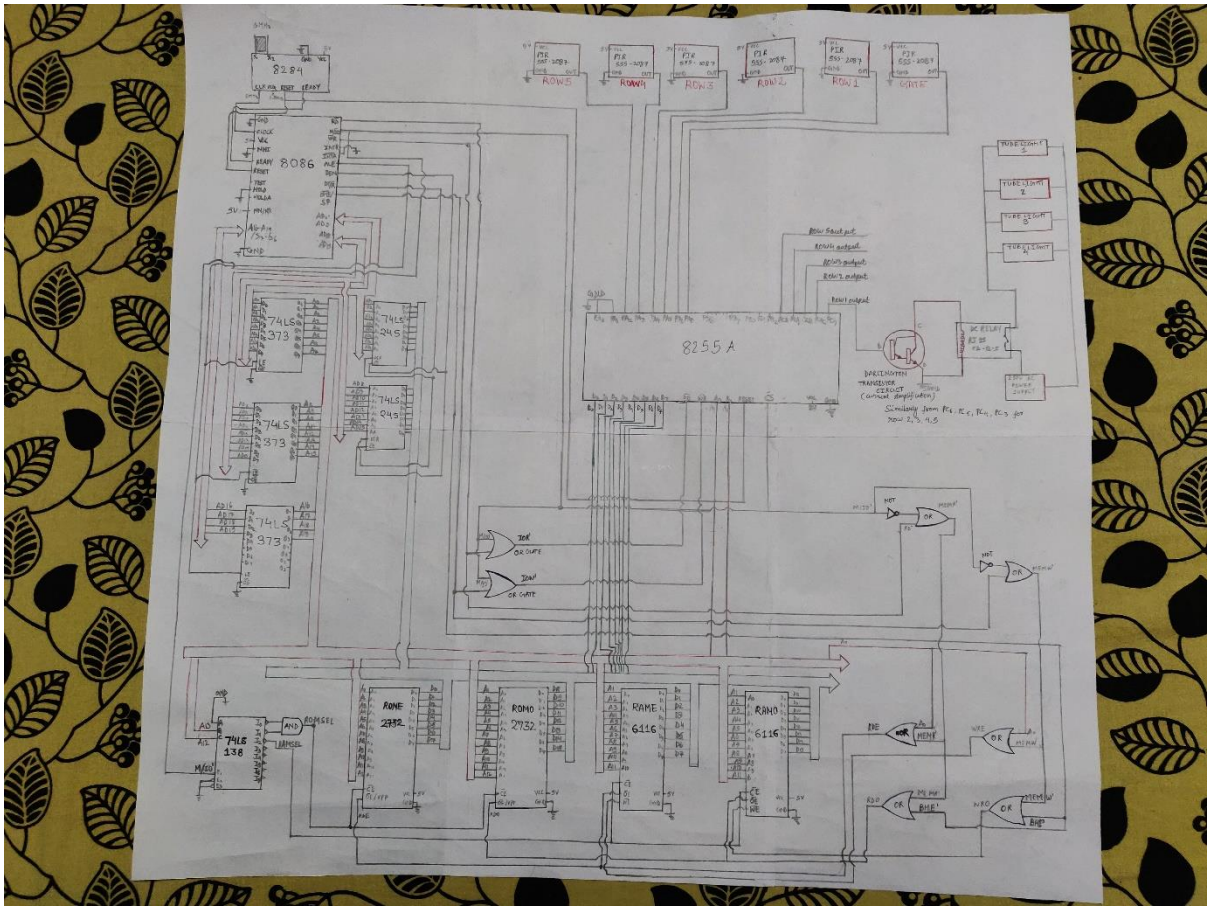

15MHz
5V
X1
X2
GND
Vcc
8284
CLK PCLK RESET READY
5MHz
2.5MHz
GND
CLOCK
5V
Vcc
NMI
READY
RESET
TEST
HOLD
HOLDA
5V
MN/MX
A16-A19
/S3-S6
GND
8086
RD
M/IO
WR
INTR
INTA
ALE
DEN
DT/R
BHE/
SF
AD0-
AD7
AD8
-AD15
74LS
373
74LS
245
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
DIR

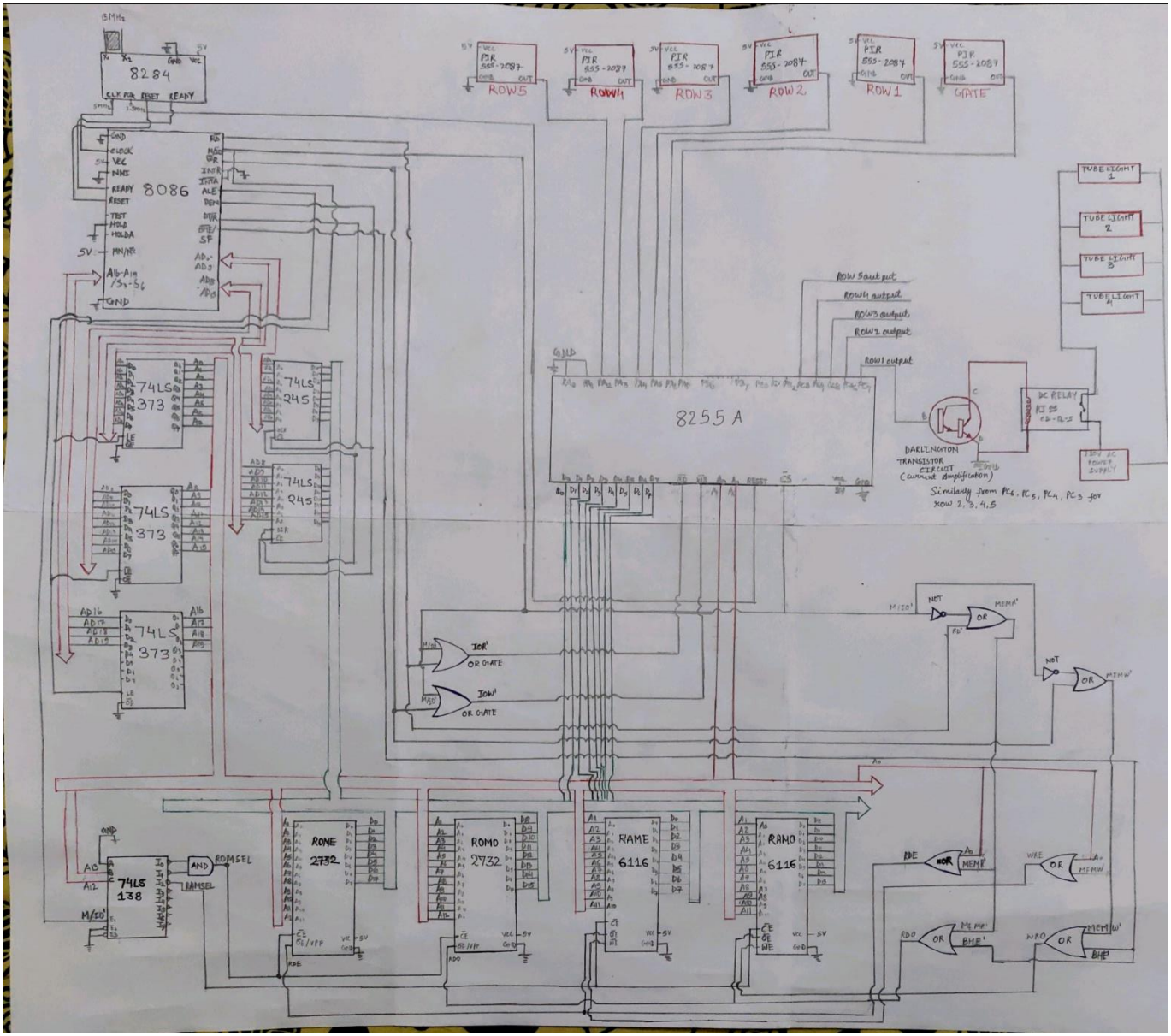

74LS 373
AD11
AD12
AD13
AD14
AD15
A11
A12
A13
A14
A15
LE
OE
AD16
AD17
AD18
AD19
A16
A17
A18
A19
74LS 373
LE
OE
DIR
CE
GND
A13
A12
M/IO'
74LS 138
AND
ROMSEL
RAMSEL
ROME 2732
CE
OE/VPP
Vcc
5V
GND
RDE

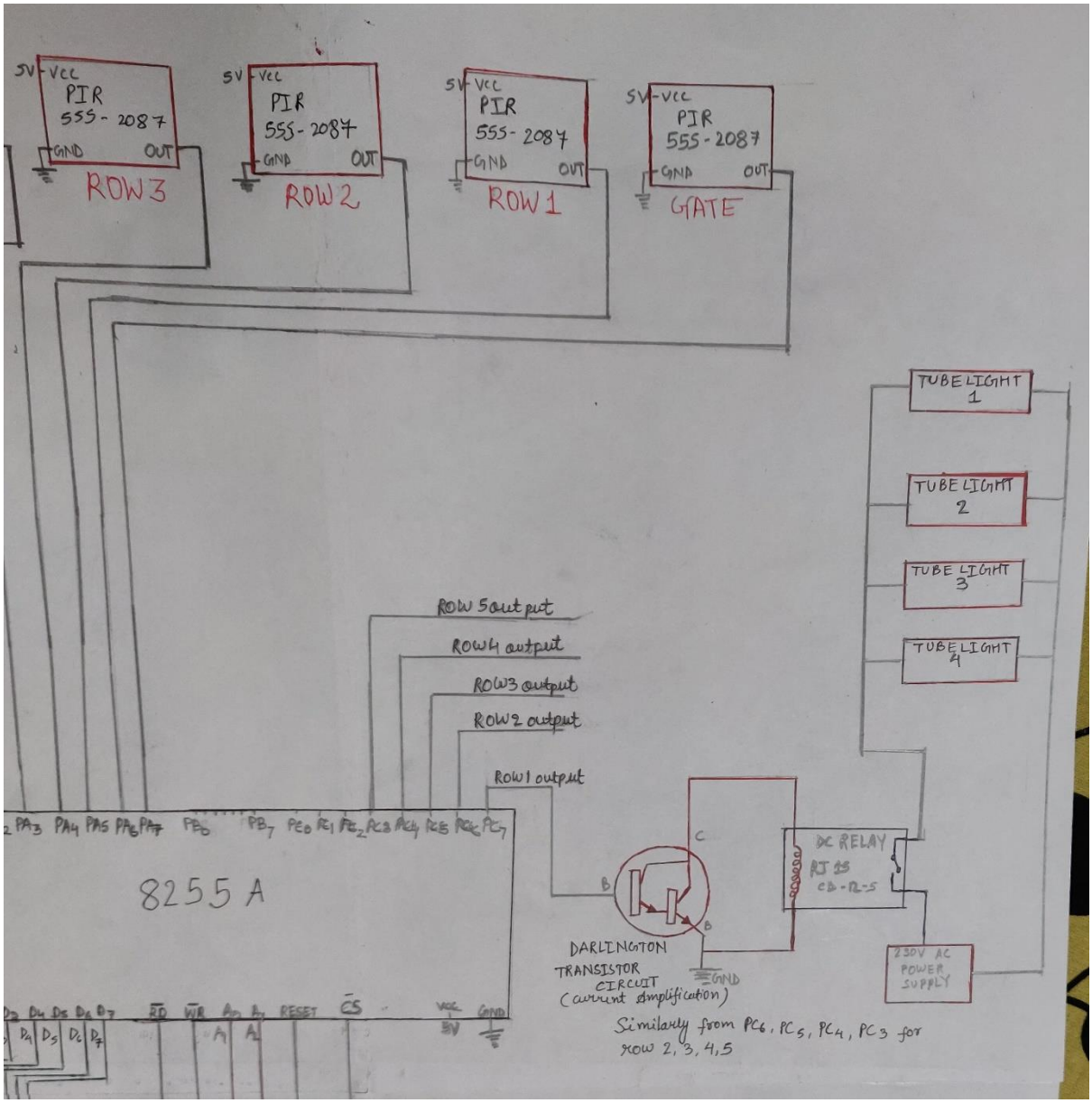

74LS 245
74LS 245
8255 A
M/IO'
IOR'
OR GATE
IOW'
OR GATE
ROME 2732
ROMO 2732
RAME 6116
RAMO 6116
RDE
RDO
5V


8284
8086
8255 A
74LS 373
74LS 245
74LS 138
ROM0 2732
ROM1 2732
RAM0 6116
RAM1 6116
ROW5
ROW4
ROW3
ROW2
ROW1
GATE
ROW5 output
ROW4 output
ROW3 output
ROW2 output
ROW1 output
TUBE LIGHT 1
TUBE LIGHT 2
TUBE LIGHT 3
TUBE LIGHT 4
DARLINGTON TRANSISTOR CIRCUIT (current amplification)
AC RELAY
IOR' OR GATE
IOW' OR GATE
NOT
OR
AND
ROMSEL
RAMSEL
MEMR'
MEMW'
RDO
WRO
BHE'


5V
VCC
PIR
555-2087
GND
OUT
ROW5
ROW4
ROW3
ROW2
74LS
245
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
DIR
CE
8255 A
M/IO
IOR'
OR GATE


8284
8086
74LS 373
74LS 245
74LS 373
74LS 245
74LS 373
8255 A
ROW5
ROW4
ROW3
ROW2
ROW1
GATE
ROME 2732
ROMO 2732
RAME 6116
RAMO 6116
74LS 138
AND
ROMSEL
RAMSEL
OR
NOT
NOR
MEMR'
MEMW'
BHE'
RDO
WRO
DARLINGTON TRANSISTOR CIRCUIT (current amplification)
Similarly from PC6, PC5, PC4, PC3 for row 2, 3, 4, 5


8284
8086
8255 A
74LS 373
74LS 245
74LS 138
ROM0 2732
ROM1 2732
RAM0 6116
RAM1 6116
PIR 555-2087
ROW5
ROW4
ROW3
ROW2
ROW1
GATE
TUBE LIGHT 1
TUBE LIGHT 2
TUBE LIGHT 3
TUBE LIGHT 4
DC RELAY
DARLINGTON TRANSISTOR CIRCUIT (current amplification)
Similarly from PC6, PC5, PC4, PC3 for row 2, 3, 4, 5
IOR' OR GATE
IOW' OR GATE
NOT
OR
AND
ROMSEL
RAMSEL



There is also a walkthrough video on YouTube made by us that explains the Code, it's logic and it's working

It can be found at:

https://youtu.be/lshg31mhzko