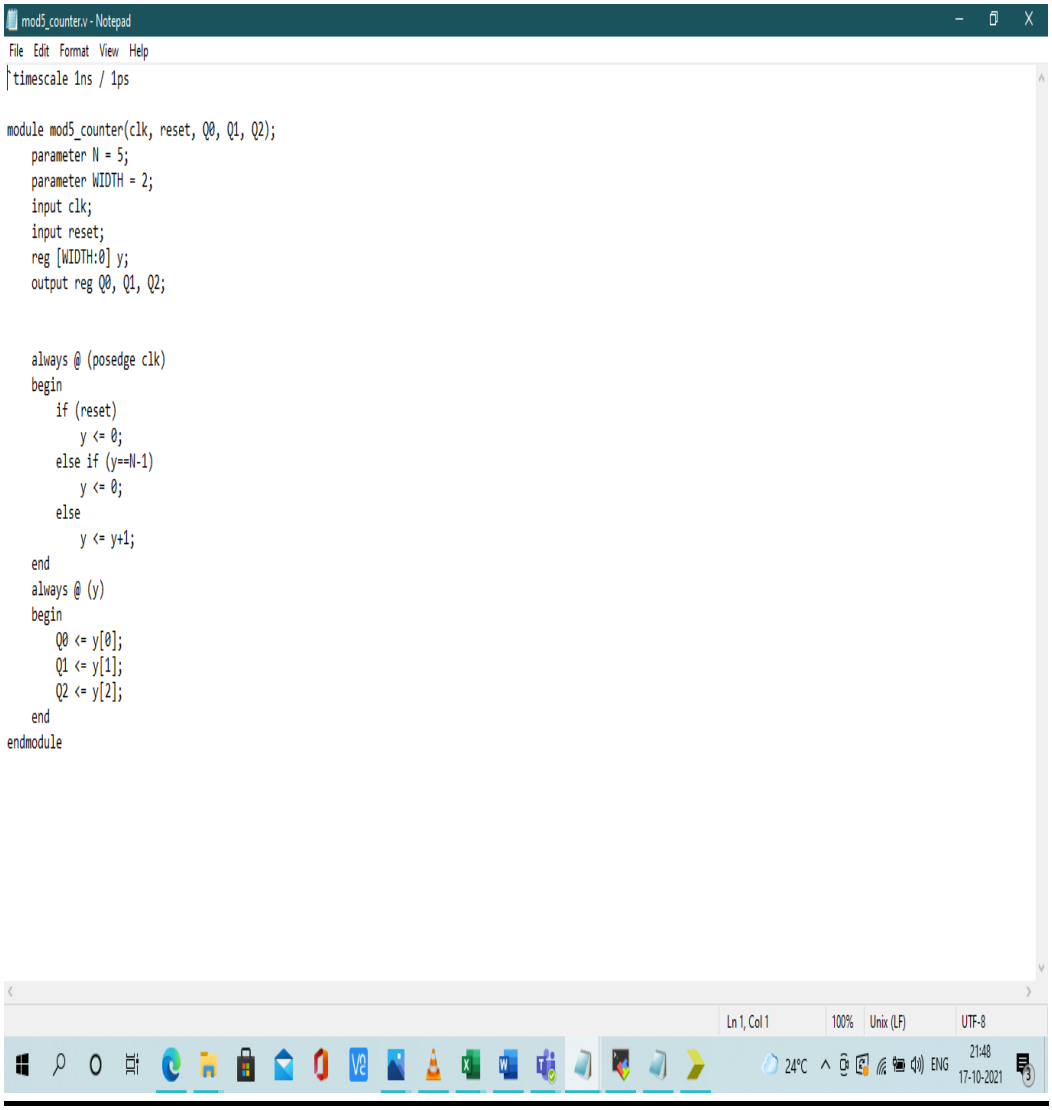
LAB REPORT

Pranav Kumar Rai

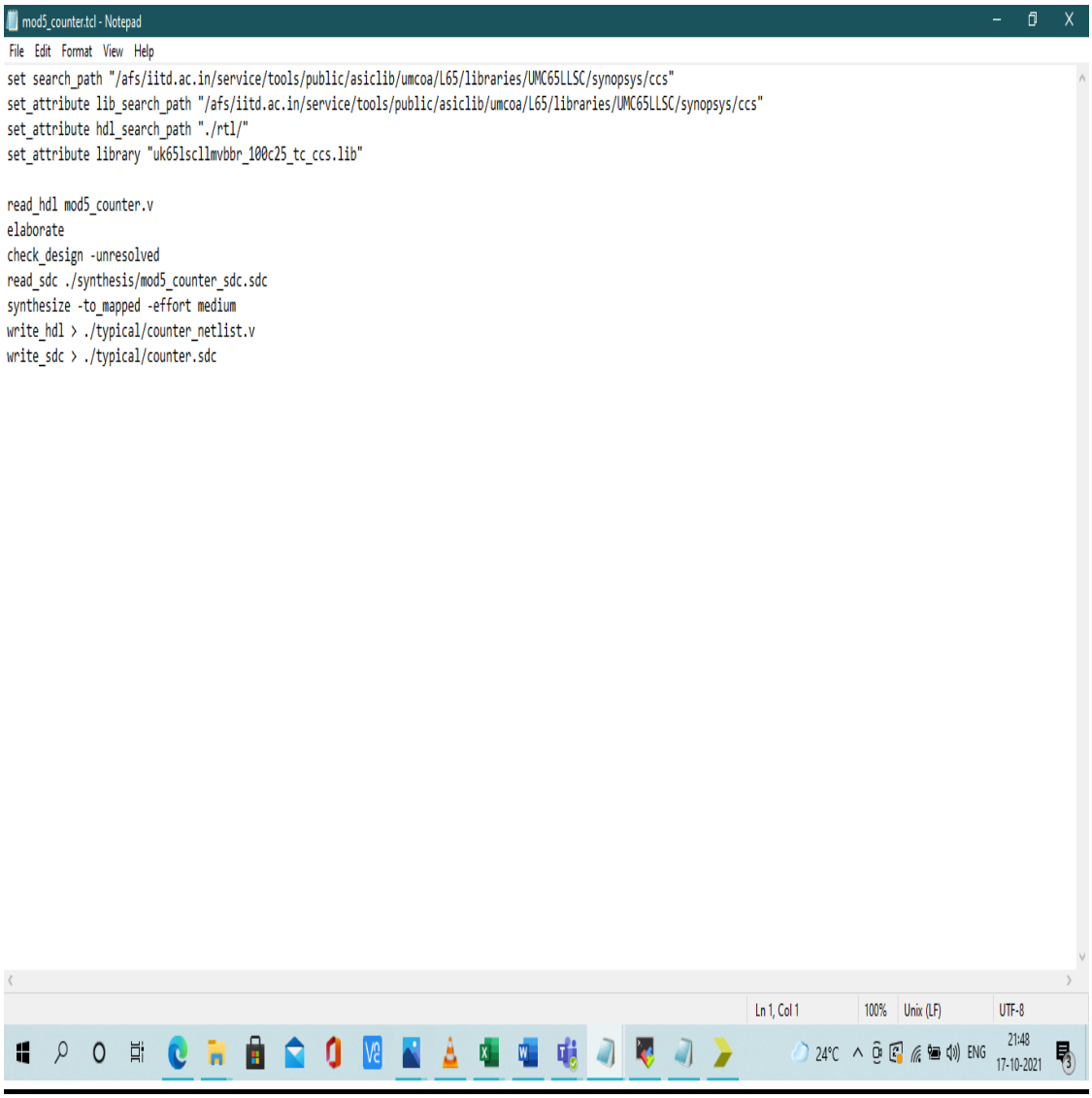
https://github.com/pranavrai1995iit/2021jvl2384/tree/main/Lab%20Report2

Physical Design of MOD_S_UP_COUNTER

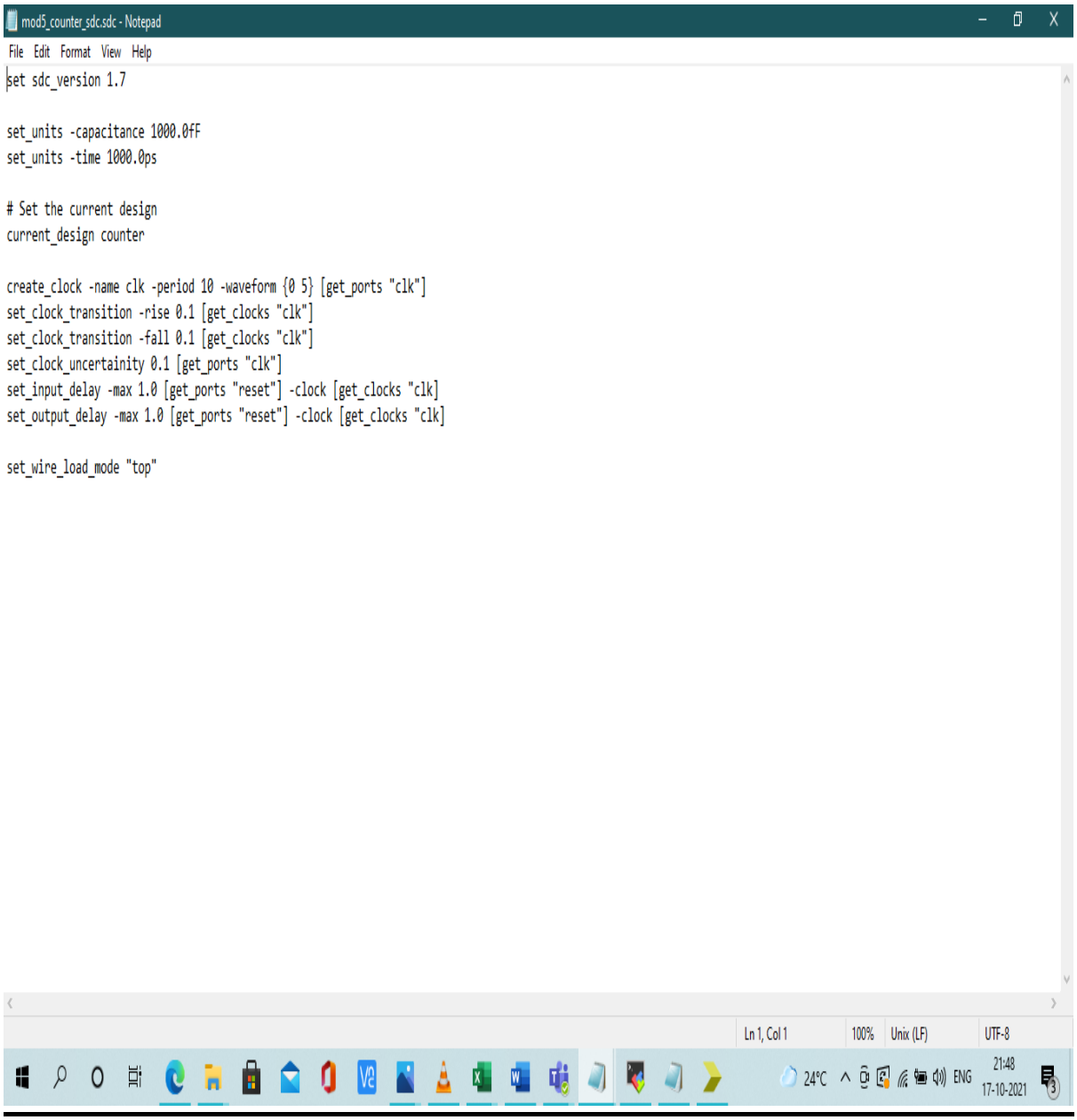
Verilog Code-



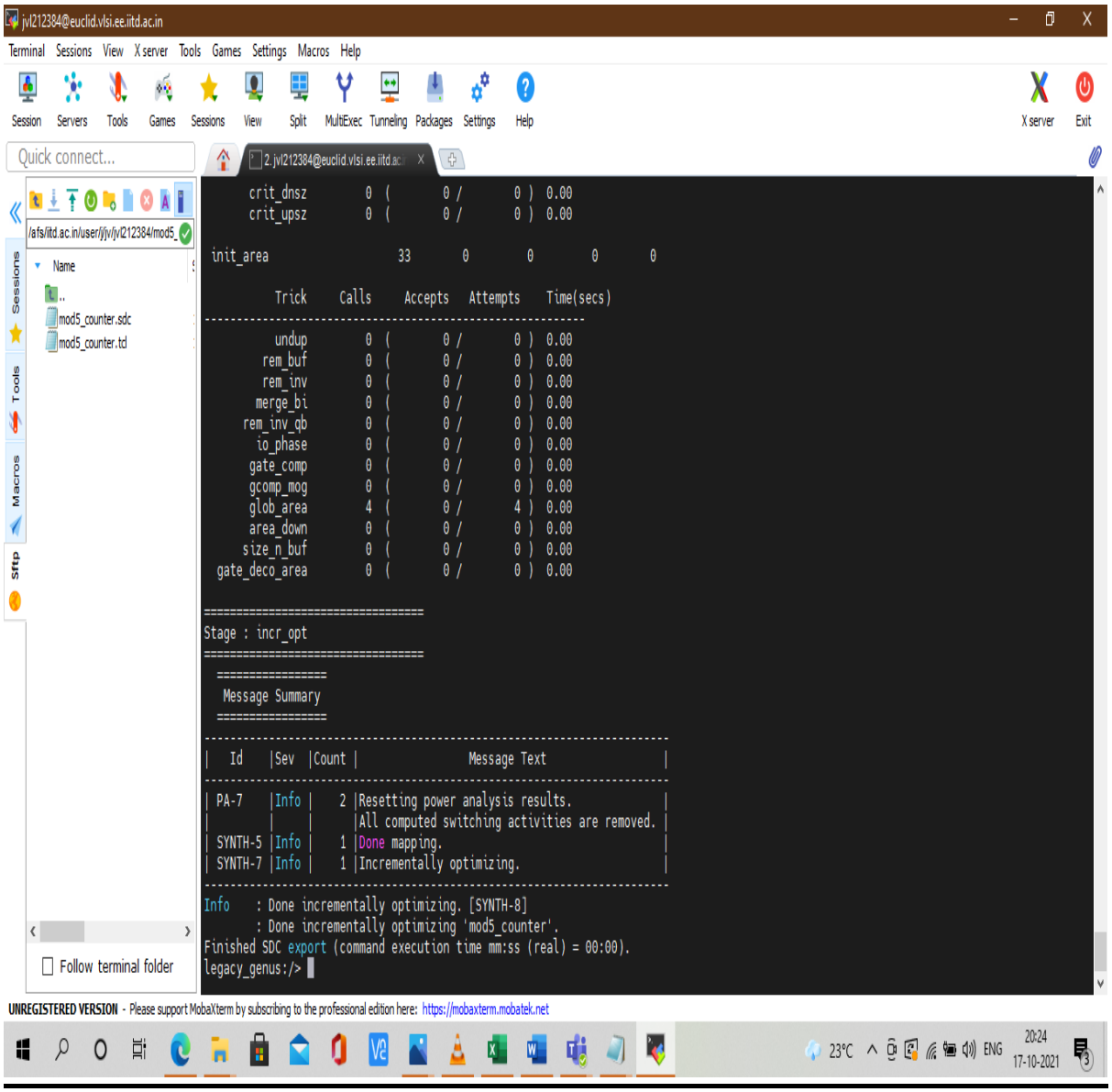
TCL File


mod5_counter.tcl - Notepad
File Edit Format View Help
set search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute lib_search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute hdl_search_path "./rtl/"
set_attribute library "uk65lscllmvbbr_100c25_tc_ccs.lib"
read_hdl mod5_counter.v
elaborate
check_design -unresolved
read_sdc ./synthesis/mod5_counter_sdc.sdc
synthesize -to_mapped -effort medium
write_hdl > ./typical/counter_netlist.v
write_sdc > ./typical/counter.sdc
Ln 1, Col 1
100%
Unix (LF)
UTF-8
24°C
ENG
21:48
17-10-2021

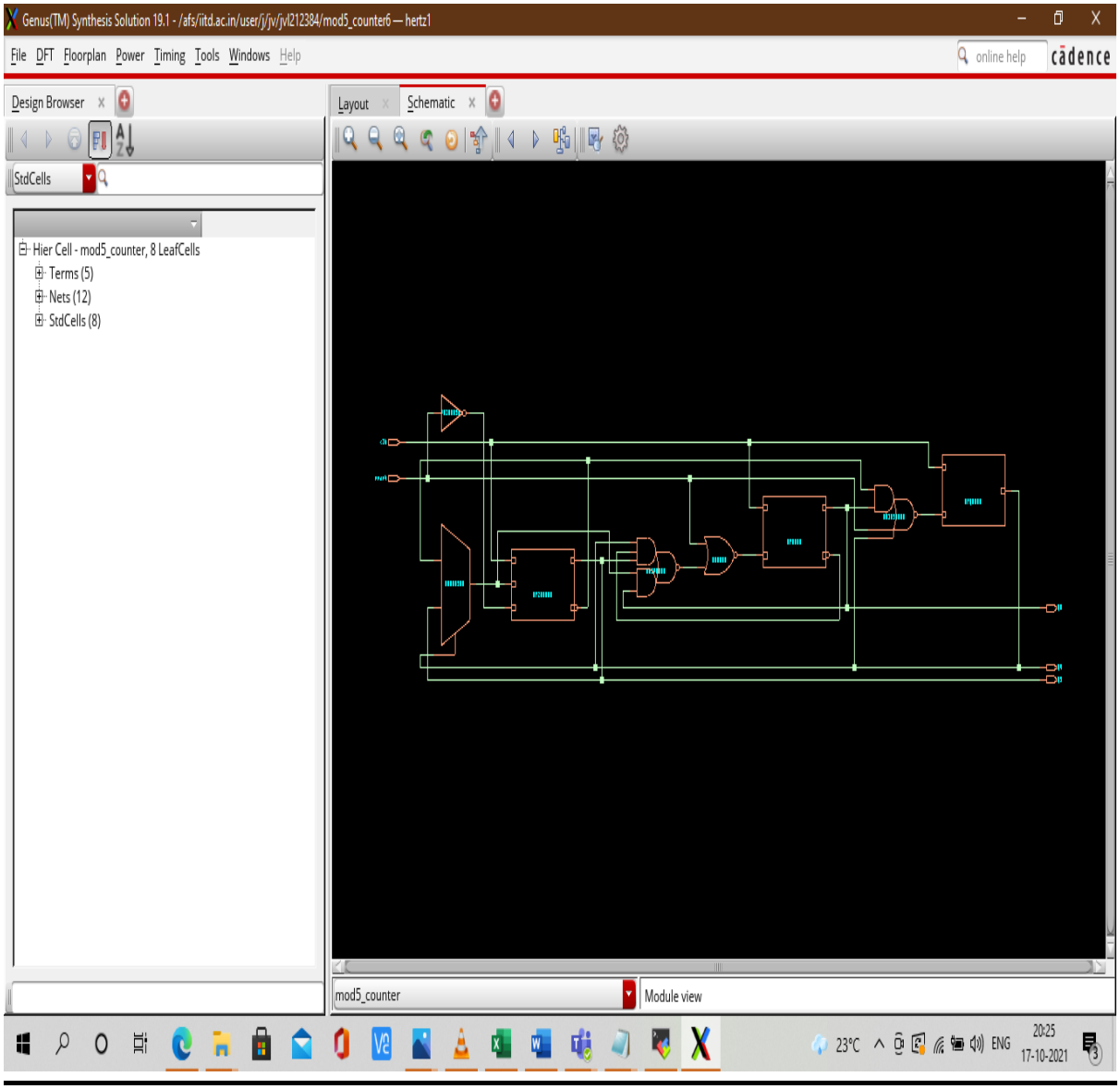
SDC File


mod5_counter_sdc.sdc - Notepad
File Edit Format View Help
set sdc_version 1.7
set_units -capacitance 1000.0fF
set_units -time 1000.0ps
Set the current design
current_design counter
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainity 0.1 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk]
set_output_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk]
set_wire_load_mode "top"
Ln 1, Col 1
100%
Unix (LF)
UTF-8
24°C
ENG
21:48
17-10-2021

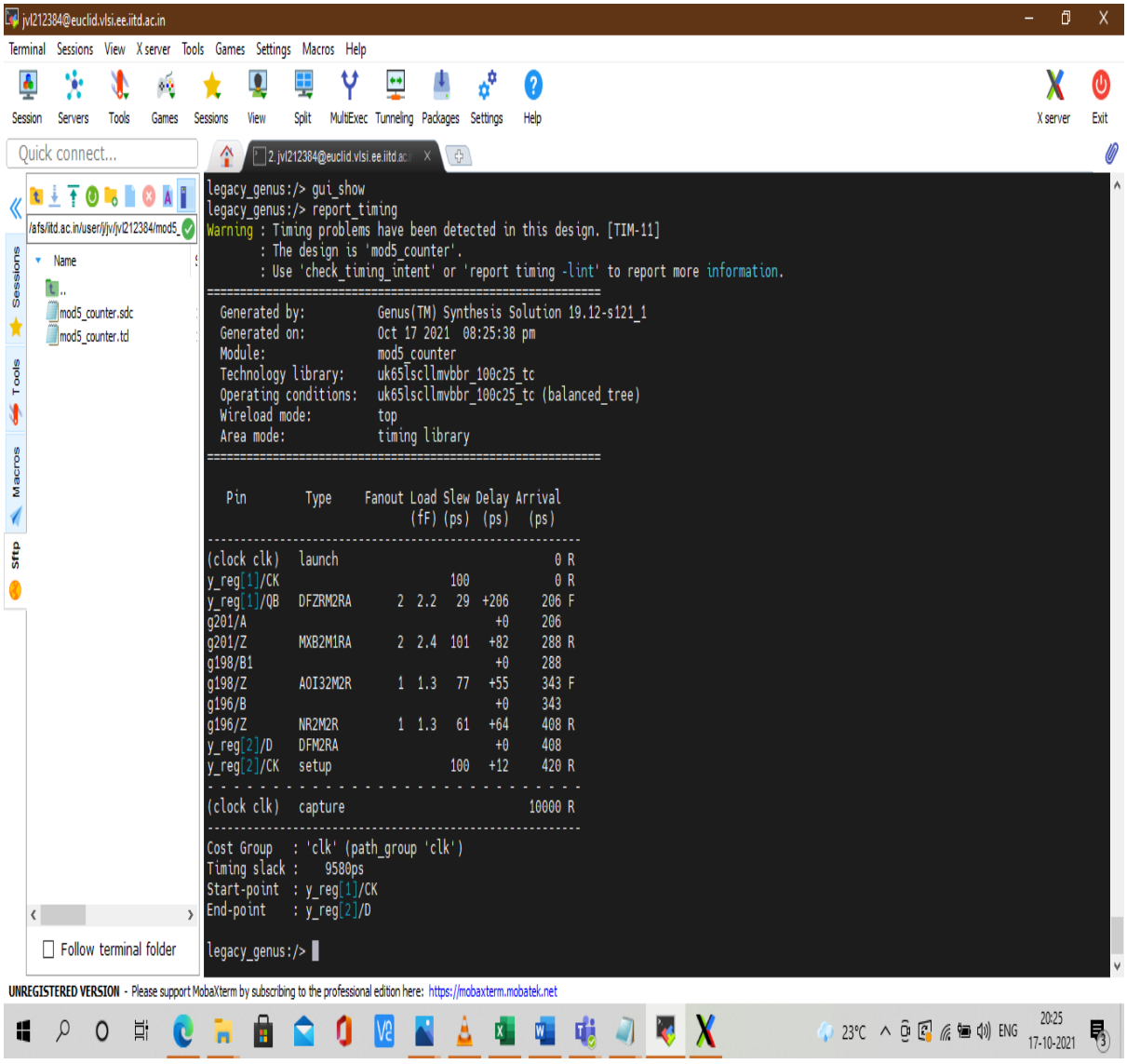
SYNTHESIS USING GENUS TOOL



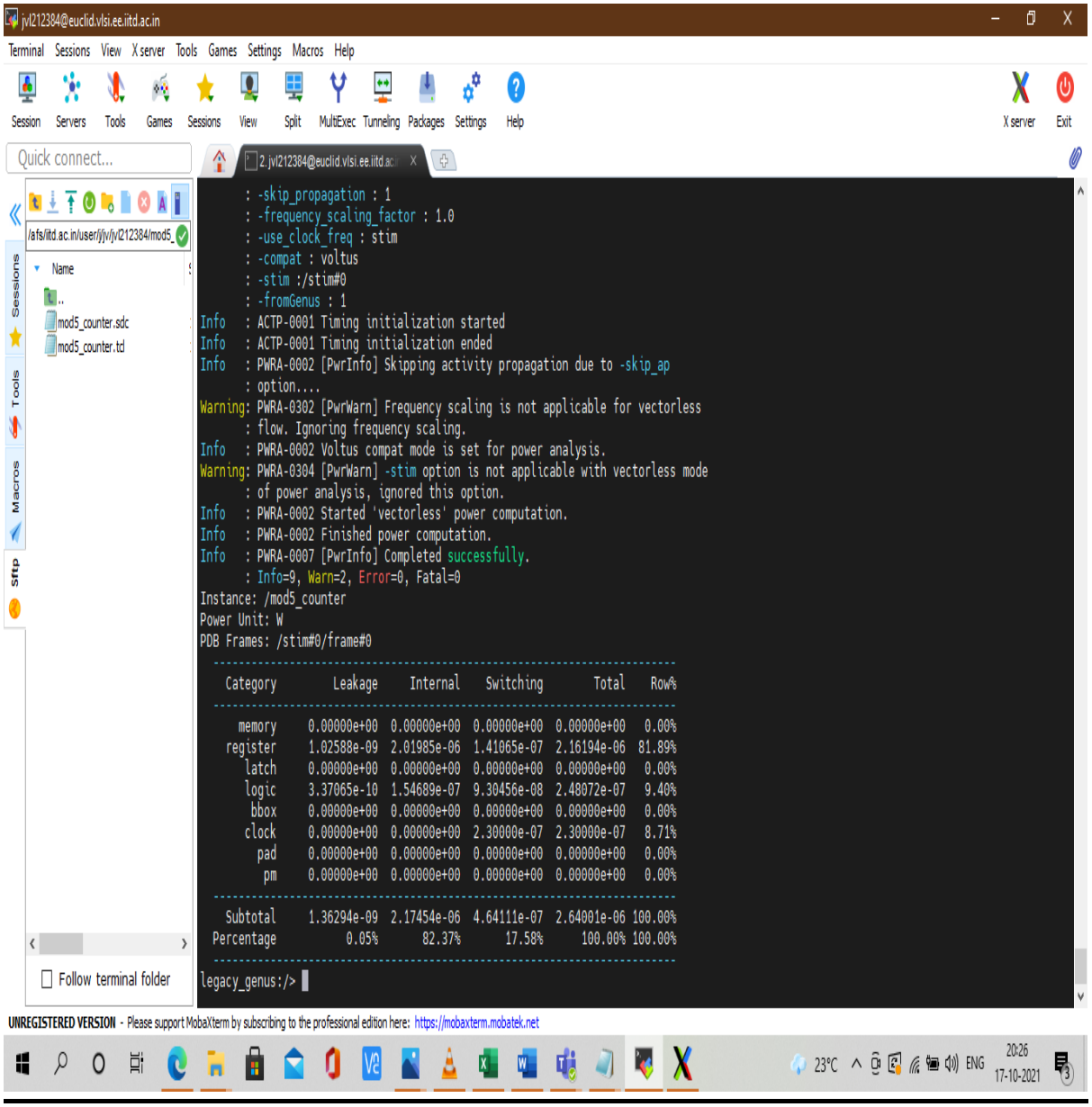
GATE LEVEL NETLIST



TIMING ANALYSIS

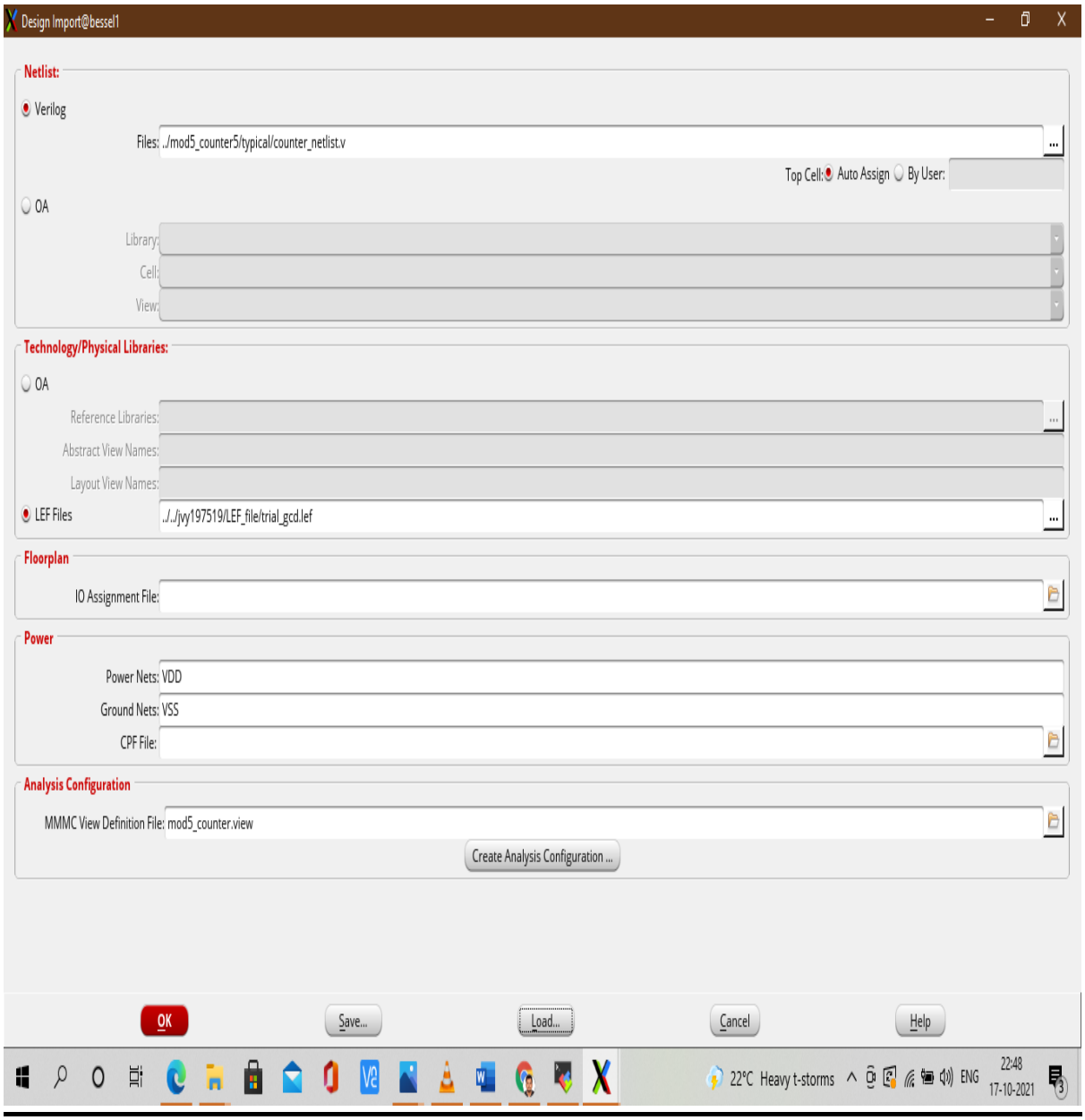


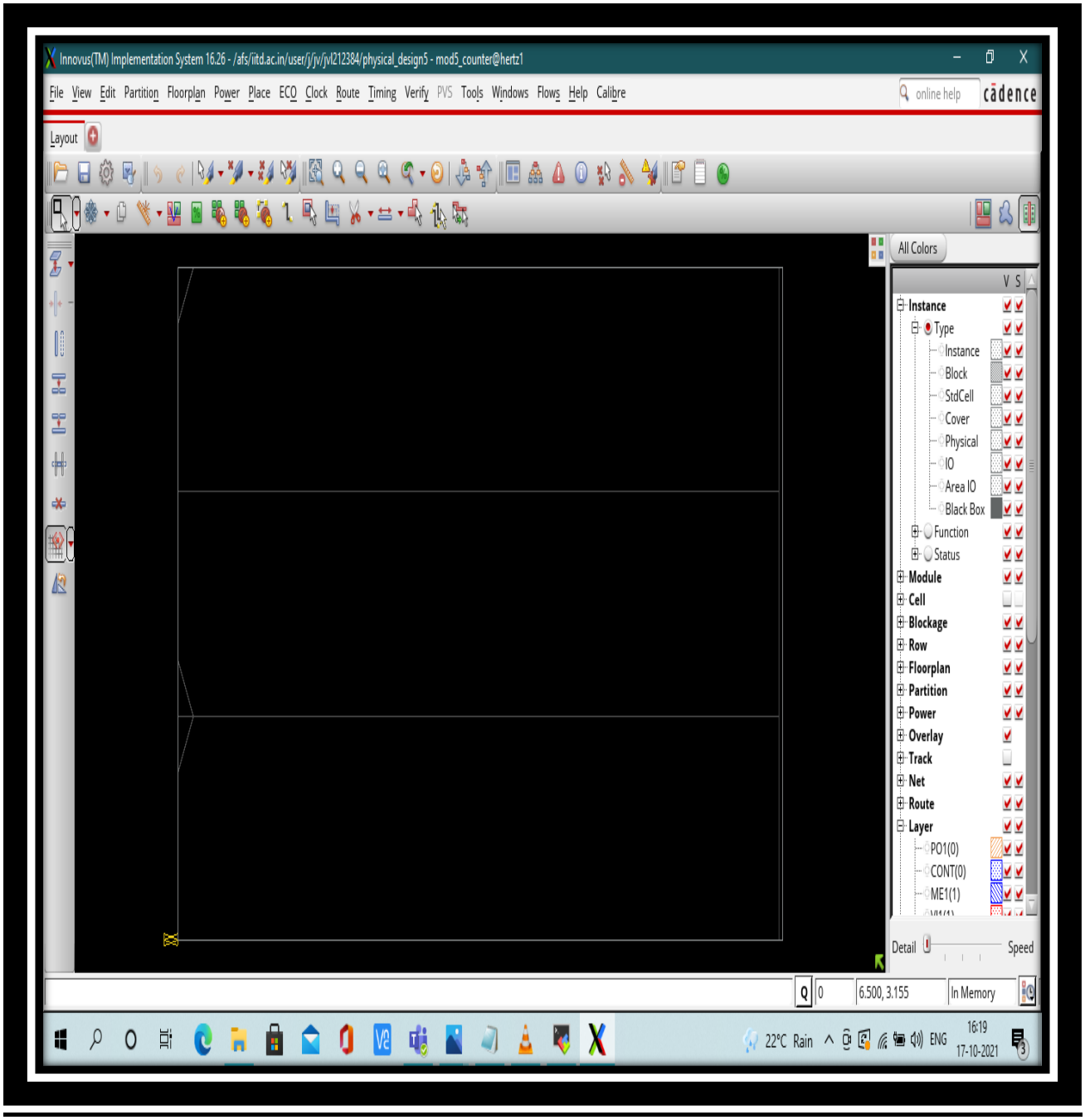
POWER ANALYSIS



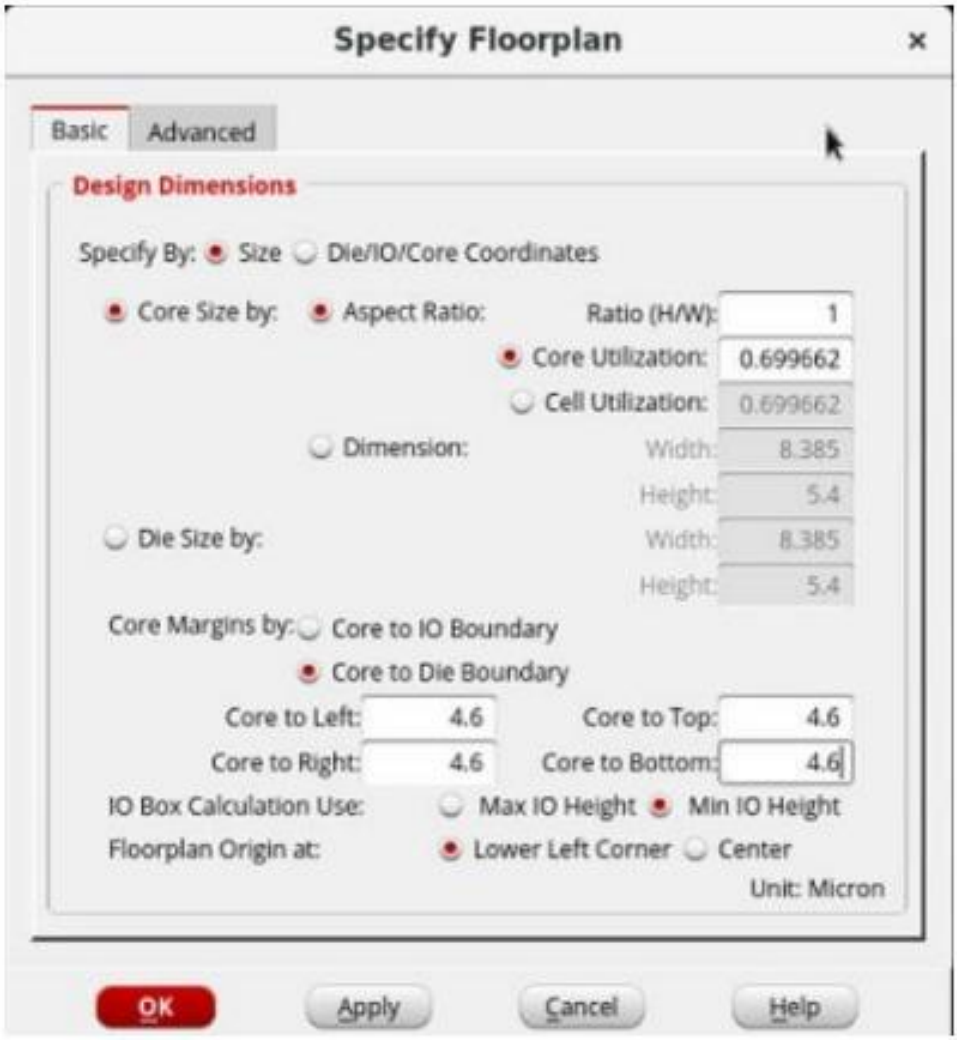
PHYSICAL DESIGN USING INNOVUS

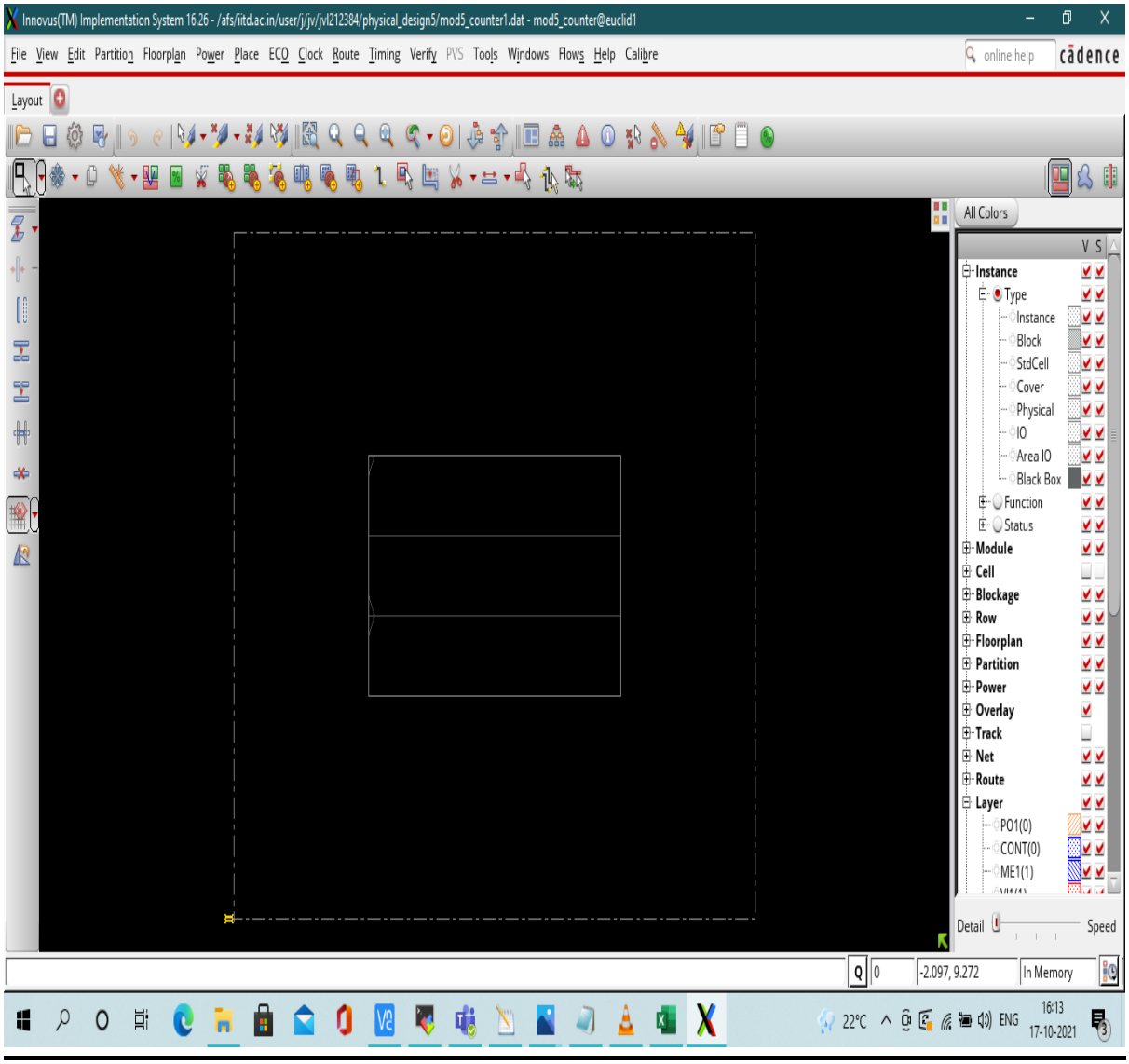
AFTER IMPORTING THE DESIGN




Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl212384/physical_design5 - mod5_counter@hertz1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
online help
cadence
Layout
All Colors
V S
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
Detail
Speed
Q
0
6.500, 3.155
In Memory
22°C Rain
ENG
16:19
17-10-2021

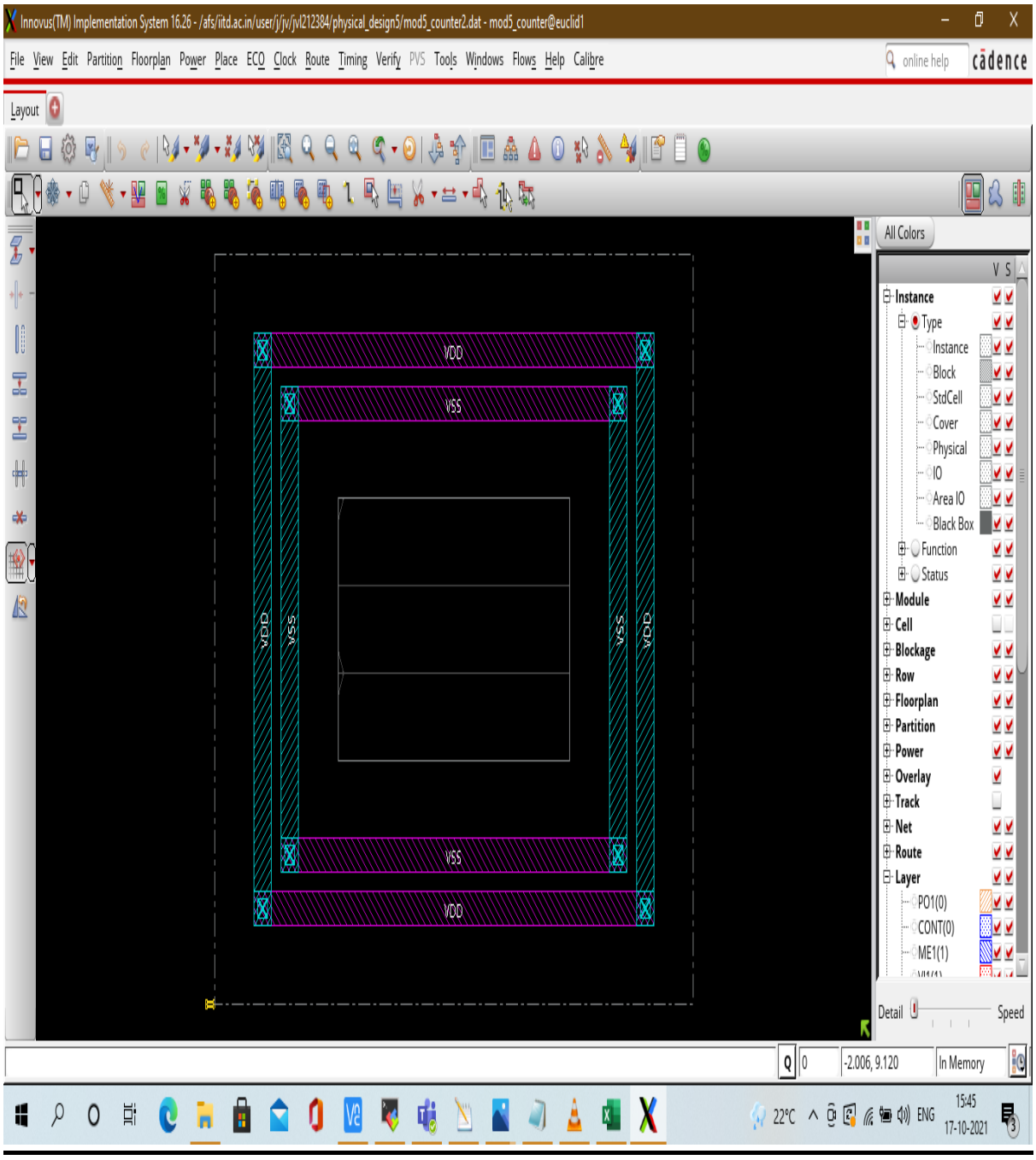
FLOOR PLANNING



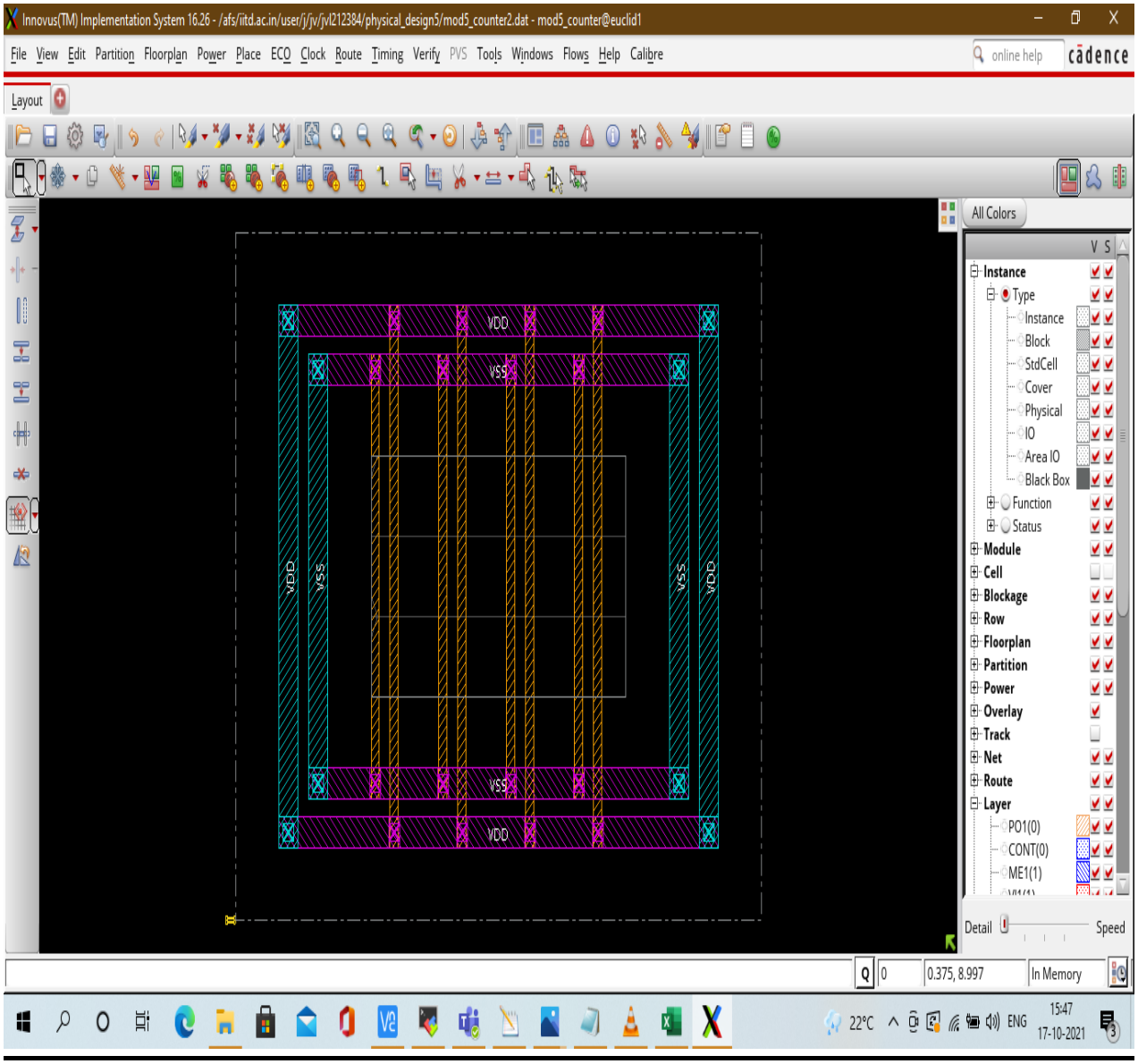

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl212384/physical_design5/mod5_counter1.dat - mod5_counter@euclid1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
online help
cadence
Layout
All Colors
V S
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
Detail
Speed
0
-2.097, 9.272
In Memory
22°C
ENG
16:13
17-10-2021

POWER PLANNING

ADDING RINGS

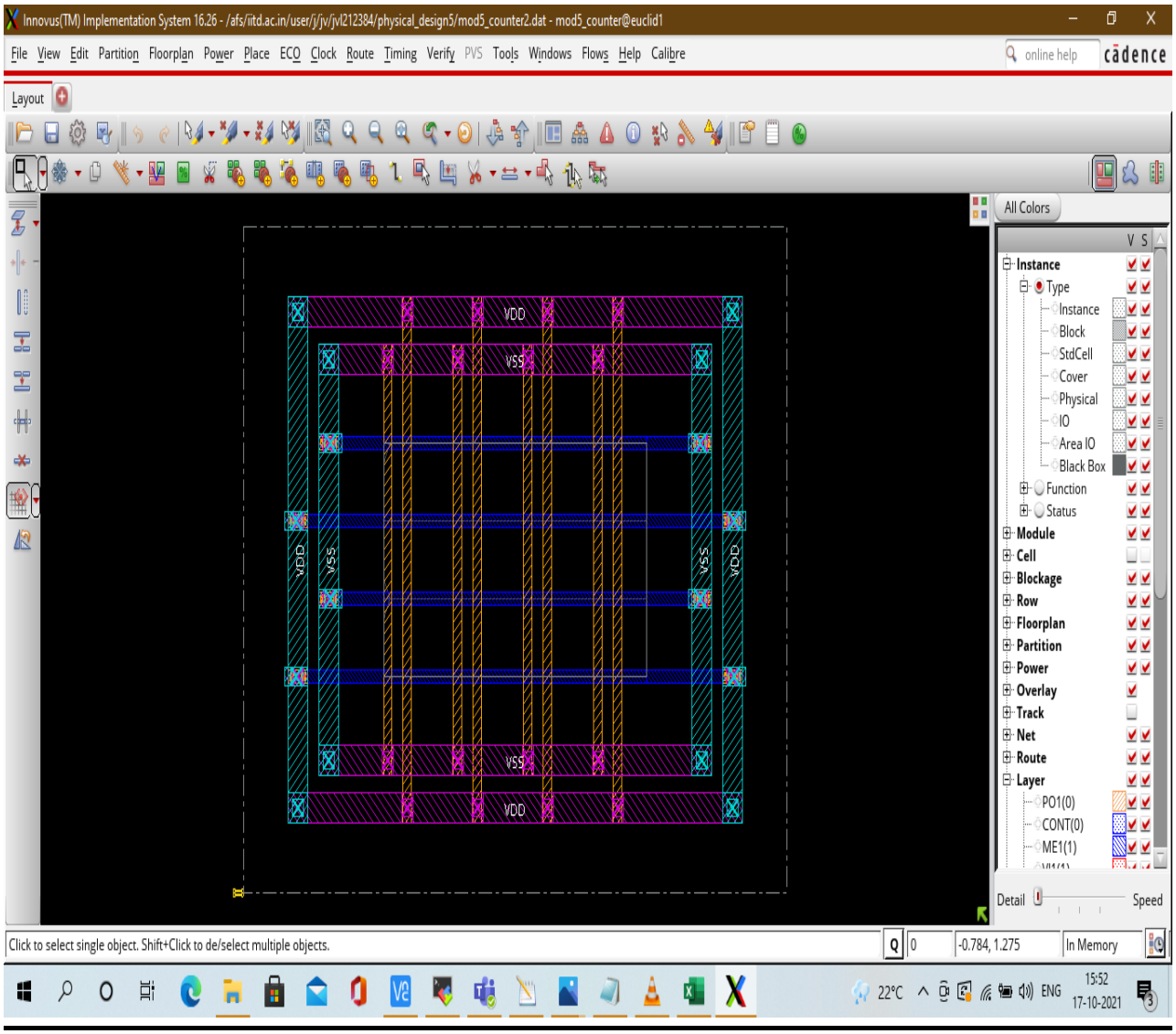

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl212384/physical_design5/mod5_counter2.dat - mod5_counter@euclid1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
online help
cadence
Layout
All Colors
V S
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
Detail
Speed
VDD
VSS
VSS
VDD
VSS
VDD
0
-2.006, 9.120
In Memory
22°C
ENG
15:45
17-10-2021

ADDING STRIPS

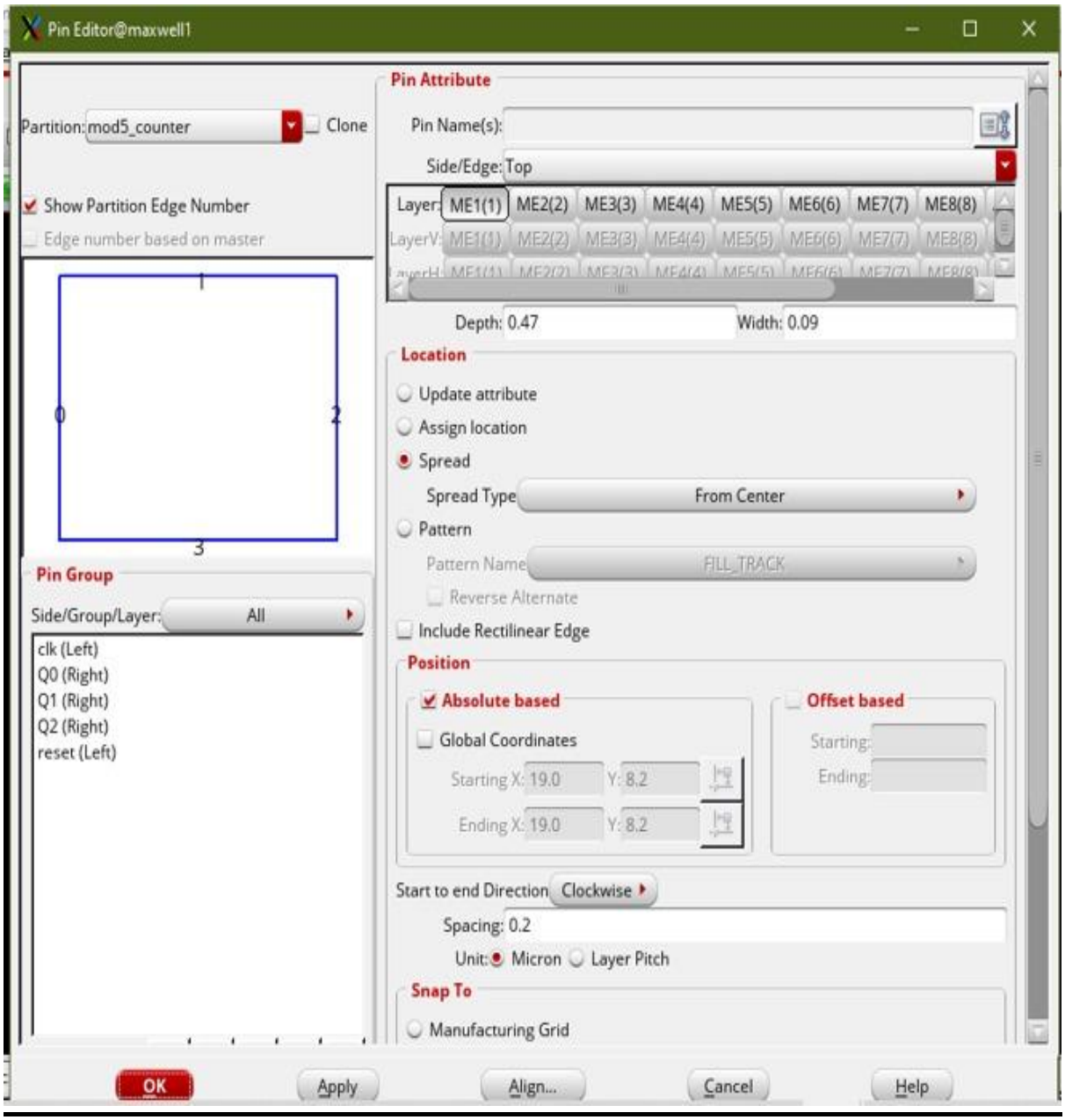

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl212384/physical_design5/mod5_counter2.dat - mod5_counter@euclid1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
online help
cadence
Layout
All Colors
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
Detail
Speed
VDD
VSS
VSS
VDD
VSS
VDD
0
0.375, 8.997
In Memory
22°C
ENG
15:47
17-10-2021

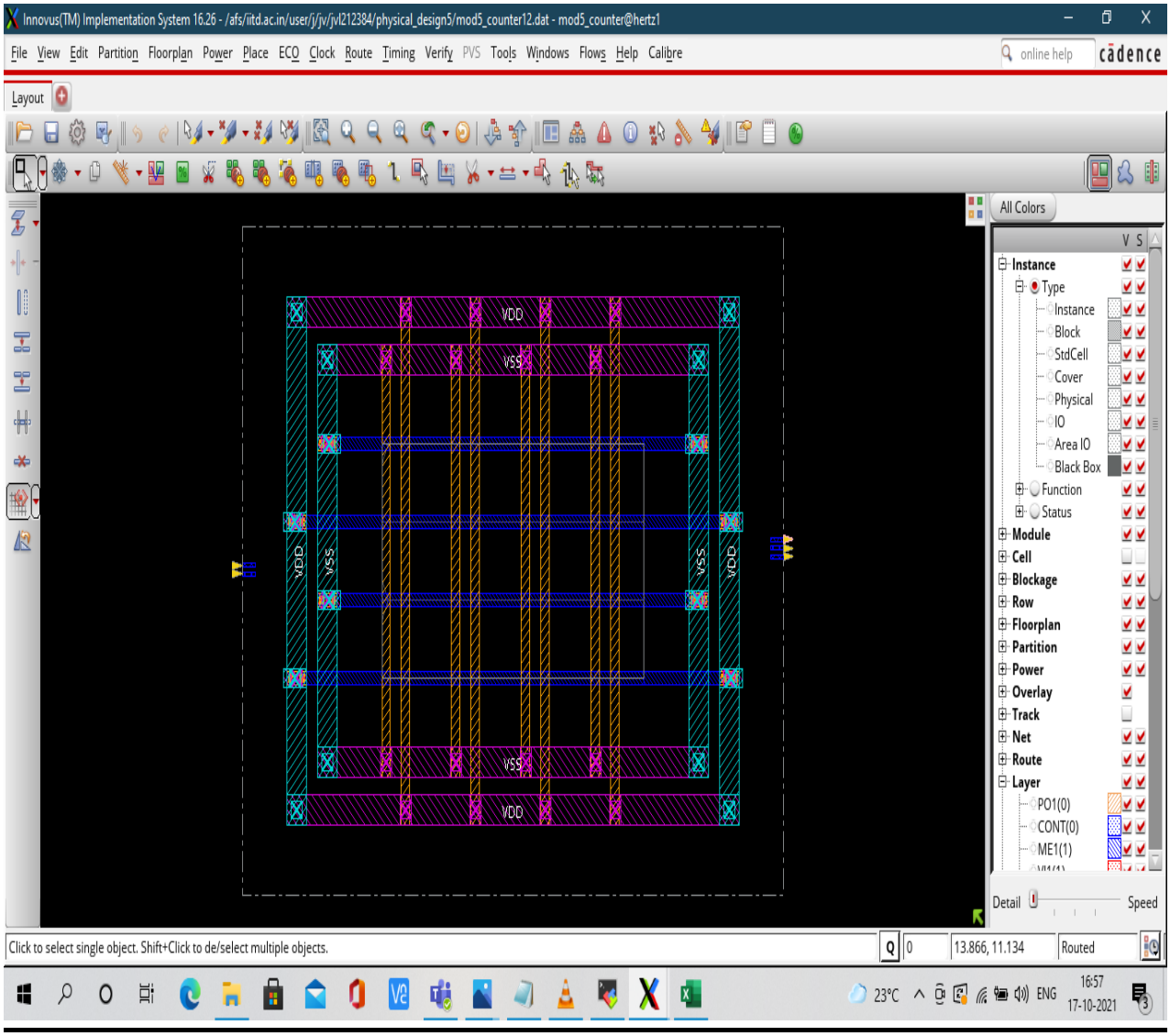
SROUTE


SRoute
Basic
Advanced
Via Generation
Net(s): VDD VSS
SRoute
Block Pins
Pad Rings
Floating Stripes
Pad Pins
Follow Pins
Secondary Power Pins
Routing Control
Layer Change Control
Top Layer: ME8(8)
Bottom Layer: ME1(1)
Allow Jogging
Allow Layer Change
Specify Area
X1:
Y1:
X2:
Y2:
Connect to Target Inside The Area Only
Power Domain Selection
All
Selected
Named:
Delete Existing Routes
Generate Progress Messages
Mode Setup
Target Editing Options
OK
Apply
Defaults
Cancel
Help

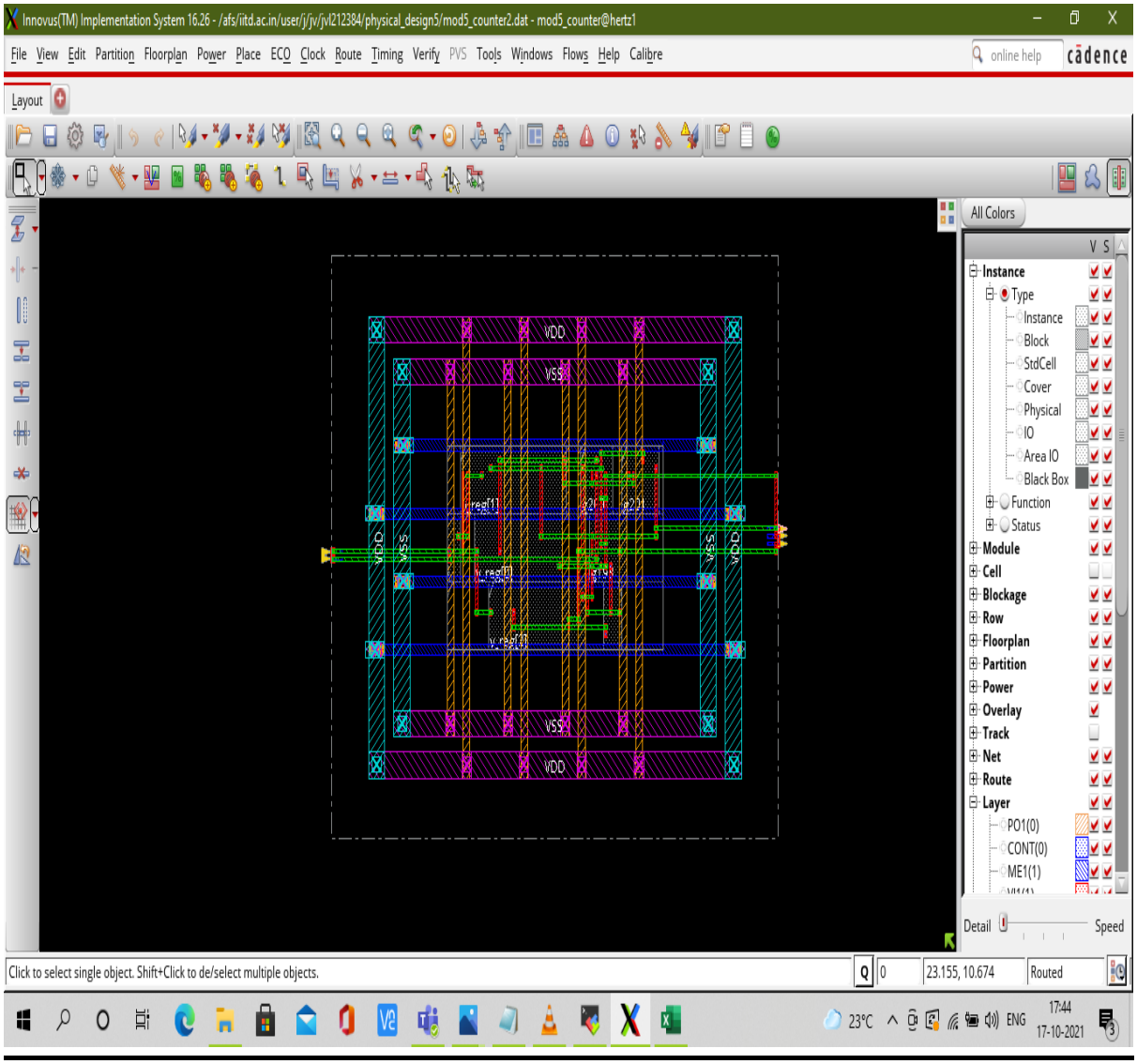

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl212384/physical_design5/mod5_counter2.dat - mod5_counter@euclid1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
online help
cadence
Layout
All Colors
V S
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
Detail
Speed
VDD
VSS
VSS
VDD
VSS
VDD
Click to select single object. Shift+Click to de/select multiple objects.
0
-0.784, 1.275
In Memory
22°C
ENG
15:52
17-10-2021

PIN PLACEMENT

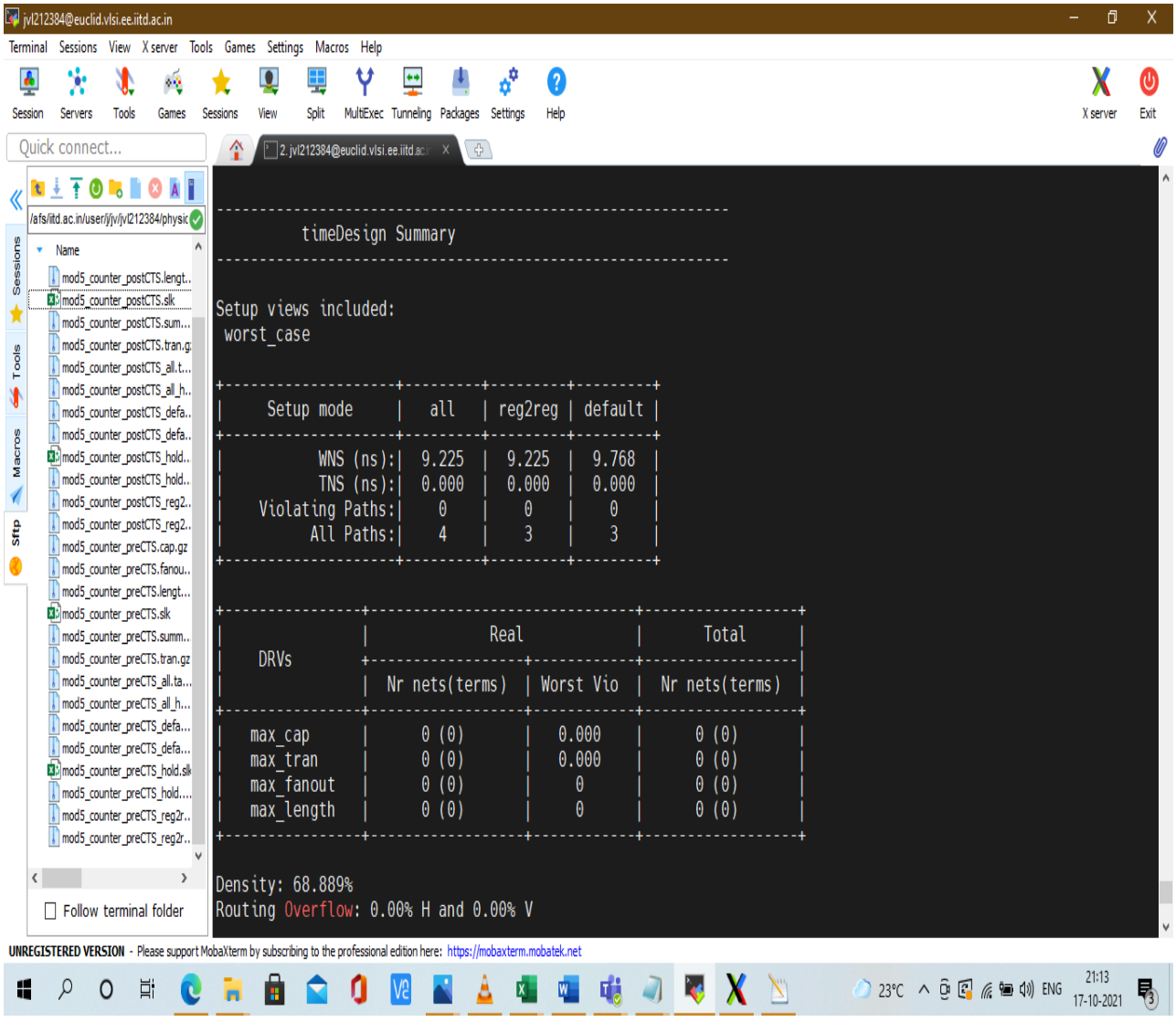



Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl212384/physical_design5/mod5_counter12.dat - mod5_counter@hertz1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
online help
cadence
Layout
All Colors
V S
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
Detail
Speed
VDD
VSS
VDD
VSS
VSS
VDD
VSS
VDD
Click to select single object. Shift+Click to de/select multiple objects.
0
13.866, 11.134
Routed
23°C
ENG
16:57
17-10-2021

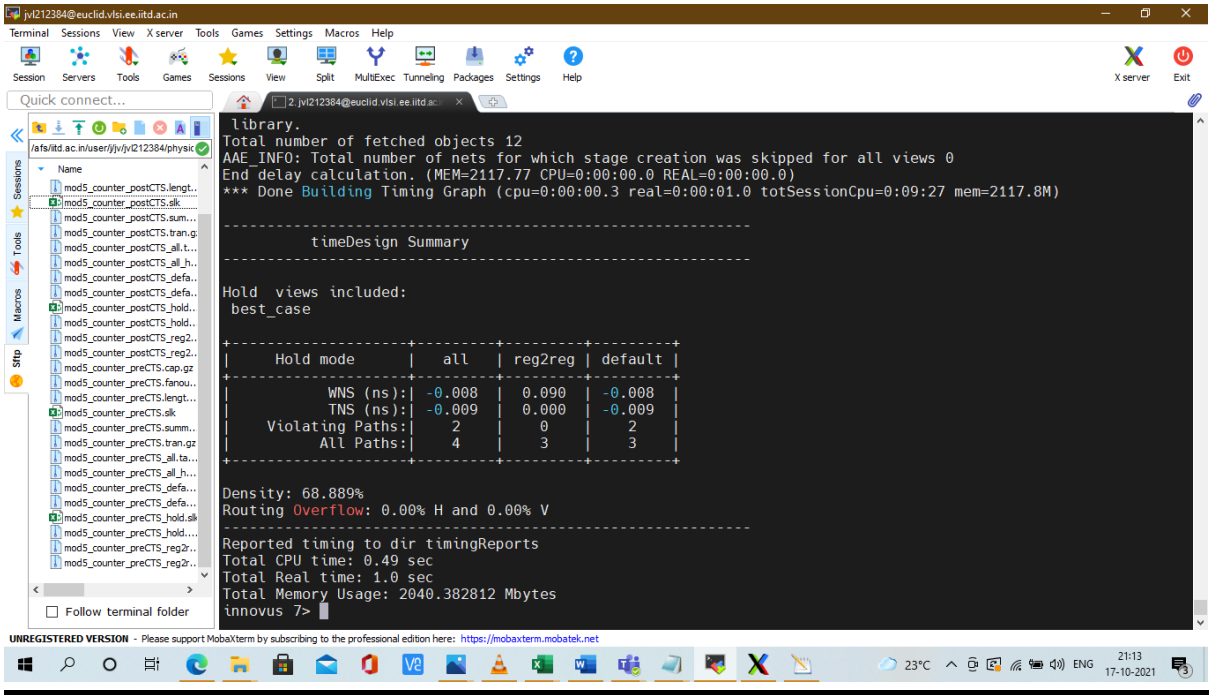
STANDARD CELL PLACEMENT



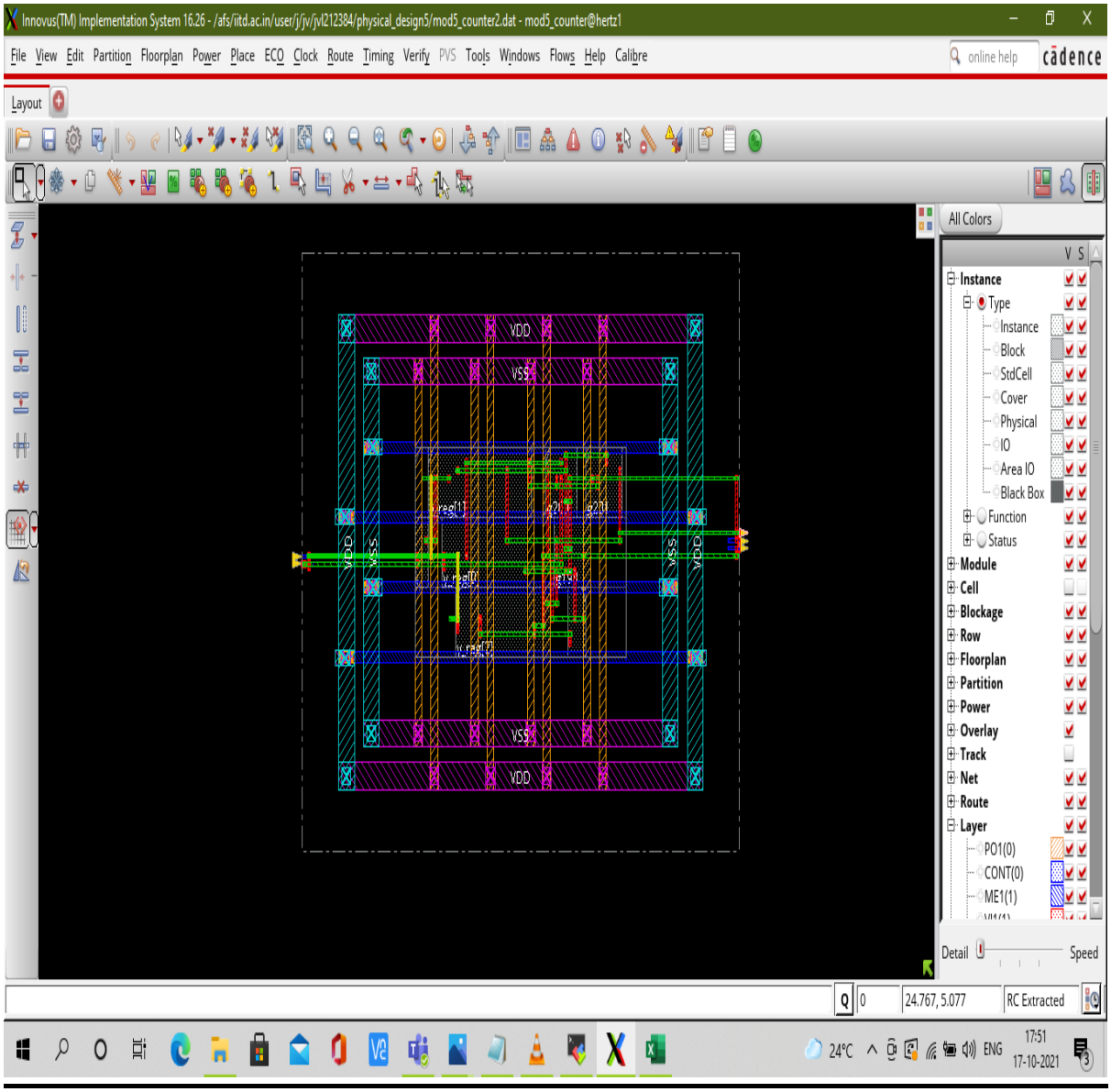

Timing Analysis
Basic
Advanced
Use Existing Extraction and Timing Data
Design Stage
Pre-Place
Pre-CTS
Post-CTS
Post-Route
Sign-Off
Analysis Type
Setup
Hold
Include SI
Reporting Options
Number of Paths:
50
Report file(s) Prefix:
Mod5Counter_preCTS
Output Directory:
timingReports
OK
Apply
Cancel
Help


jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
2. jvl212384@euclid.vlsi.ee.iitd.ac
/afs/iitd.ac.in/user/j/jv/jvl212384/physic
Name
mod5_counter_postCTS.lengt..
mod5_counter_postCTS.slk
mod5_counter_postCTS.sum...
mod5_counter_postCTS.tran.g
mod5_counter_postCTS_all.t...
mod5_counter_postCTS_all_h..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_reg2..
mod5_counter_postCTS_reg2..
mod5_counter_preCTS.cap.gz
mod5_counter_preCTS.fanou..
mod5_counter_preCTS.lengt...
mod5_counter_preCTS.slk
mod5_counter_preCTS.summ..
mod5_counter_preCTS.tran.gz
mod5_counter_preCTS_all.ta...
mod5_counter_preCTS_all_h...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_hold.sk
mod5_counter_preCTS_hold....
mod5_counter_preCTS_reg2r..
mod5_counter_preCTS_reg2r..
Follow terminal folder
Sessions Tools Macros Sftp
timeDesign Summary
Setup views included:
worst_case
Setup mode | all | reg2reg | default
WNS (ns): | 9.225 | 9.225 | 9.768
TNS (ns): | 0.000 | 0.000 | 0.000
Violating Paths: | 0 | 0 | 0
All Paths: | 4 | 3 | 3
DRVs | Real | Total
Nr nets(terms) | Worst Vio | Nr nets(terms)
max_cap | 0 (0) | 0.000 | 0 (0)
max_tran | 0 (0) | 0.000 | 0 (0)
max_fanout | 0 (0) | 0 | 0 (0)
max_length | 0 (0) | 0 | 0 (0)
Density: 68.889%
Routing Overflow: 0.00% H and 0.00% V
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
23°C ENG 21:13 17-10-2021

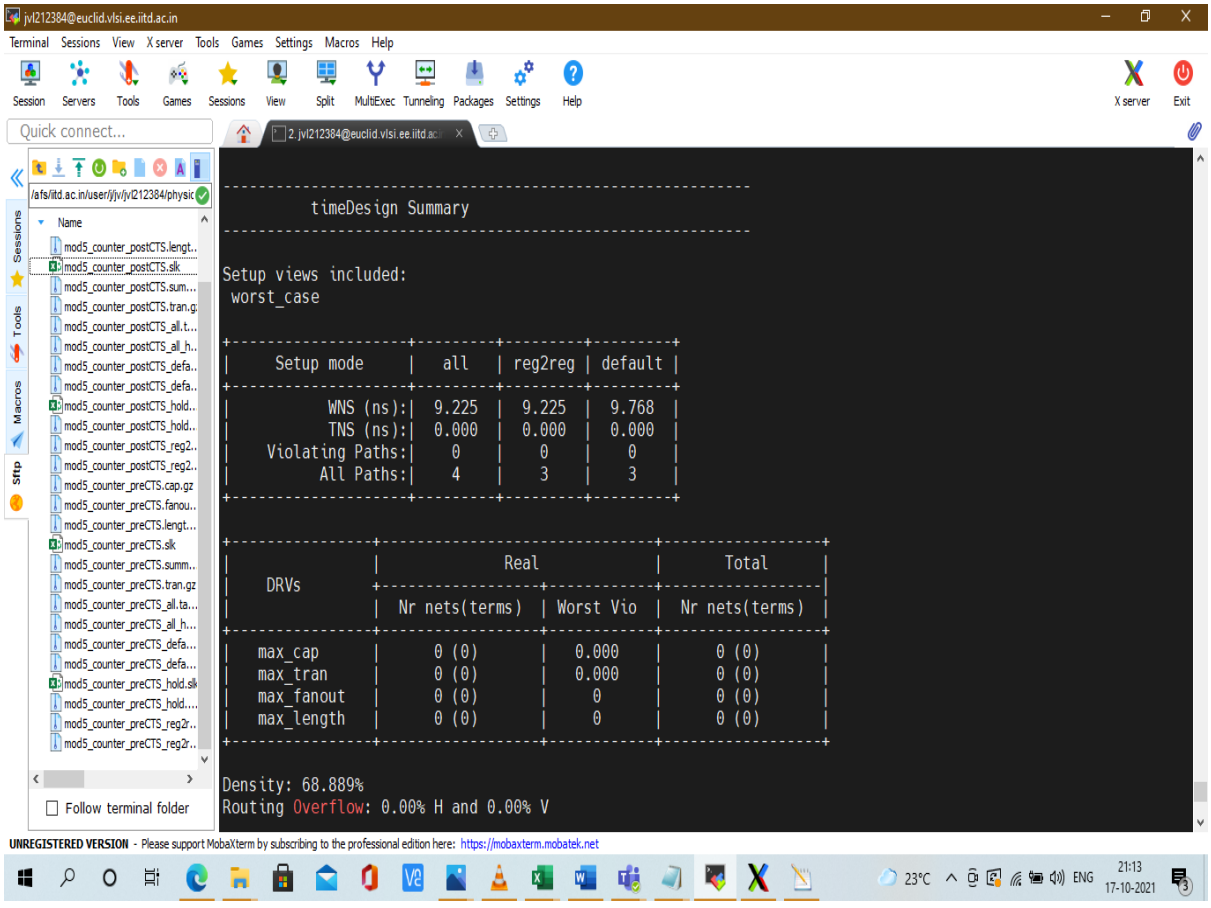

Timing Analysis
Basic
Advanced
Use Existing Extraction and Timing Data
Design Stage
Pre-Place
Pre-CTS
Post-CTS
Post-Route
Sign-Off
Analysis Type
Setup
Hold
Include SI
Reporting Options
Number of Paths:
50
Report file(s) Prefix:
Mod5Counter_preCTS
Output Directory:
timingReports
OK
Apply
Cancel
Help


jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
library.
Total number of fetched objects 12
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2117.77 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.3 real=0:00:01.0 totSessionCpu=0:09:27 mem=2117.8M)
timeDesign Summary
Hold views included:
best_case
Hold mode | all | reg2reg | default
WNS (ns): -0.008 | 0.090 | -0.008
TNS (ns): -0.009 | 0.000 | -0.009
Violating Paths: 2 | 0 | 2
All Paths: 4 | 3 | 3
Density: 68.889%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 0.49 sec
Total Real time: 1.0 sec
Total Memory Usage: 2040.382812 Mbytes
innovus 7>
Follow terminal folder
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
23°C
ENG
21:13
17-10-2021

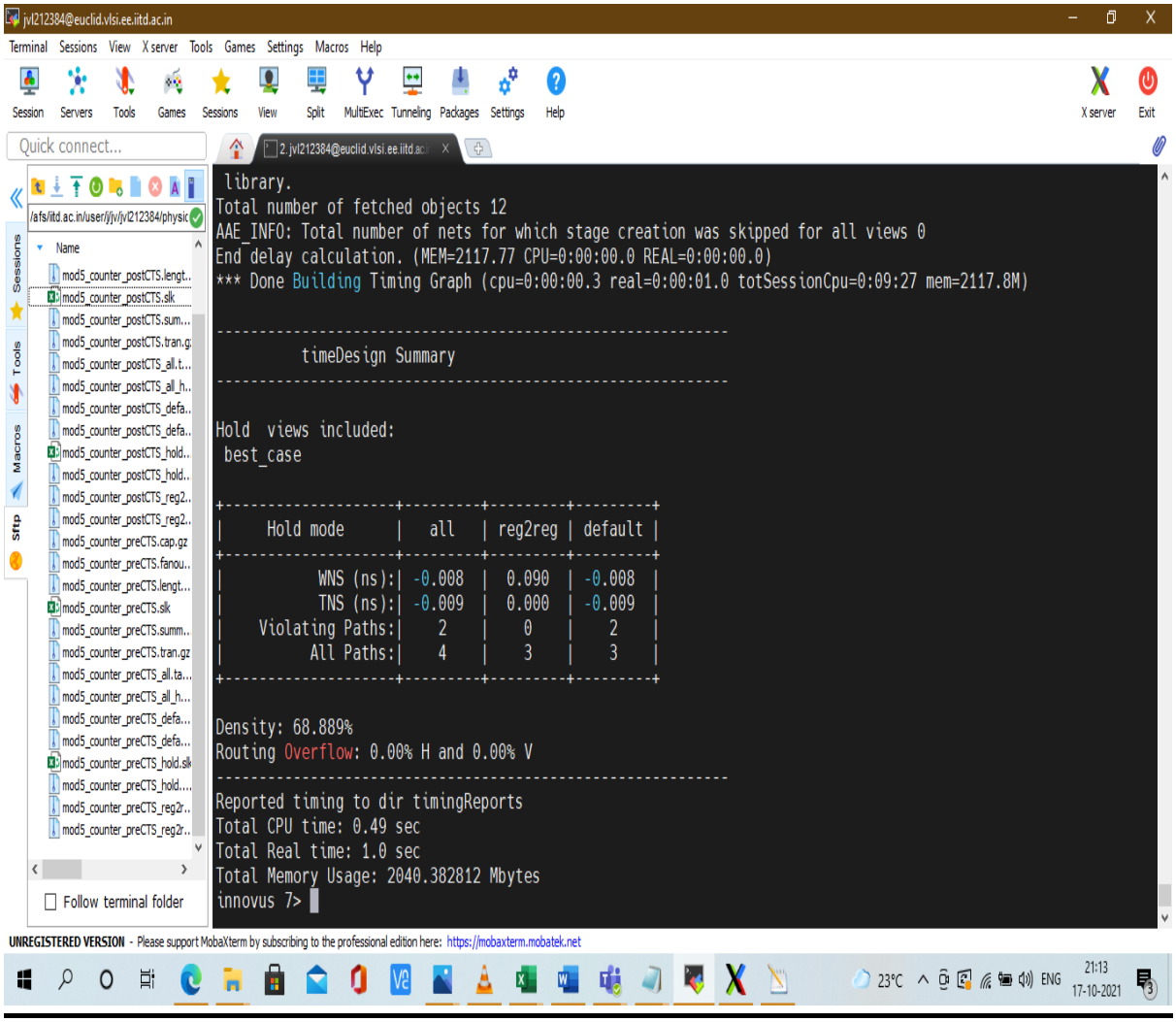
CLOCK TREE SYNTHESIS




Timing Analysis
Basic
Advanced
Use Existing Extraction and Timing Data
Design Stage
Pre-Place
Pre-CTS
Post-CTS
Post-Route
Sign-Off
Analysis Type
Setup
Hold
Include SI
Reporting Options
Number of Paths:
50
Report file(s) Prefix:
Mod5Counter_postCTS
Output Directory:
timingReports
OK
Apply
Cancel
Help


jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
timeDesign Summary
Setup views included:
worst_case
Setup mode	all	reg2reg	default
WNS (ns):	9.225	9.225	9.768
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	4	3	3
DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)
Density: 68.889%
Routing Overflow: 0.00% H and 0.00% V
Follow terminal folder
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
23°C ENG 21:13 17-10-2021


Timing Analysis
Basic
Advanced
Use Existing Extraction and Timing Data
Design Stage
Pre-Place
Pre-CTS
Post-CTS
Post-Route
Sign-Off
Analysis Type
Setup
Hold
Include SI
Reporting Options
Number of Paths: 50
Report file(s) Prefix: Mod5Counter_postCTS
Output Directory: timingReports
OK
Apply
Cancel
Help


jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
2. jvl212384@euclid.vlsi.ee.iitd.ac
/afs/iitd.ac.in/user/j/jv/jvl212384/physic
Name
mod5_counter_postCTS.lengt..
mod5_counter_postCTS.slk
mod5_counter_postCTS.sum...
mod5_counter_postCTS.tran.g
mod5_counter_postCTS_all.t...
mod5_counter_postCTS_all_h...
mod5_counter_postCTS_defa...
mod5_counter_postCTS_defa...
mod5_counter_postCTS_hold...
mod5_counter_postCTS_hold...
mod5_counter_postCTS_reg2...
mod5_counter_postCTS_reg2...
mod5_counter_preCTS.cap.gz
mod5_counter_preCTS.fanou...
mod5_counter_preCTS.lengt...
mod5_counter_preCTS.slk
mod5_counter_preCTS.summ...
mod5_counter_preCTS.tran.gz
mod5_counter_preCTS_all.ta...
mod5_counter_preCTS_all_h...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_hold.slk
mod5_counter_preCTS_hold....
mod5_counter_preCTS_reg2r...
mod5_counter_preCTS_reg2r...
Follow terminal folder
Sessions Tools Macros Sftp
library.
Total number of fetched objects 12
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2117.77 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.3 real=0:00:01.0 totSessionCpu=0:09:27 mem=2117.8M)
timeDesign Summary
Hold views included:
best_case
Hold mode | all | reg2reg | default
WNS (ns): -0.008 | 0.090 | -0.008
TNS (ns): -0.009 | 0.000 | -0.009
Violating Paths: 2 | 0 | 2
All Paths: 4 | 3 | 3
Density: 68.889%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 0.49 sec
Total Real time: 1.0 sec
Total Memory Usage: 2040.382812 Mbytes
innovus 7>
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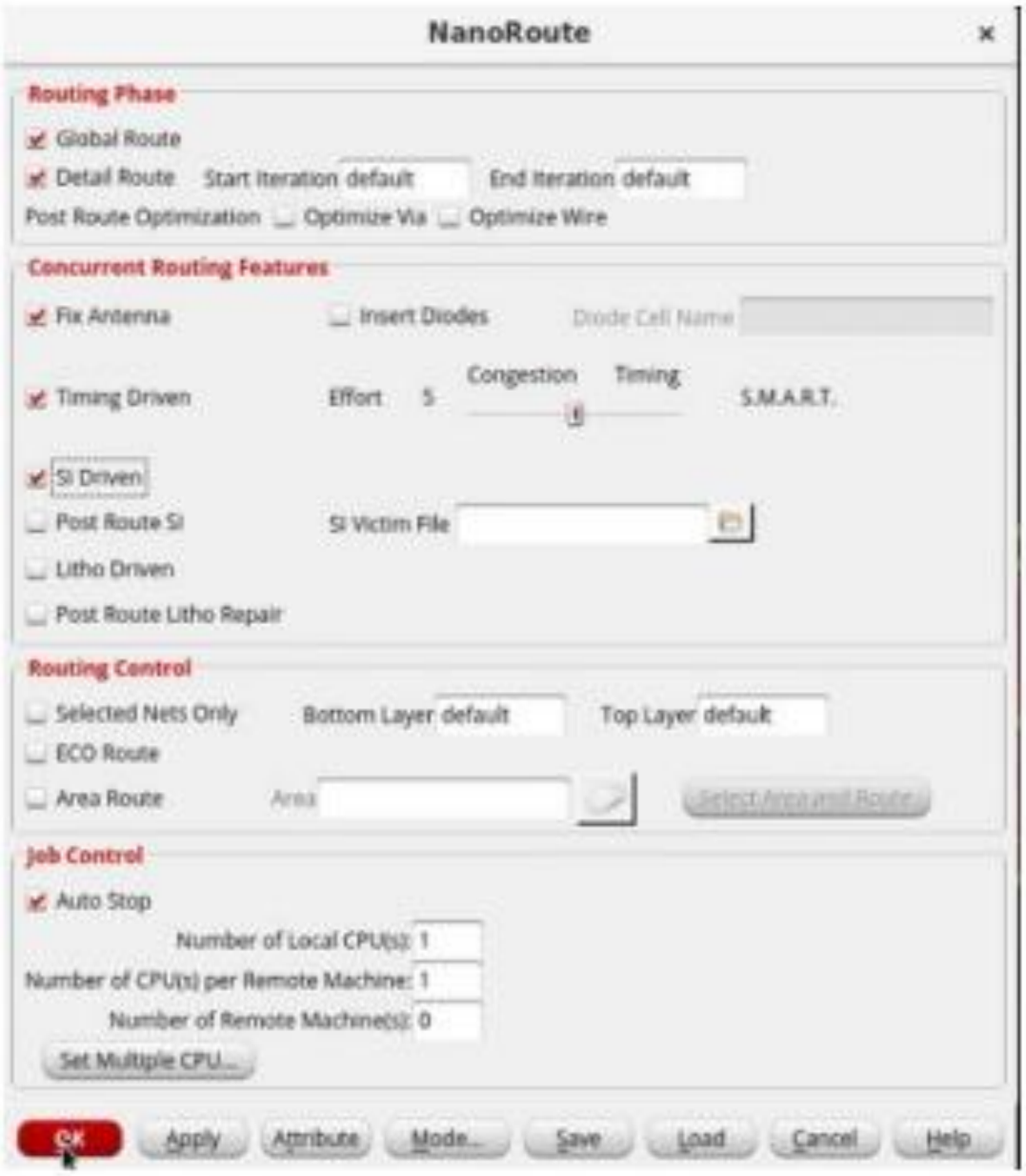
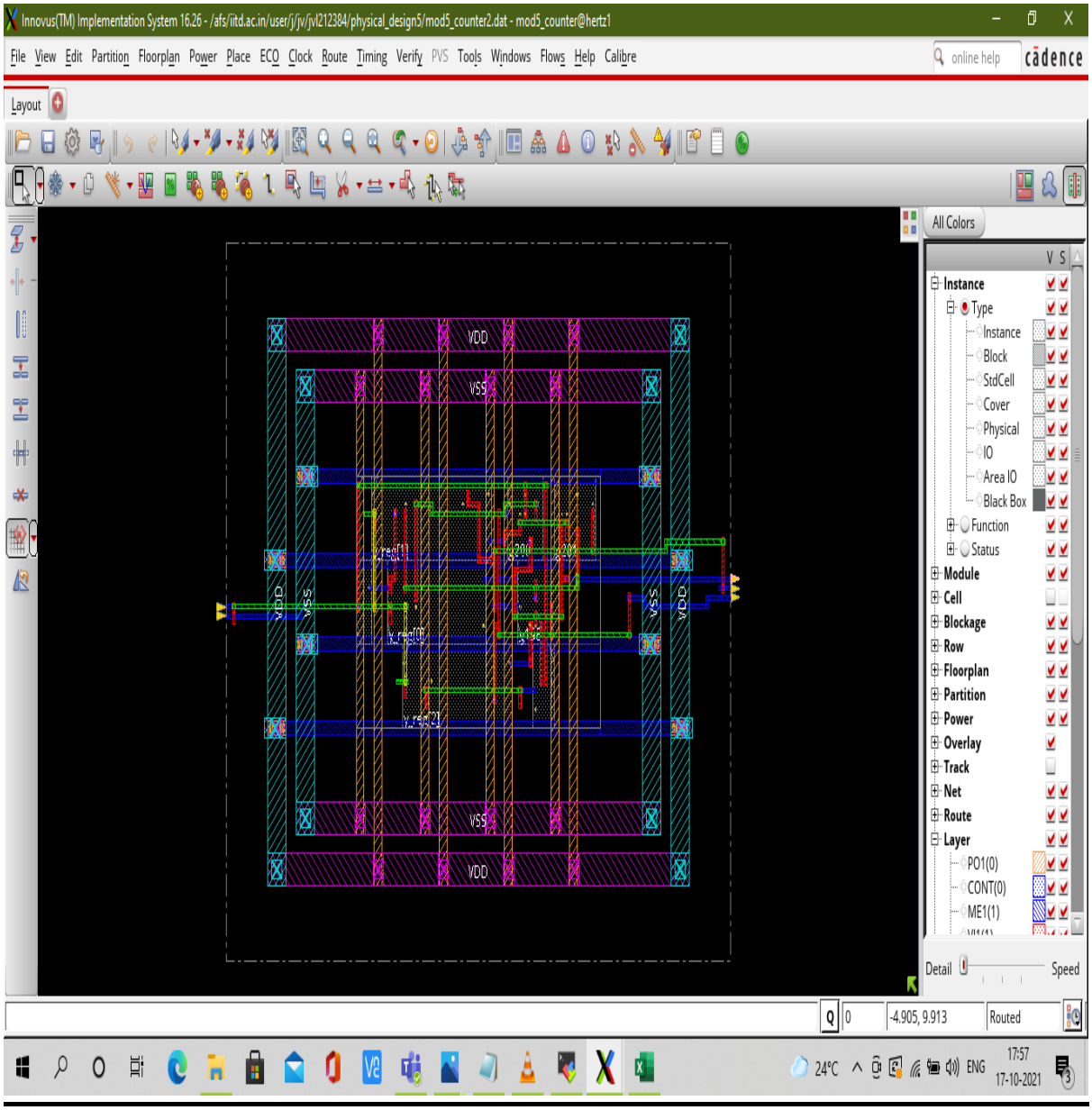
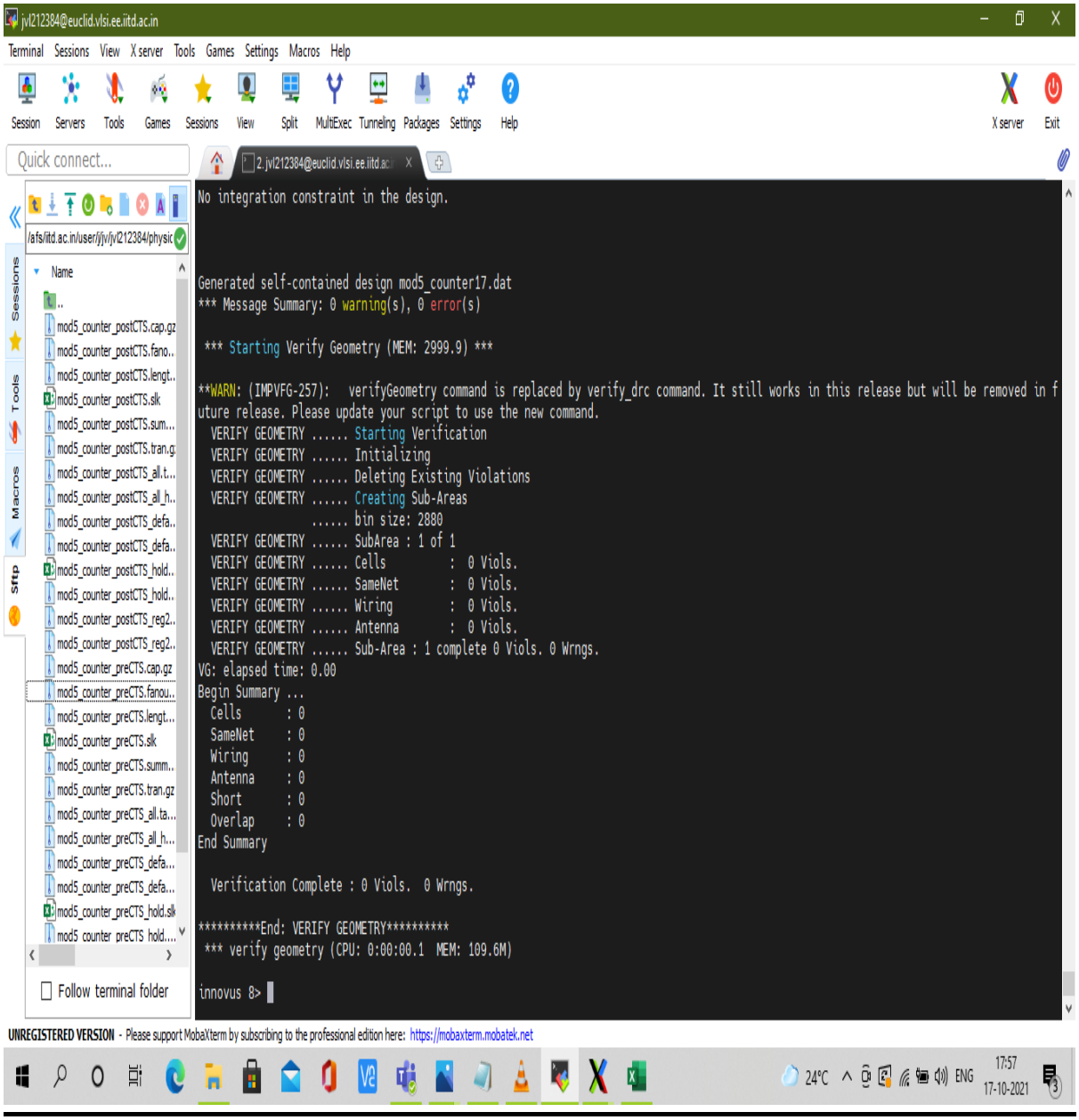
23°C ENG 21:13 17-10-2021

ROUTING THE DESIGN




Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl212384/physical_design5/mod5_counter2.dat - mod5_counter@hertz1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
online help
cadence
Layout
All Colors
V S
Instance
Type
Instance
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO1(0)
CONT(0)
ME1(1)
Detail
Speed
VDD
VSS
VSS
VDD
VSS
VDD
0
-4.905, 9.913
Routed
24°C
ENG
17:57
17-10-2021

VERIFY GEOMETRY


jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
2. jvl212384@euclid.vlsi.ee.iitd.ac
/afs/iitd.ac.in/user/j/jv/jvl212384/physic
Name
mod5_counter_postCTS.cap.gz
mod5_counter_postCTS.fano..
mod5_counter_postCTS.lengt..
mod5_counter_postCTS.slk
mod5_counter_postCTS.sum...
mod5_counter_postCTS.tran.g
mod5_counter_postCTS_all.t...
mod5_counter_postCTS_all_h..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_reg2..
mod5_counter_postCTS_reg2..
mod5_counter_preCTS.cap.gz
mod5_counter_preCTS.fanou..
mod5_counter_preCTS.lengt...
mod5_counter_preCTS.slk
mod5_counter_preCTS.summ..
mod5_counter_preCTS.tran.gz
mod5_counter_preCTS_all.ta...
mod5_counter_preCTS_all_h...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_hold.slk
mod5_counter_preCTS_hold....
Follow terminal folder
Sessions Tools Macros Sftp
No integration constraint in the design.
Generated self-contained design mod5_counter17.dat
*** Message Summary: 0 warning(s), 0 error(s)
*** Starting Verify Geometry (MEM: 2999.9) ***
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 2880
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
**********End: VERIFY GEOMETRY**********
*** verify geometry (CPU: 0:00:00.1 MEM: 109.6M)
innovus 8>
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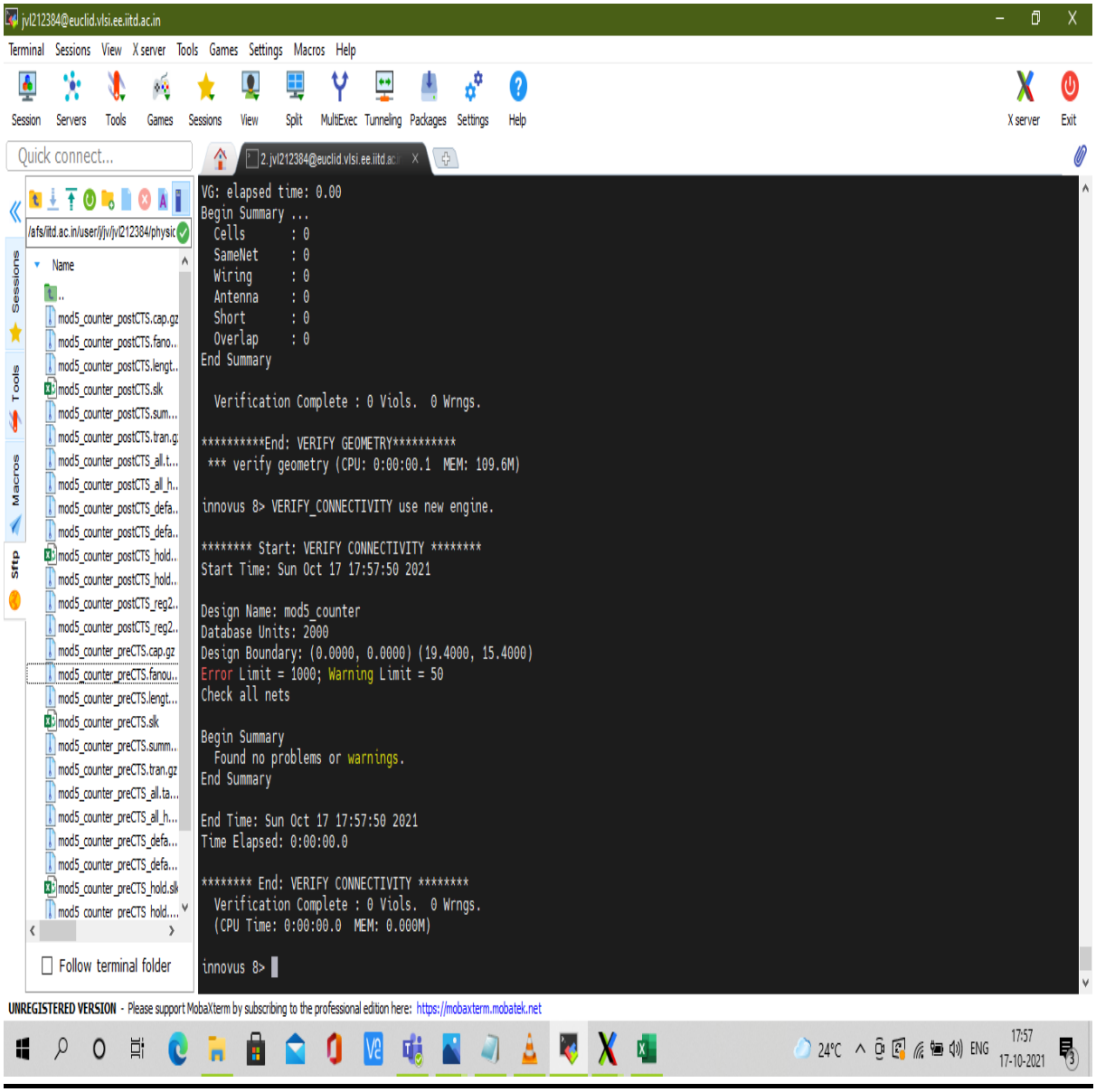
VERIFY CONNECTIVITY


jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
2. jvl212384@euclid.vlsi.ee.iitd.ac
/afs/iitd.ac.in/user/j/jv/jvl212384/physic
Name
mod5_counter_postCTS.cap.gz
mod5_counter_postCTS.fano..
mod5_counter_postCTS.lengt..
mod5_counter_postCTS.slk
mod5_counter_postCTS.sum...
mod5_counter_postCTS.tran.g..
mod5_counter_postCTS_all.t...
mod5_counter_postCTS_all_h..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_reg2..
mod5_counter_postCTS_reg2..
mod5_counter_preCTS.cap.gz
mod5_counter_preCTS.fanou..
mod5_counter_preCTS.lengt...
mod5_counter_preCTS.slk
mod5_counter_preCTS.summ..
mod5_counter_preCTS.tran.gz
mod5_counter_preCTS_all.ta...
mod5_counter_preCTS_all_h...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_hold.slk
mod5_counter_preCTS_hold....
Follow terminal folder
Sessions Tools Macros Sftp
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
**********End: VERIFY GEOMETRY**********
*** verify geometry (CPU: 0:00:00.1 MEM: 109.6M)
innovus 8> VERIFY_CONNECTIVITY use new engine.
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Oct 17 17:57:50 2021
Design Name: mod5_counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (19.4000, 15.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets
Begin Summary
Found no problems or warnings.
End Summary
End Time: Sun Oct 17 17:57:50 2021
Time Elapsed: 0:00:00.0
******** End: VERIFY CONNECTIVITY ********
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)
innovus 8>
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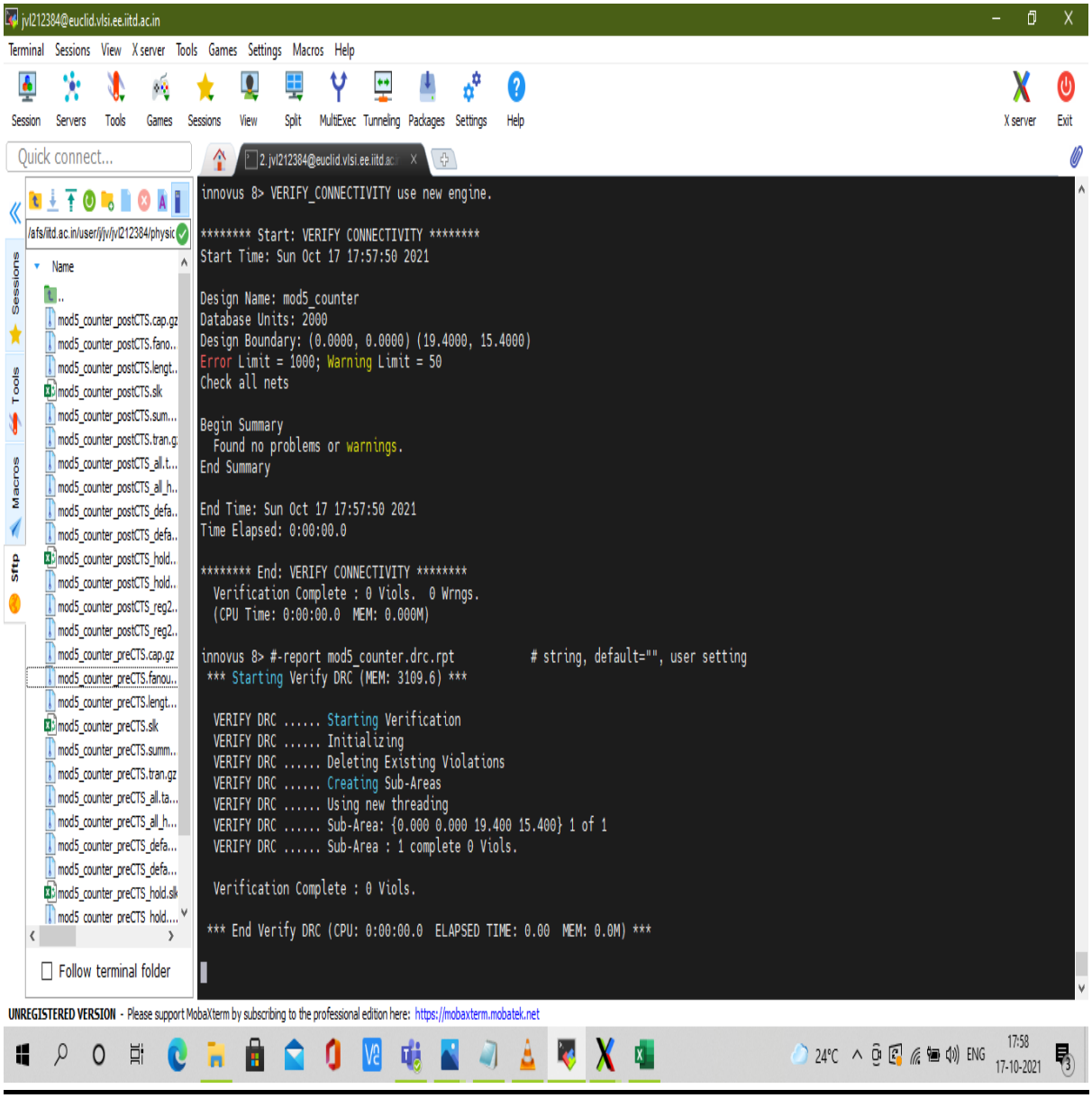
24°C ENG 17:57 17-10-2021

VERIFY DRC


Verify DRC
Basic
Advanced
Verification Area
Entire area
Specify
X1:
0
Y1:
0
X2:
0
Y2:
0
Layer Range:
Bottom Layer:
Top Layer:
Disable Rules
Color
Cut Spacing
Enclosure
EOL Spacing
Min Area
Min Cut
Min Step
Protrusion
OK
Apply
Cancel
Help


jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
2. jvl212384@euclid.vlsi.ee.iitd.ac
/afs/iitd.ac.in/user/j/jv/jvl212384/physic
Name
mod5_counter_postCTS.cap.gz
mod5_counter_postCTS.fano..
mod5_counter_postCTS.lengt..
mod5_counter_postCTS.slk
mod5_counter_postCTS.sum...
mod5_counter_postCTS.tran.g
mod5_counter_postCTS_all.t...
mod5_counter_postCTS_all_h..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_defa..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_hold..
mod5_counter_postCTS_reg2..
mod5_counter_postCTS_reg2..
mod5_counter_preCTS.cap.gz
mod5_counter_preCTS.fanou..
mod5_counter_preCTS.lengt...
mod5_counter_preCTS.slk
mod5_counter_preCTS.summ..
mod5_counter_preCTS.tran.gz
mod5_counter_preCTS_all.ta...
mod5_counter_preCTS_all_h...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_defa...
mod5_counter_preCTS_hold.slk
mod5_counter_preCTS_hold....
Follow terminal folder
Sessions Tools Macros Sftp
innovus 8> VERIFY_CONNECTIVITY use new engine.
******* Start: VERIFY CONNECTIVITY *******
Start Time: Sun Oct 17 17:57:50 2021
Design Name: mod5_counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (19.4000, 15.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets
Begin Summary
Found no problems or warnings.
End Summary
End Time: Sun Oct 17 17:57:50 2021
Time Elapsed: 0:00:00.0
******* End: VERIFY CONNECTIVITY *******
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)
innovus 8> #-report mod5_counter.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 3109.6) ***
VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 19.400 15.400} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***
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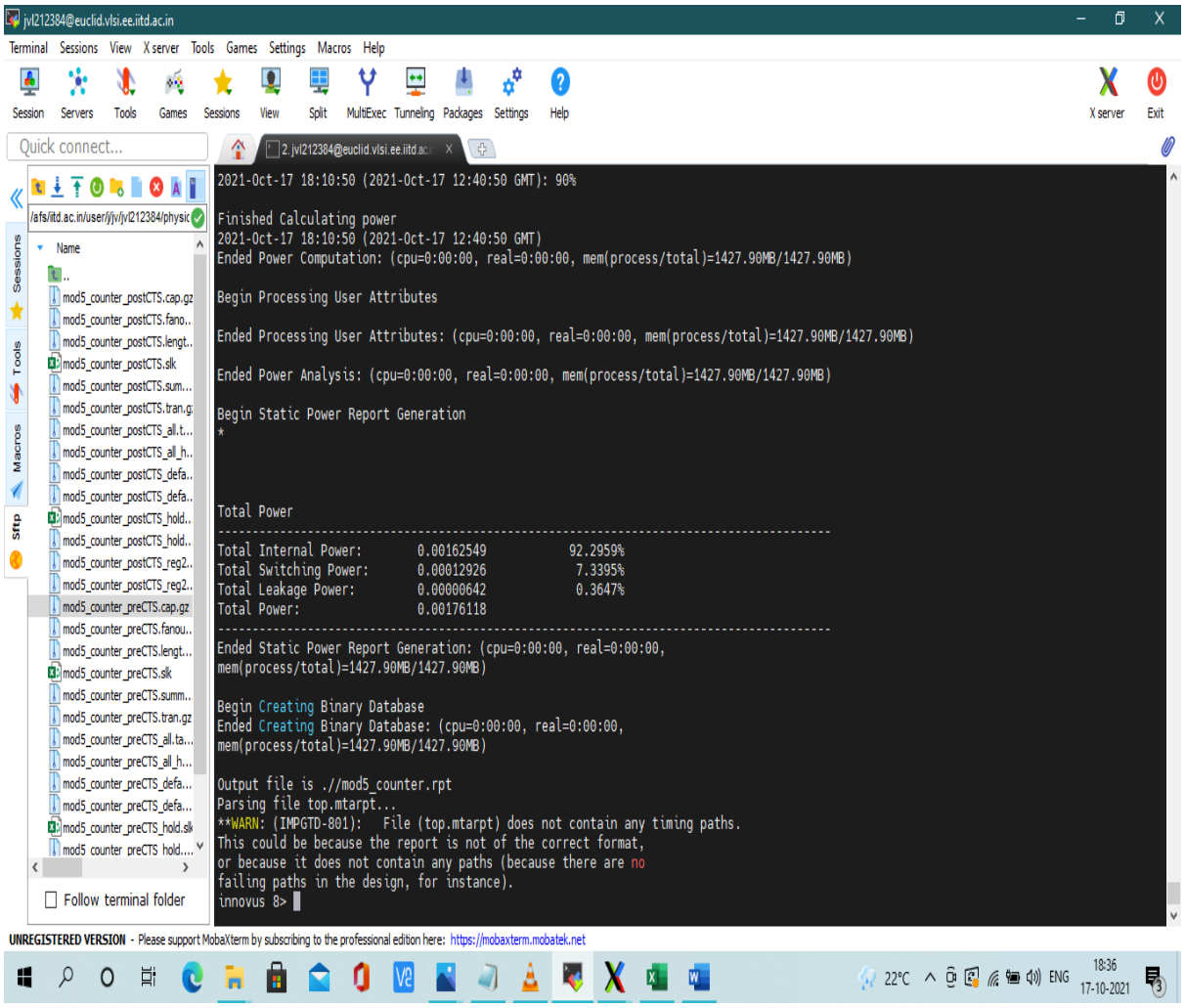
POWER ANALYSIS



NO VIOLATION