LAB REPORT

JVL2384 (PRANAV KUMAR RAI)

- **AIM**

To Design MOD5 Synchronous Up Counter using JK Flipflop

- **PROCEDURE**

First of all, made schematic and layout of INVERTER

Then of

NAND2

AND2

NAND3

SR LATCH

JK FF

MOD_5_SYNCHRONOUS_UP_COUNTER

Simulated each circuit

Cleared all DRC error of each circuit

Cleared LVS error of each circuit

I have attached the Schematic, layout, Simulation, DRC, LVS, PEX reports.

- **RESULTS**

Frequency of operation 250Mhz

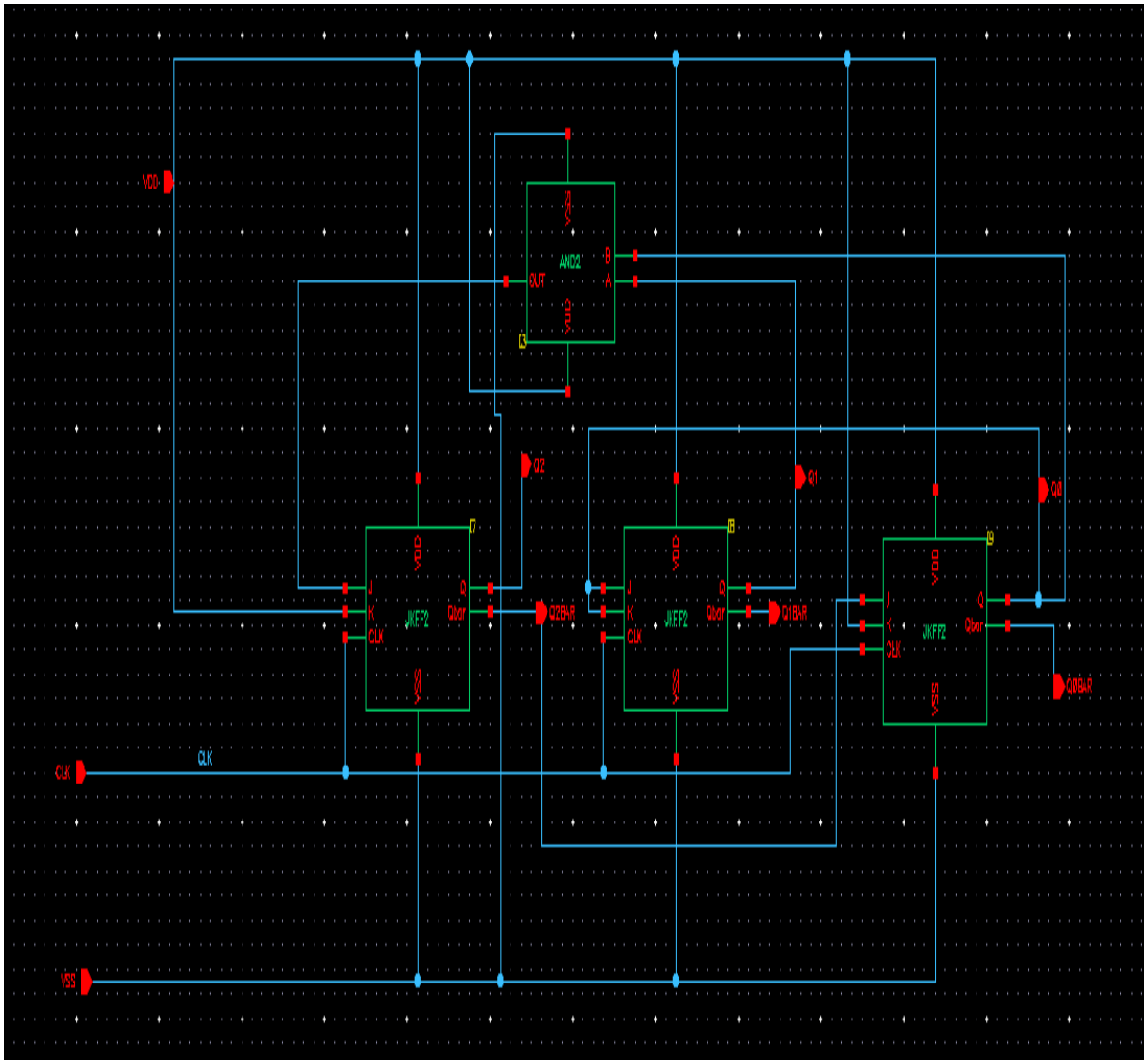
Counter input CLK

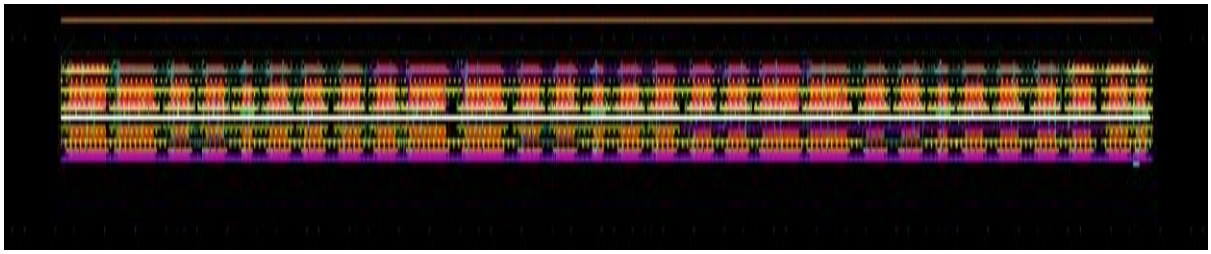
Counter Output Q2 Q1 Q0

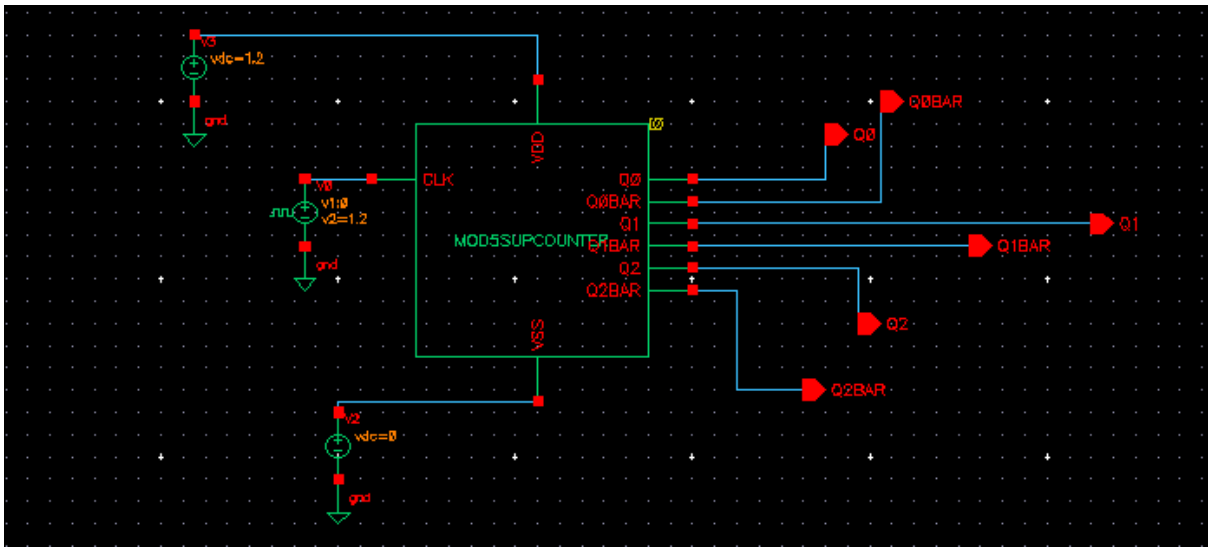
Different states of counter

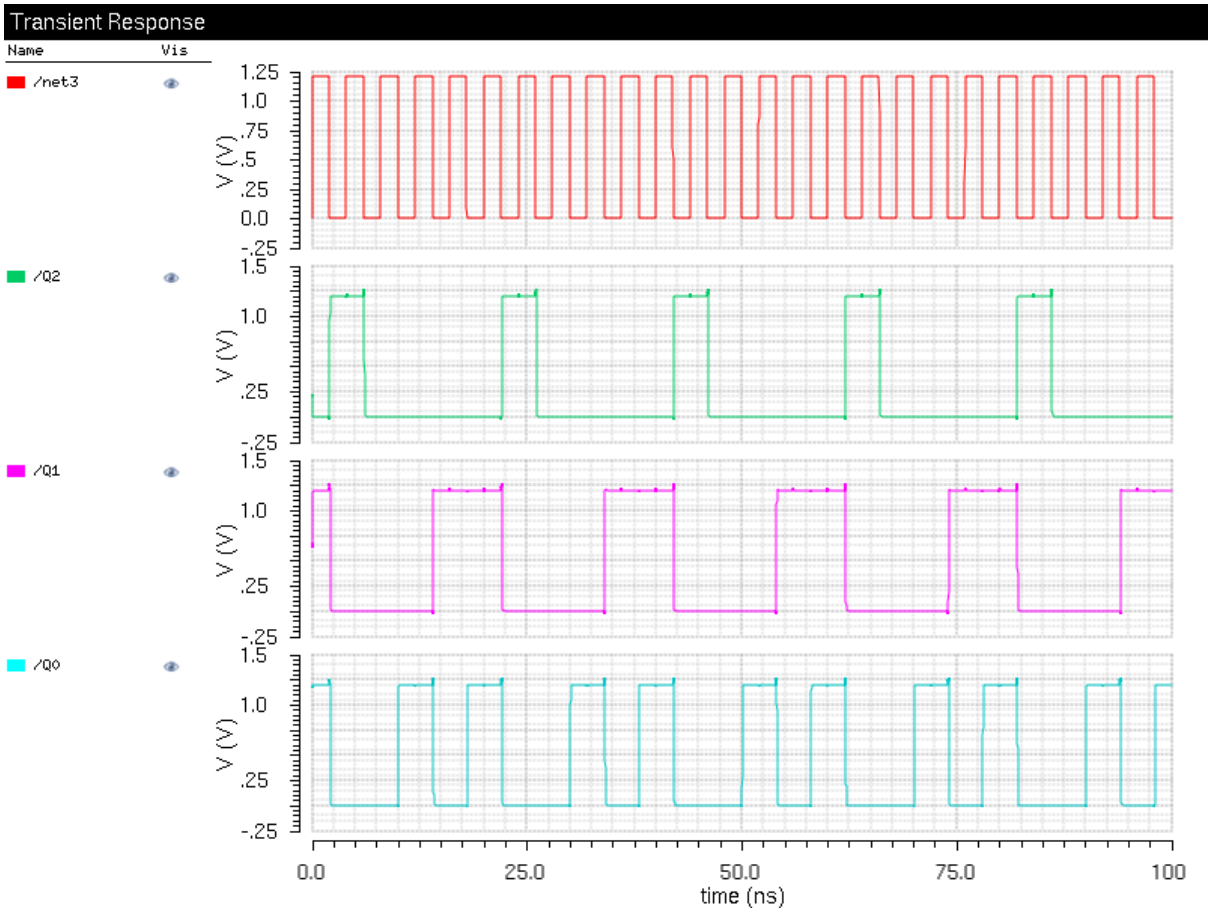
000 001 010 011 100 000 001 so on

Counter Schematic Symbol Simulation Layout






VDD
vdc=1.2
gnd
CLK
Q0
Q0BAR
Q1
Q1BAR
Q2
Q2BAR
MOD5SUPCOUNTER
VSS
vdc=0


Transient Response
Name
Vis
/net3
/Q2
/Q1
/Q0
V (V)
1.25
1.0
.75
.5
.25
0.0
-.25
1.5
0.0
25.0
50.0
75.0
100
time (ns)