

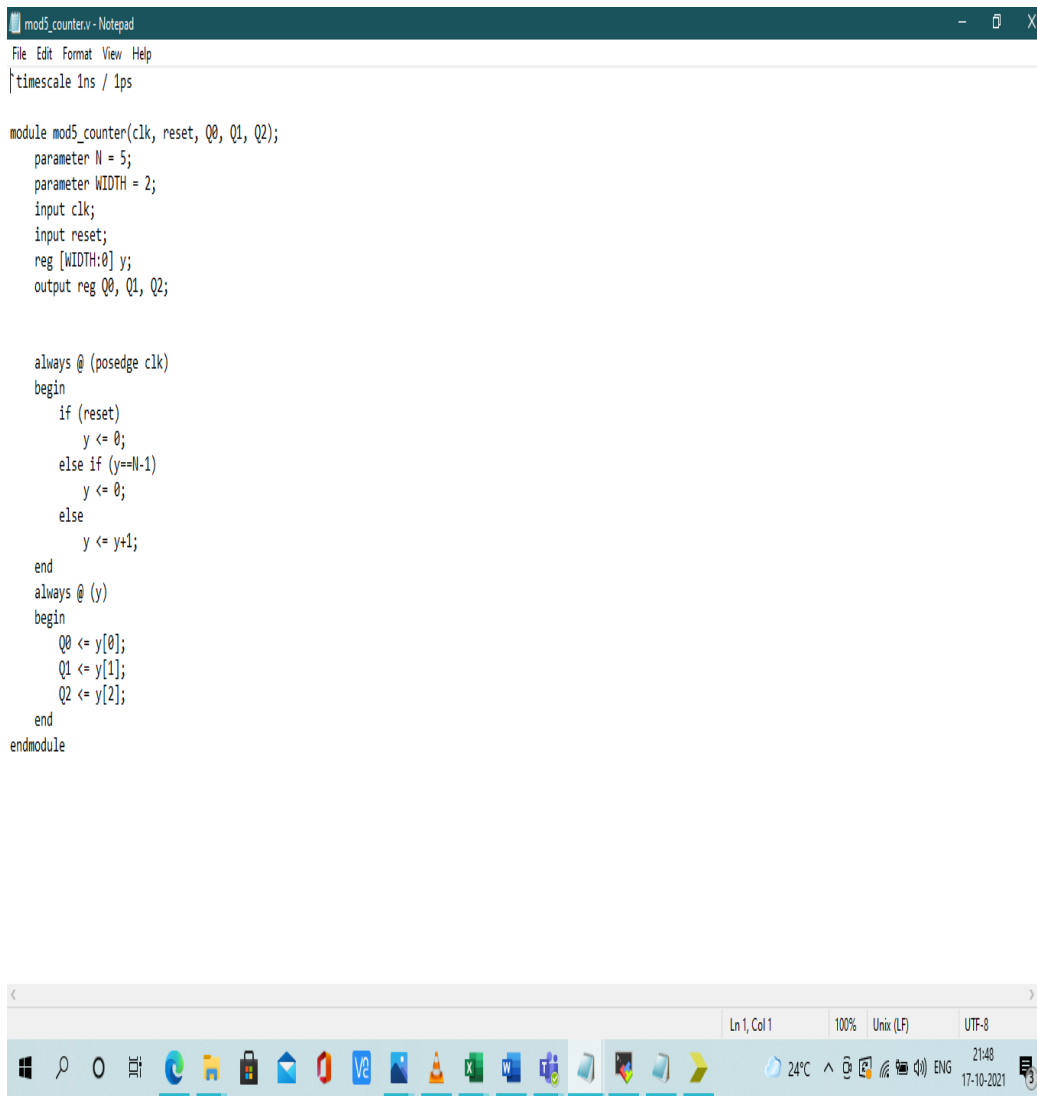
LAB REPORT

Pranav Kumar Rai

<https://github.com/pranavrai1995iit/2021jvl2384/tree/main/Lab%20Report2>

Physical Design of MOD_S_UP_COUNTER

Verilog Code-



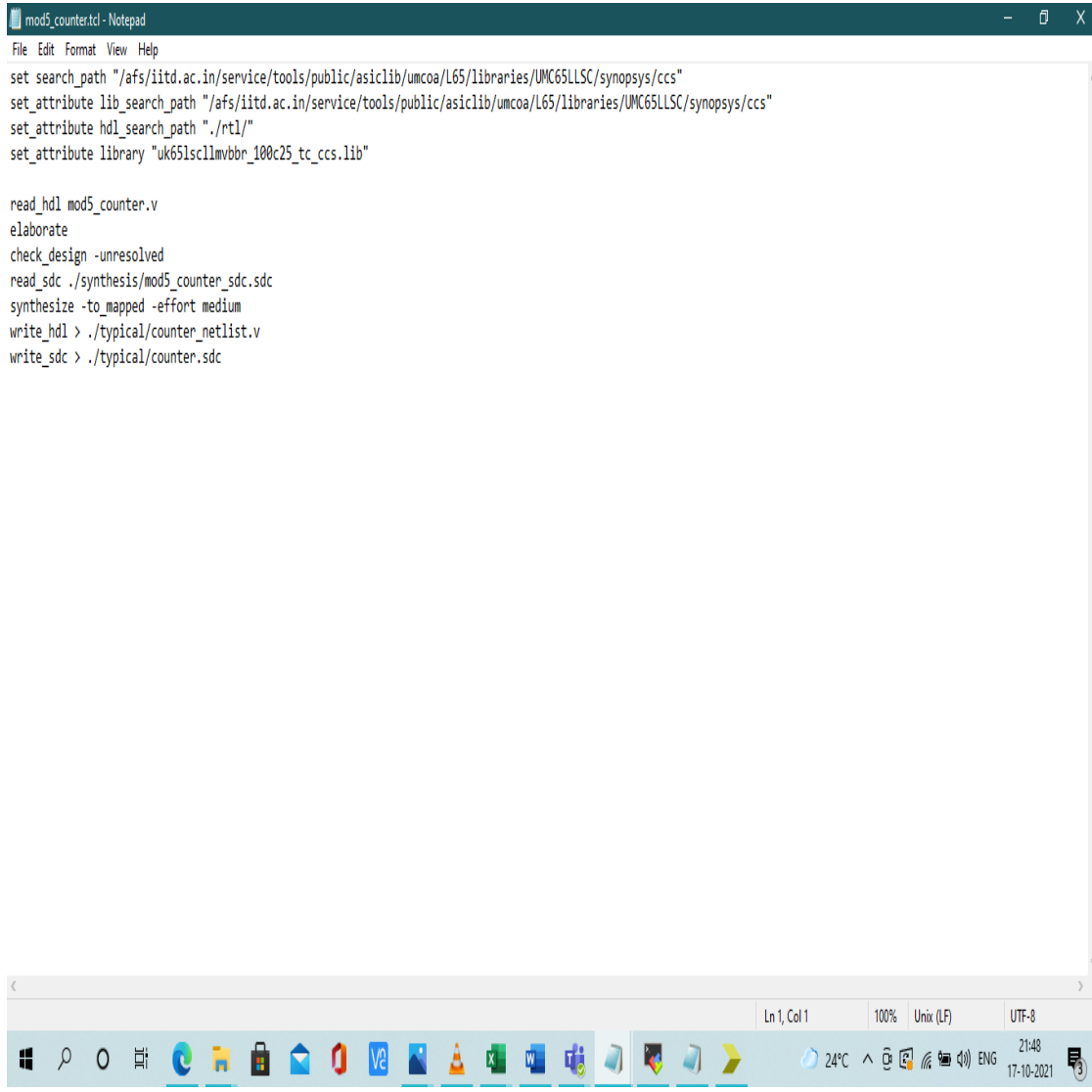
```
mod5_counter.v - Notepad
File Edit Format View Help
| timescale 1ns / 1ps

module mod5_counter(clk, reset, Q0, Q1, Q2);
    parameter N = 5;
    parameter WIDTH = 2;
    input clk;
    input reset;
    reg [WIDTH:0] y;
    output reg Q0, Q1, Q2;

    always @ (posedge clk)
    begin
        if (reset)
            y <= 0;
        else if (y==N-1)
            y <= 0;
        else
            y <= y+1;
    end
    always @ (y)
    begin
        Q0 <= y[0];
        Q1 <= y[1];
        Q2 <= y[2];
    end
endmodule

Ln 1, Col 1    100%    Unix (LF)    UTF-8
21:48
17-10-2021
```

TCL File



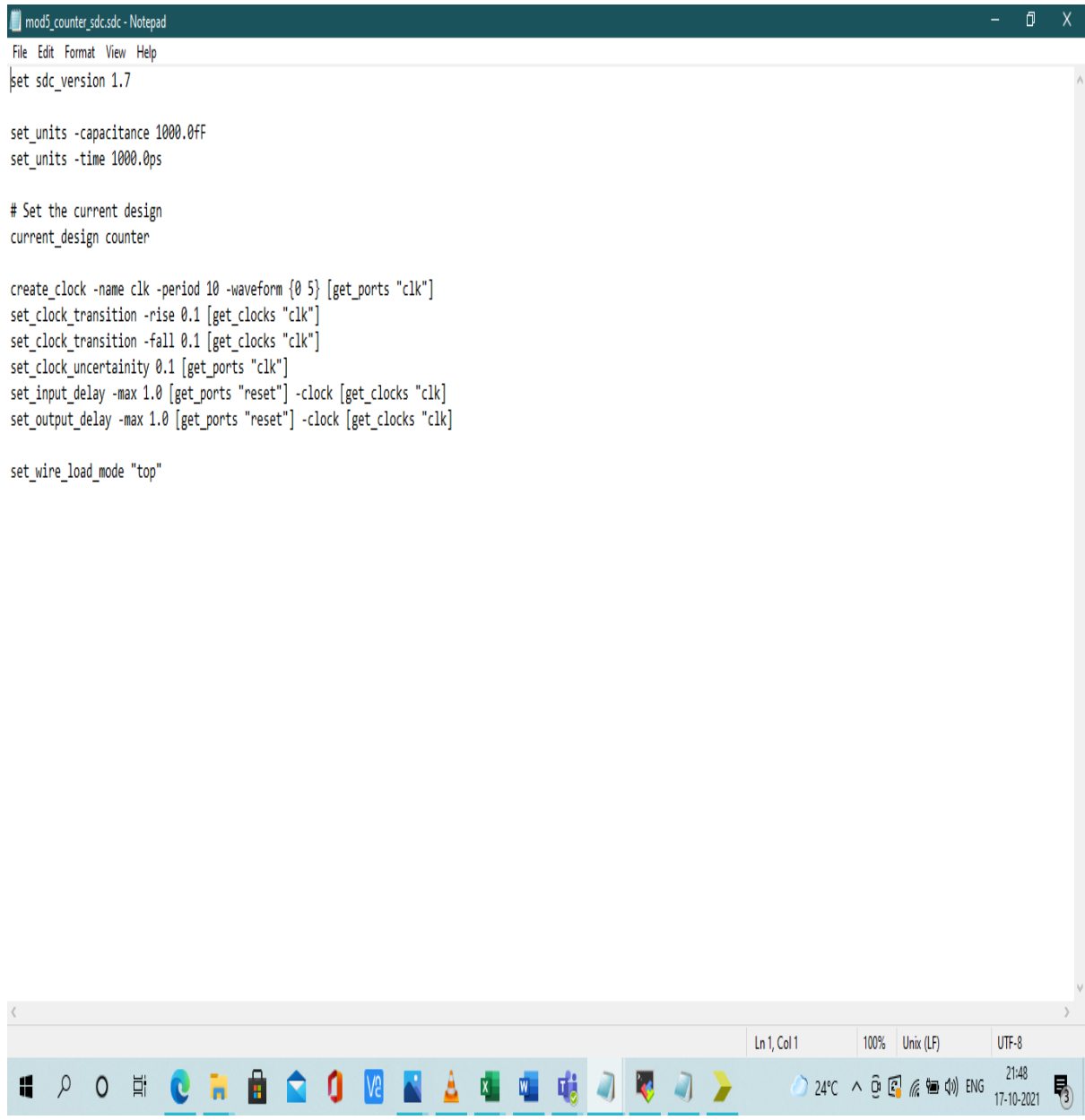
```
mod5_counter.tcl - Notepad
File Edit Format View Help
set search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute lib_search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute hdl_search_path "./rtl/"
set_attribute library "uk65lsc1lmvbb_100c25_tc_ccs.lib"

read_hdl mod5_counter.v
elaborate
check_design -unresolved
read_sdc ./synthesis/mod5_counter.sdc
synthesize -to_mapped -effort medium
write_hdl > ./typical/counter_netlist.v
write_sdc > ./typical/counter.sdc
```

Ln 1, Col 1 100% Unix (LF) UTF-8

24°C 21:48 17-10-2021

SDC File



```
mod5_counter_sdc.sdc - Notepad
File Edit Format View Help
set sdc_version 1.7

set_units -capacitance 1000.0fF
set_units -time 1000.0ps

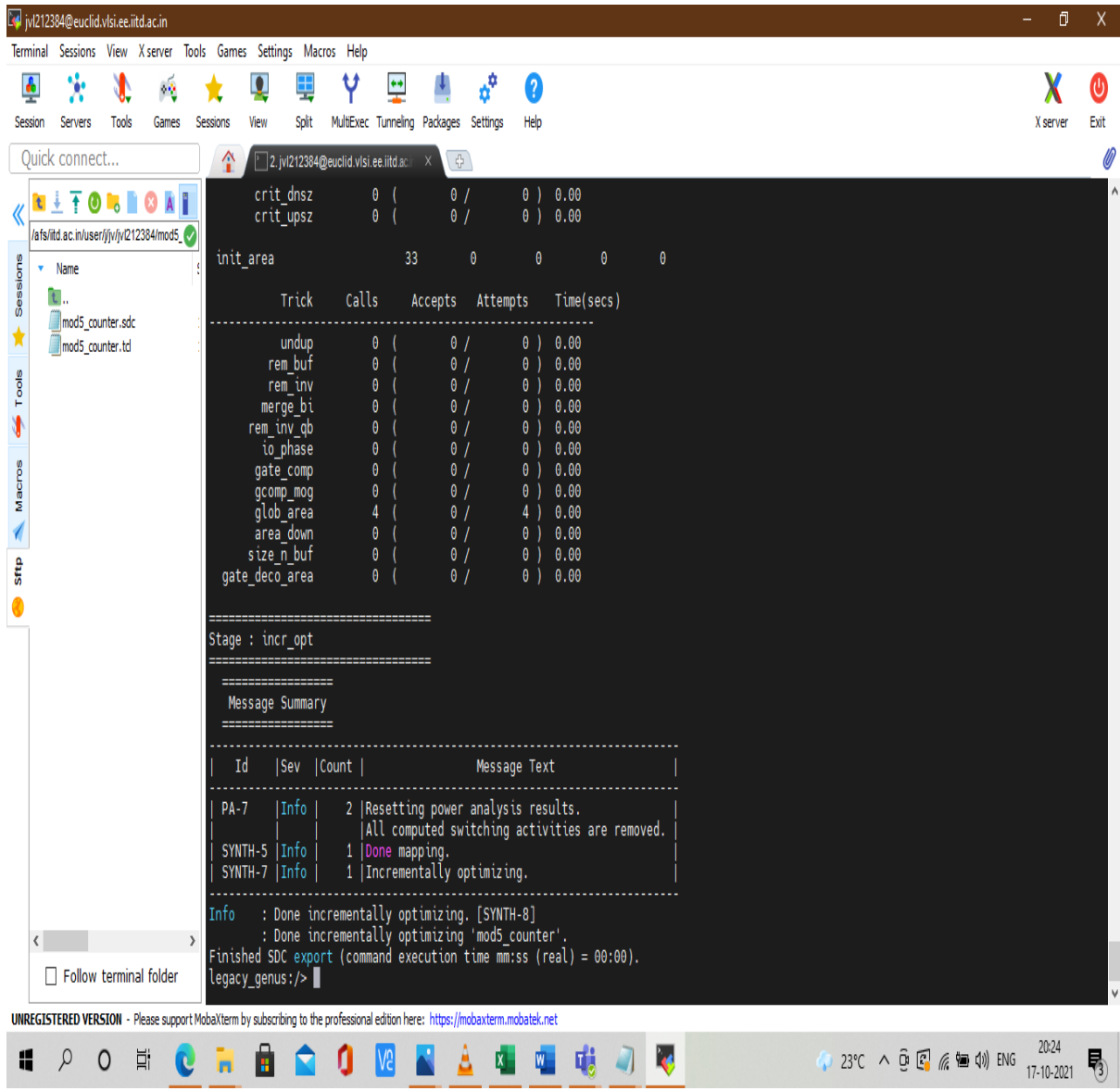
# Set the current design
current_design counter

create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.1 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]

set_wire_load_mode "top"

Ln 1, Col 1 100% Unix (LF) UTF-8
24°C 21:48 17-10-2021
```

SYNTHESIS USING GENUS TOOL



Terminal window showing the execution of the GENUS tool. The terminal output includes statistics, a table of tricks, and a message summary.

```
jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
/a/s/iitd.ac.in/user/jvl212384/mod5
Name
mod5_counter.sdc
mod5_counter.td
Sftp
Follow terminal folder
```

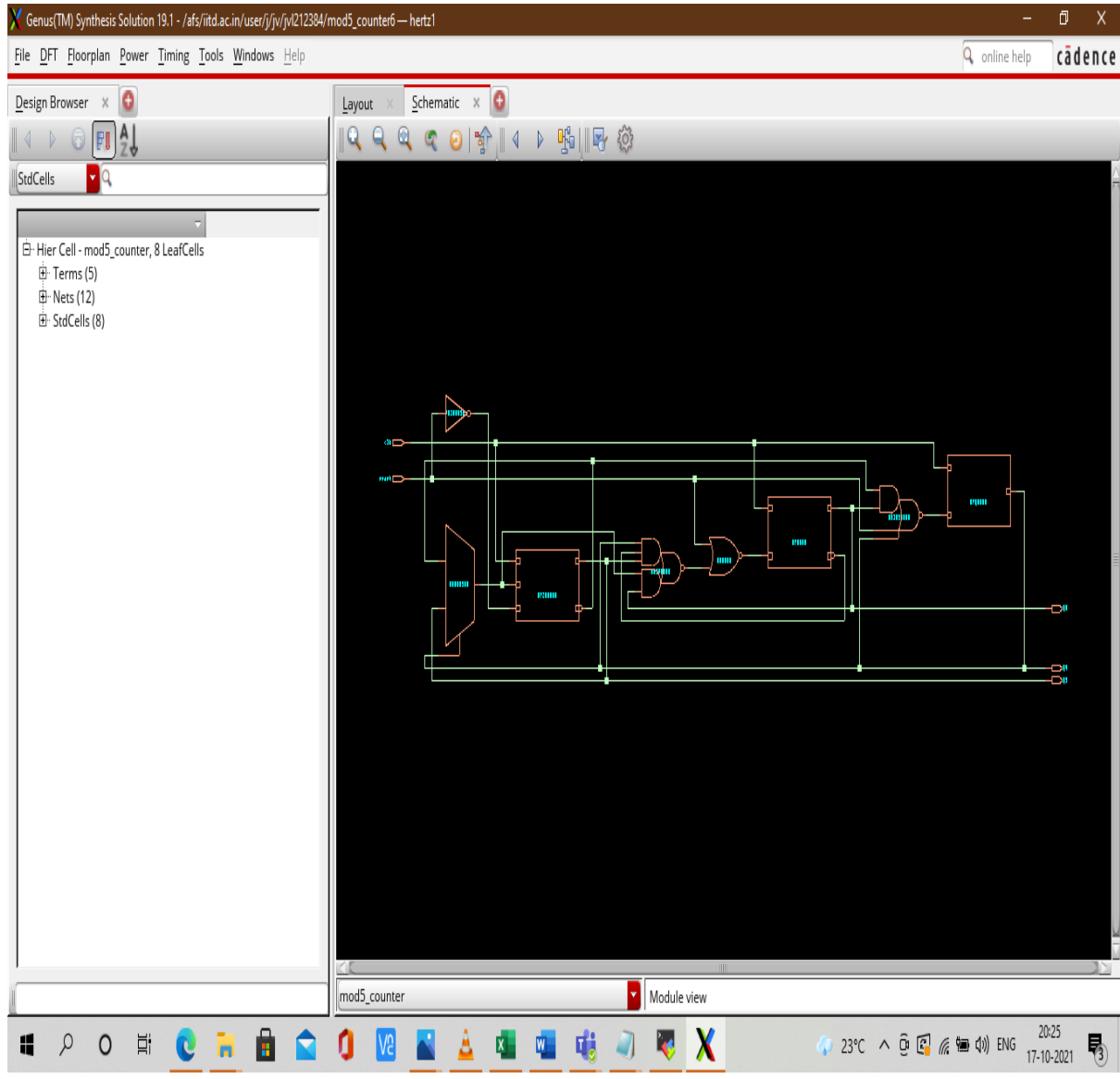
Trick	Calls	Accepts	Attempts	Time(secs)
undup	0	0	0	0.00
rem_buf	0	0	0	0.00
rem_inv	0	0	0	0.00
merge_bi	0	0	0	0.00
rem_inv_gb	0	0	0	0.00
io_phase	0	0	0	0.00
gate_comp	0	0	0	0.00
gcomp_mog	0	0	0	0.00
glob_area	4	0	4	0.00
area_down	0	0	0	0.00
size_n_buf	0	0	0	0.00
gate_deco_area	0	0	0	0.00

```
crit_dnsz 0 ( 0 / 0 ) 0.00
crit_upsz 0 ( 0 / 0 ) 0.00
init_area 33 0 0 0 0
Stage : incr_opt
Message Summary
Id | Sev | Count | Message Text
PA-7 | Info | 2 | Resetting power analysis results.
SYNTH-5 | Info | 1 | Done mapping.
SYNTH-7 | Info | 1 | Incrementally optimizing.
Info : Done incrementally optimizing. [SYNTH-8]
Info : Done incrementally optimizing 'mod5_counter'.
Finished SDC export (command execution time mm:ss (real) = 00:00).
legacy_genus:/>
```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

23°C 20:24 17-10-2021

GATE LEVEL NETLIST



TIMING ANALYSIS

Terminal window showing the output of the 'report_timing' command in the legacy_genus tool. The output includes a warning about timing problems, generation details, and a table of timing data for various pins and signals.

```
legacy_genus:/> gui_show
legacy_genus:/> report_timing
Warning : Timing problems have been detected in this design. [TIM-11]
: The design is 'mod5_counter'.
: Use 'check_timing_intent' or 'report_timing -lint' to report more information.
```

Generated by: Genus(TM) Synthesis Solution 19.12-s121_1
Generated on: Oct 17 2021 08:25:38 pm
Module: mod5_counter
Technology library: uk65lsc1lmvobr_100c25_tc
Operating conditions: uk65lsc1lmvobr_100c25_tc (balanced_tree)
Wireload mode: top
Area mode: timing library

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)
(clock clk)	launch					0 R
y_reg[1]/CK				100		0 R
y_reg[1]/QB	DFZRM2RA	2	2.2	29	+206	206 F
g201/A					+0	206
g201/Z	MXB2M1RA	2	2.4	101	+82	288 R
g198/B1					+0	288
g198/Z	A0I32M2R	1	1.3	77	+55	343 F
g196/B					+0	343
g196/Z	NR2M2R	1	1.3	61	+64	408 R
y_reg[2]/D	DFM2RA				+0	408
y_reg[2]/CK	setup			100	+12	420 R
(clock clk)	capture					10000 R

Cost Group : 'clk' (path_group 'clk')
Timing slack : 9580ps
Start-point : y_reg[1]/CK
End-point : y_reg[2]/D

legacy_genus:/>

POWER ANALYSIS

The screenshot shows a MobaXterm terminal window with the following content:

```
jvl212384@euclid.vlsi.ee.iitd.ac.in
Terminal Sessions View Xserver Tools Games Settings Macros Help
Sessions Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
jvl212384@euclid.vlsi.ee.iitd.ac.in
/afs/iitd.ac.in/user/jvl212384/mod5
Name
mod5_counter.sdc
mod5_counter.td
: -skip_propagation : 1
: -frequency_scaling_factor : 1.0
: -use_clock_freq : stim
: -compat : voltus
: -stim : /stim#0
: -fromGenus : 1
Info : ACTP-0001 Timing initialization started
Info : ACTP-0001 Timing initialization ended
Info : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
: option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
: flow. Ignoring frequency scaling.
Info : PWRA-0002 Voltus compat mode is set for power analysis.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
: of power analysis, ignored this option.
Info : PWRA-0002 Started 'vectorless' power computation.
Info : PWRA-0002 Finished power computation.
Info : PWRA-0007 [PwrInfo] Completed successfully.
: Info=9, Warn=2, Error=0, Fatal=0
Instance: /mod5_counter
Power Unit: W
PDB Frames: /stim#0/frame#0

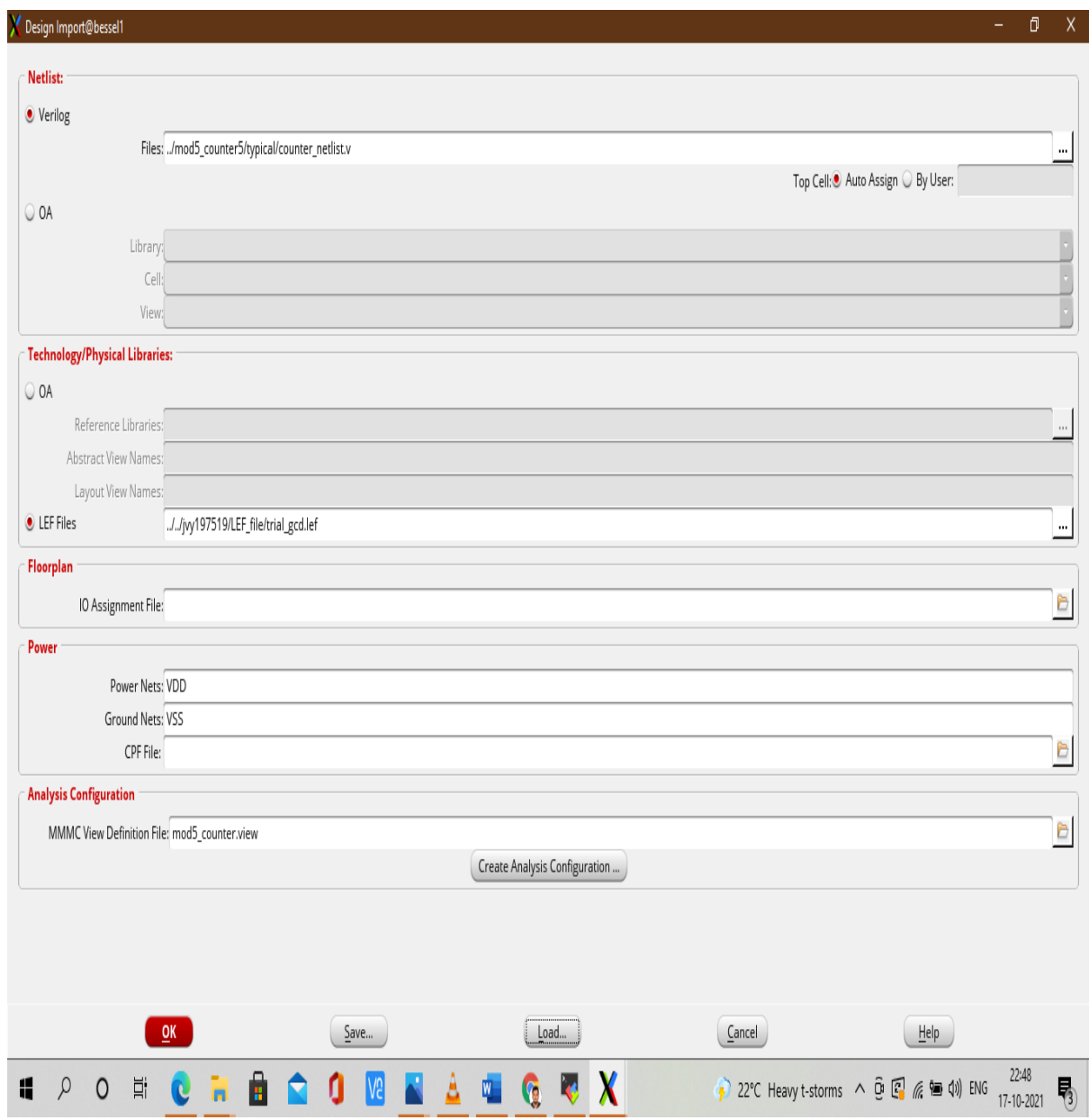
-----
Category      Leakage      Internal      Switching      Total      Row%
-----
memory        0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
register      1.02588e-09  2.01985e-06  1.41065e-07  2.16194e-06  81.89%
latch         0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
logic         3.37065e-10  1.54689e-07  9.30456e-08  2.48072e-07  9.40%
bbox          0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
clock         0.00000e+00  0.00000e+00  2.30000e-07  2.30000e-07  8.71%
pad           0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
pm            0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
-----
Subtotal      1.36294e-09  2.17454e-06  4.64111e-07  2.64001e-06  100.00%
Percentage    0.05%      82.37%      17.58%      100.00% 100.00%
-----
Legacy_genus:/>
```

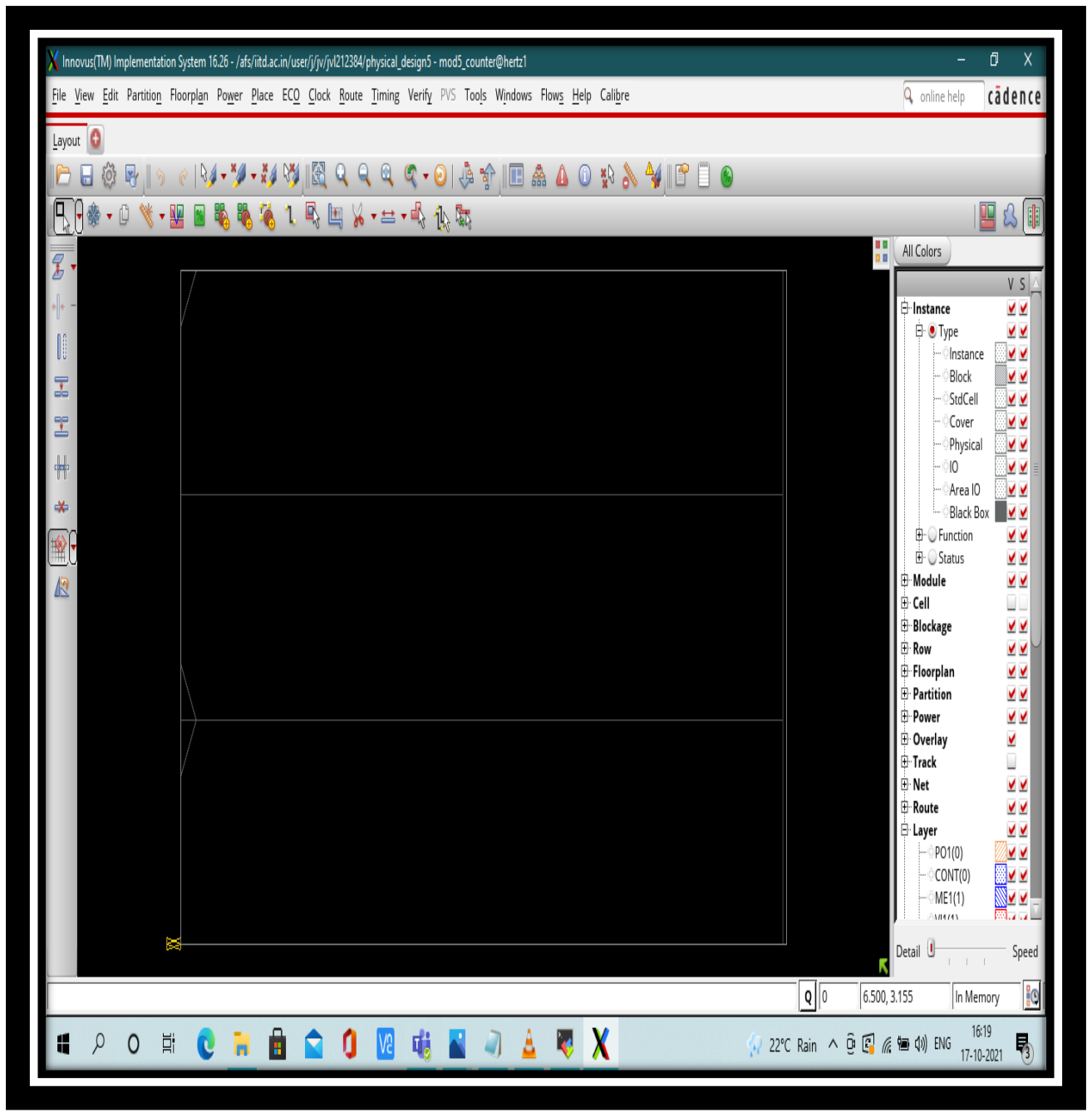
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

Windows taskbar at the bottom shows the system clock as 20:26 on 17-10-2021, with temperature at 23°C and language set to ENG.

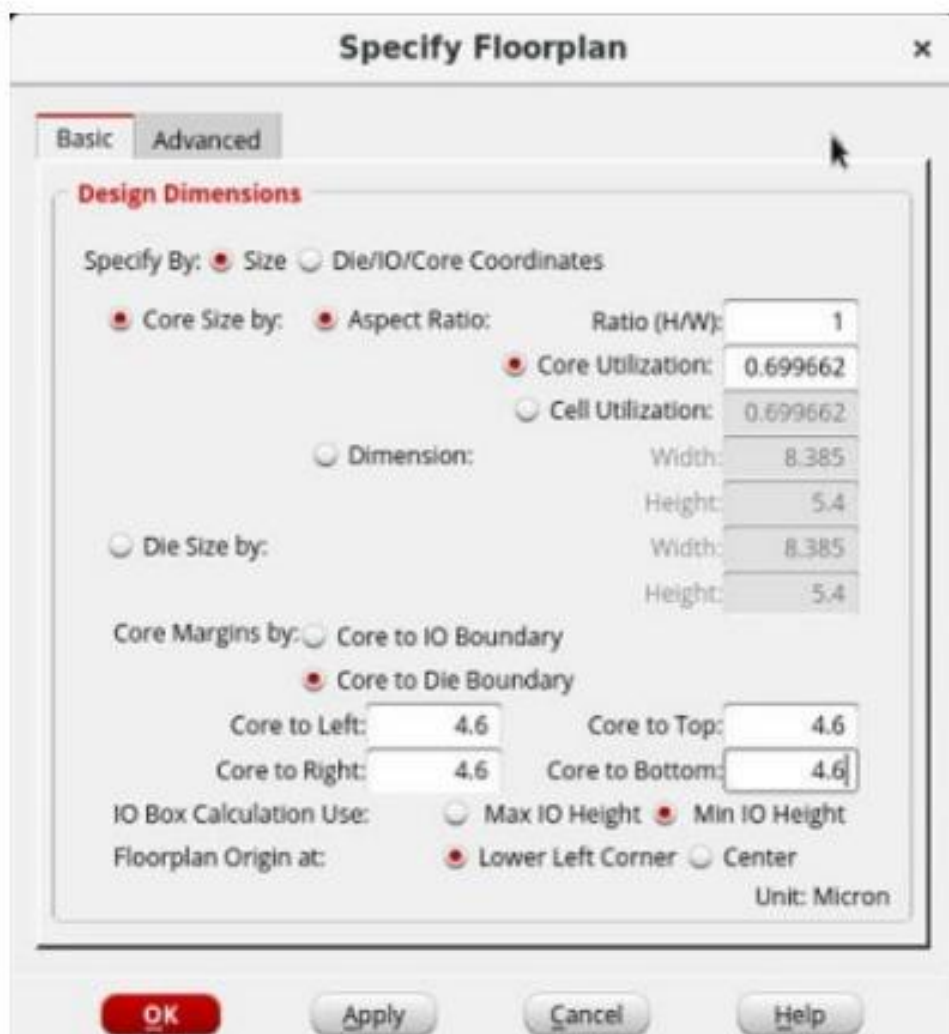
PHYSICAL DESIGN USING INNOVUS

AFTER IMPORTING THE DESIGN





FLOOR PLANNING



The image shows a 'Specify Floorplan' dialog box with two tabs: 'Basic' and 'Advanced'. The 'Basic' tab is selected. The 'Design Dimensions' section contains several options and input fields. The 'Specify By' section has two radio buttons: 'Size' (selected) and 'Die/IO/Core Coordinates'. Under 'Size', there are two sub-sections. The first sub-section has 'Core Size by:' with a radio button, 'Aspect Ratio:' with a radio button, and a 'Ratio (H/W):' input field with the value '1'. The second sub-section has 'Core Utilization:' with a radio button (selected) and 'Cell Utilization:' with a radio button. Both have input fields with the value '0.699662'. The 'Dimension:' section has a radio button and two input fields: 'Width:' with the value '8.385' and 'Height:' with the value '5.4'. The 'Die Size by:' section has a radio button and two input fields: 'Width:' with the value '8.385' and 'Height:' with the value '5.4'. The 'Core Margins by:' section has two radio buttons: 'Core to IO Boundary' and 'Core to Die Boundary' (selected). Below this are four input fields: 'Core to Left:' with the value '4.6', 'Core to Top:' with the value '4.6', 'Core to Right:' with the value '4.6', and 'Core to Bottom:' with the value '4.6'. The 'IO Box Calculation Use:' section has two radio buttons: 'Max IO Height' and 'Min IO Height' (selected). The 'Floorplan Origin at:' section has two radio buttons: 'Lower Left Corner' (selected) and 'Center'. The 'Unit: Micron' label is at the bottom right of the 'Design Dimensions' section. At the bottom of the dialog box are four buttons: 'OK' (red), 'Apply', 'Cancel', and 'Help'.

Specify Floorplan

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☒ Aspect Ratio: Ratio (H/W):

☒ Core Utilization:

☐ Cell Utilization:

☐ Dimension: Width:

Height:

☐ Die Size by: Width:

Height:

Core Margins by: ☐ Core to IO Boundary

☒ Core to Die Boundary

Core to Left: Core to Top:

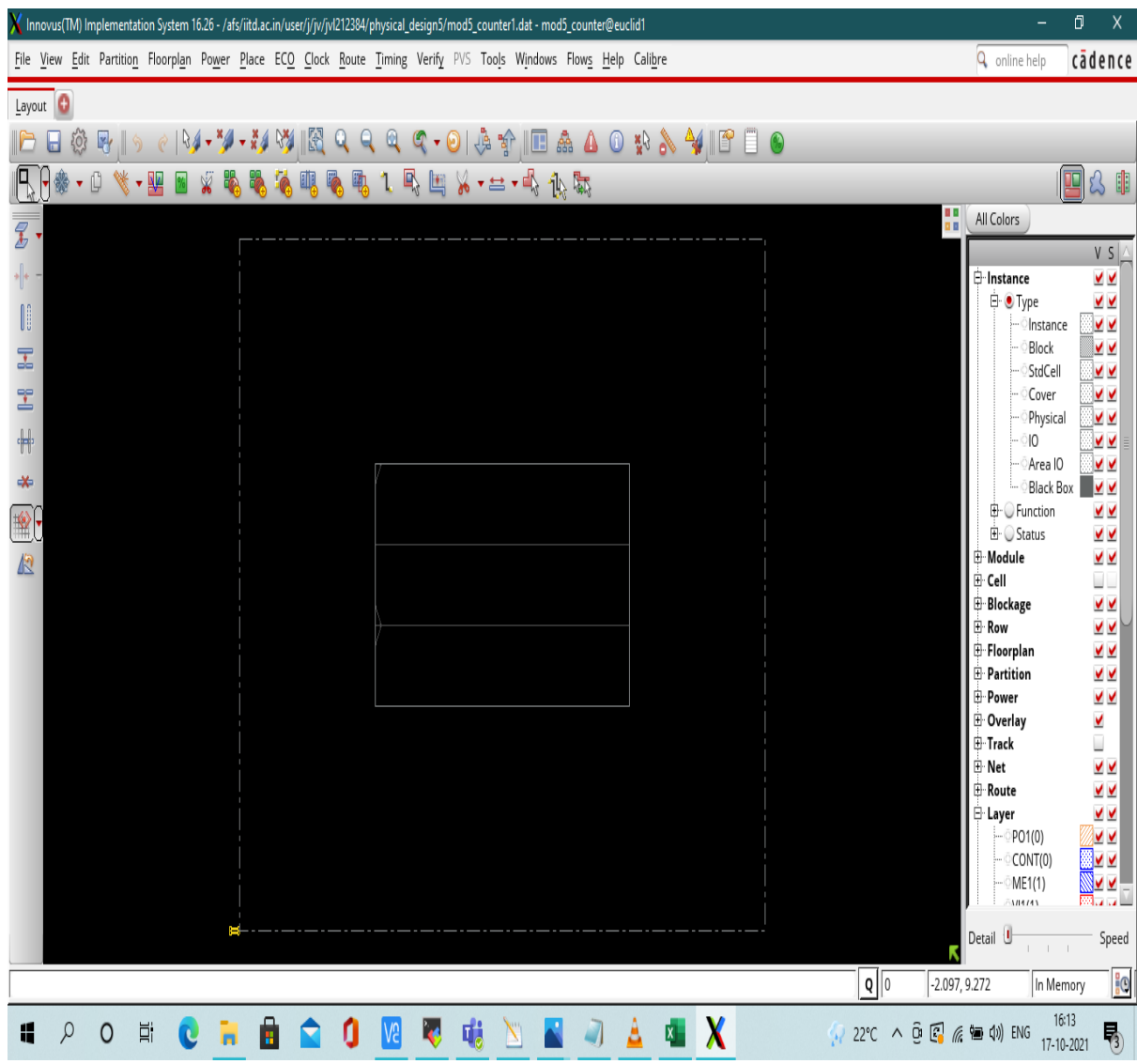
Core to Right: Core to Bottom:

IO Box Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

Unit: Micron

OK Apply Cancel Help



POWER PLANNING

ADDING RINGS

Add Rings

Basic Advanced Via Generation Mode Preview

Net(s): VDD VSS

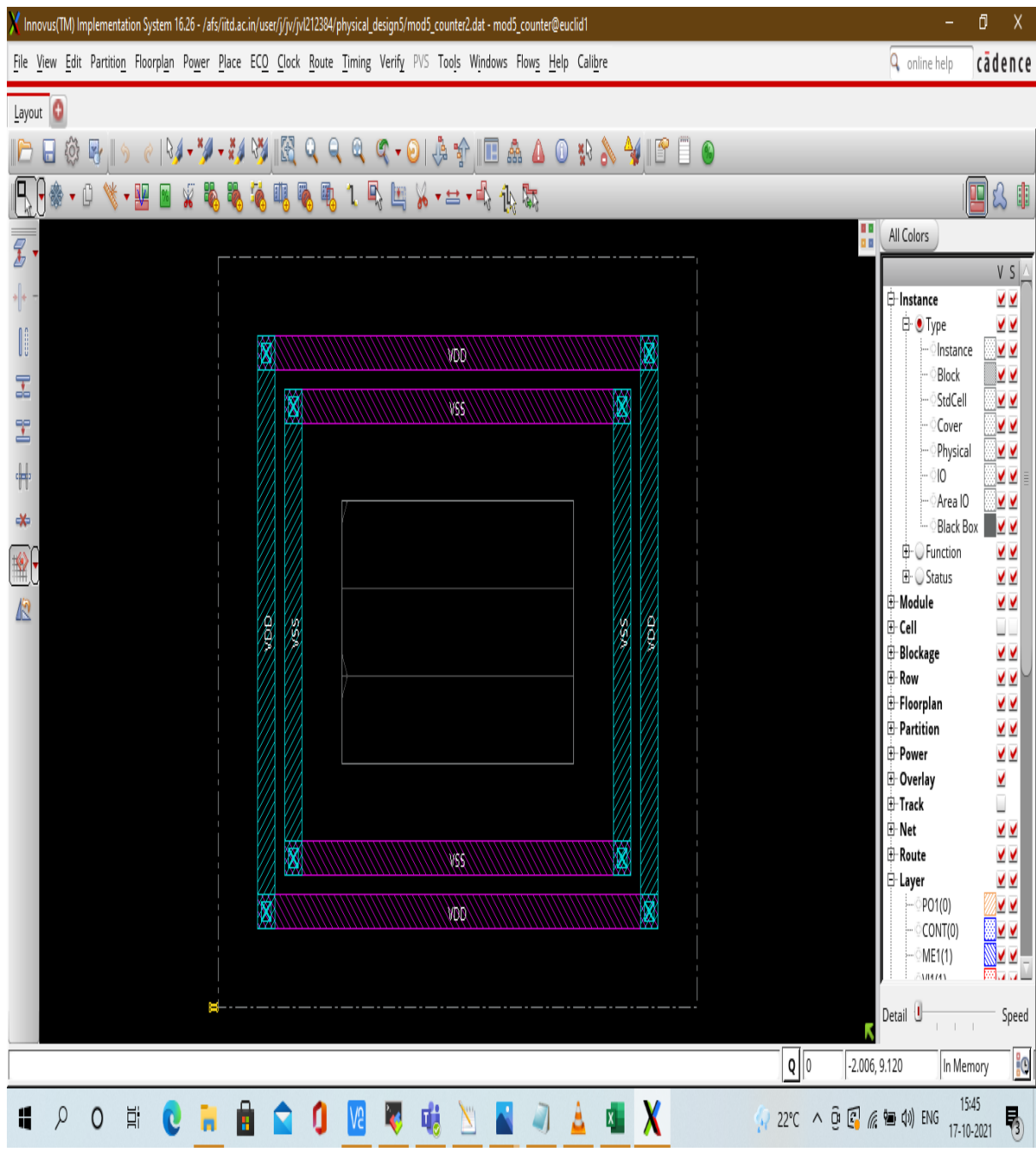
Ring Type

- ☒ Core ring(s) contouring
 - Around core boundary ☐ Exclude selected objects
- ☐ Block ring(s) around
 - Each block *
- ☐ User defined coordinates: Core ring, *

Ring Configuration

	Layer:	Width:	Spacing:	Offset:
Top:	ME7(7) H ▶	0.7	0.985	1.8
Bottom:	ME7(7) H ▶	0.7	0.985	1.8
Left:	ME8(8) V ▶	0.7	0.985	1.8
Right:	ME8(8) V ▶	0.7	0.985	1.8

☒ Offset: Center in channel



ADDING STRIPS

Add Stripes

Basic Advanced Via Generation Mode Preview

Set Configuration

Net(s): VDD VSS

Layer: ME6(6) Directions: ☒ Vertical ☐ Horizontal

Width: 0.3 Spacing: 0.4 Update

Set Pattern

☒ Set-to-set distance: 2.5 ☐ Number of sets: 1 ☐ Bumps Over *

☐ Over P/G pins Pin layer: Top pin layer * Pin Width:

☐ Master name: Selected blocks ☒ All blocks

☐ Over Physical Pins Pin layer: Top pin layer * Pin Width:

Stripe Boundary

☒ Core ring ☐ Pad ring: Outer * ☐ All domains

☐ Design boundary ☒ Create pins ☐ Each selected block/domain/fence

☐ Specify rectangular area

X1: Y1: X2: Y2:

☐ Specify rectilinear area

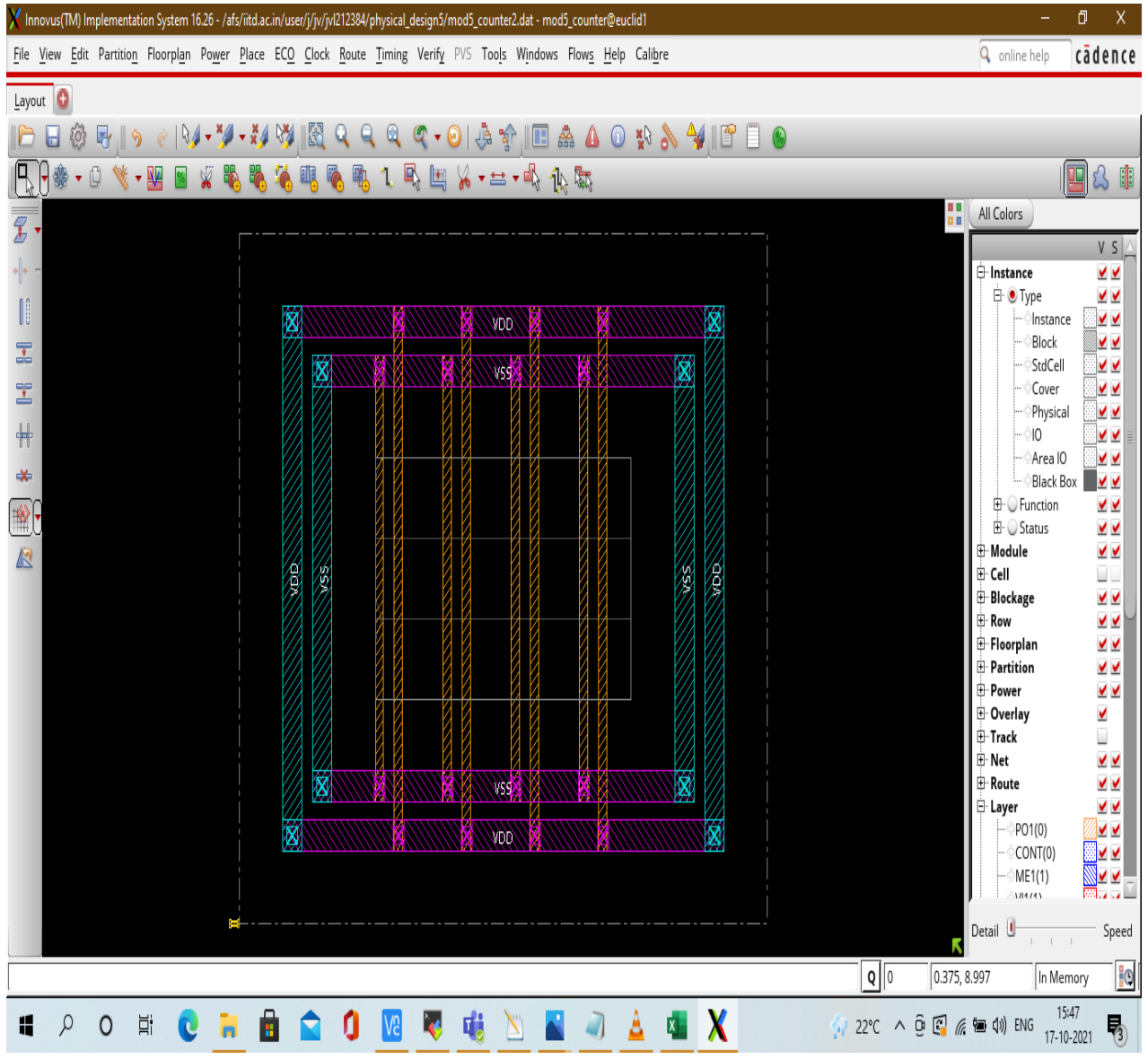
First/Last Stripe

Start from: ☒ Left ☐ Right ☐ Top ☐ Bottom

☒ Relative from core or selected area Start: 0.4 Stop:

☐ Absolute Start: Stop:

OK Apply Defaults Cancel Help



SROUTE

SRoute x

Basic Advanced Via Generation

Net(s): VDD VSS ...

SRoute

☐ Block Pins ☐ Pad Rings ☐ Floating Stripes
☐ Pad Pins ☒ Follow Pins ☐ Secondary Power Pins

Routing Control

Layer Change Control

Top Layer: ME8(8) Bottom Layer: ME1(1)

☒ Allow Jogging ☒ Allow Layer Change

☐ Specify Area

X1: Y1: 
X2: Y2: 

☐ Connect to Target Inside The Area Only

Power Domain Selection

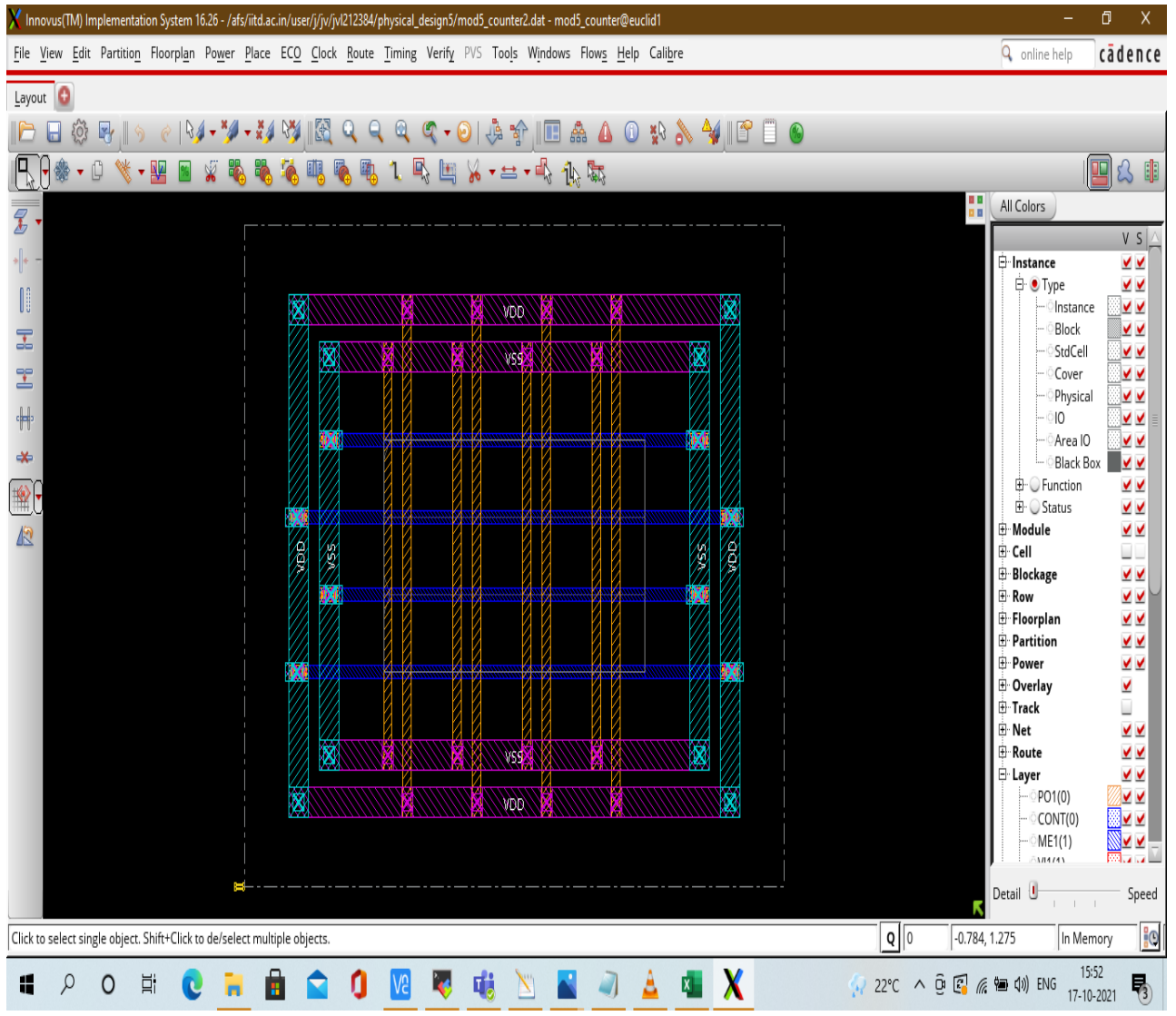
☒ All ☐ Selected

☐ Named:

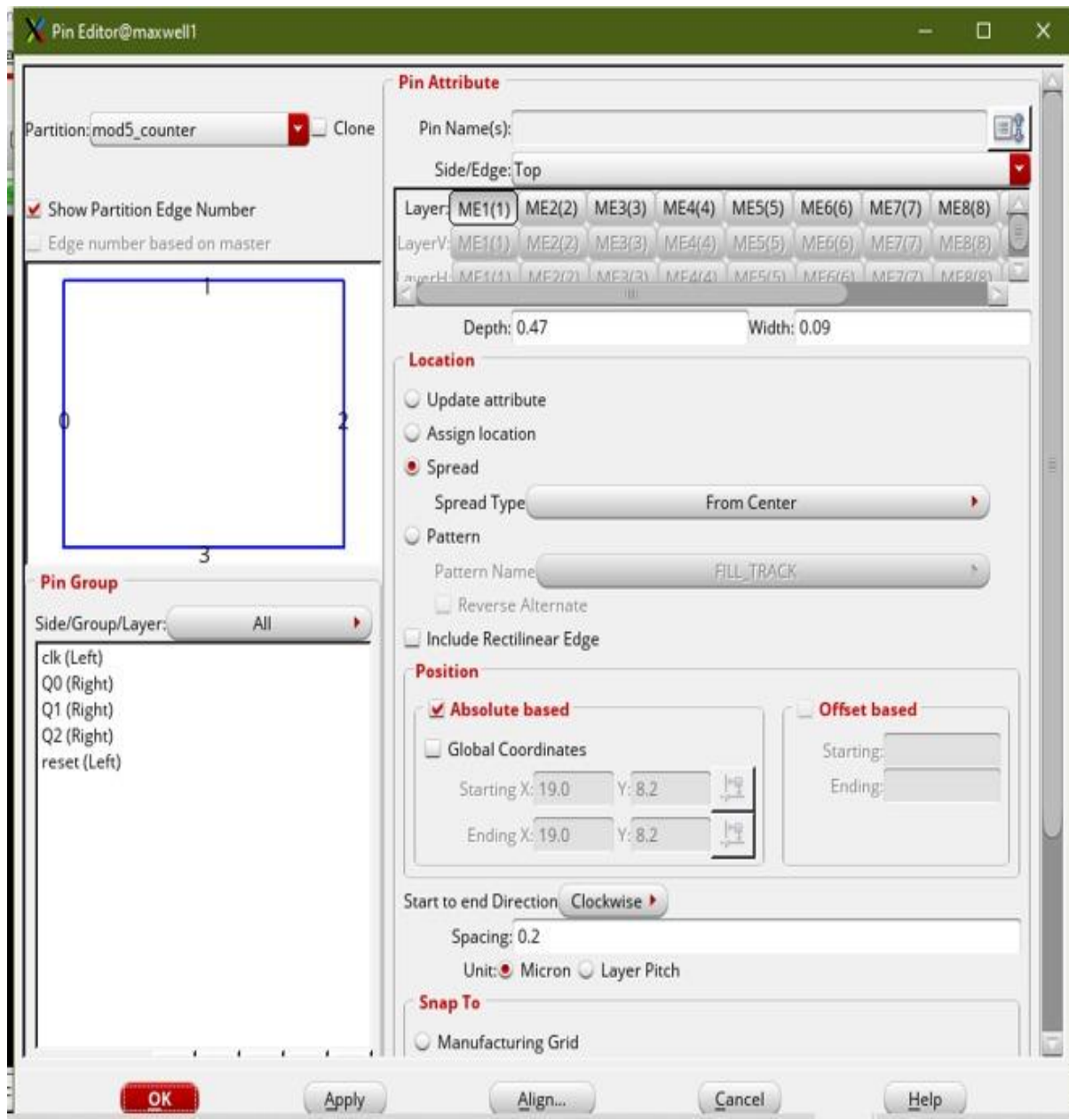
☐ Delete Existing Routes ☐ Generate Progress Messages

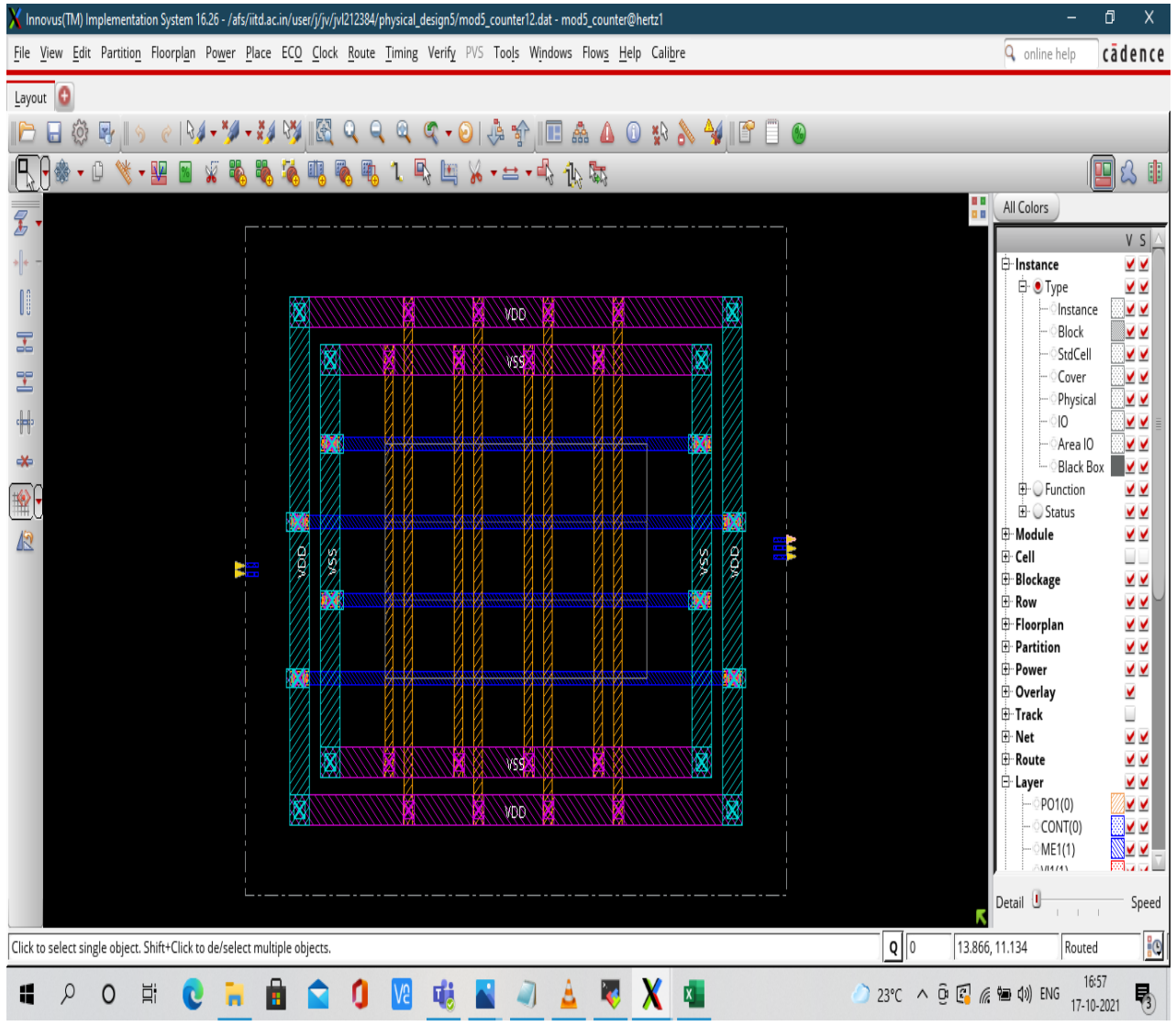
Mode Setup Target Editing Options

OK Apply Defaults Cancel Help

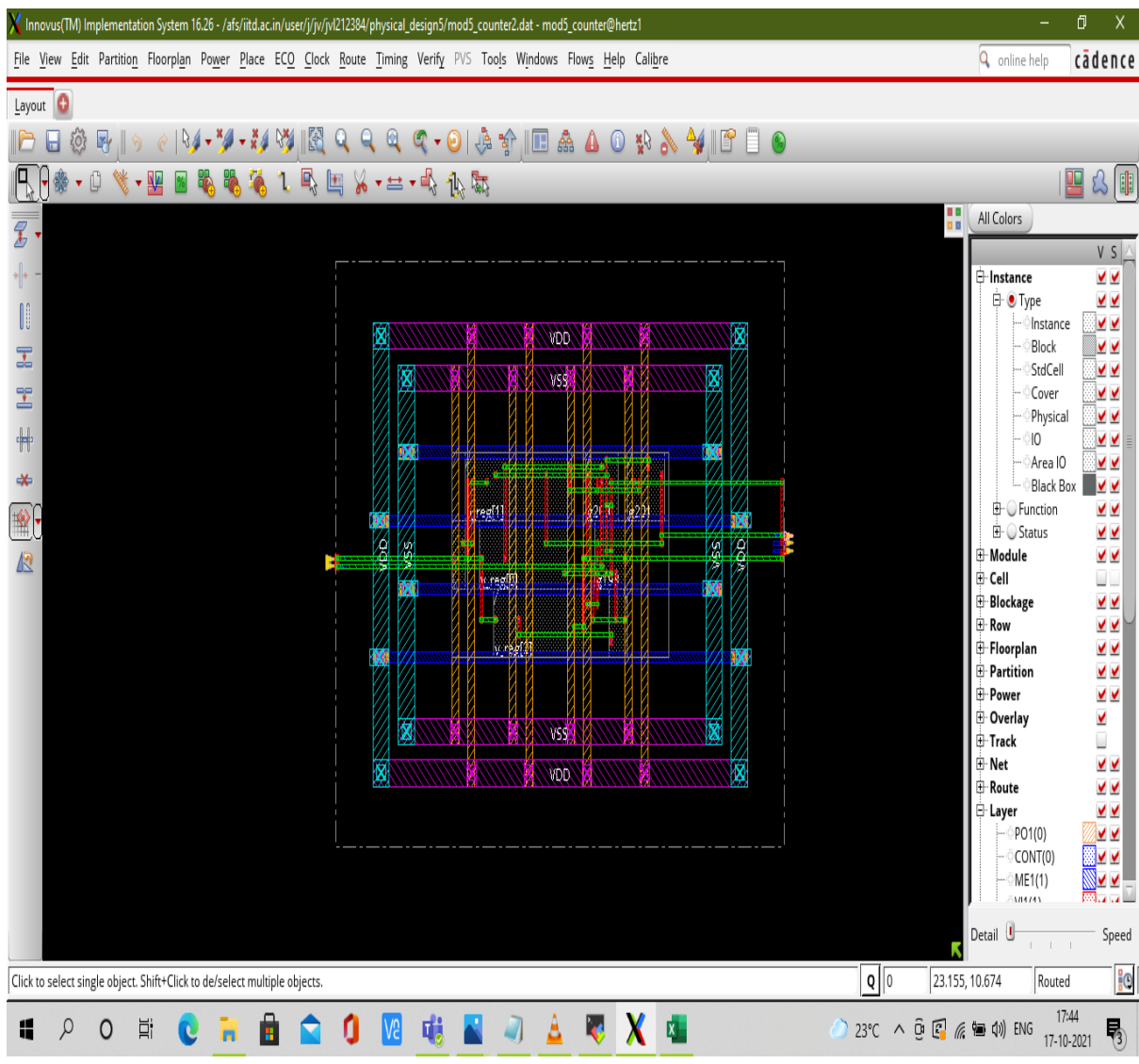


PIN PLACEMENT





STANDARD CELL PLACEMENT



Timing Analysis

×

Basic

Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☒ Pre-CTS ☐ Post-CTS ☐ Post-Route ☐ Sign-Off

Analysis Type

☒ Setup ☐ Hold

☐ Include SI

Reporting Options

Number of Paths:

50

Report file(s) Prefix:

Mod5Counter_preCTS

Output Directory:

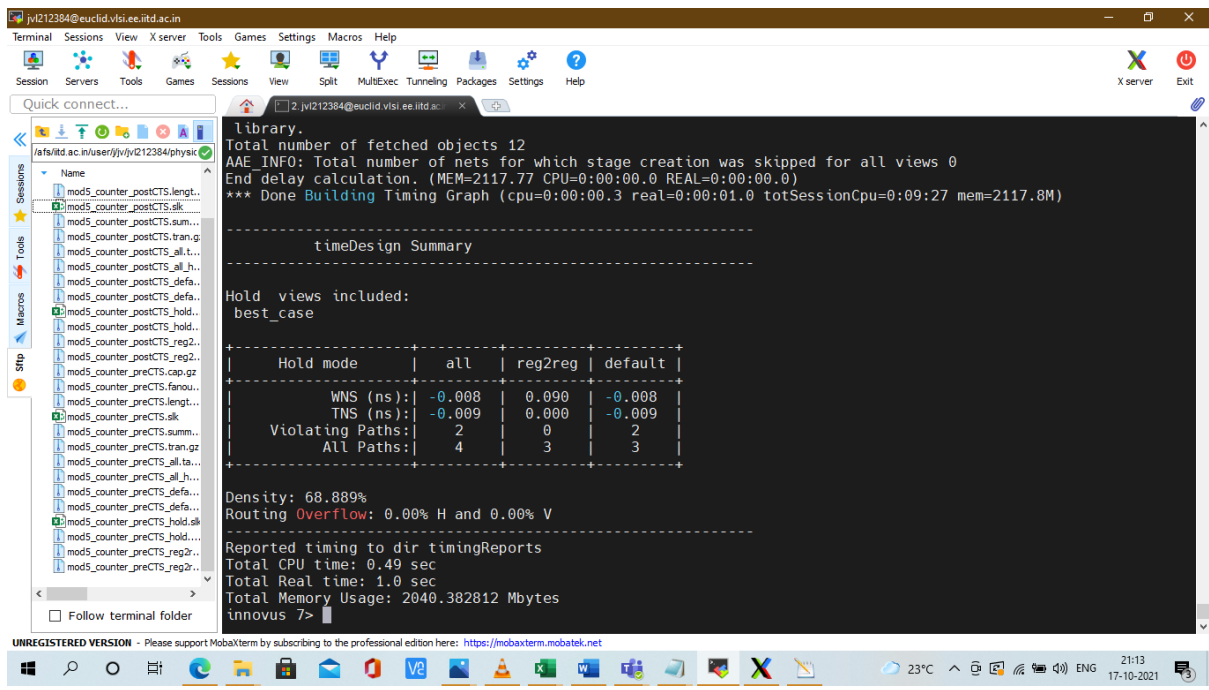
timingReports

OK

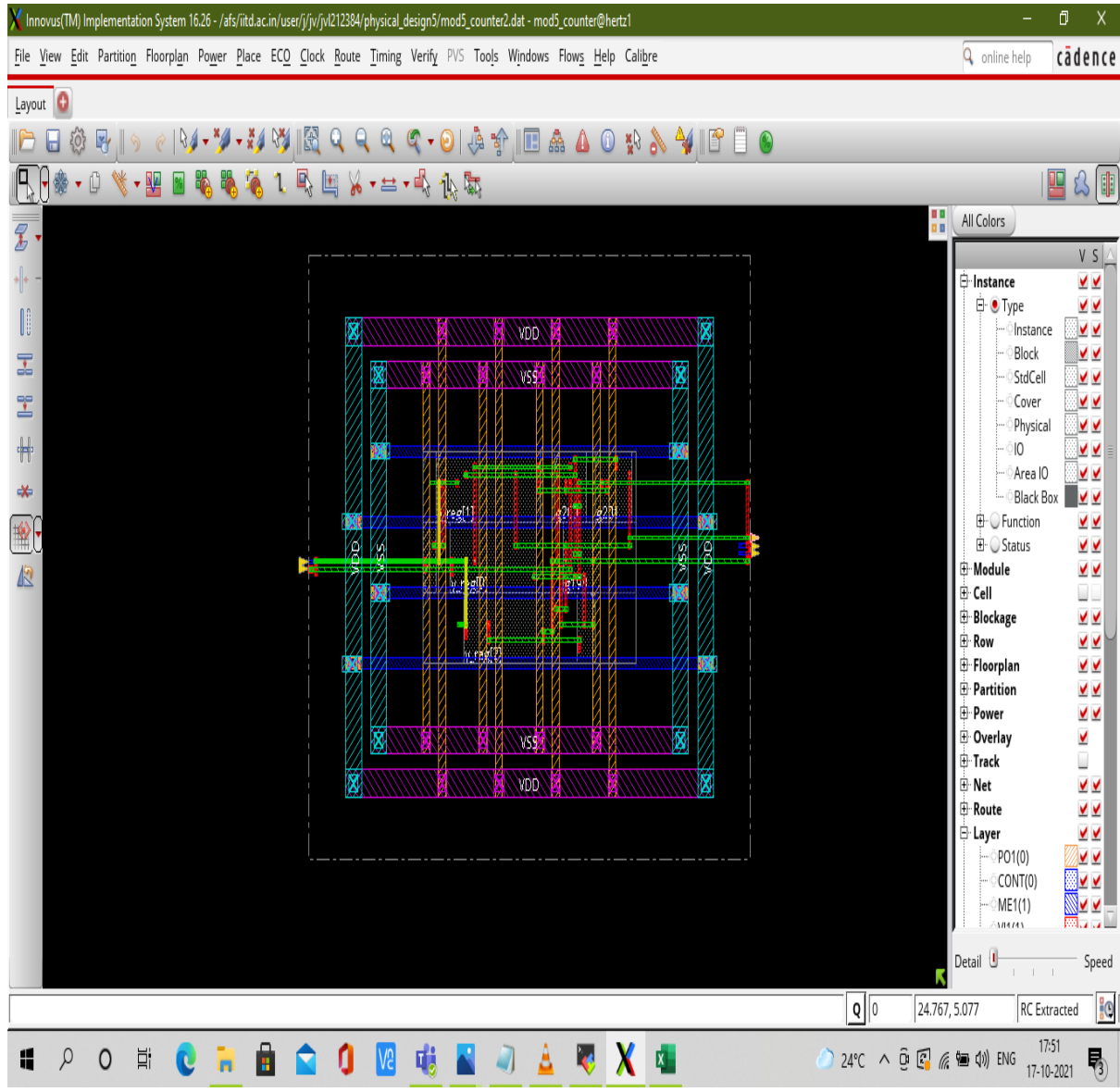
Apply

Cancel

Help



CLOCK TREE SYNTHESIS



Timing Analysis

Basic

Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place

☐ Pre-CTS

☒ Post-CTS

☐ Post-Route

☐ Sign-Off

Analysis Type

☒ Setup

☐ Hold

☐ Include SI

Reporting Options

Number of Paths:

50

Report file(s) Prefix:

Mod5Counter_postCTS

Output Directory:

timingReports

Apply

Cancel

Help

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

2 jv1212384@euclid.vlsi.ee.iitd.ac.in

timeDesign Summary

Setup views included:
worst_case

Setup mode	all	reg2reg	default
WNS (ns):	9.225	9.225	9.768
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	4	3	3

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 68.889%
Routing Overflow: 0.00% H and 0.00% V

UNREGISTERED VERSION - Please support MobaTerm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

23°C 21:13 17-10-2021

Timing Analysis

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☒ Post-CTS ☐ Post-Route ☐ Sign-Off

Analysis Type

☐ Setup ☒ Hold ☐ Include SI

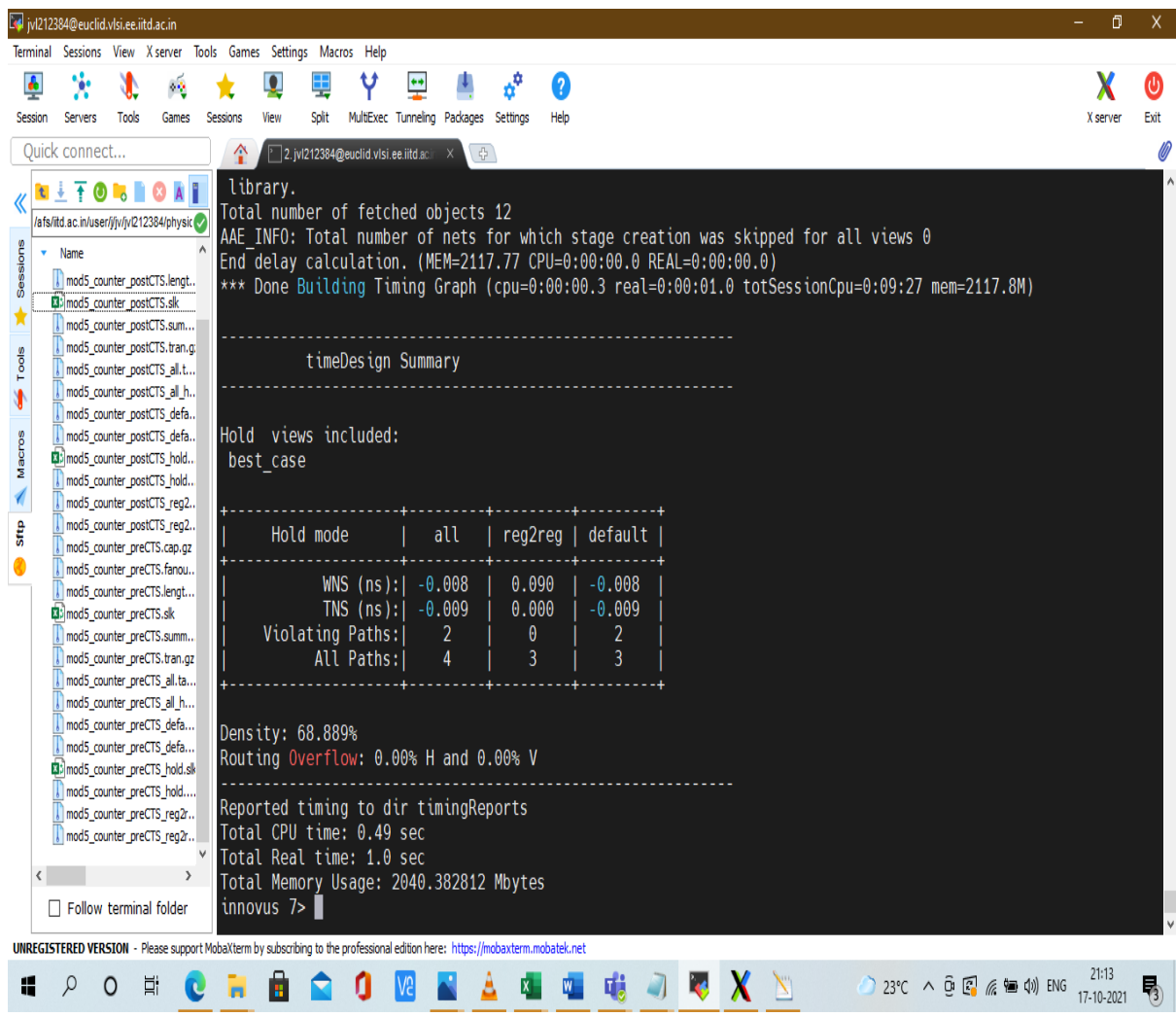
Reporting Options

Number of Paths: 50

Report file(s) Prefix: Mod5Counter_postCTS

Output Directory: timingReports

OK Apply Cancel Help



ROUTING THE DESIGN

The image shows a software window titled "NanoRoute" with a close button (X) in the top right corner. The window is divided into several sections, each with a red header:

- Routing Phase**
 - ☒ Global Route
 - ☒ Detail Route. Start Iteration: default, End Iteration: default
 - Post Route Optimization: ☐ Optimize Via, ☐ Optimize Wire
- Concurrent Routing Features**
 - ☒ Fix Antenna. ☐ Insert Diodes. Diode Cell Name: [text box]
 - ☒ Timing Driven. Effort: 5, Congestion: [slider], Timing: S.M.A.R.T.
 - ☒ SI Driven
 - ☐ Post Route SI. SI Victim File: [text box] [browse icon]
 - ☐ Litho Driven
 - ☐ Post Route Litho Repair
- Routing Control**
 - ☐ Selected Nets Only. Bottom Layer: default, Top Layer: default
 - ☐ ECO Route
 - ☐ Area Route. Area: [text box] [browse icon] [Select Area and Route button]
- Job Control**
 - ☒ Auto Stop
 - Number of Local CPU(s): [text box: 1]
 - Number of CPU(s) per Remote Machine: [text box: 1]
 - Number of Remote Machine(s): [text box: 0]
 - [Set Multiple CPU... button]

At the bottom of the window is a row of buttons: a red "OK" button, followed by "Apply", "Attribute", "Mode...", "Save", "Load", "Cancel", and "Help".

VERIFY GEOMETRY



The image shows a 'Verify Geometry' dialog box with a title bar and a close button. It has two tabs: 'Basic' and 'Advanced'. The 'Basic' tab is selected. The 'Verification Area' section has two radio buttons: 'Entire area' (selected) and 'Specify'. Below 'Specify' are input fields for X1, Y1, X2, and Y2, all set to 0. There are also 'Layer Range' buttons for 'Bottom Layer' (ME1(1)) and 'Top Layer' (AL RDL(9)). The 'Check' section contains two columns of checkboxes, all of which are checked. The 'Allow' section contains five checkboxes, all of which are unchecked. At the bottom are buttons for 'OK', 'Apply', 'Reset', 'Cancel', and 'Help'.

Verify Geometry x

Basic Advanced

Verification Area

☒ Entire area

☐ Specify

X1: 0 Y1: 0

X2: 0 Y2: 0

☐ Layer Range: Bottom Layer: ME1(1) Top Layer: AL RDL(9)

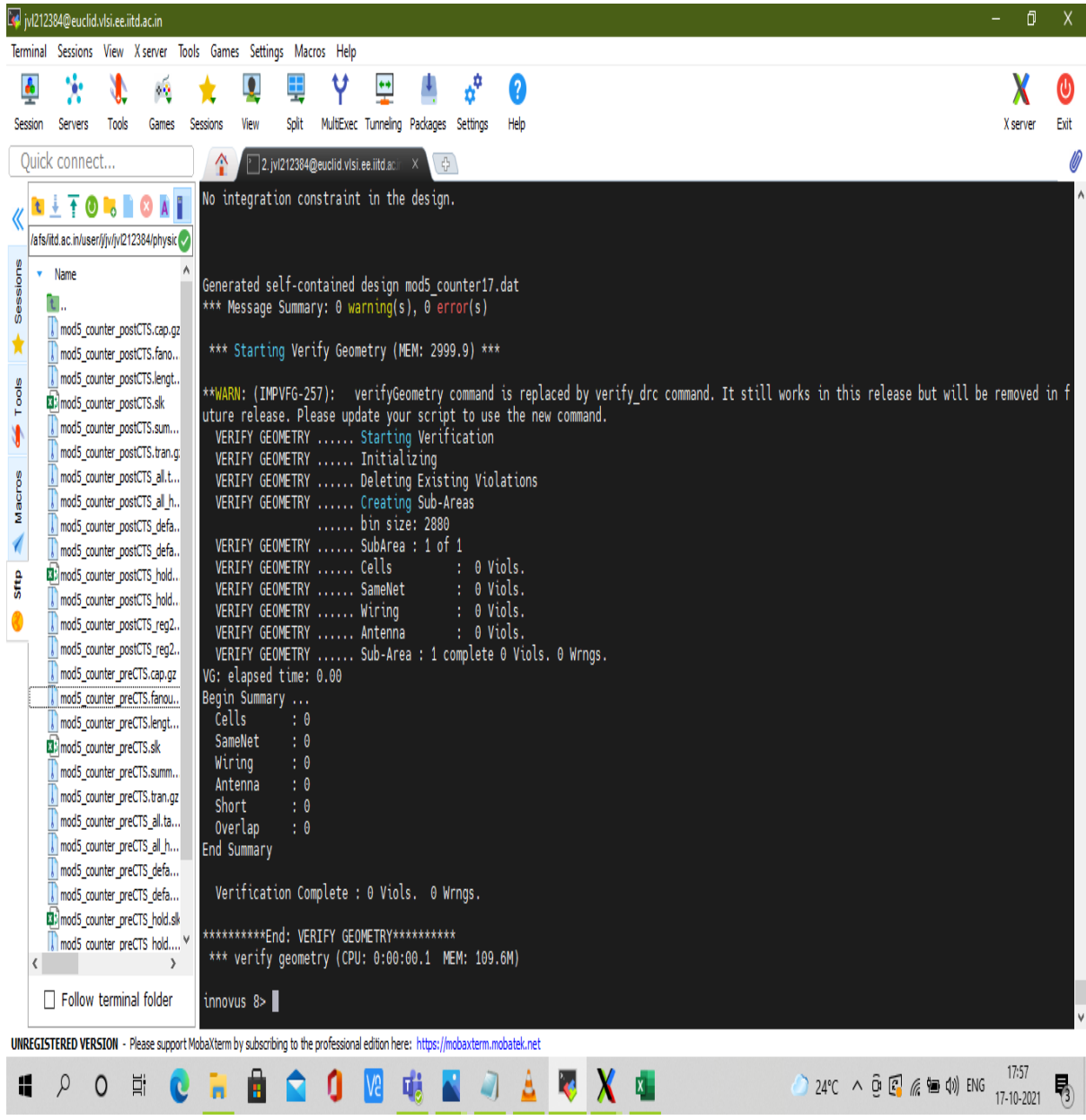
Check

<input checked="" type="checkbox"/> Minimum Width	<input checked="" type="checkbox"/> Minimum Spacing
<input checked="" type="checkbox"/> Minimum Area	<input checked="" type="checkbox"/> Same Net Spacing
<input checked="" type="checkbox"/> Short	<input type="checkbox"/> Geometry Antenna
<input checked="" type="checkbox"/> Cell Overlap	<input type="checkbox"/> Off Routing Grid
<input checked="" type="checkbox"/> Insufficient Metal Overlap	<input checked="" type="checkbox"/> Off Manufacturing Grid
<input checked="" type="checkbox"/> MinHole	<input checked="" type="checkbox"/> Implant Check
<input checked="" type="checkbox"/> Minimum Cut	<input checked="" type="checkbox"/> MinStep
<input checked="" type="checkbox"/> Via Enclosure	<input checked="" type="checkbox"/> Merged MGrid Check

Allow

<input checked="" type="checkbox"/> Pin In Blockage
<input checked="" type="checkbox"/> Same Cell Violations
<input type="checkbox"/> Different Cell Violations
<input type="checkbox"/> Overlap of Pad Filler Cells
<input type="checkbox"/> Overlap of Routing Blockages And Pins
<input type="checkbox"/> Overlap of Routing Blockage And Cell Blockage

OK Apply Reset Cancel Help



VERIFY CONNECTIVITY



The image shows a 'Verify Connectivity' dialog box with a title bar and a close button. It contains several sections: 'Net Type' with radio buttons for 'All', 'Regular Only', and 'Special Only'; 'Nets' with radio buttons for 'All', 'Selected', and 'Named'; 'Check' with a grid of checkboxes for various error types like 'Open', 'UnConnected Pin', 'Unrouted Net', etc.; a text field for 'Verify Connectivity Report' with a file icon; 'Report Limits' with input fields for 'Error' and 'Warning'; a 'Set Multiple CPU...' button; and a bottom row of 'OK', 'Apply', 'Cancel', and 'Help' buttons.

Verify Connectivity

Net Type

☒ All
☐ Regular Only
☐ Special Only

Nets

☒ All
☐ Selected
☐ Named:

Check

<input checked="" type="checkbox"/> Open	<input checked="" type="checkbox"/> UnConnected Pin	<input checked="" type="checkbox"/> Unrouted Net
<input type="checkbox"/> Connectivity Loop	<input checked="" type="checkbox"/> DanglingWire (Antenna)	<input checked="" type="checkbox"/> Weakly Connected Pin
<input type="checkbox"/> Geometry Loop	<input type="checkbox"/> Geometry Connectivity	<input type="checkbox"/> Keep Previous Results
<input type="checkbox"/> Divide Power Net	<input checked="" type="checkbox"/> Soft PG Connect	<input type="checkbox"/> Raw Violations Mark
<input type="checkbox"/> Use new open Vio	<input type="checkbox"/> Remove old open Vio	<input type="checkbox"/> Use Virtual Connection
<input type="checkbox"/> TSV Die Abstract File <input type="text"/>		

Verify Connectivity Report:

Report Limits

Error:
Warning:

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

2.jv1212384@euclid.vlsi.ee.iitd.ac.in

Follow terminal folder

```
VG: elapsed time: 0.00
Begin Summary ...
Cells      : 0
SameNet    : 0
Wiring     : 0
Antenna    : 0
Short      : 0
Overlap    : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 109.6M)

innovus 8> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sun Oct 17 17:57:50 2021

Design Name: mod5 counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (19.4000, 15.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Sun Oct 17 17:57:50 2021
Time Elapsed: 0:00:00.0


***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 8>
```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

24°C 17:57 17-10-2021

VERIFY DRC



The image shows a 'Verify DRC' dialog box with a title bar and a close button. It has two tabs: 'Basic' and 'Advanced'. The 'Basic' tab is selected. The 'Verification Area' section has a red header and contains a radio button for 'Entire area' (which is selected) and a radio button for 'Specify'. The 'Specify' option has two sub-options: 'By Layer' and 'By Area'. The 'By Layer' option is selected. Below this, there are input fields for 'X1', 'Y1', 'X2', and 'Y2', all set to '0'. There is also a 'Layer Range' section with a 'Bottom Layer' dropdown set to 'ME1(1)' and a 'Top Layer' dropdown set to 'AL_PDL(9)'. The 'Disable Rules' section has a red header and contains eight checkboxes: 'Color', 'Enclosure', 'Min Area', 'Min Step', 'Cut Spacing', 'EOL Spacing', 'Min Cut', and 'Protrusion'. All checkboxes are currently unchecked. At the bottom of the dialog are four buttons: 'OK', 'Apply', 'Cancel', and 'Help'.

Verify DRC

Basic Advanced

Verification Area

☒ Entire area

☐ Specify

X1: 0 Y1: 0

X2: 0 Y2: 0

☐ Layer Range: Bottom Layer: ME1(1) Top Layer: AL_PDL(9)

Disable Rules

☐ Color ☐ Cut Spacing

☐ Enclosure ☐ EOL Spacing

☐ Min Area ☐ Min Cut

☐ Min Step ☐ Protrusion

OK Apply Cancel Help

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

2 jv1212384@euclid.vlsi.ee.iitd.ac.in

innovus 8> VERIFY_CONNECTIVITY use new engine.

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Sun Oct 17 17:57:50 2021

Design Name: mod5_counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (19.4000, 15.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sun Oct 17 17:57:50 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 8> #report mod5_counter.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 3109.6) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 19.400 15.400} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

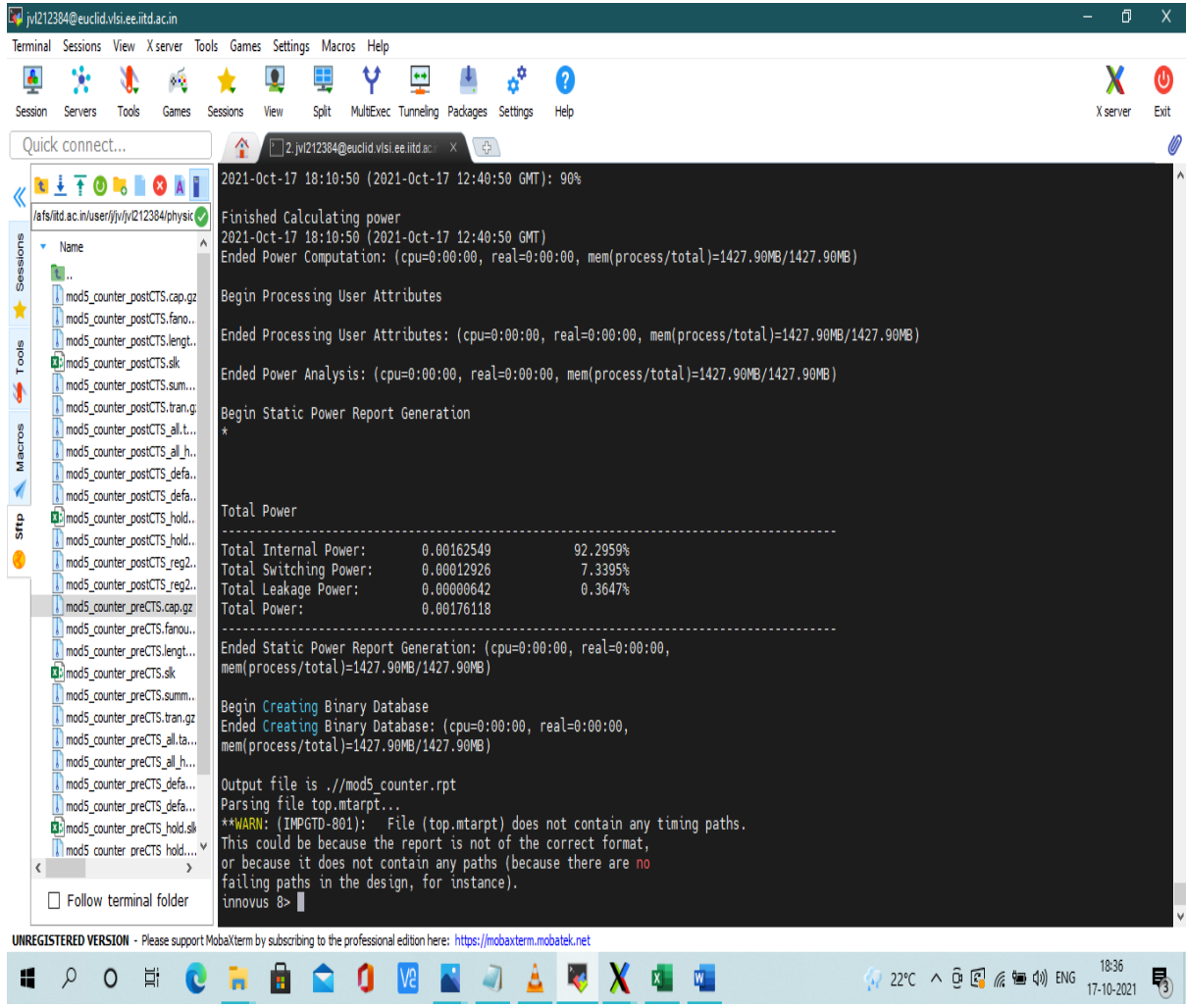
Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***
```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

24°C 17:58 17-10-2021

POWER ANALYSIS



The screenshot shows a MobaXterm terminal window with a file explorer on the left and a terminal output on the right. The terminal output displays the results of a power analysis performed on a design file. The analysis includes calculating power, processing user attributes, and generating a static power report. The results show a total internal power of 0.00162549 (92.2959%), total switching power of 0.00012926 (7.3395%), total leakage power of 0.00000642 (0.3647%), and a total power of 0.00176118. A warning message indicates that the file (top.mtarpt) does not contain any timing paths, which could be due to the report not being in the correct format or because it does not contain any paths (because there are no failing paths in the design, for instance).

```
2021-Oct-17 18:10:50 (2021-Oct-17 12:40:50 GMT): 90%
Finished Calculating power
2021-Oct-17 18:10:50 (2021-Oct-17 12:40:50 GMT)
Ended Power Computation: (cpu=0:00:00, real=0:00:00, mem(process/total)=1427.90MB/1427.90MB)

Begin Processing User Attributes
Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00, mem(process/total)=1427.90MB/1427.90MB)
Ended Power Analysis: (cpu=0:00:00, real=0:00:00, mem(process/total)=1427.90MB/1427.90MB)

Begin Static Power Report Generation
*

Total Power
-----
Total Internal Power:    0.00162549    92.2959%
Total Switching Power:   0.00012926    7.3395%
Total Leakage Power:     0.00000642    0.3647%
Total Power:            0.00176118

-----
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total)=1427.90MB/1427.90MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total)=1427.90MB/1427.90MB)

Output file is ../mod5_counter.rpt
Parsing file top.mtarpt...
**WARN: (IMPGTD-801): File (top.mtarpt) does not contain any timing paths.
This could be because the report is not of the correct format,
or because it does not contain any paths (because there are no
failing paths in the design, for instance).
innovus 8>
```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

NO VIOLATION

