LAB REPORT

JVL2384 (PRANAV KUMAR RAI)

- **AIM**

To Design MOD 5 Synchronous Up Counter using Master Slave JK Flipflop.

Frequency of Operation 250Mhz

For Schematic

NMOS W=200nm L=60nm

PMOS W=400nm L=60nm

For Layout

Length 1.4um

Width 80um

Area 112.0umsq

- **PROCEDURE**

First of all, made schematic and layout of INVERTER

Then of

NAND2

AND2

NAND3

SR LATCH

JK FF

MOD_5_SYNCHRONOUS_UP_COUNTER

Simulated each circuit

Cleared all DRC error of each circuit

Cleared LVS error of each circuit

I have attached the Schematic, layout, Simulation, DRC, LVS, PEX reports.

- **RESULTS**

Frequency of operation 250Mhz

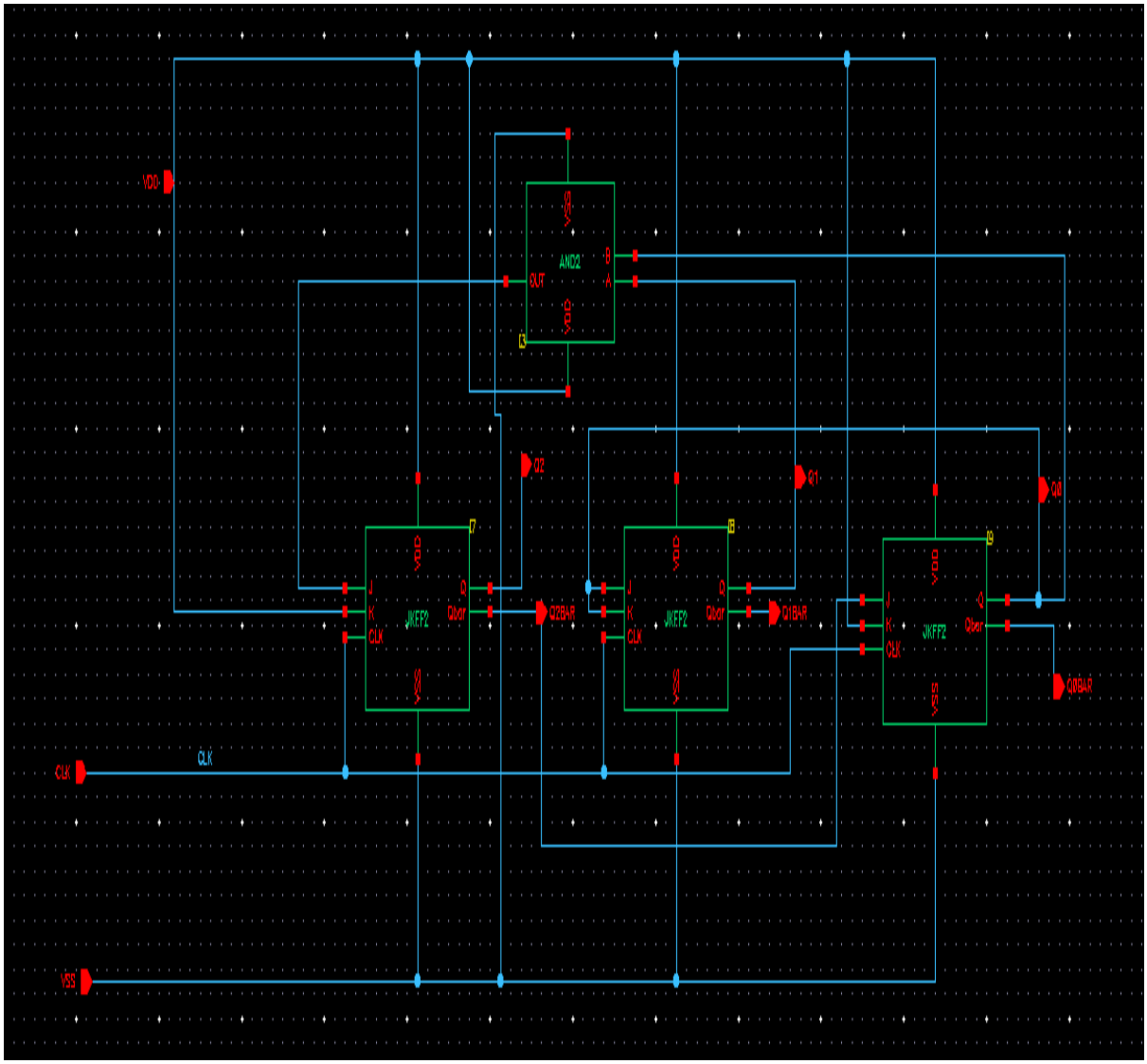
Counter input CLK

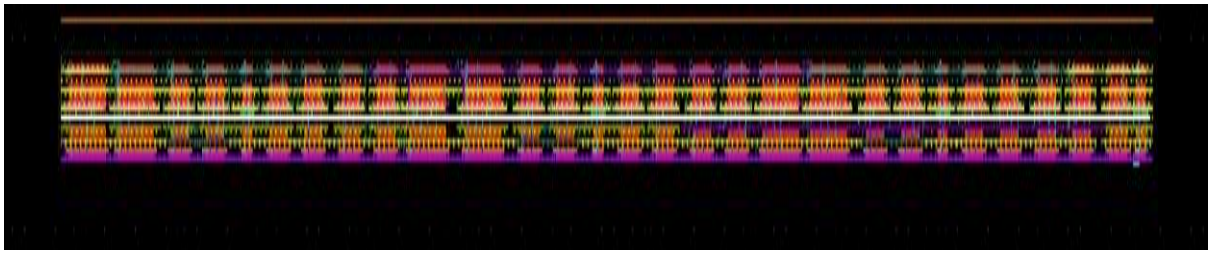
Counter Output Q2 Q1 Q0

Different states of counter

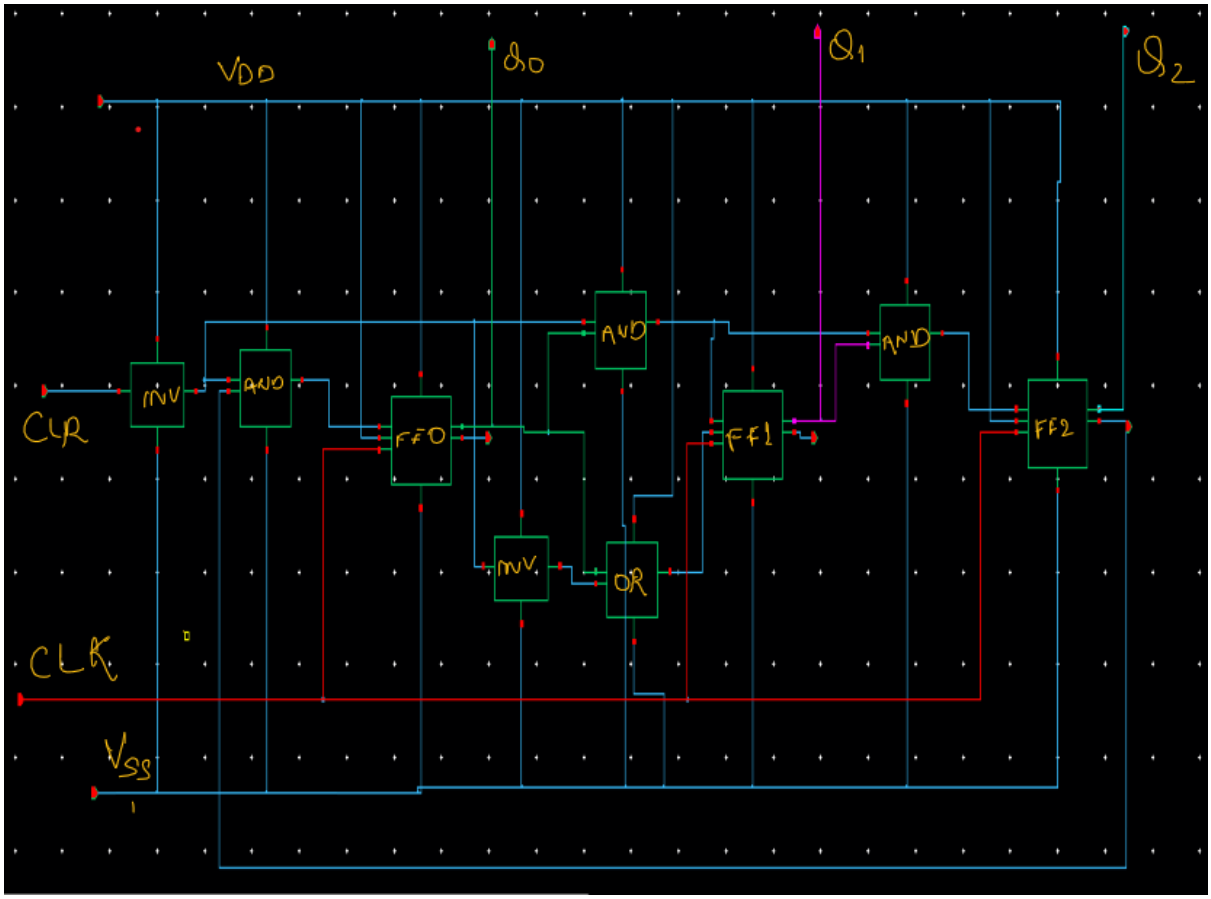
000 001 010 011 100 000 001 so on

Counter Schematic Symbol Simulation Layout

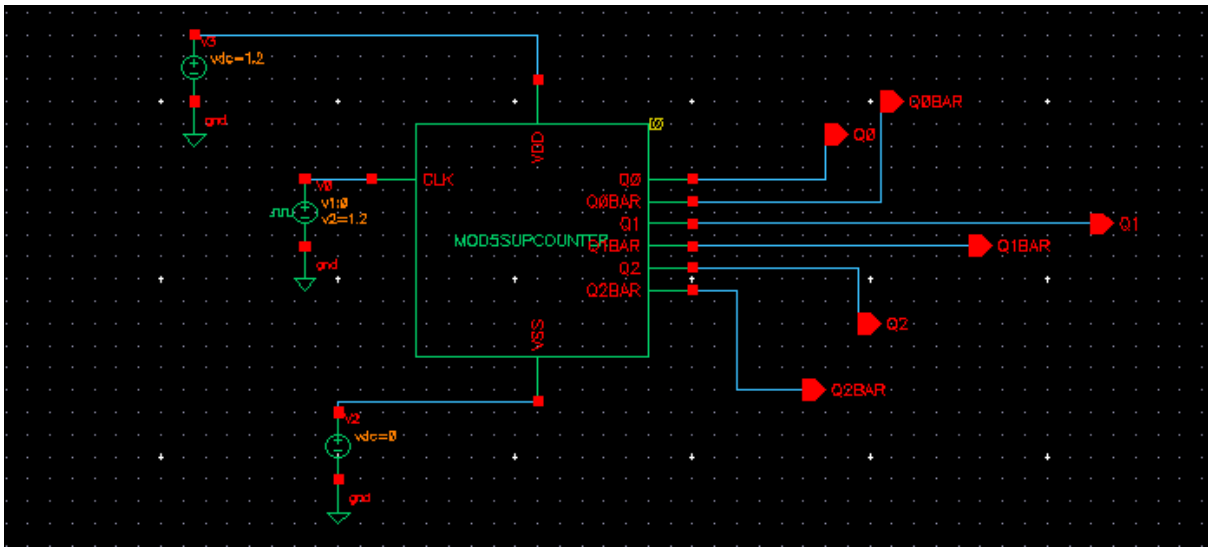


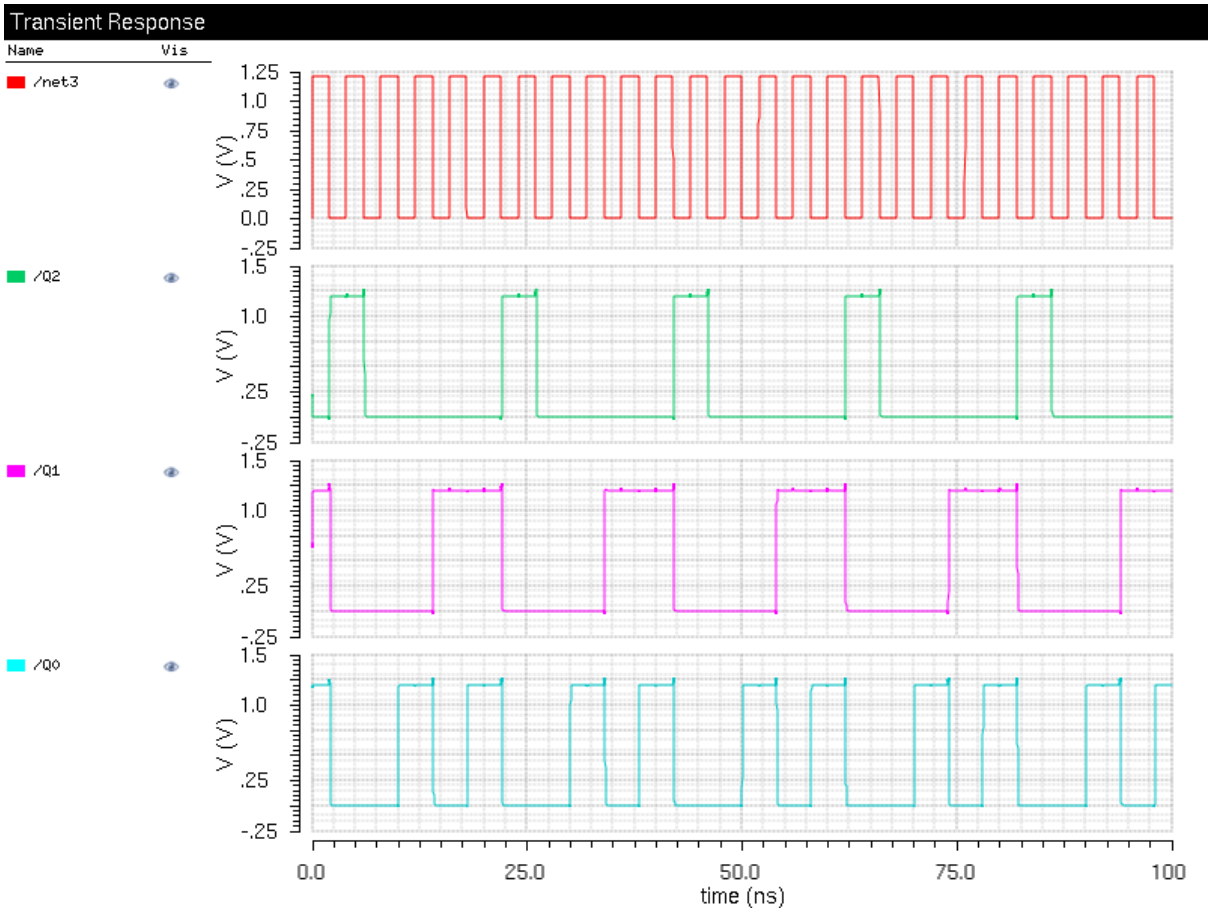


SCHEMATIC WITH CLEAR INPUT



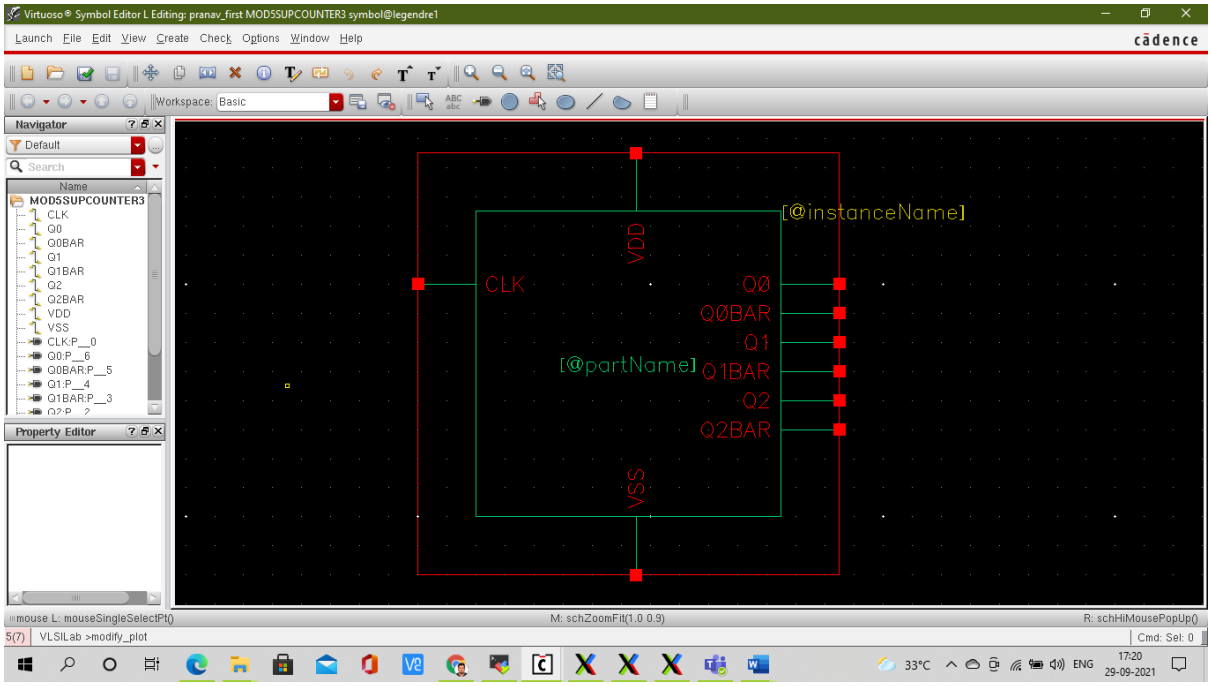
Schematic Simulation





POST EXTRACTION SIMULATION

Post Extraction Symbol



TIMING RESULT

Timing Results

Inverter

Rise time 34.81E-12

Fall time 34.81E-12

Rise Delay time 22.4119ps

Fall Delay Time 14.1314ps

Counter

For Q0

Rise time 44.5E-12

Fall time 72.28E-12

For Q1

Rise time 35.75E-12

Fall time 54.66E-12

For Q2

Rise time 27.53E-12

Fall time 39.53E-12

Rise Delay Time

From CLK to Q0 71.91E-12

From CLK to Q1 65.02E-12

From CLK to Q2 61.4E-12

Fall Delay Time

From CLK to Q0 105.75E-12

From CLK to Q1 97.87E-12

From CLK to Q2 97.5E-12

Post Extraction

For Q0

Rise time 455.6E-12

Fall time 683.2E-12

For Q1

Rise time 439.2E-12

Fall time 435.4E-12

For Q2

Rise time 226.8E-12

Fall time 355.1E-12

Rise Delay Time

From CLK to Q0 495.9E-12

From CLK to Q1 380.4E-12

From CLK to Q2 340.8E-12

Fall Delay Time

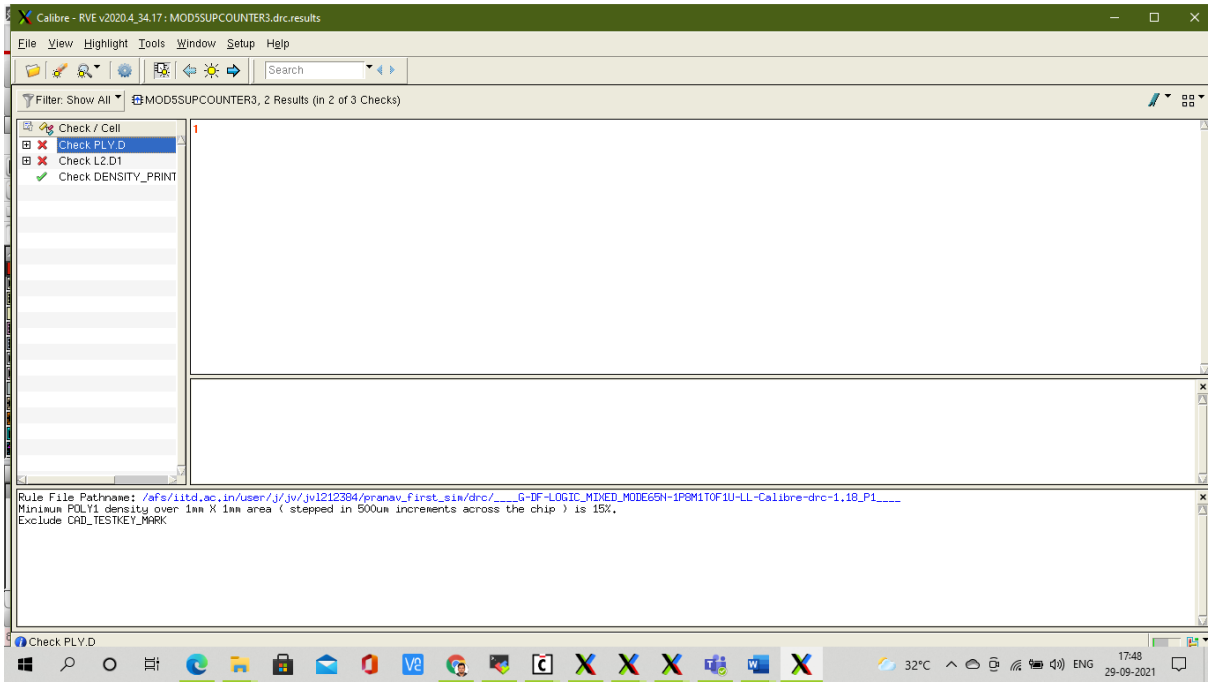
From CLK to Q0 895.8E-12

From CLK to Q1 687.6E-12

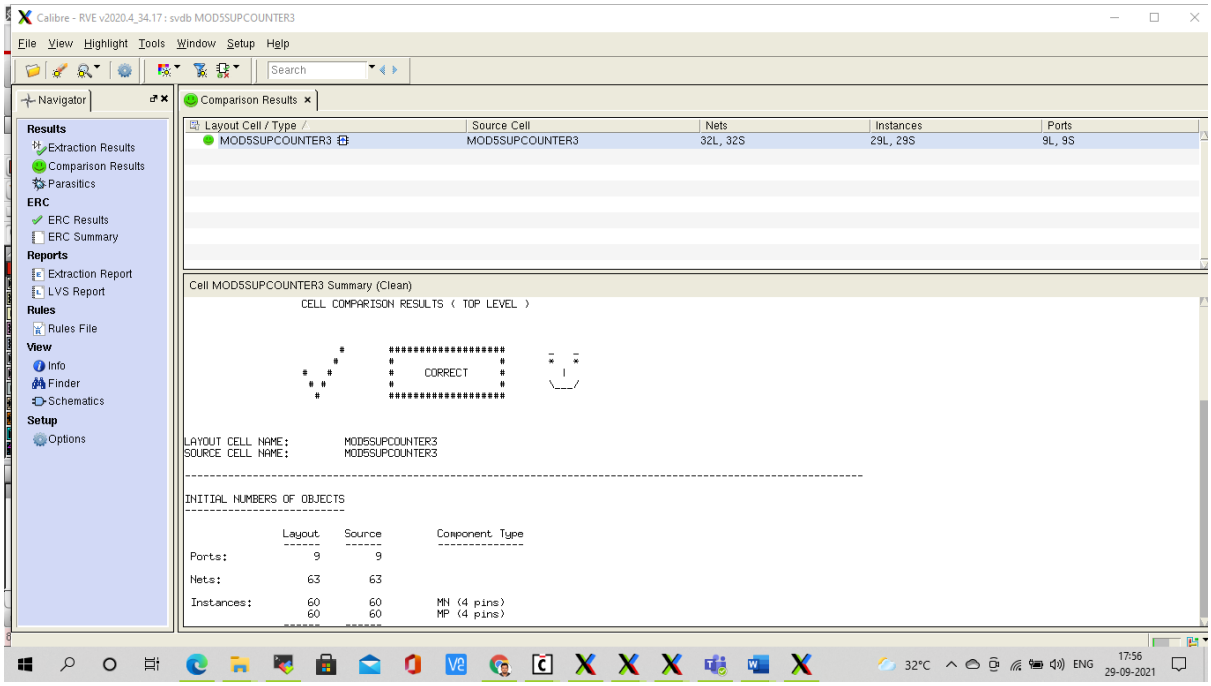
From CLK to Q2 632.4E-12

SCREENSHOTS OF DRC LVS PEX (Files were already attached)

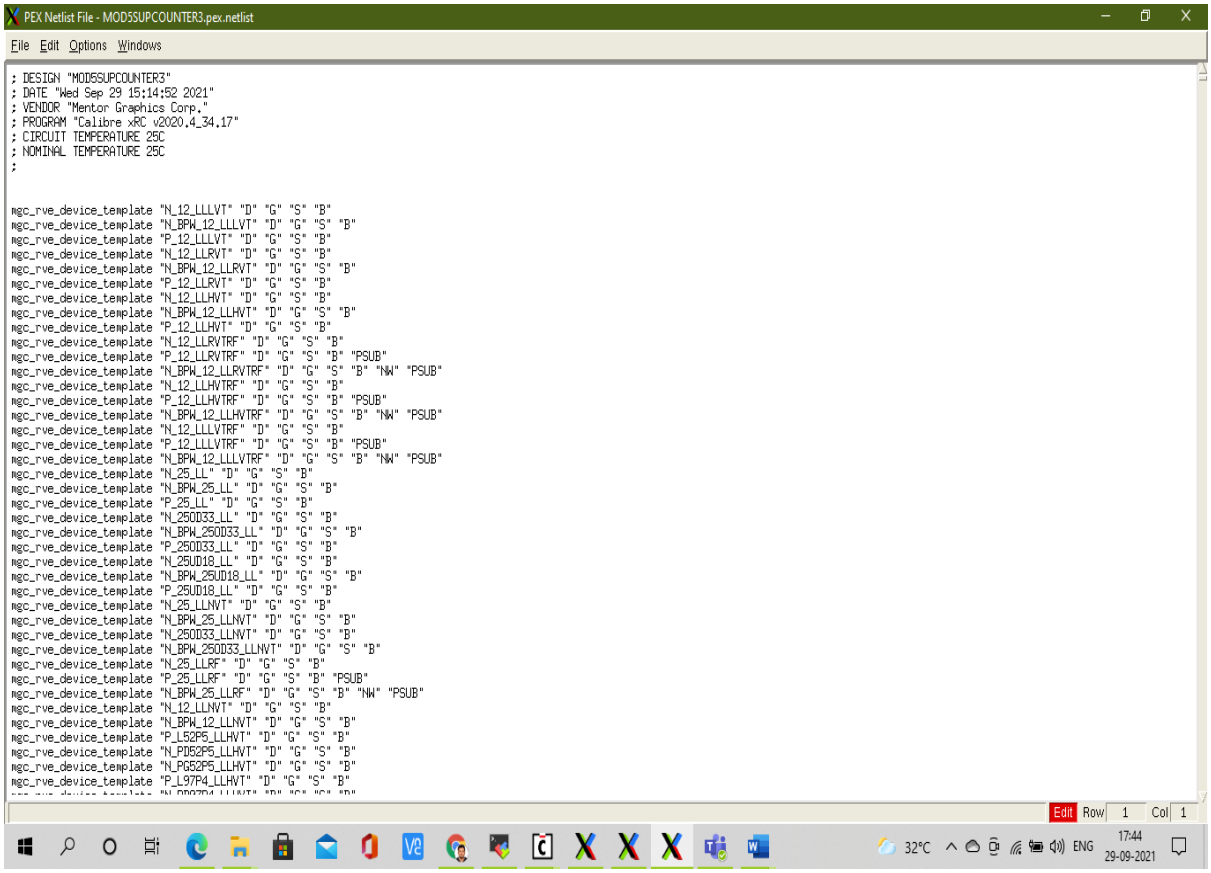
DRC



LVS


Calibre - RVE v2020.4_34.17 : svdb MOD5SUPCOUNTER3
File View Highlight Tools Window Setup Help
Search
Navigator
Results
Extraction Results
Comparison Results
Parasitics
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
MOD5SUPCOUNTER3
MOD5SUPCOUNTER3
32L, 32S
29L, 29S
9L, 9S
Cell MOD5SUPCOUNTER3 Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: MOD5SUPCOUNTER3
SOURCE CELL NAME: MOD5SUPCOUNTER3
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 9 9
Nets: 63 63
Instances: 60 60 MN (4 pins)
60 60 MP (4 pins)
32°C
ENG
17:56
29-09-2021

PEX


PEX Netlist File - MOD5SUPCOUNTER3.pex.netlist
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; DESIGN "MOD5SUPCOUNTER3"
; DATE "Wed Sep 29 15:14:52 2021"
; VENDOR "Mentor Graphics Corp."
; PROGRAM "Calibre xRC v2020.4_34.17"
; CIRCUIT TEMPERATURE 25C
; NOMINAL TEMPERATURE 25C
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32°C
ENG
17:44
29-09-2021