Digital Systems Lab Assignment - 1

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Objectives:

1) To learn to write test bench
2) To design a MUX using verilog
3) To peform left shift and right shift operations in order to multiply and divide by 2.
4) To peform various operations like &, |, ~ and ^, to represent AND, OR, NAND, NOR, Ex-OR and Ex NOR. gates.
5) To call a small module in large module in verilog.

Description:

Logic gates are used to carry out logical operations on single or multiple binary inputs to give binary outputs. They regulate the flow of electricity through an electronic circuit, by receiving and modifying binary input and output.

The circuits of logic gates make electronic logic operation possible, which are encorporated into larger electronic systems like performing arithmetic operations, multiplexers, encoders, decoders, microprocessors, etc.

- AND Gate Module gives output 1, when all the inputs are 1.
- OR Gate gives all the output 0, when all the inputs are zero, else 1
- NAND Gates gives output 0 only when all inputs are 1, else it gives 1.
- NOR Gate gives output 1 only when all inputs are zero, else it gives 0.
- Ex-OR Gate gives output 1 only when odd inputs are 1, else it gives 0.
- Ex-NOR Gate gives output 1 only when even inputs are 1, else it gives 0.

- Multiply_by2 module peforms Left Shift operation.
- Divide_by2 module peforms Right Shift operation.
- MUX 2 to 1 pef uses conditional gates to peform $y = \bar{S}A + SB$ operation
- MUX 4 to 1 peforms the following :
  $y = \bar{S}_1\bar{S}_0A + \bar{S}_1S_0B + S_1\bar{S}_0C + S_1S_0D$
- MUX 8 to 1 peforms the following :
  $y = \bar{S}_2\bar{S}_1\bar{S}_0A_1 + \bar{S}_2\bar{S}_1S_0A_2 + \bar{S}_2S_1\bar{S}_0A_3 + \bar{S}_2S_1S_0A_4$
  $+ S_2\bar{S}_1\bar{S}_0A_5 + \bar{S}_2\bar{S}_1S_0A_6 + S_2S_1\bar{S}_0A_7 + S_2S_1S_0A_8$

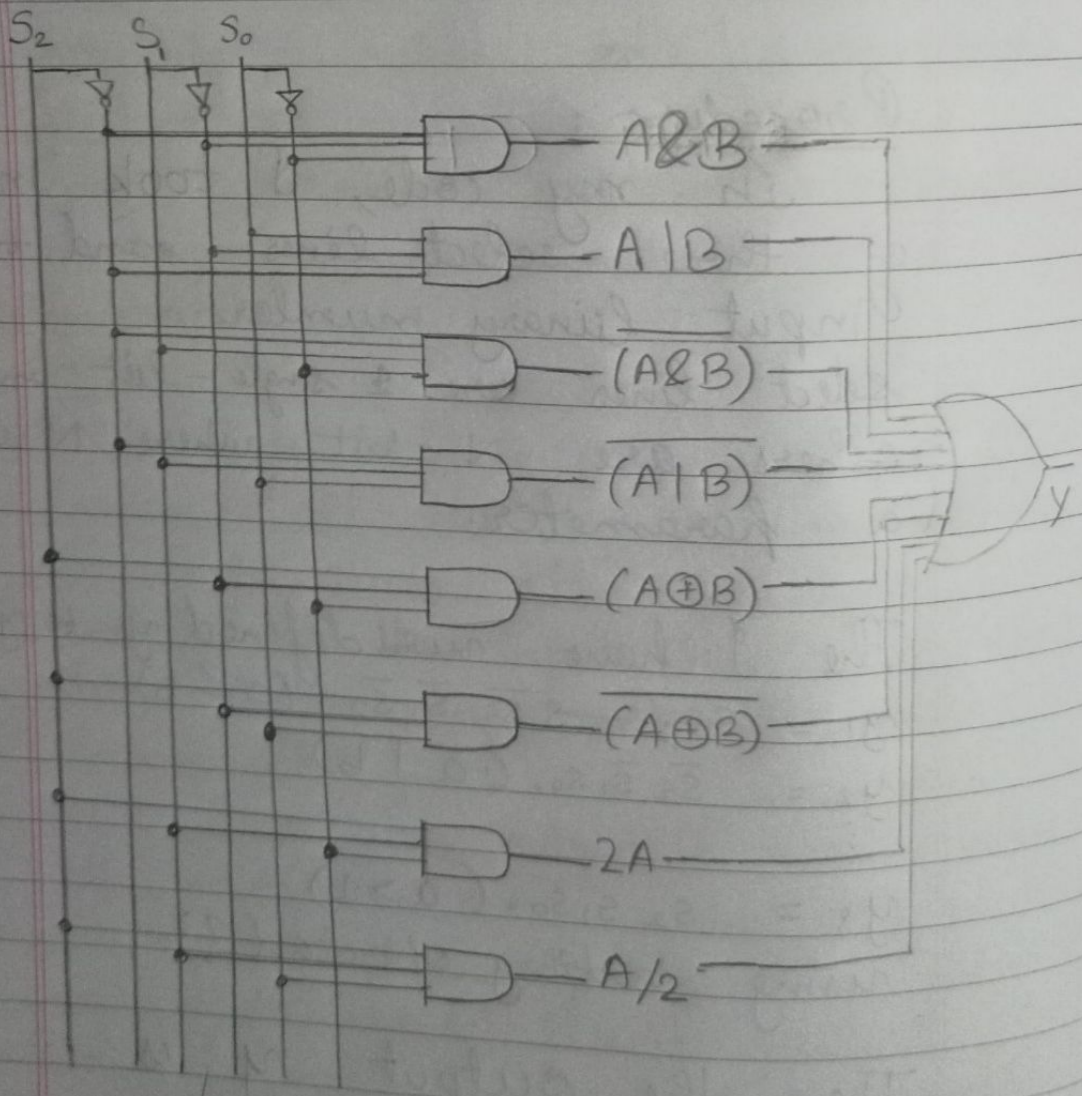
Procedure :

In my code, I took inputs of three select lines and two input binary numbers. select lines are 3 single-bit and others are N-bit where N is a parameter.

The I have redefined y_1 to y_8 as
$y_1 = \bar{S}_2\bar{S}_1\bar{S}_0$. (a & b)
$y_2 = \bar{S}_2\bar{S}_1S_0$. (a | b)
⋮
$y_8 = S_2S_1S_0$. (a > 1)
using tertiary operator (?:)

Then the output y is
$y = y_1 + y_2 + \dots + y_8$;

In Test Bench, I registered ~~corr~~ variables corresponding to input in first code, and wired the output Y.
Then I defined A = 1111 and B = 110, ~~folded~~ followed by all eight operations in the questions on the pair of A and B, with a time ~~day~~ delay of 10 units.



Wave forms:
(attached in form of Screen Shot)

Result:

~~A = 1111~~, A = 000001111, B = 000000110

$S_2S_1S_0$	Output (Obs)	Operation
000	000000110	$A \wedge B$
001	000001111	$A \vee B$
010	11111 1001	$\sim(A \wedge B)$
011	11111 0000	$\sim(A \vee B)$
100	000001001	$A \oplus B$
101	111110110	$\sim(A \oplus B)$
110	000011110	2*A
111	000000111	A/2