# Design of a 4*4 SRAM Array using Adiabatic logic in Cadence Virtuoso

Thannir Pranay,
UG Student, Dept. of ECE,
CMR College of Engineering & Technology,
Medchal, Hyderabad, Telangana, India.

Vemula Panduranga,
Associate professor, Dept. of ECE,
CMR College of Engineering & Technology,
Medchal, Hyderabad, Telangana, India.

***Abstract* — In recent years, a circuit's instantaneous power consumption and overall energy dissipation have become critical aspects to consider in sophisticated VLSI system design solutions. The adiabatic logic is a method for improving the power dissipation and energy recovery capacity of these circuits, and it allows VLSI circuits to recycle utilised power. In the Adiabatic SRAM good high degree of power reduction is observed. By applying the aforementioned technique same SRAM is investigated by varying technology. In this study, the power values of adiabatic SRAM cells and standard SRAM cells are compared. As compared to the typical 6T CMOS SRAM cell, adiabatic logic uses less power and energy.Cadence® EDA environment has been employed to design the SRAM cell, and power and energy values are estimated for the CMOS processes of 90nm and 45nm technology.**

***Keywords— VLSI,SRAM(Static Random Access Memory), Adiabatic Logic, CMOS, Power consumption, Sense amplifier..***

## I. INTRODUCTION

Energy-efficient CPUs are becoming essential due to the rising demand for portable battery-operated systems. Energy efficiency is of utmost importance for applications like wearable computing. The batteries in these embedded systems must be repeatedly charged. With wireless sensor networks that are used to monitor environmental data, the issue is more serious. Some systems may not have access to battery charging. We are aware that the power dissipation of SoC processors is influenced by on-chip memory. Thus, it is crucial to have SRAM that is reliable, low power, and energy efficient because it is mostly utilised for on-chip memory.

To limit power dissipation, a number of strategies are used, including power gating and the design of circuits with power supply voltage scaling. A lower power supply voltage quadratically and exponentially lowers dynamic power and leakage power, respectively. Yet, scaling the power supply reduces the noise margin. A lot of SRAM arrays are built around lowering the swing voltage and active capacitance. With typical SRAM, the power loss while reading is more than the power loss during writing because when reading, the bit line voltage swing is much less than it is during writing. During a read operation, the power lost in bit lines accounts for around 60% of the total dynamic power used. The bit line capacitance, the square of the bit line voltage, and the writing frequency all influence how much power bit lines need while writing.

Limiting voltage variations between conducting devices reduces power loss. Voltage waveforms that change over time are used to achieve this. This process is also known as adiabatic charging. The SRAM needs several phase power clocks in order to operate solely on adiabatic charging principles. To increase the RNM by minimising the power consumption in single bit-line SRAM utilising an adiabatic variation of word-line.

SRAM power savings are essential, but caution also has to be taken to ensure that performance metrics are not significantly impacted. In this project, efforts were undertaken to utilise and reduce the power that was previously stored in the bit lines. In order to charge and discharge the bit lines, a very basic, compact, and effective adiabatic driver was used. The bit lines may be charged and discharged according to the input signal thanks to the adiabatic driver's D.C. power clock. As a result, there is far less power lost to the ground during the "1" to "0" transition in SRAM.

Before or after reading, no separate pre-charging circuit is utilised. As just bit lines are used, no synchronisation circuit is required. The data is sensed using a low-power sense amplifier. The write driver and the pre-charge circuit must be removed from the traditional SRAM architecture. ( Other performance aspects including power, Noise Margin, read and write latency, and power savings are also made possible under a variety of memory operating situations when this adiabatic logic circuit is used with a typical SRAM cell. The impact of the circuit's device characteristics on the power, RNM, and latency of the SRAM cell has been studied.

## II. Principle of Adiabatic Logic:

When adiabatic logic is used on a circuit, power consumption is decreased because the circuit nodes' stored energy is reused. As a result, the phrase "adiabatic logic" refers to low-power VLSI circuits that enable energy recovery from the circuit nodes. The power clock is crucial to the operation of adiabatic circuits. Each phase of \ the power clock guides the operation of each stage of the adiabatic circuit. The following are the fundamental properties of adiabatic circuits that experience either no or extremely minimal power dissipation:

1) The transistor should never be turned on while a voltage (VDS > 0) exists between its drain and source.
2) The second rule is to never turn off a transistor device if there is a current flowing through it at any point in time (IDS≠0).
3) A diode that is a component of the adiabatic logic should never have currently passed through it.

When the nodes are discharging from their charged state, or during their recovery phase, the adiabatic circuits recuperate the energy. Thus, this logic helps to lower the overall power and energy dissipation of the circuits.Incorporation of such adiabatic logic in the memory cell design

will save a large amount of power in high-density systems. In the literature, a number of adiabatic logic circuits driven by trapezoidal power clocks have been described.

## III. Existing model:

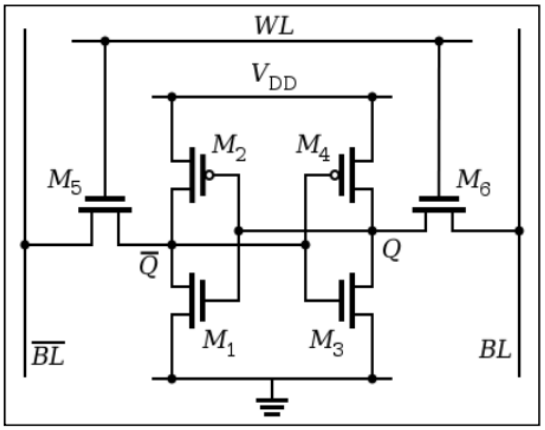


Fig 1. Conventional 6T SRAM cell

Six MOSFETs typically make up an SRAM cell. Four transistors (M1, M2, M3, M4) that make up two cross-coupled inverters (M1, M2, M3, M4) store each bit in an SRAM. For read and write operations, two extra access transistors serve to regulate the access to a storage cell, as can be seen in Figure 2. The heart of a six-transistor SRAM cell with a dual bit line, which stores one bit of data, is made up of two CMOS inverters, with the output potential of each inverter serving as the input for the other Q bar. The inverters are stabilised to their respective states by this feedback loop.

To read from or write to the cell, one uses access transistors and the word and bit lines, WL and BL. The word line is low in standby mode, shutting off the access transistors. The inverters are in a complementary condition at this time. Potential Qbar is high when the p-channel MOSFET in the left inverter is switched on, and when the p-channel MOSFET in inverter two is turned off, Q is low. The data is written on the bit line, and the inverse data is written on the inverse bit line, or BLbar, to write information. The word line is then switched to high to activate the access transistors. As the bit line driver is significantly more powerful, it may assert the inverter transistors. The access transistors can be disabled after the information has been stored in the inverters so that the information there will not be lost. As the data is being sensed at the bit lines, the word line is switched on to turn on the access transistors.

### *A. Read Operation*

To execute a certain operation in SRAM, the word line must always be high. Memory will be used for performing read operations. Assume Q=1 and Q'=0 for memory. The word line is raised for read operations. The output lines are BL and BLB, and these bit lines are already pre-charged, i.e. node voltage Vdd is present at bit and bit b. There is no voltage drop in the circuit since the upper bit is Q. Because Q' is 0 at BLB, there must be a voltage differential between Q' and the node voltage. As a result, the voltage at bit b falls, causing a current flow in the circuit due to the discharge.Because bit and bit b are linked to the sense amplifier, it functions as a comparator. When bit' is low, the sensing amplifier's output is 1.

As a result, when Q=1, the output is also 1, indicating that the read operation was successful. Assume Q=0 and Q'=1 in memory as well. An electrical discharge develops in the circuit at Q and bit as a result of the voltage difference. The transistors must have specified ratios such that Q falls under the P2/D2 threshold zone. This is known as the read limitation. As the bit voltage lowers, the output is 0. With Q = 0, the output is also 0. As a result, the read operation was successfully confirmed in both circumstances.

### *B. Write Operation*

Vdd is charged to write a '0,' and BL is discharged through the ground. Following these two procedures, WL is activated and the data is written to the cell. Consider memory bits with Q=0 and Q=1 values. There are two input lines in the write operation, bit and bit'. To regulate the input lines, we first link bit b to the ground, resulting in a large voltage differential between Q' and bit b [11]. To write '1' to the SRAM cell, we must set Q=1, which may be done by altering the aspect ratio of the transistors so that D2 is stronger than P2. As a result, Q will be 1. Originally, Q=1 following the operation, indicating a successful write operation into memory.

## IV. SENSE AMPLIFIER

The sensing amplifier must detect the BL and BLB to provide precise monitoring. It improves memory cell read and write speeds while also lowering the amount of power required for operation. The sensing amplifier's principal role is to magnify the voltage difference created on the BL and BLB during read and write operations.

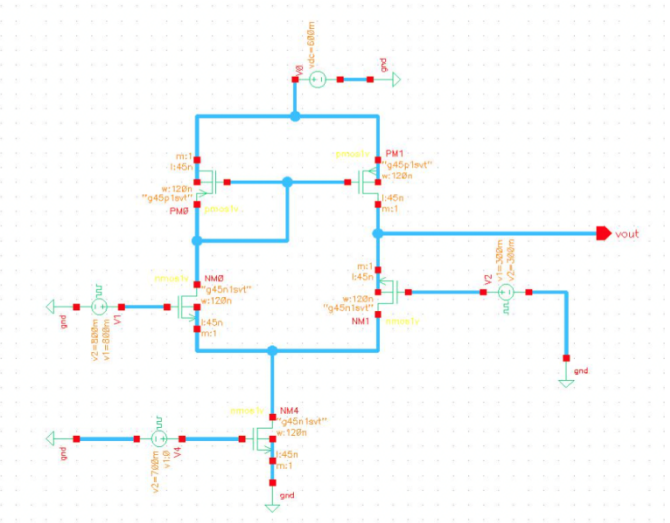


Fig 2. Schematic of the Sense amplifier

To read "1," which is made up of BL=1 and BLB=0, transistors NM0 and NM2 are turned on, while NM1 is turned off, activating PM0 and PM1. This causes VDD to rise at the output logic. When the logic "0" is read using BL=0 and BLB=1, transistors NM1 and NM2 are switched on, while

NM0 is turned off, deactivating PM0 and PM1. As a result, there is no link between VDD and the output, and the output displays logic "0." The waveform indicates that the data stored in the BL is read out when SE is strong for a certain period of time.

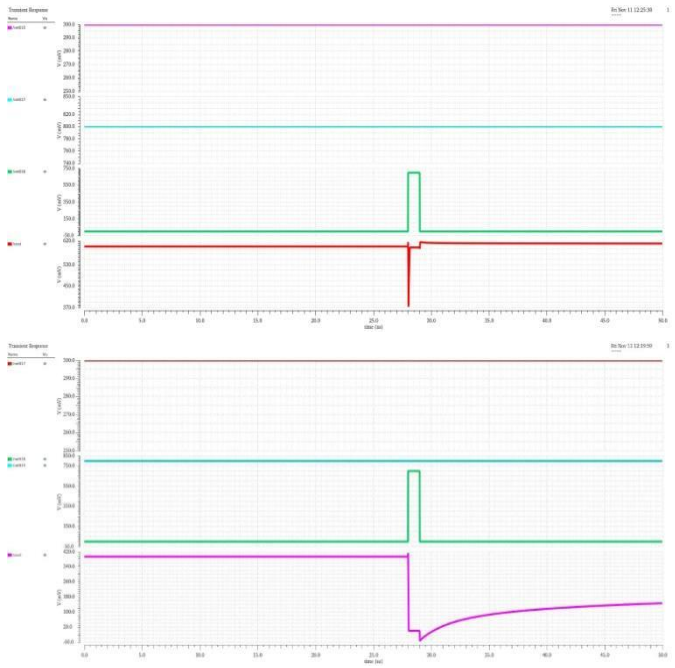

Fig 3. Waveforms of the Sense amplifier

## V. Proposed model

In write mode, the 6T SRAM cell employed in this design features an adiabatically charged bit line. According to Figure 2, the SRAM cell is made up of two switching transistors, MN1 and MP1 (NMOS and PMOS), as well as conventional 6T-SRAM. With an MCPL (Memory Cell Power Line) node, several transistors along the rows can share the switching transistors. Via this sharing, the original number of transistors, or 6T, may be maintained while still achieving adiabatic charging on the bit line in writing mode, which results in a minimal area penalty. In contrast to the NMOS, which is linked between the ground and MCPL, the PMOS is connected between the power line VDD and MCPL. See Figure 2 to comprehend how the adiabatic SRAM functions.

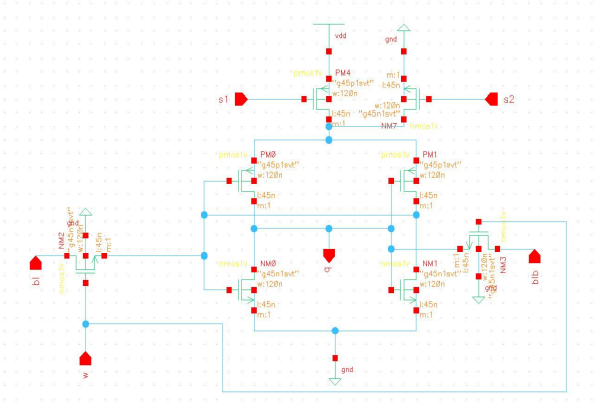

Fig 4. 6T SRAM using MPCL circuit.

Unlike typical SRAM, MCPL logic does not require a steady power source. In Figures 4 , there are two switches labelled S1 and S2. The PMOS is linked between the power line VDD and the MCPL, whereas the NMOS is connected between the ground and the MCPL.

The control signals S1 and S2 are utilised to control the MCPL node. The MCPL node has either VDD, ground, or a floating node depending on how S1 and S2 operate. When the S1 and S2 are both turned off, the PMOS is activated and the MCPL follows the VDD. When the S1 and S2 are turned on, the MCPL follows the GND since NMOS is turned on.When S1 is turned on and S2 is turned off, both the NMOS and PMOS are turned off, and the MCPL node is floating. The charge from the bit lines is then utilised to charge the node MCPL through the cross coupled inverters.

The BL (Bit Line) is gradually charged following the control signals during write mode operation. When S1 is turned on and S2 is turned off, the Q node follows the BL. The MCPL is already in free fall. When Q is charged to HIGH, P1 is turned off and N1 is turned on.Likewise, if Qb is LOW, P2 is ON, and N2 is OFF. There is now a channel for charge to go from Q node to MCPL through P2.

During read mode operation, the control signals S1 and S2 are turned off, and the SRAM operates as a traditional 6T SRAM using MCPL as the power rail VDD.

## VI. 4x4 ARRAY LOGIC

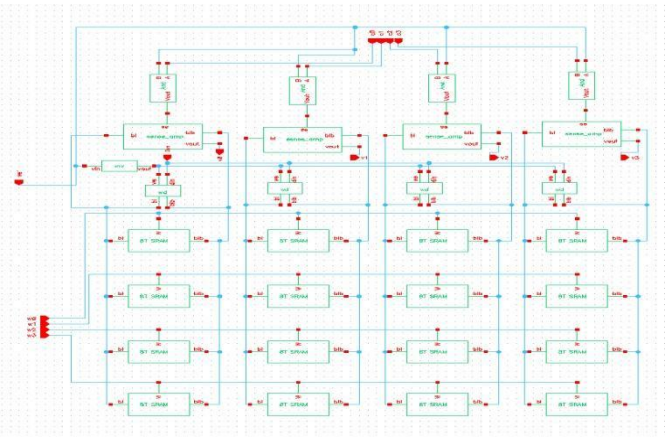

Fig 8. Schematic of 4x4 array

Each cell may hold a single bit of binary data. There are four-word lines and four-bit lines in this array. Hence, there are a total of 4x4 unique memory cells in this configuration.To access a given memory cell in this structure, the matching word line and bit line must be chosen based on the address coming from outside the memory array.Row and column decoders can be used to perform row and column selection operations, respectively. The row decoder circuit picks one of four-word lines, whereas the column decoder circuit selects one of four-bit lines.Using 16-bit RAM, we created a 4x4 SRAM Memory Array.

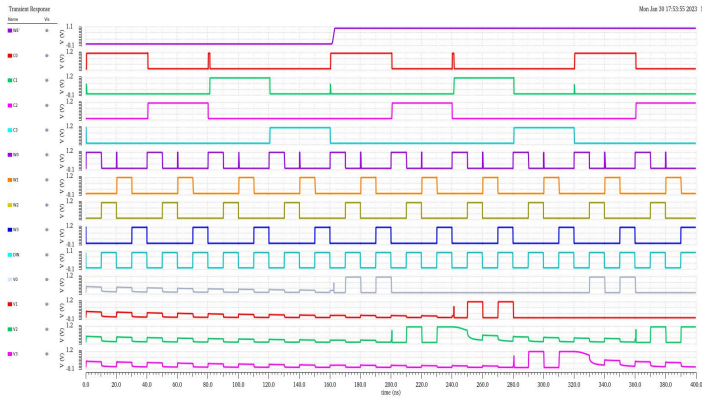

Fig 9. Transient Response for 16-bit SRAM Memory Array

## VIII. SIMULATION RESULTS

Table 1: Performance Comparison between Conventional SRAM cell in 45nm,180nm and 6T SRAM Cell using MCPL

| ***Parameter*** | | ***Conventinal 90nm*** | ***Conventional 45 nm*** | ***Adiabatic 45nm (Current Project)*** |
|---|---|---|---|---|
| Power Consumption | SIngle Cell | 128uW | 338nW | 258nW |
| | 4X4 Array | 456m | 5.6uw | 4.4uW |
| Read Delay | | 0.02us | 0.03ns | 0.04ns |
| Write Delay | | 0.25us | 0.118ns | 0.546ns |

## IX. CONCLUSION

Adiabatic Logic has been implemented over the 6T SRAM and was compared with the conventional SRAM in various technologies. The results show that the proposed SRAM has less power consumption than the conventional SRAM. 4X4 Memory Arrray has been designed and tested for read and write operations.

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