

A Major Project Report on
DESIGN OF 6T SRAM CELL USING ADIABATIC LOGIC

Submitted in partial fulfilment of the Academic requirements for the award of the
degree of

Bachelor of Technology

in

Electronics & Communication Engineering

Submitted by

**Under the esteemed Guidance of
Mr. V. PANDURANGA
Associate Professor of ECE Department**



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
(NAAC Accredited with ‘A+’ Grade & NBA Accredited)
(Approved by AICTE, Permanently Affiliated to JNTU Hyderabad)
KANDLAKOYA, MEDCHAL ROAD, HYDERABAD-501401

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING



CERTIFICATE

This is to certify that the major project report entitled "**“DESIGN OF 6T SRAM CELL USING ADIABATIC LOGIC”**" is a bonafide work done by **T. PRANAY (19H51A04L7)** in partial fulfillment of the requirements for the award of the degree of Bachelor of Technology in Electronics & Communication Engineering, submitted to the Department of Electronics & Communication Engineering, CMR College of Engineering & Technology, Hyderabad during the Academic Year 2022-23.

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Ultimately, we owe all our success to our beloved parents, whose vision, love, and inspiration have made us reach out for these glories.

T.PRANAY

19H51A04L7

DECLARATION

We hereby declare that results embodied in this Report of Project on “**DESIGN OF 6T SRAM USING ADIABATIC LOGIC**” are from work carried out by using partial fulfillment of the requirements for the award of B. Tech degree. We have not submitted this report to any other university/institute for the award of any other degree.

Signature

T.PRANAY

19H51A04L7

ABSTRACT

This paper presents “**DESIGN OF 6T SRAM USING ADIABATIC LOGIC**”, where the performance of the conventional 6T SRAM circuit is compared with the performance of the Adiabatic 6T SRAM. In the adiabatic SRAM, a good high degree of power reduction is reported. By applying the aforementioned technique the same SRAM is investigated by varying technology. Other parameters such as delay and power delay product (PDP) have also been calculated for all the SRAM. SRAM is designed to provide an interface with the CPU and to replace DRAM in systems that require very low power consumption. An SRAM cell must meet the requirements for the operation in submicron/nano ranges. The Scaling of CMOS technology has significant impacts on SRAM cell—random fluctuation of electrical characteristics and substantial leakage current. The random fluctuation of electrical property causes the SRAM cell to have a huge mismatch in transistor threshold voltage. Consequently, the static noise margin (Read Margin) and the write margin are degraded dramatically. The requirements of low-power integrated circuits are very important in all electronic portable equipment. Normally SRAM consumes more power during read and writes operations, because of more power consumption speed of the circuit will be reduced and finally, the performance will be degraded. To reduce power consumption and increase RNM (Read Noise Margin) the adiabatic change of word line voltage is used in single-bit line SRAM and also sense amplifier flip flop and pre-charge circuit is used. During the read operation, the pre-charge circuit is connected with selective bit lines to minimize the overall RAM power consumption and a sense amplifier flip-flop is used to increase the speed of the operation. Using adiabatic circuits in single-bit line SRAM, the power consumption is reduced from 80% to 50%.

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CHAPTER-1

INTRODUCTION

1.1 INTRODUCTION

Nowadays one of the widely used electronic devices or electronic circuits is SRAM. Stability in SRAM when designed using Complementary Metal–Oxide– Semiconductor (CMOS) technologies generally depends on the SNM. SRAM memory technology is used because of its speed and robustness. As the device is scaled down in size several design challenges arise in the nanometer-size SRAM design. In an SRAM cell operation generally, supply voltage scaling is performed. The minimum voltage also referred to as DRV is the need for an SRAM cell to store the data. Reducing the VDD reduces subthreshold leakage current and gate leakage. For analyzing high-speed SRAM calculation of read margin and WM is necessary. A significant vision in this paper is to analyze 6T SRAM cells based on noise marginal by evaluating the DRV, Read Margin and Write Margin. Nowadays focus is on low supply voltage which reduces the SNM. The stability of SRAM cells can be analyzed based on the SNM value because performance is proportional to the SNM. Therefore as SNM reduces the performance of SRAM cells also reduces or vice versa. For improving the performance of a 6T SRAM cell parameter such as Cell Ratio (CR), Pull up Ratio (PR), and Voltage Supplies (VDD) is generally considered. SRAM design Methodology is provided and SRAM's Simulation Results are explained in detail.

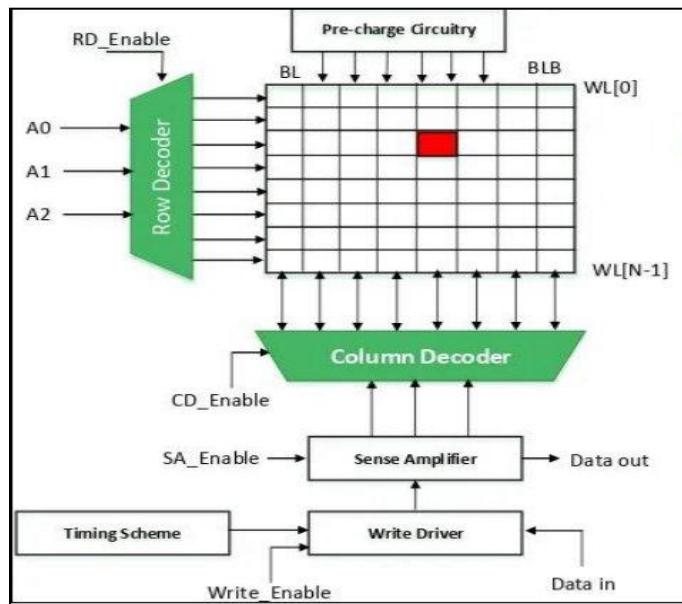


Fig.1.1 Block diagram of 6T SRAM cell

CMOS

The term CMOS stands for “Complementary Metal Oxide Semiconductor”. CMOS technology is one of the most popular technologies in the computer chip design industry and is broadly used today to form integrated Circuits in numerous and varied applications. Today's computer memories, CPUs and cellphones make use of this technology due to several key advantages. This technology makes use of both P-channel and N-channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology.

This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits (ASICs). The main Advantage of CMOS over NMOS and BIPOLEAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLEAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit switches. This allows the integrating of more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide Semiconductor transistors consist of P-channel MOS (PMOS) and N-channel MOS (NMOS).

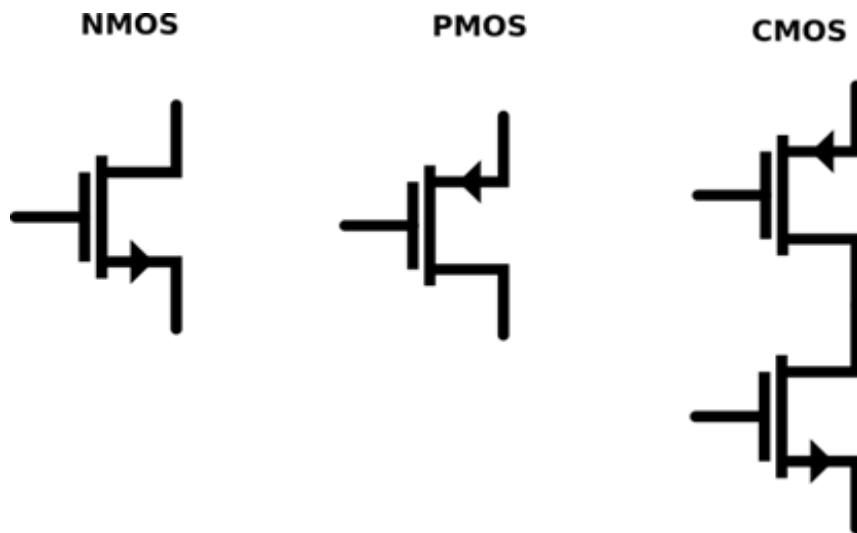


Fig.1.2 The NMOS symbol, PMOS symbol and CMOS symbol

NMOS

NMOS is built on a p-type substrate with an n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes. N-type metal-oxide-semiconductor logic uses n-type -MOSFETs (metal-oxide-semiconductor field-effect transistors) to implement logic gates and other digital circuits. These nMOS transistors operate by creating an inversion layer in a p-type transistor body. This inversion layer, called the n-channel, can conduct electrons between n-type "source" and "drain" terminals. The n-channel is created by applying a voltage to the third terminal, called the gate. Like other MOSFETs, nMOS transistors have four modes of operation: cut-off (or subthreshold), triode, saturation (sometimes called active), and velocity saturation.

For many years, NMOS circuits were much faster than comparable PMOS and CMOS circuits, which had to use much slower p-channel transistors. It was also easier to manufacture NMOS than CMOS, as the latter has to implement p-channel transistors in special n-wells on the p-substrate. The major drawback with NMOS (and most other logic families) is that a DC current must flow through a logic gate even when the output is in a steady state (low in the case of NMOS). This means static power dissipation, i.e. power drain even when the circuit is not switching.

MOS logic utilizes n-type MOSFETs to operate by making an inversion layer within a p-type transistor. This layer is known as the n-channel layer which conducts electrons among n-type-like source & drain terminals. This channel can be created by applying voltage toward the 3rd terminal namely the gate terminal. Similar to other metal oxide semiconductor field-effect transistors, nMOS transistors include different operation modes like a cut-off, triode, saturation & velocity saturation.

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The logic family of NMOS utilizes N-channel MOSFETS. NMOS devices (N-channel MOS) need a smaller chip region for each transistor as compared to P-channel devices, where NMOS gives a higher density. The NMOS logic family gives high speed too because of the high mobility of the charge carriers within N-channel devices.

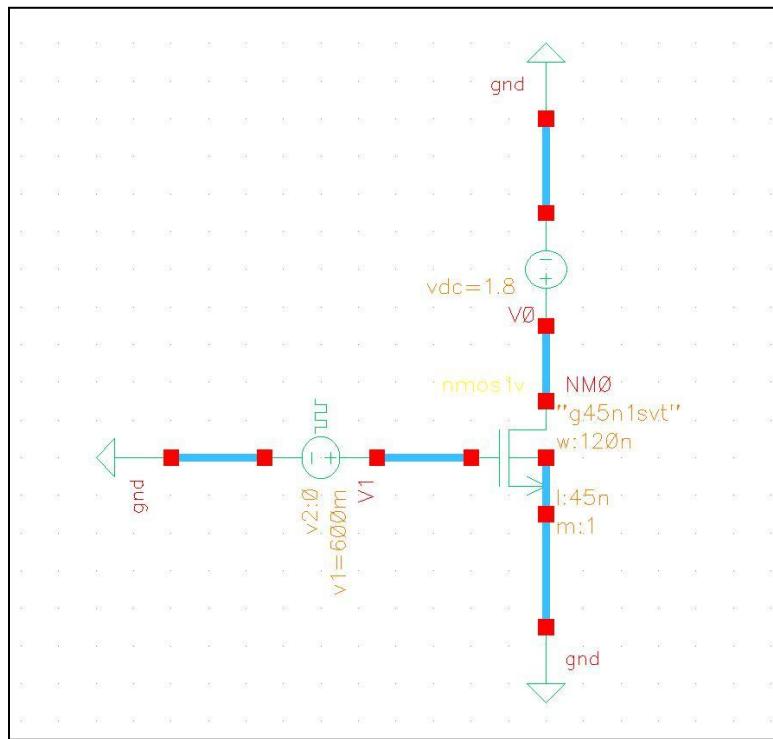


Fig.1.3 Schematic of NMOS

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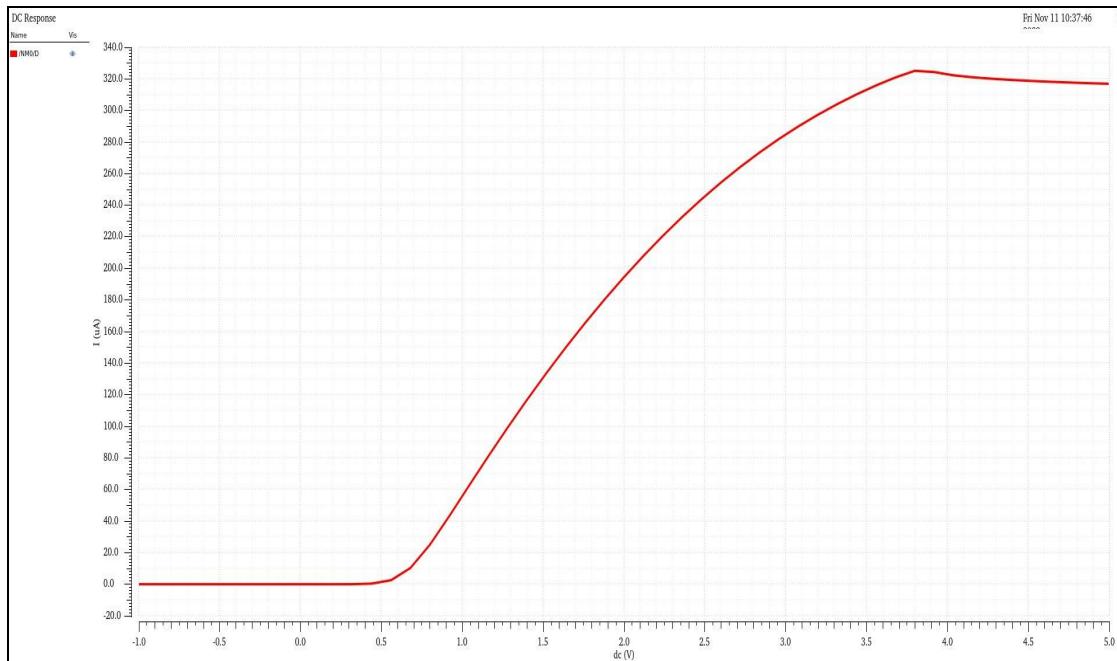


Fig.1.4 DC Response of NMOS

PMOS

P-channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. PMOS devices are more immune to noise than NMOS devices.

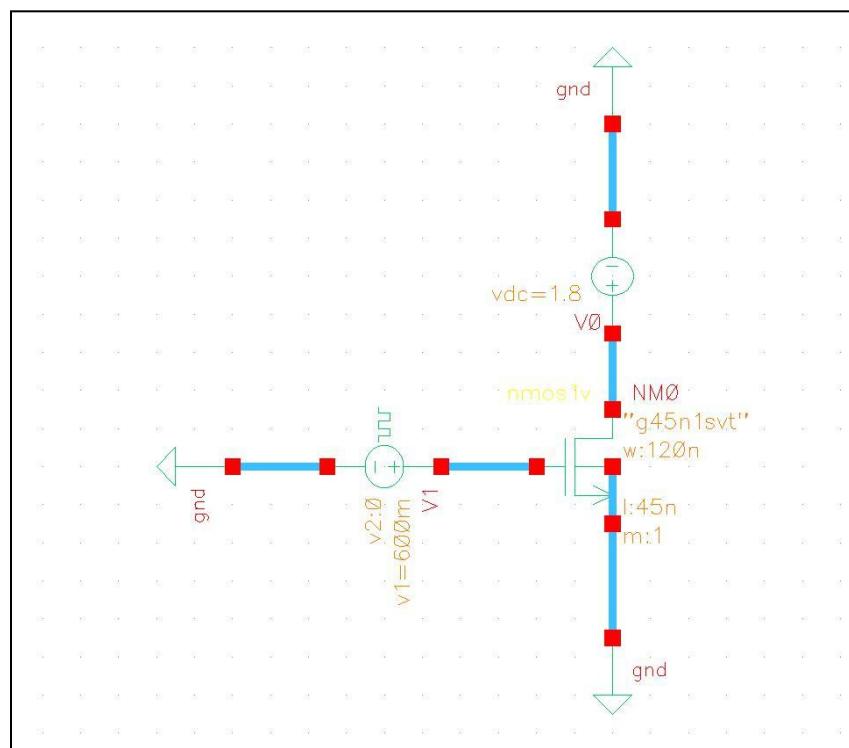
PMOS logic (from P-channel metal–oxide–semiconductor) is a family of digital circuits based on p-channel, enhancement mode metal–oxide–semiconductor field-effect transistors (MOSFETs). PMOS circuits have a number of disadvantages compared to the NMOS and CMOS alternatives, including the need for several different supply voltages (both positive and negative), high-power dissipation in the conducting state, and relatively large features. Also, the overall switching speed is lower. PMOS uses p-channel (+) metal-oxide-semiconductor field effect transistors (MOSFETs) to implement logic gates and other digital circuits. PMOS transistors operate by creating an inversion layer in an n-type transistor body. This inversion layer, called the p-channel, can conduct holes

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between p-type "source" and "drain" terminals. The p-channel is created by applying a negative voltage (-25V was common) to the third terminal, called the gate.

Like other MOSFETs, PMOS transistors have four modes of operation: cut-off (or subthreshold), triode, saturation (sometimes called active), and velocity saturation. While PMOS logic is easy to design and manufacture (a MOSFET can be made to operate as a resistor, so the whole circuit can be made with PMOSFETs), it has several shortcomings as well. The worst problem is that there is a direct current (DC) through a PMOS logic gate when the so-called "pull-up network" (PUN) is active, that is, whenever the output is high, which leads to static power dissipation even when the circuit sits idle.

Also, PMOS circuits are slow to transition from high to low. When transitioning from low to high, the transistors provide low resistance, and the capacitive charge at the output accumulates very quickly (similar to charging a capacitor through a very low resistance). But the resistance between the output and the negative supply rail is much greater, so the high-to-low transition takes longer (similar to discharge of a capacitor through a high resistance). Using a resistor of lower value will speed up the process but also increases static power dissipation.



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Fig.1.5 Schematic of PMOS

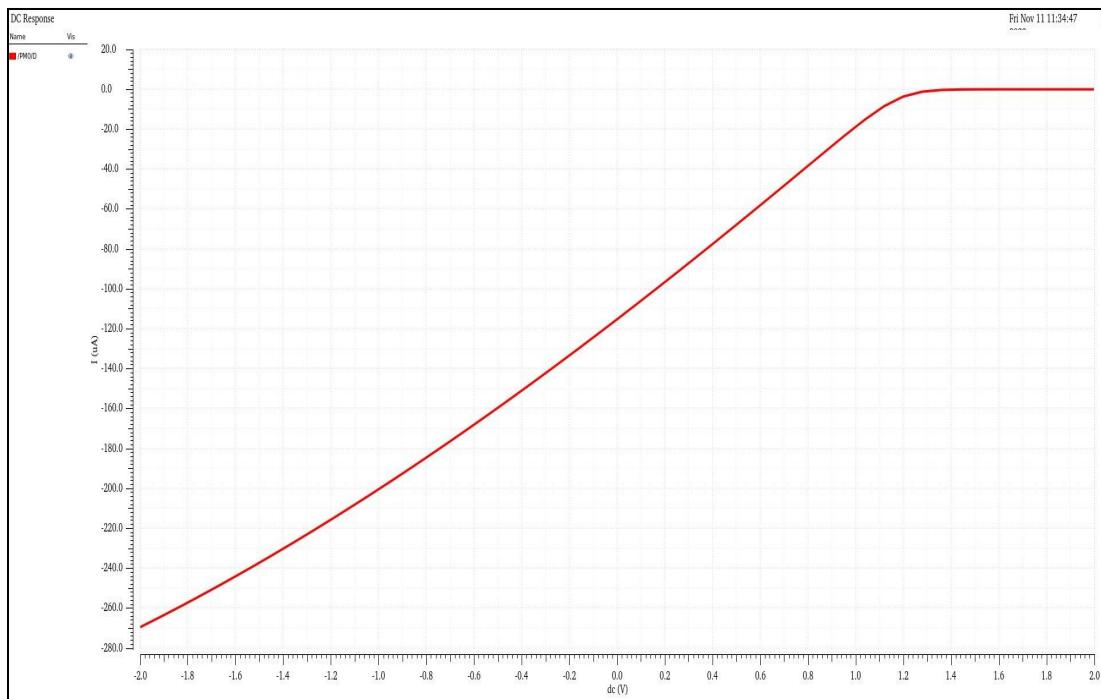


Fig.1.6 DC Response of PMOS

1.2 HISTORICAL PERSPECTIVE

Semiconductor bipolar SRAM was invented in 1963 by Robert Norman at Fairchild Semiconductor. MOS SRAM was invented in 1964 by John Schmidt at Fairchild Semiconductor. It was a 64-bit MOS p channel SRAM.

SRAM has been the main driver behind any new CMOS-based technology fabrication process since 1959 when CMOS was invented. In 1965, Arnold Farber and Eugene Schlig, working for IBM, created a hard-wired memory cell, using a transistor gate and tunnel diode latch. They replaced the latch with two transistors and two resistors, a configuration that became known as the Farber-Schlig cell. In 1965, Benjamin Augusta and his team at IBM created a 16-bit silicon memory chip based on the Farber-Schlig cell, with 80 transistors, 64 resistors, and 4 diodes.

1.3 EXISTING METHODOLOGY

For nearly 40 years CMOS devices have been scaled down in order to achieve higher

speed, performance and lower power consumption. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. As process technology is scaled down, threshold voltage and leakage current variations are increased. In the conventional 6T cell, it is difficult to find an optimum design because both read stability and write margin must be considered. At low supply voltage, 6T cells worsen in read stability. Leakage power is a high-priority consideration due to feature scaling in high-performance processor design. In today's processors, the leakage power of the cache was a major source of power dissipation because the cache occupies more than 50% of the chip area. Low leakage SRAM design has been an active area of research over the past years. Low Power and high stability have been the main themes of SRAM designs in the last decade.

1.4 OBJECTIVES

1. To design low-power SRAM memory cells, we are using a 6T configuration at 45nm (where T represents the transistor) using Cadence Virtuoso.
2. To analyze the static noise margin of the SRAM cell.
3. To implement SRAM using Adiabatic Technology.
4. Calculate and compare the Power consumption of 6T and 6T using Adiabatic.

To reduce power consumption and increase RNM (Read Noise Margin) the adiabatic change of word line voltage is used in single-bit line SRAM and also sense amplifier flip flop and the pre-charge circuit is used. During the read operation, the pre-charge circuit is connected with selective bit lines to minimize the overall RAM power consumption and a

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sense amplifier flip-flop is used to increase the speed of the operation. Using adiabatic circuits in single-bit line SRAM, the power consumption is reduced.

CHAPTER-2

LITERATURE SURVEY

2.1 REVIEW OF THE LITERATURE

Shunji Nakata,2008 [1]: An adiabatic quasi 6T-SRAM is proposed in which a memory cell shares the writing and reading ports between a flip-flop and a bit line so that the transistor number in a memory cell is decreased to about six. The gradual charging operation in the circuit can avoid electromigration and hot carrier effects. In the writing mode, the voltage of the memory cell power line is reduced to the ground gradually by using a high-resistivity nMOSFET, and the nMOSFET is turned off to set the memory cell power line in a high-impedance state. Then, an adiabatic signal from the shared writing port is input to charge the memory cell power line to VDD. In the reading mode, the shared reading port, which connects the flip-flop and the bit line, is used for stable operation. The bit line can be precharged to a small value (for example, $VDD/4$), which

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enables a small current flow during the reading mode. Logic data are read by sensing the voltage decrease in the precharged bit line.

M.Durgadevi, R. Lavanya,2015 [2]: The requirements of low-power integrated circuits are very important in all electronic portable equipment. NormallySRAM consumes more power during read and writes operations because more power consumption speed of the circuit will be reduced and finally the performance will be degraded. To reduce power consumption and increase RNM (Read NoiseMargin) the adiabatic change of word line voltage is used in single-bit line SRAM and also sense amplifier flip flop and the pre-charge circuit are used. During read operation pre-Charge circuit is connected with selective bit lines to minimize the overall RAM power consumption and a sense amplifier flip-flop is used to increase the speed of the operation. Using adiabatic circuits in single-bit line SRAM, the power consumption is reduced from 80% to 50%.

P. Sasipriya,2017 [3]: This paper presents the quasi-adiabatic logic for low power powered by two-phase sinusoidal clock signals. The proposed logic called two-phase adiabatic dynamic logic (2PADL) realizes the advantages of energy efficiency through the use of gate overdrive and reduced switching power. It has a single rail output and the proposed logic does not require complementary input signals for any of its variables. The 2PADL logic is operated by two complementary clock signals acting as a power supply. The validation of the proposed logic is carried out through practical circuits such as (i)sequential circuits using an energy recovery technique suitable for memory circuits, (ii)an adiabatic carry look-ahead adder (CLA) designed using 2PADL to study the speed performance and prove its energy efficiency across a range of frequencies and (iii) a multiplier circuit using 2PADL compared against CMOS counterpart. The CLA adder is also implemented using the other static adiabatic logics, namely, quasi-static energy recovery logic (QSERL), clocked CMOS adiabatic logic (CCAL) and conventional static CMOS logic to compare against 2PADL and validate its power advantages. The performance of the CCAL logic is tested for higher frequencies by implementing the widely presented CLA circuit. The result proves that the design is energy efficient and operates up to the frequency of 600 MHz. The simulation was

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carried out using the industry-standard Cadence Virtuoso tool using 180nm technology library files.

Savitha S, Rajani,2018[4]: In the VLSI era, compact electronic devices are popular. The reliability and durability of such compact devices rely on low power utilization. The purpose of this project was to implement a low-power adiabatic Static Random Access Memory (SRAM), with the following objectives - To reduce the power waste by means of stepwise charging using tank capacitors which is an adiabatic way of generating a power clock. This method is capable of recuperating the electrical energy back to the source. Further to examine the Static Noise Margin (SNM) – a parameter that gives detailed information about the cell stability – in contrast with conventional 6T, 7T and 8T topologies of SRAM under 180 nm technology. Finally, SNM variations with respect to process parameters are also discussed. All the implementations and analyses were made using the CADENCE tool and MATLAB tool.

C Anudeep Varma and P Sasipriya,2018[5]: In this paper the design of low power SRAM has been presented. SRAM memory cells have been realized using adiabatic logic to achieve low power operation. Adiabatic SRAMhas been realized using two methods such as i) gradual charging and discharging of bit-line during writing mode and ii) utilizing control transistor based adiabatic circuit i.e., Two PhaseAdiabatic Dynamic Logic (2PADL) circuit for the design of memory cell. Furthermore, energy recovery of word line and bit line charge stored in the interconnect capacitances has been realized for the benefit of energy savings. Charge recovery circuits based on 2PADL has been employed in the proposed SRAM memory core to achieve energy recovery. SRAM memory array of (4×4) has been designed as a test circuit. All the circuits are implemented using 180nm CMOS technology and simulations are carried out using Cadence® Virtuoso tool. Simulation results prove that the proposed memory cell has a significant amount of energy savings when compared to the conventional static CMOS SRAM cell.

Ramya Sri Penugonda, V. Ravi,2020[6]: In VLSI system design power consumption

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and energy dissipation are becoming more important. To optimize the power consumption we are using adiabatic logic which has the capability of reusing power. In this paper we proposed a novel 7T SRAM cell using MCPL adiabatic logic. We compared the performance of energy dissipation and power consumption of conventional 7T SRAM and adiabatic SRAM. Furthermore, the conventional 6T,7T SRAM cell and the designs which are related are designed using FINFET devices to achieve low power.7T SRAM is more stable compared to 6T SRAM but due to excess transistor in 7T SRAM the power consumption will be more. SRAM cells are designed in a cadence EDA environment and layouts for these circuits are carried out in cadence Assura tool.

P Vinay Kumar & Ashish Kumar,2021[7]:Static Random Access Memory (SRAM) has been an important memory deviceIn VLSI circuits. SRAM is used widely because of its huge storage capacity and can be accessed in less time with low power consumption.This paper presents design and implementation of 16 Bit 6T SRAM using different CMOS technologies using Cadence Virtuoso tool.Duet to the requirement of more storage, usage of16-bitSRAM is convenient.The performance analysis of SRAM with respect toPowerDissipationand Average Delay is observed and compared.

Yasuhiro Takahashi, Nazrul Anuar Nayan,2014[8]:In this paper, the authors propose a novel static random access memory (SRAM) that employs the adiabatic logic principle. To reduce energy dissipation, the proposed adiabatic SRAM is driven by two trapezoidal-wave pulses. The cell structure of the proposed SRAM has two high-value resistors based on a p-type metal-oxide semiconductor transistor, a cross-coupled n-type metal-oxide semiconductor (NMOS) pair and an NMOS switch to reduce the short-circuit current. The inclusion of a transmission-gate controlled by a write word line signal allows the proposed circuit to operate as an adiabatic SRAM during data writing. Simulation results show that the energy dissipation of the proposed SRAM is lower than that of a conventional adiabatic SRAM.

Irfan M. Trasgar & Dr. H P. Rajani,2019[9]:The need for power efficient, optimal area IC's are always in demand, hence there is a need for compact electronic devices or chips.

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We can say that a device is compact if the durability and reliability are good, which in-turn depend on low power consumption. The main aim of this work is to implement SRAM (Static Random Access Memory) cell (6T-SRAM) using Conventional and Adiabatic logic where different power consumption parameters like static power consumption, dynamic power consumption, average power, peak power, energy consumption, total power dissipation are tested and compared.

Shobha Goutam & D. K.Mishra,2013[10]:This paper presents the design of an Adiabatic SRAM with a bit line driver that reduces power dissipation by efficiently recovering energy from the bit capacitors in 180nm technology. Cadence simulation of a simple 1 bit Asymmetrical Adiabatic SRAM, that includes the energy recovering bit line drivers, and the sense amplifiers, show over 35% of power savings at 1.8V, in comparison with its conventional counterpart.

CHAPTER 3

TECHNICAL APPROACH

3.1 IDENTIFICATION OF SOFTWARE ASPECTS

Cadence is a leading provider of EDA and semiconductor IP. Our custom/analogue tools help engineers design the transistors, standard cells, and IP blocks that make up SoCs. Cadence also offers a growing portfolio of design IP and verification IP for memories, interface protocols, analogue/mixed-signal components, and specialized processors. And reaching up to the systems level, Cadence offers an integrated suite of hardware/software

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co-development platforms. In short, Cadence technology helps customers build great products that connect the world. We are going to use cadence technology and in that, and by using CMOS technology we will implement a 6T SRAM cell.

Cadence enables electronic systems and semiconductor companies to create innovative end products that transform how people live, work and play. Cadence software, hardware and semiconductor IP are used by customers to deliver products to market faster. The company's System Design Enablement strategy helps customers develop differentiated products from chips to boards to systems—in mobile, consumer, cloud datacenter, automotive, aerospace, IOT, industrial and other market segments. Cadence is listed as one of Fortune Magazine's 100 Best Companies to Work.

3.2 CADENCE TOOL IN VLSI

The tool depends on the hierarchy level of your design.

- Composer -> Schematic editor
- Virtuoso -> Layout editor
- Analog Artist → Preparing simulation (SpectreS in this tutorial)
- DIVA → Design Rule Check (DRC) , Layout Versus Schematic Check (LVS), Extraction

3.3 DESIGN FLOW

The following figure shows some of the steps in designing integrated circuits in the Cadence environment

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

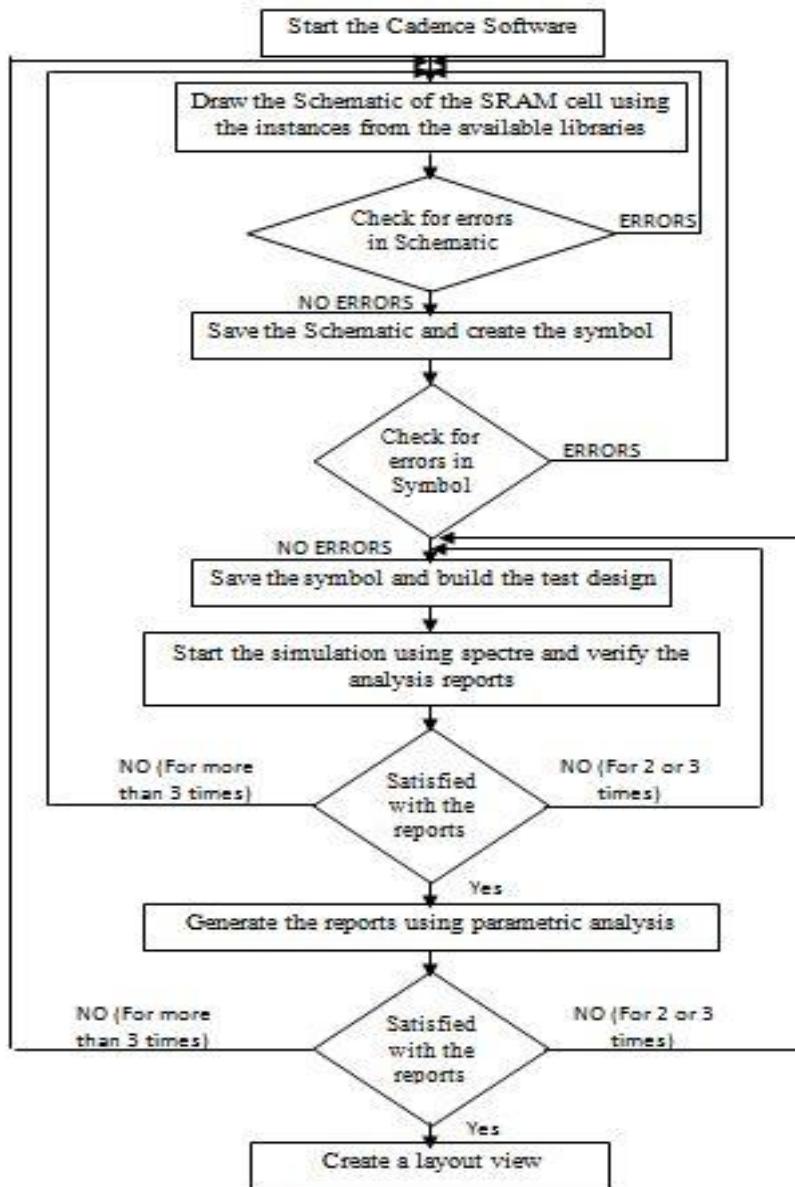


Fig.3.1 Design Flow

3.4 SCHEMATIC AND SYMBOL TOOLS

To create the schematic the tool Virtuoso Schematic Composer is used. This editor is an interactive system for building schematics by instantiating some basic components and connecting them to each other. The values (properties) of the components can be edited to

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

suit the specifications. Text and comments can also be included. The editor will also create symbols of the cells so that they can be used in other parts of the construction.

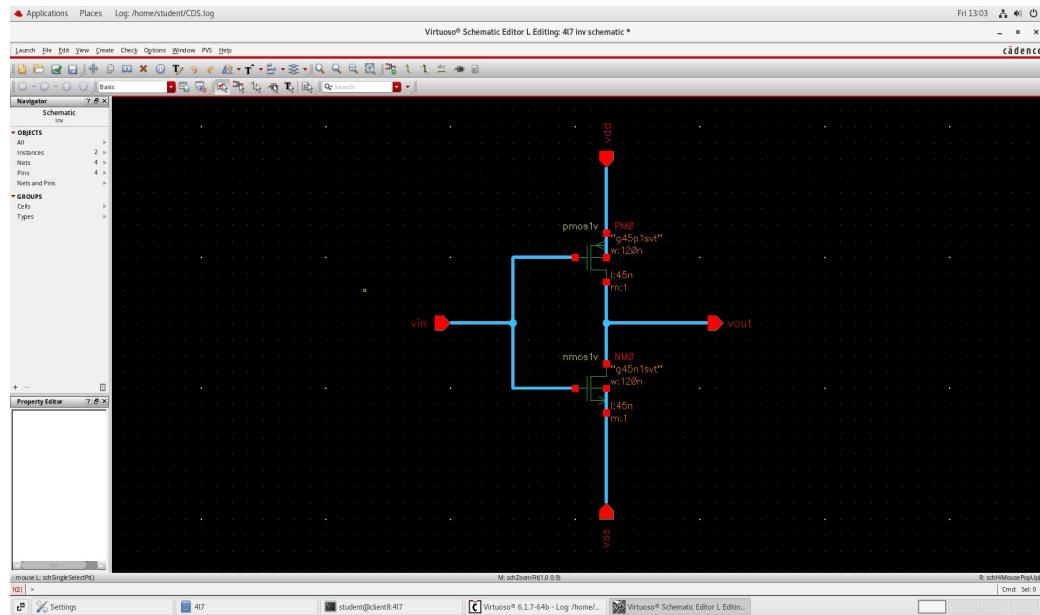


Fig.3.2 Schematic View

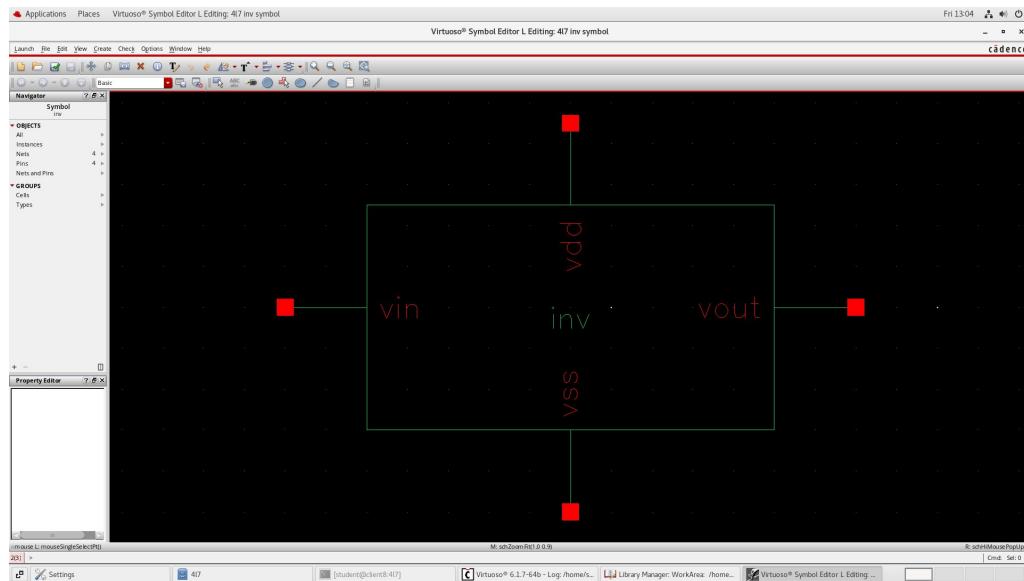


Fig.3.3 Symbol View

3.5 SIMULATION

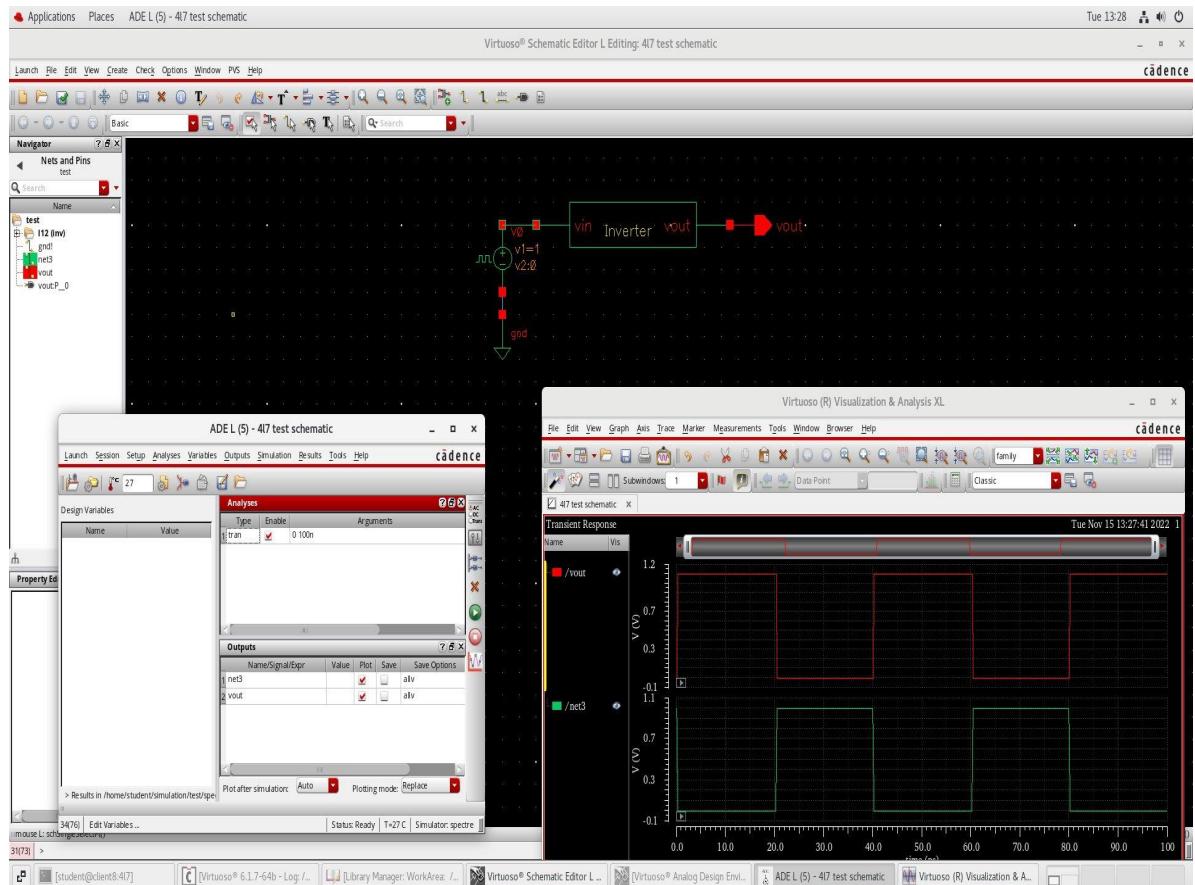
The simulation tool is started directly from the schematic editor and all the necessary netlists describing the design will be created. A simulation is usually performed in a test bench, which is also a schematic, with the actual design included as an instance. The test

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

bench also includes signal sources and a power supply. By using parameters for the properties of the components used it is possible to quickly analyze the design for a wide range of variables.

The simulator is run from within Affirma Analog Circuit Design Environment which is a tool that handles the interface between the user and the simulator. The simulator offers a wide range of analyses (DC, frequency sweep, transient, noise, etc.) and the results can be presented graphically and saved.

Fig.3.4 Simulation of Inverter



3.6 LAYOUT EDITOR

1. The most important factor determining the actual layout is the signal flow.

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

2. The signal flow diagram is just a concept that you can visualize for a particular circuit.
3. The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects.
4. A tool built into the Layout Editor, called Design Rule Checker, is used to detect any design rule violations during and after the mask layout design.
5. The mask layout only contains physical data. (In fact, it just contains coordinates of rectangles drawn in different layers).
6. The extraction process identifies the devices and generates a netlist associated with the layout.

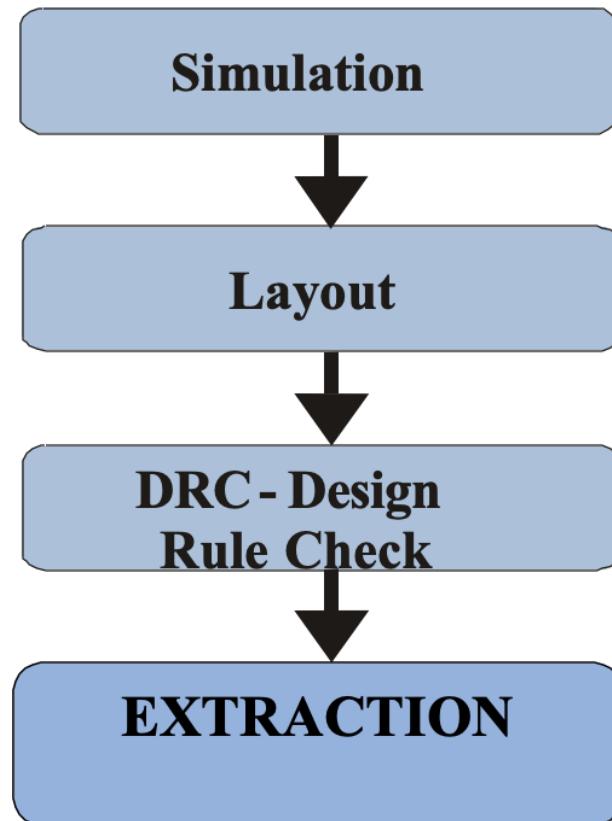


Fig.3.5 Layout Editor

3.7 ANALOG ARTIST (Preparing Simulation)

Steps of Post Layout Simulation

1. Extracting from the Layout
2. The Extracted Cell View
3. Layout Versus Schematic
4. Summary of the Cell Views
5. Simulating the Extracted CellView

3.8 DIFFERENT TYPES OF CELL VIEWS IN CADENCE

1. Schematic View

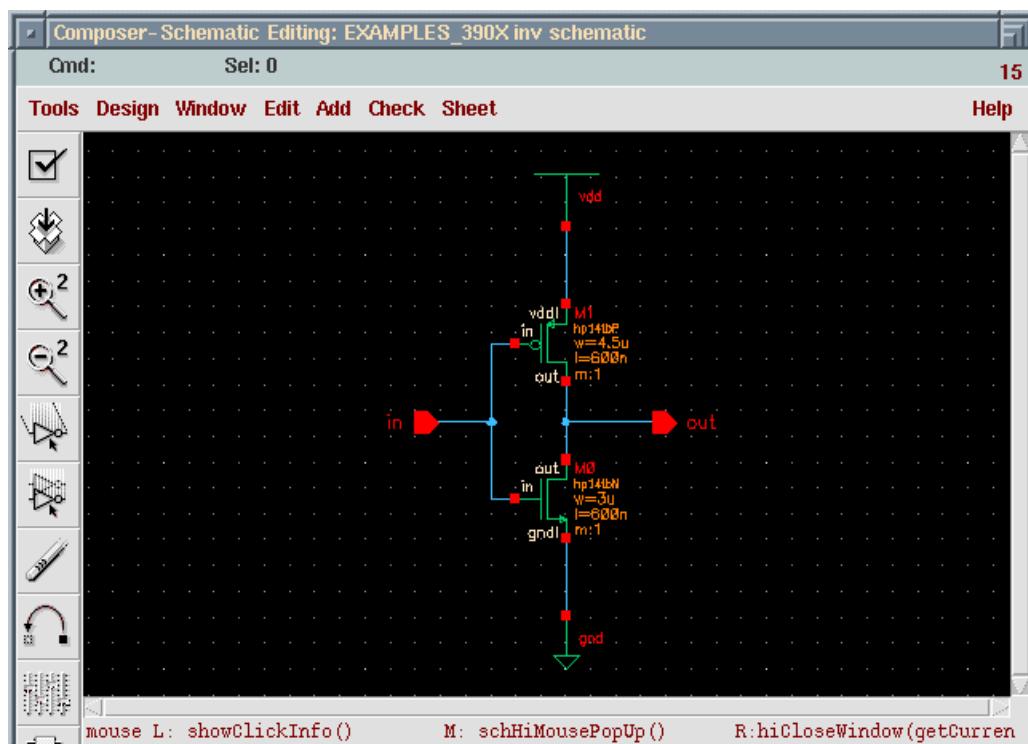


Fig.3.6 Schematic view

2. Symbol view

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

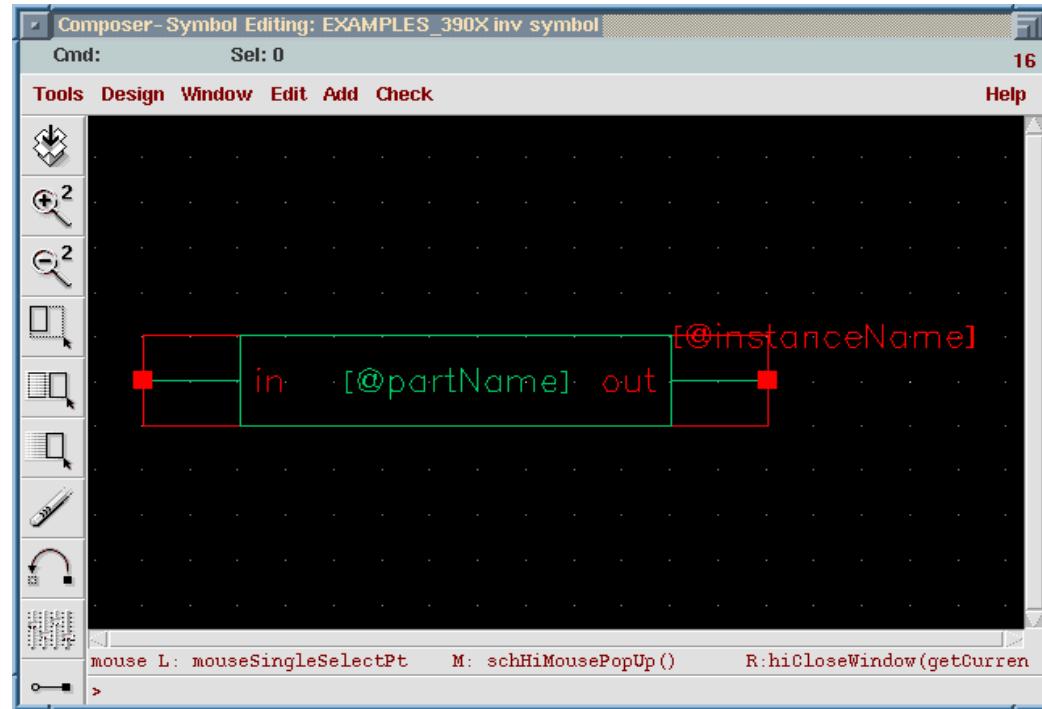


Fig.3.7 Symbol view

3. Layout view

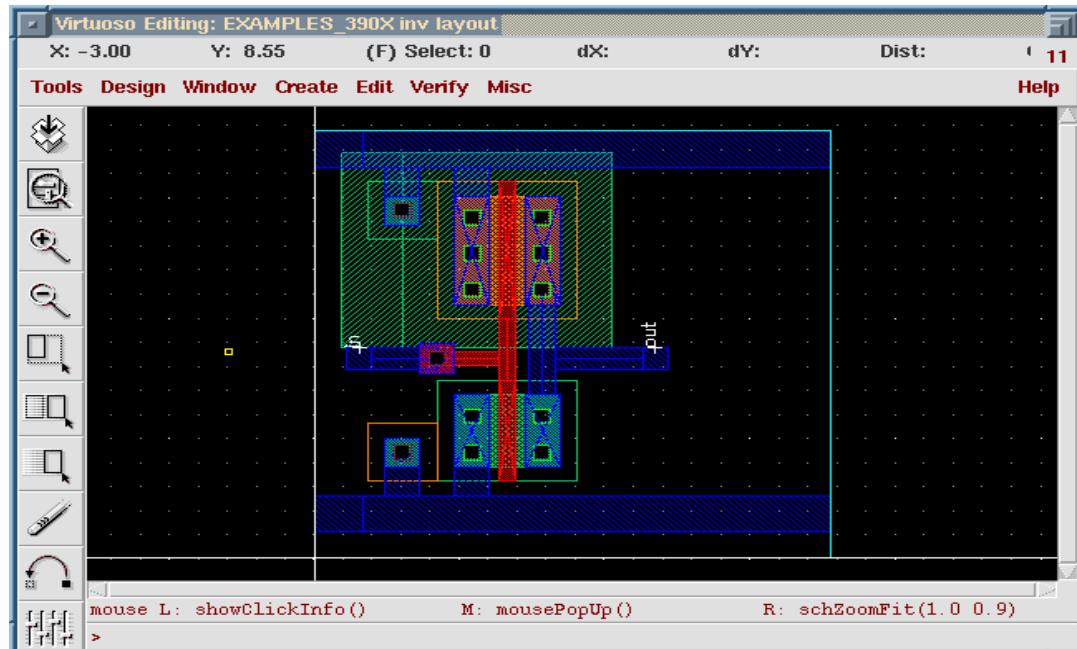


Fig.3.8 Layout view

4. Extracted view

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

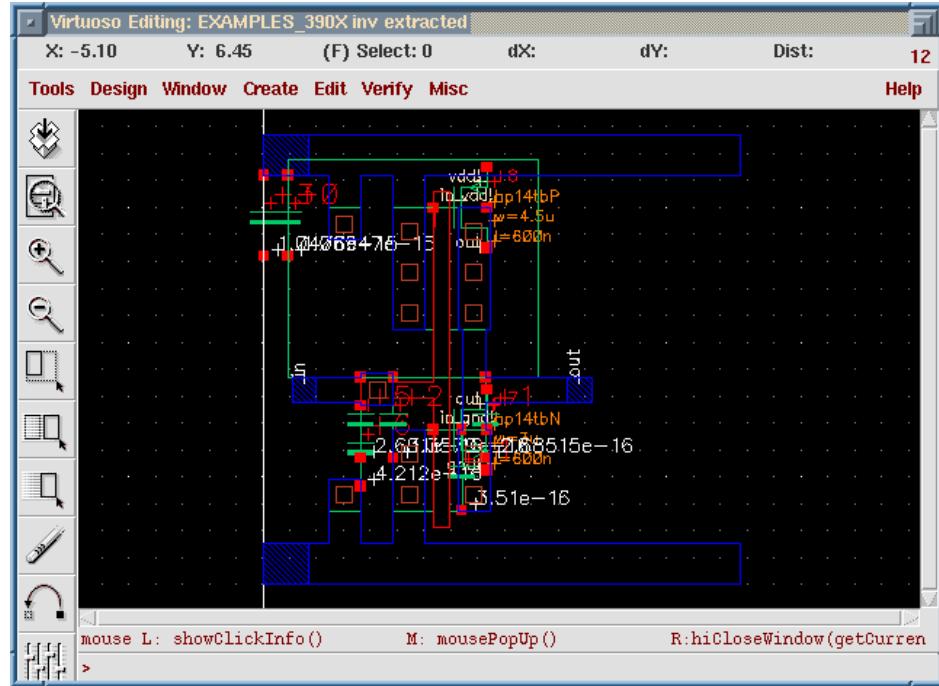


Fig.3.9 Extracted view

5. Test schematic view

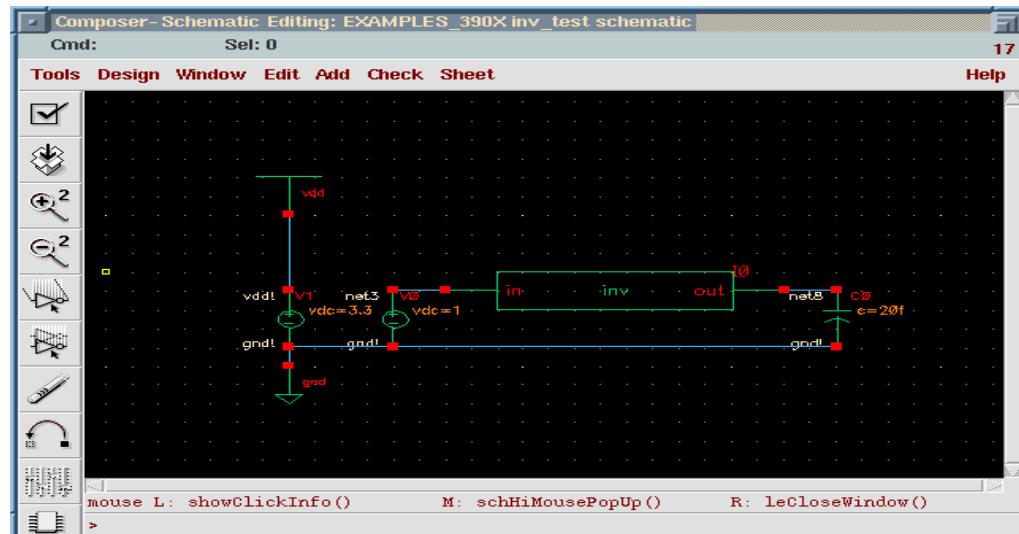


Fig.3.10 Test schematic view

3.9 CALCULATION OF POWER CONSUMPTION

There are mainly three types of power dissipation in a CMOS-based circuit:

1. Static power dissipation
2. Dynamic power dissipation
3. Short circuit dissipation.

3.9.1 Static Power Dissipation

It is related to the logical states of the circuit rather than switching activities. In CMOS logic, leakage current is the only source of static power dissipation.

When the input = '0', the associated n-device is off and the p-device is on. The output voltage is V_{dd} or logic '1'. When the input = '1', the associated n-device is on and the p-device is off. The output voltage is '0' volts or V_{ss} . From Figure 2 it can be seen that one of the transistors is always off when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no Dc path from V_{dd} to V_{ss} the resultant steady-state current and the power P_s are zero.

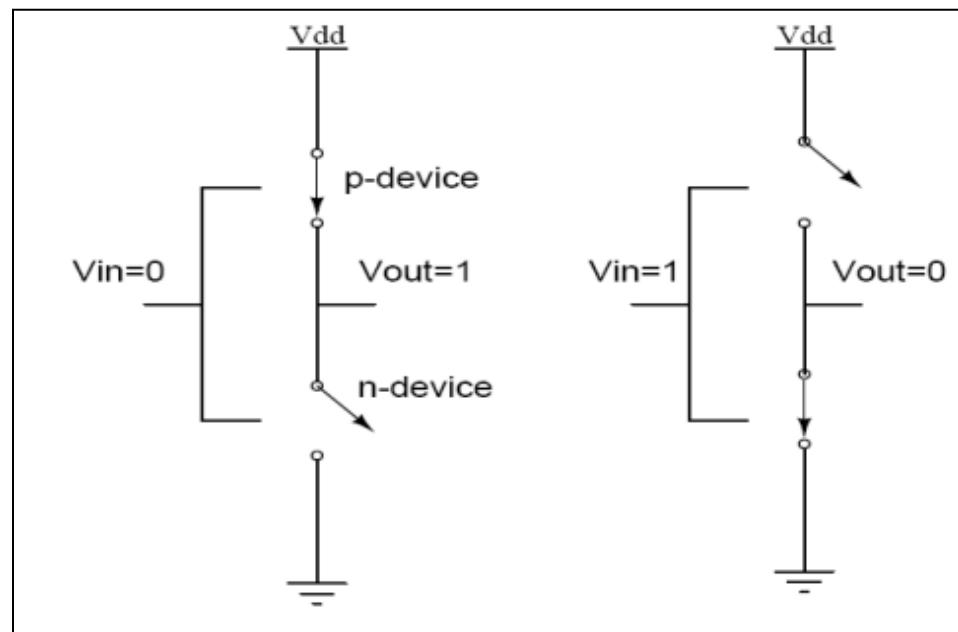


Fig.3.11 CMOS inverter model for static power dissipation

The static power components become important when the circuits are at rest, i.e. when there is no activity in the circuits and they are all biased to a specific state of the circuit. The static power dissipation mainly includes

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

- Reverse bias-pn junction leakage current
- Subthreshold leakage current
 - Drain-induced barrier lowering
 - V_{th} roll off
 - Effect of operating temperature
- Tunneling into and through gate oxide leakage current
- Leakage current due to hot carrier injection from the substrate to gate oxide
- Leakage current due to gate-induced drain lowering (GIDL)

1. Reverse-Bias pn Junction Leakage Current

The drain/source and substrate junctions in a MOS transistor are reverse-biased during transistor operation. This results in reverse-biased leakage current in the device. This leakage current can be due to the drift/diffusion of minority carriers in the reverse-biased region and electron-hole pair generation due to the avalanche effect. The pn junction reverse-biased leakage current depends on doping concentration and junction area.

For heavily doped pn junction of drain/source and substrate regions, the band-to-band tunneling (BTBT) effect dominates the reverse bias leakage current. In band-to-band tunneling, electrons tunnel directly from the valence band of the p region to the conduction band of the n region. BTBT is visible for electric fields greater than 10^6 V/cm.

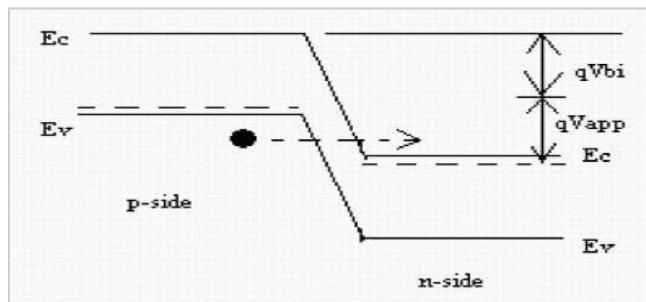


Fig.3.12 Band-to-band tunneling in reverse-biased pn junction of a MOS transistor.

2. Subthreshold Leakage Current

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When the gate voltage is less than the threshold voltage (V_{th}) but greater than zero, the transistor is said to be biased in the subthreshold or weak inversion region. In a weak inversion, the concentration of minority carriers is small but not zero. In such a case, for typical values of $|V_{DS}| > 0.1V$ and the entire voltage drop takes place across the drain-substrate pn junction.

The electric field component between the drain and source, parallel to the Si-SiO₂ interface, is small. Due to this negligible electric field, the drift current is negligible and the subthreshold current mainly consists of diffusion current.

a. Drain-Induced Barrier Lowering (DIBL)

Subthreshold leakage current is mainly due to drain-induced barrier lowering or DIBL. In short channel devices, the depletion region of drain and source interact with each other and reduce the potential barrier at the source. The source is then able to inject charge carriers into the surface of the channel resulting in subthreshold leakage current.

DIBL is pronounced in high drain voltages and short channel devices.

b. V_{th} Roll Off

The threshold voltage of MOS devices reduces due to channel length reduction. This phenomenon is called V_{th} roll-off (or threshold voltage roll-off). In short channel devices, the drain and source depletion region enter further into the channel length, depleting a part of the channel.

Due to this, a lesser gate voltage is required to invert the channel reducing the threshold voltage. This phenomenon is pronounced for higher drain voltages. The reduction in threshold voltages increases the subthreshold leakage current as the subthreshold current is inversely proportional to the threshold voltage.

c. Effect of Operating Temperature

Temperature also plays a part in leakage current. Threshold voltage decreases with increasing temperature. Or, in other words, the subthreshold current increases with increasing temperature.

3. Tunneling into and Through Gate Oxide Leakage Current

In short channel devices, a thin gate oxide results in high electric fields across the SiO₂ layer. Low oxide thickness with high electric fields results in electrons tunneling from the substrate to the gate and from the gate to the substrate through the gate oxide, resulting in gate oxide tunneling current.

Consider the energy band diagrams as shown

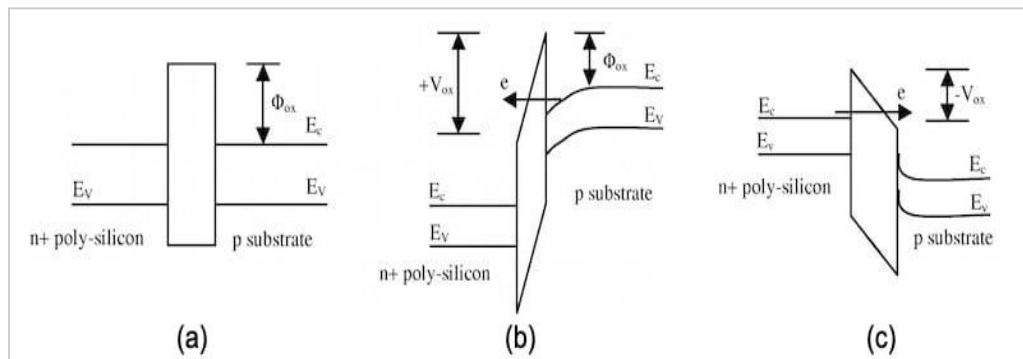


Fig.3.13 Energy band diagrams of MOS transistors with (a) flat band, (b) a positive gate voltage, and (c) a negative gate voltage

The first diagram, Figure 3.13(a), is of a flat band MOS transistor, i.e., where there is no charge present in it.

When the gate terminal is positively biased, the energy band diagram changes as shown in the second diagram, Figure 3.13(b). The electrons at the strongly inverted surface tunnel into or through the SiO₂ layer giving rise to gate current.

On the other hand, when a negative gate voltage is applied, electrons from the n+ polysilicon gate tunnel into or through the SiO₂ layer giving rise to gate current, as shown in Figure 3.13(c).

4. Leakage Current Due to Hot Carrier Injection from the Substrate to Gate Oxide

In short channel devices, the high electric field near the substrate-oxide interface energizes the electrons or holes and they cross the substrate-oxide interface to enter the oxide layer. This phenomenon is known as hot carrier injection.

This phenomenon is more likely to affect electrons than holes. This is because electrons have a lesser effective mass and a lesser barrier height as compared to holes.

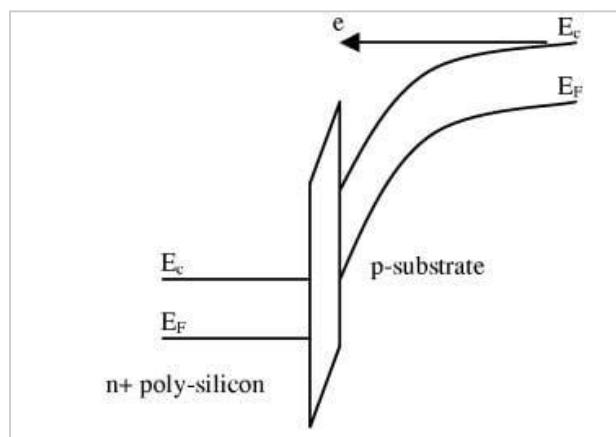


Fig.3.14 Energy band diagram depicting electrons gaining sufficient energy due to high electric field and crossing over the oxide barrier potential (hot carrier injection effect)

5. Leakage Current Due to Gate-Induced Drain Lowering (GIDL)

Consider an NMOS transistor with a p-type substrate. When there is a negative voltage at the gate terminal, positive charges accumulate just at the oxide-substrate interface. Due to the accumulated holes at the substrate, the surface behaves as a p-region more heavily doped than the substrate.

This results in a thinner depletion region at the surface along the drain-substrate interface (when compared to the thickness of the depletion region in the bulk).

Due to a thin depletion region and higher electric fields, the avalanche effect and band-to-band tunneling (as discussed in the first section of this article) take place. Thus,

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

minority carriers in the drain region underneath the gate are generated and are pushed into the substrate by the negative gate voltage. This adds to the leakage current.

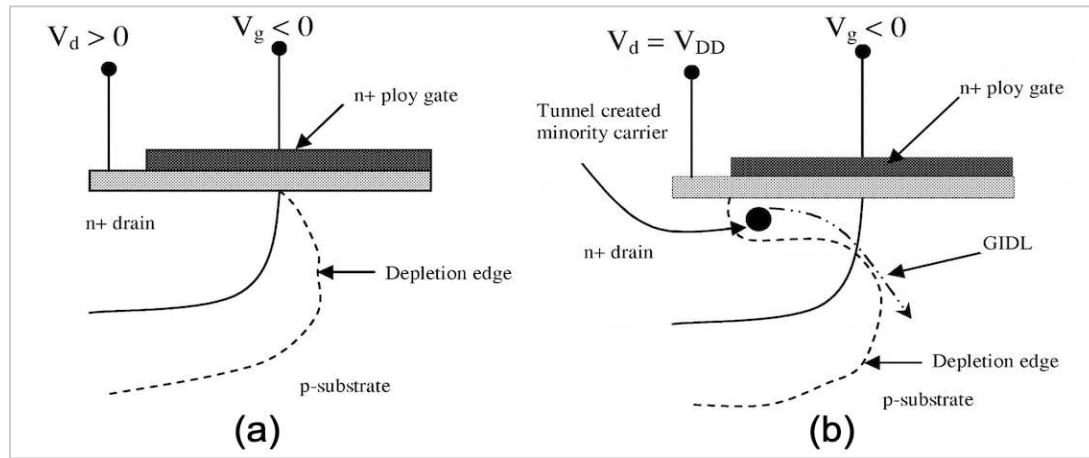


Fig.3.15 (a) Formation of thin depletion region at the drain-substrate interface along the surface and (b) flow of GIDL current due to carriers generated by avalanche effect and BTBT

6. Leakage Current Due to Punch-Through Effect

In short channel devices, due to the proximity of drain and source terminals, the depletion region of both the terminals come together and eventually merge. In such a condition, "punch-through" is said to have taken place.

The punch-through effect lowers the potential barrier for the majority of carriers from the source. This increases the number of carriers entering into the substrate. Some of these carriers are collected by the drain and the rest contribute to leakage current.

3.9.2 Dynamic Power Dissipation:

In Figure 3.16, During switching from '0' to '1' or '1' to '0', both n- and p-transistors are on for a short period of time. This results in a short current pulse from V_{dd} to V_{ss} . Current is also required to charge and discharge the output capacitive load. The current pulse from V_{dd} to V_{ss} results in 'short circuit dissipation' that is dependent on the input rise/fall time, the load capacitance and gate design.

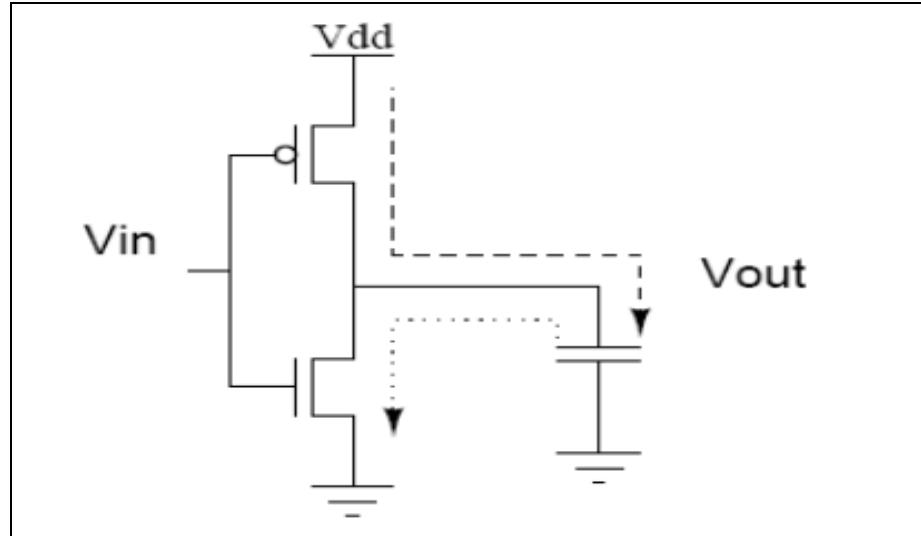


Fig.3.16 Power dissipation due to charging and discharging of capacitor

Dynamic power dissipation can be subdivided into three major categories: switched power dissipation, short circuit dissipation, and glitch power dissipation. All of them more or less depend on the signal, load capacitance, and supply voltage of the electronic circuit. The continuous charging and discharging of the load capacitance are necessary to transmit information in CMOS circuits

3.9.3 Short circuit power dissipation

This type of power dissipation takes place due to the large rise and fall time of the signal. This component of power dissipation occurs when the pull-up and pull-down networks both turn ON simultaneously. This can be minimized by reducing the rise and fall time and keeping both symmetrical.

$$P = P_{dyn} + P_{sc} + P_{leak}. \quad (1)$$

$$P_{dyn} = \alpha * C_L * V_{dd}^2 * f, \quad P_{sc} = I_{peak} * (V_{dd} - 2V_{th}) * T_{rise/fall} * f,$$

$$P_{leak} = V_{dd} * I_{(sl+gol)}.$$

where α =actively factor, f =frequency.

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The first term in equation (1) represents the dynamic power, where α is the switching activity, CL is the loading capacitance, f_{clock} is the clock frequency and V_{dd} supply voltage. The second term represents short circuit current I_{sc} which arises when both the NMOS and PMOS transistors are simultaneously active, resulting in conducting current directly from supply to ground. Last is leakage current leakage which can arise from substrate injection and sub-threshold effects are primarily determined by fabrication technology considerations.

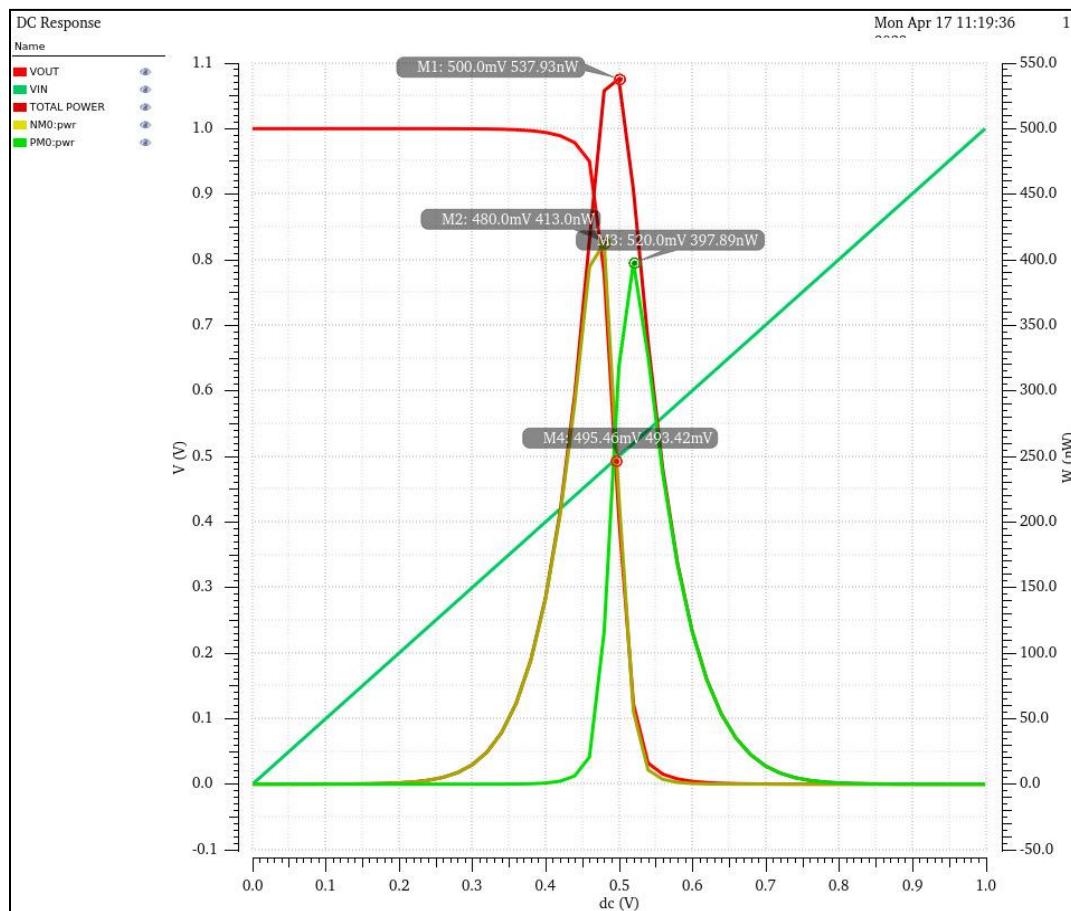


Fig.3.17 DC Characteristics and Power Consumption of Inverter.

CHAPTER-4

DESIGNING OF THE

PROJECT

4.1 SRAM CELL

Static RAMs use a memory cell with internal feedback that retains its value as long as power is applied. It has the following attractive properties:

1. Denser than flip-flops
2. Compatible with standard CMOS processes
3. Faster than DRAM
4. Easier to use than DRAM

For these reasons, SRAMs are widely used in applications from caches to register files to tables to scratchpad buffers. The SRAM consists of an array of memory cells along with the row and column circuitry. This section begins by examining the design and operation of each of these components. It then considers important special cases of SRAMs, including multi-ported register files, large SRAMs, and subthreshold SRAMs.

An SRAM cell needs to be able to read and write data and to hold the data as long as the power is applied. An ordinary flip-flop could accomplish this requirement, but the size is quite large. The 6T cell achieves its compactness at the expense of more complex peripheral circuitry for reading and writing the cells.

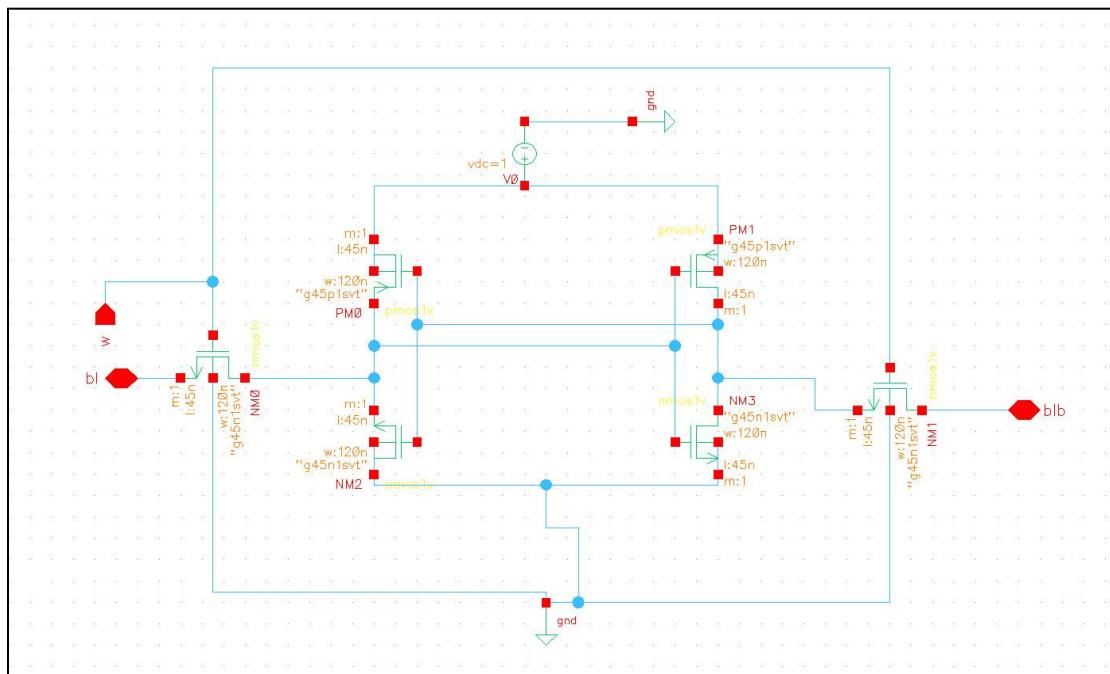


Fig.4.1 Schematic view of 6T SRAM cell

The 6T SRAM cell contains a pair of weak cross-coupled inverters holding the state and a pair of access transistors to read or write the state. The positive feedback corrects disturbances caused by leakage or noise. The cell is written by driving the desired value and its complement onto the bit lines, bit, and bit_b, then raising the word line, word. The new data overpowers the cross-coupled inverters. It is read by pre-charging the two-bit lines high and then allowing them to float. When the word is raised, bit or bit_b pulls down, indicating the data value. The central challenges in SRAM design are minimizing its size and ensuring that the circuitry holding the state is weak enough to be overpowered during a write, yet strong enough not to be disturbed during a read.

The write driver circuit is implied on both the bit lines. The write driver is typically an AND gate whose two inputs are Write Enable (WE) and Data (Din). The output of the AND gate is applied to the bit line. Whenever the WE is on the data DI travels to the bit lines. Otherwise, the data is disconnected from the bit lines. Figure 5.5 represents the simulation waveform of the conventional 6T SRAM.

These inputs are taken in such a way that in 10ns time duration, the writing, reading and hold operations are performed. This can be seen that when the input WE and WL is high the data DI is written over Q and QB. Both Q and QB are complementary to each other. In the case of reading one can see that when WL and REN are ON and WE are OFF, reading takes place. For very small intervals only reading is carried out. The output of the sense amplifier is taken out.

All the transistor widths and lengths are taken according to normal considerations. For the n-type transistor the ratio of width and length is taken as 1:1, except for the pre-charge transistor whose ratio is taken as 2:1. For the p-type transistor the width is taken either twice, thrice or four times the length of the particular transistor. There are three variants of 6T SRAM that are simulated according to the technology variation (90nm, 45nm). The de voltages applied to SRAM are 1.5v and 1.0v for 90nm and 45nm respectively. The output waveform is seen to be almost similar in all the variants, the only changes occur.

4.1.1 Write operation

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting the BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input drivers are designed to be much stronger than the relatively weak transistors in the cell itself so that they can easily override the previous state of the cross-coupled inverters.

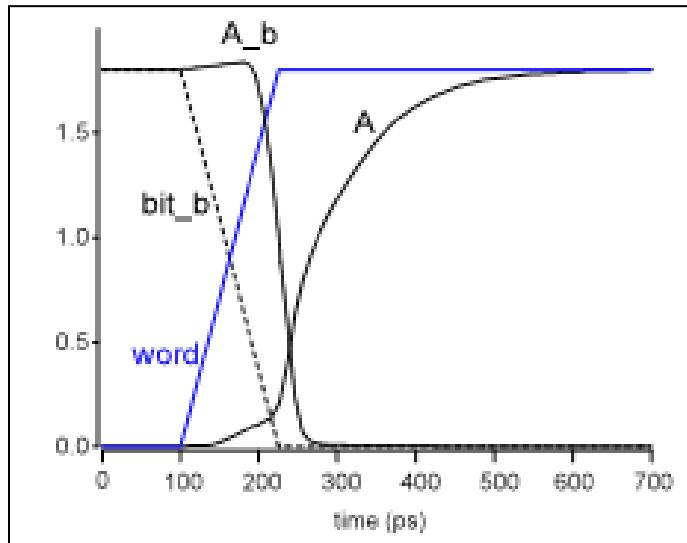


Fig.4.2 Write operation

4.1.2 Read operation

In read mode WL is selected and it enables the two pass transistors which are connected to the bit lines. Now the value stored at nodes A and B is transferred to the bit lines. 1st assume 1 is stored at the node so they will discharge through the N1 and the BL is pulled up through P1 to VDD. In this mode of operation, P1 and N2 transistors are turned off but the transistors N1 and P2 operate in linear mode.

4.2 ADIABATIC LOGIC OVERVIEW

Normally conventional SRAM consumes more power for satisfactory working. To reduce this power requirement the author uses the most promising approach of the adiabatic technique in the SRAM circuit. It is seen that when input logic 1 is written over the cell, the value remains high until and unless a low logic is overwritten over that particular cell.

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

Consider that you want to write logic 0 into the cell and previously the data present in the cell is 1. Now to overwrite the new value one has to pass all the previous data (i.e. logic 1) towards the ground so that the new data in the cell is logic 0. This discharge of the high potential towards the ground is just a waste of energy. This wastage can be recovered with the help of an energy recovery technique.

Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits get smaller and faster, their energy dissipation greatly increases, a problem that adiabatic circuits promise to solve. Most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies dissipate energy as heat, mostly when switching. In order to solve this problem there are two fundamental rules CMOS adiabatic circuits must follow

1. Never turn on a transistor when there is a voltage difference between the drain and the source.
2. The second says never to turn off a transistor that has current flowing through it.

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits that implement reversible logic. In this, the main design changes are focused on the power clock which plays a vital role in the principle of operation. Each phase of the power clock allows the user to achieve the two major design rules for the adiabatic circuit design. During the recovery phase, energy will be restored to the power clock, resulting in considerable energy savings. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. By properly mixing the ideas derived for adiabatic and static CMOS circuits one can achieve low power dissipation in the circuit.

The adiabatic technique plays a vital role in portable devices that are inherently available

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

with constraints in battery life. The long battery operating life requirement of portable devices can be addressed by investigating adiabatic logic. Compared with the conventional low-power approaches, power dissipation can be significantly reduced by using adiabatic computation.

Over the years different low-power adiabatic logic circuits are proposed. Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances that cause a power dissipation which increases with the clock frequency. The adiabatic technique prevents such losses. The charge does not flow from the load capacitance to the ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. Power losses due to the resistance of the switches needed for the logic operation still occur. In order to keep these losses small, the clock frequency has to be much lower than the technological limit.

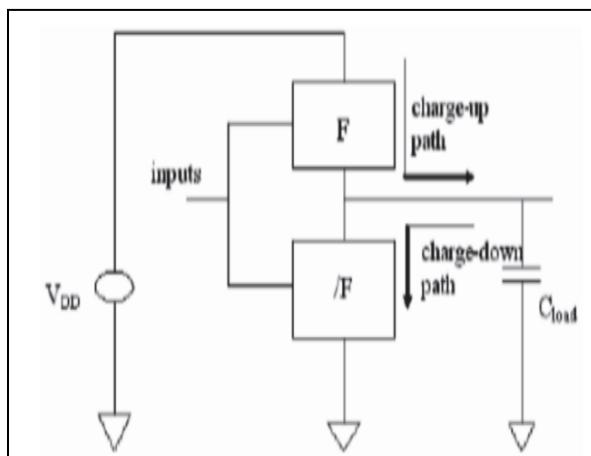


Fig.4.3 Conventional CMOS circuit

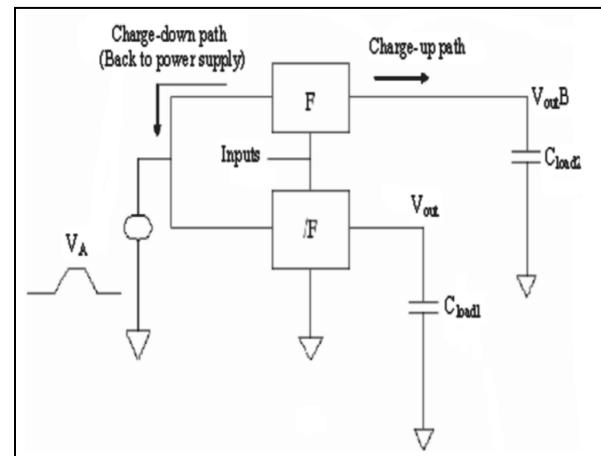


Fig.4.4 Adiabatic Logic gate

4.2.1 Working

The SRAM cell consists of traditional 6T-SRAM along with two switching transistors MN1 and MP1 (NMOS & PMOS) as shown in Figure 2. The switching transistors can be shared by many transistors along the rows through MCPL (Memory cell power line) node. Through this sharing the number of transistors can be kept as original i.e. 6T but

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

still achieve adiabatic charging on bit line in writing mode and this means there is negligible area penalty. The PMOS is connected between the power line VDD and MCPL while the NMOS is connected between the ground and MCPL. To understand the working of adiabatic SRAM, let us consider Figure 2. Based on the control signals S1 and S2 the MCPL node has been connected to either VDD or ground or a floating node. When the S1 and S2 are off, the PMOS is ON and the MCPL follows the VDD. When the S1 and S2 are on then the MCPL follows the GND as NMOS is ON. When S1 is ON and S2 is OFF then, both the NMOS and PMOS are off hence the MCPL node is floating. Thus, the data coming from the bit lines through the cross-coupled inverters charge the node adiabatically.

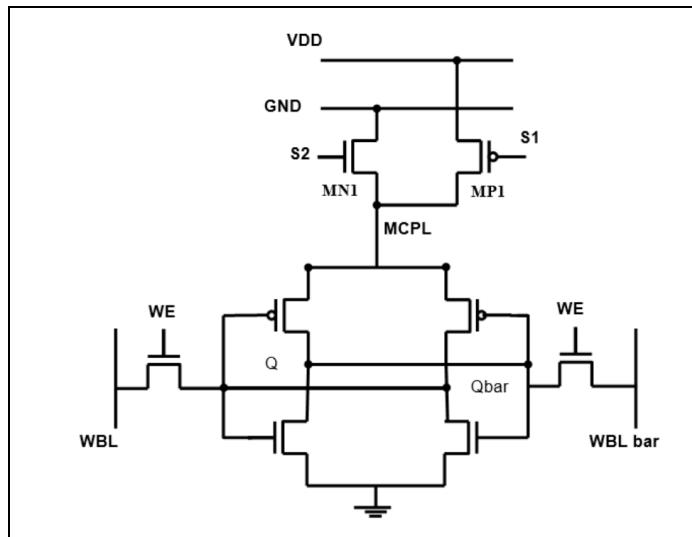


Fig.4.5 SRAM using MCPL

During the write mode of operation, the output of memory cell Q (Bit Line) is gradually charged after the control signals S1 is ON and S2 is OFF i.e., Q follows the WBL with the delay. The MCPL is already in floating mode. When Q is charged to HIGH the MP1 is OFF and MN1 is ON. Similarly, the Q Bar becomes LOW adiabatically. The same operation can be assumed when WBL is discharged and the BL bar is charged. During the read mode of operation, the control signals are provided in such a way that S1 and S2 are OFF. Hence, the SRAM memory cell works as traditional 6T SRAM with MCPL as the power rail VDD.

4.3 1-BIT SRAM CELL SCHEMATIC

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

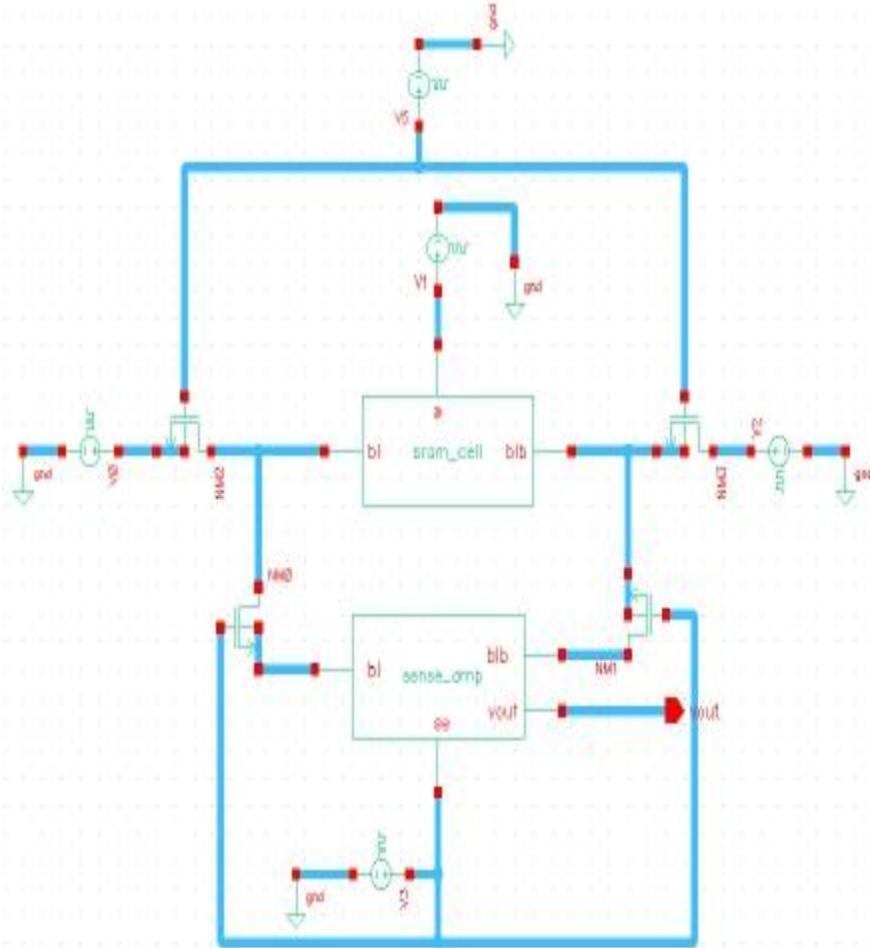


Fig.4.6 1-Bit SRAM Cell Schematic

4.4 1-BIT ADIABATIC SRAM CELL SCHEMATIC

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

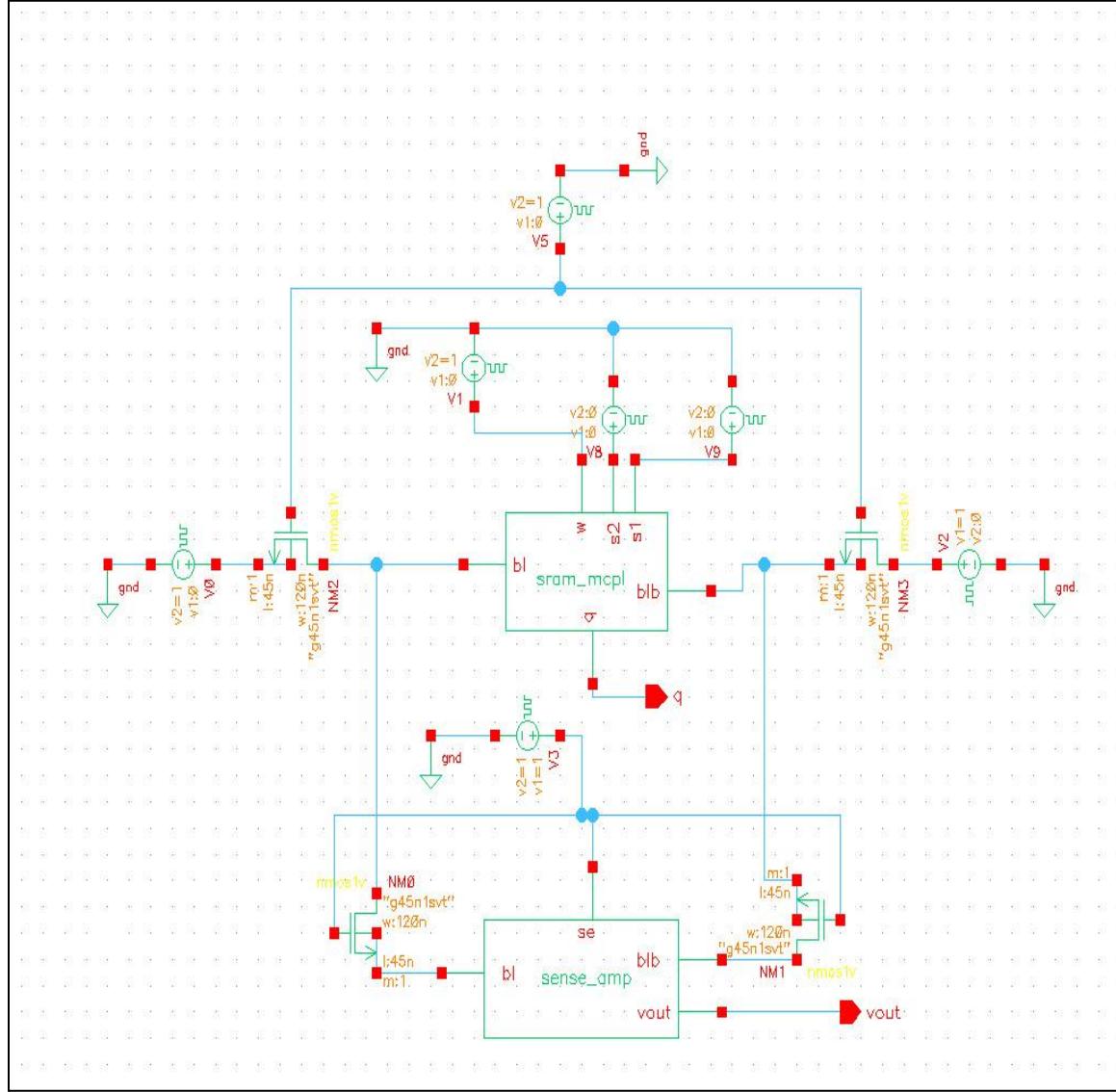


Fig.4.7 1-Bit Adiabatic SRAM Cell Schematic

4.5 MEMORY ARCHITECTURE

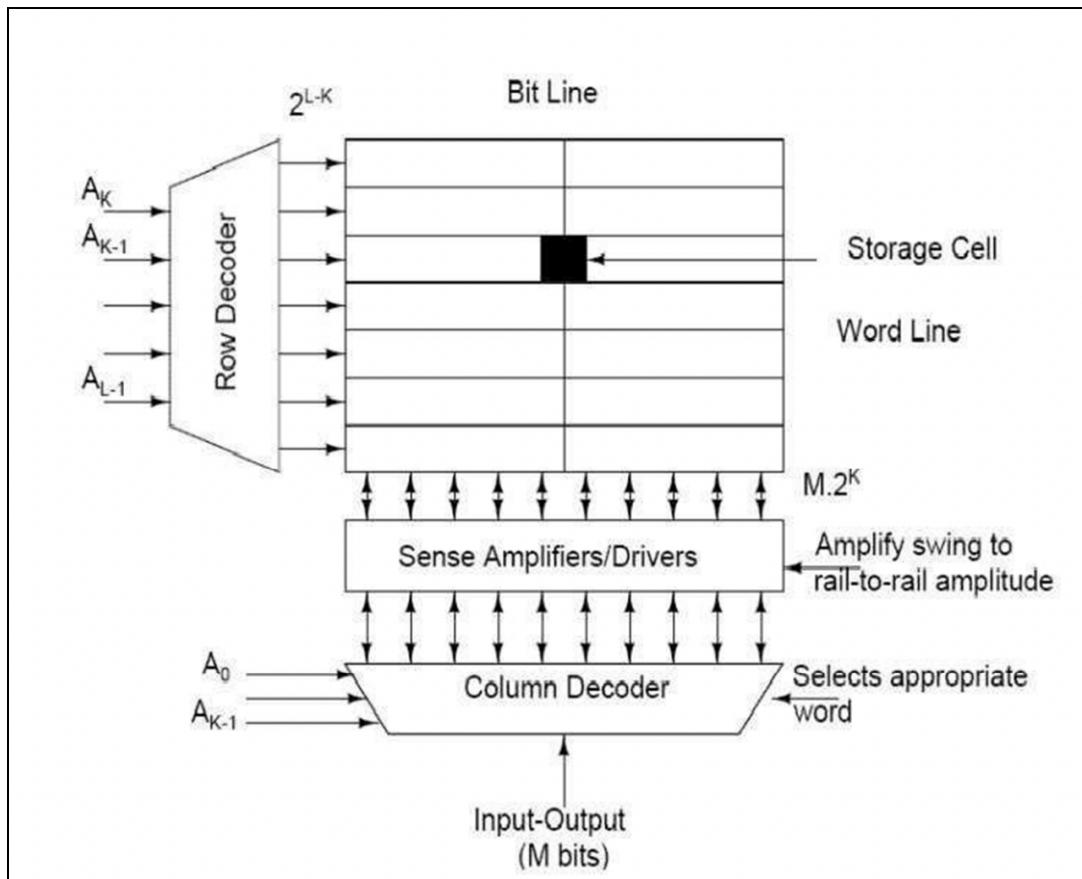


Fig.4.8 Memory Architecture

Memory Architecture describes the methods used to implement data storage in a manner that is a combination of the fastest, most reliable, most durable, and least expensive way to store and collect the information. The data storage structure consists of individual memory cells arranged in an array of horizontal rows and vertical columns. Each cell is capable of storing 1-bit of binary information. In this structure, there are $2N$ rows also called word lines and $2M$ columns also called bit lines. Thus, the total number of memory cells in this array is given as $2N \times 2M$. To access a particular memory cell, i.e., a particular data bit in this array, the corresponding word line and corresponding bit line must be selected according to the address coming from the outside of the memory array.

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

The main SRAM building blocks include various components. All these components or blocks used in the SRAM are listed as follows:

- SRAM cell
- Pre-Charge Circuit
- Write Driver circuit
- Sense Amplifier
- Row decoder

Each cell can store 1-bit of binary data. In this array, there are 4 word lines (horizontal rows) and 4 bit lines (vertical columns). Thus in this structure there are total 4x4 number of individual memory cells.

To access a specific memory cell in this structure the corresponding word line and corresponding bit line must be selected according to the address coming from the outside of the memory array. The row and column selection operation can be achieved by utilizing row and column decoders, respectively. One out of 4 word lines can be selected using the row decoder while the column decoder circuit selects one out of 4 bit-lines. We designed a 4x4 SRAM Memory Array for 16-bit RAM.

4.5.1 Row Decoder

The block diagram of the N:2N row decoder and its associated circuitry is as shown above. Basically, the decoder selects one of 2^N lines, as per the address lines. The output of the decoder is fed to the rows of SRAM cells. The row decoder selects one of those rows, depending on the N-bit address given to it. A normal decoder can be built using logic gates as we have studied in digital design courses. However, the normal decoder built using logic gates has drawbacks.

The row decoders are used to select a particular memory location in the array, based on the binary row addresses. A row decoder designed to drive a NOR ROM array must, by definition, select one of the 2^N word lines by raising its voltage to VOH.

The name “Decoder” means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an

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equivalent decimal code at its output. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of $m=2^n$ unique output lines. The binary inputs A and B determine which output line from Q0 to Q3 is “HIGH” at logic level “1” while the remaining outputs are held “LOW” at logic “0” so only one output can be active (HIGH) at any one time.

Therefore, whichever output line is “HIGH” identifies the binary code present at the input, in other words it “decodes” the binary input. Some binary decoders have an additional input pin labelled “Enable” that controls the outputs from the device. This extra input allows the decoders outputs to be turned “ON” or “OFF” as required. Output is only generated when the Enable input has value 1; otherwise, all outputs are 0. Only a small change in the implementation is required: the Enable input is fed into the AND gates which produce the outputs.

If Enable is 0, all AND gates are supplied with one of the inputs as 0 and hence no output is produced. When Enable is 1, the AND gates get one of the inputs as 1, and now the output depends upon the remaining inputs. Hence the output of the decoder is dependent on whether the Enable is high or low.

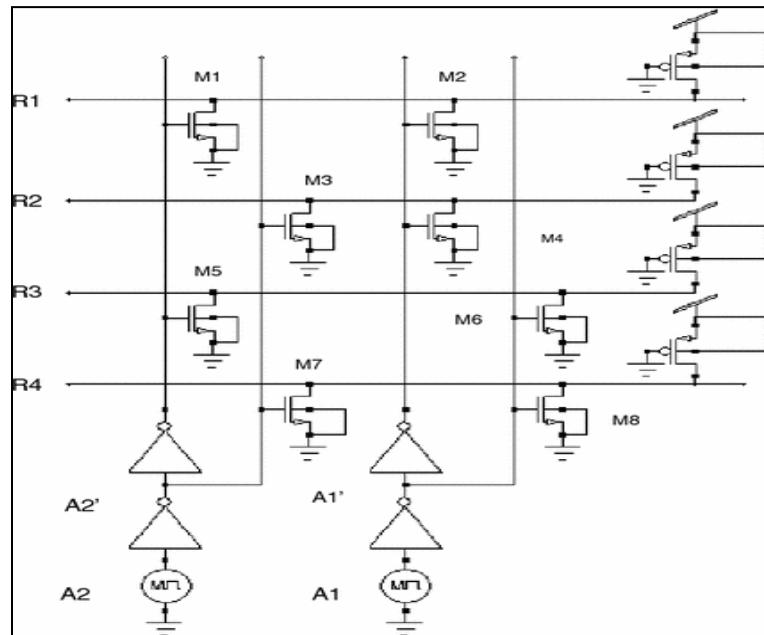


Fig.4.9 Row decoder

4.5.2 Column Decoder

The column decoder selects a particular column in the memory array for reading the contents of the selected memory cell or to modify its contents. The column selector is based on the same principles as those of the row decoder. The major modification is that the data flows both ways, that is either from the memory cell to the Data Out signal (Read cycle), or from the Data In signal to the cell (Write cycle). The binary inputs A and B determine which output line from Q0 to Q3 is “HIGH” at logic level “1” while the remaining outputs are held “LOW” at logic “0” so only one output can be active (HIGH) at any one time.

Therefore, whichever output line is “HIGH” identifies the binary code present at the input, in other words it “decodes” the binary input. Some binary decoders have an additional input pin labelled “Enable” that controls the outputs from the device. This extra input allows the decoders outputs to be turned “ON” or “OFF” as required. Output is only generated when the Enable input has value 1; otherwise, all outputs are 0. Only a small change in the implementation is required: the Enable input is fed into the AND gates which produce the outputs.

If Enable is 0, all AND gates are supplied with one of the inputs as 0 and hence no output is produced. When Enable is 1, the AND gates get one of the inputs as 1, and now the output depends upon the remaining inputs. Hence the output of the decoder is dependent on whether the Enable is high or low.

The column decoder circuitry is designed to select one out of $2M$ bit lines (columns) of the ROM array according to an M-bit column address, and to route the data content of the selected bit line to the data output.

The name “Decoder” means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of $m=2^n$ unique output lines.

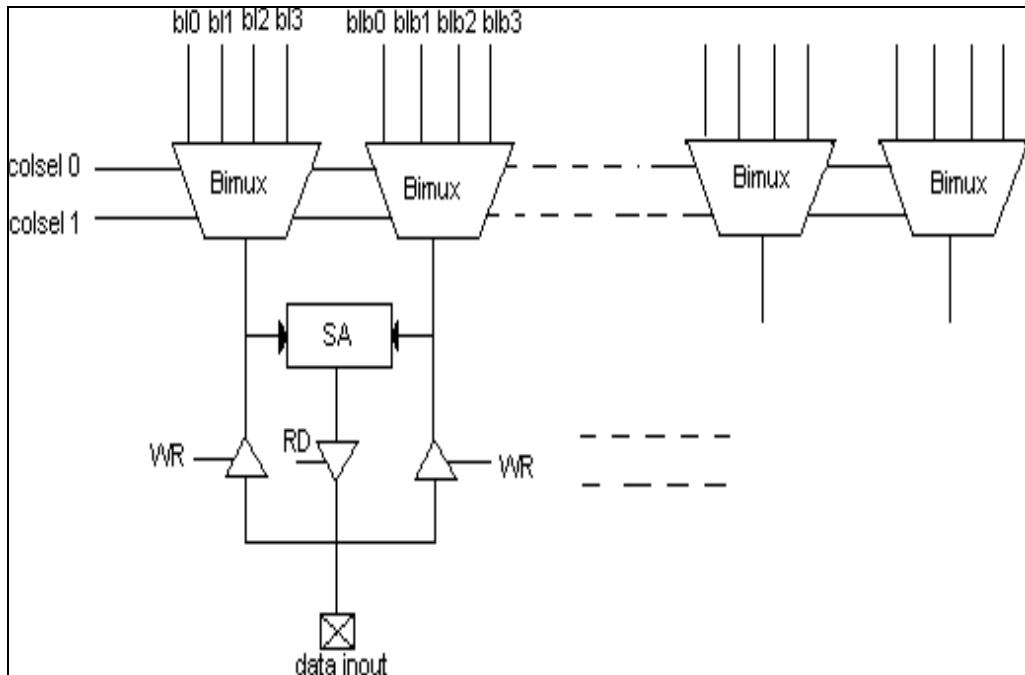


Fig.4.10 Column decoder

4.5.3 Pre-charge circuit

Precharge plays an important role in decreasing the delay while writing bits into the memory or reading the bits from memory. [1] The precharge circuit makes both, bit line and bit bar line charge to the precharge voltage before carrying out either read operation or write operation. The advantage of precharging the lines lies in the fact that only one line, either bit or bit bar is to discharge compared to the one line charged and other discharged.

Safe read and write operations require a modification of the memory array and timing sequence, based on a precharge circuit. The usual voltage of precharge is $VDD/2$. Before reading or writing to the memory, the bit lines are tied to $VDD/2$ using appropriate pass gates. When reading, the BL and \sim BL diverge from $VDD/2$ (Figure 3) and reach the "1" and "0" levels after a short time.

A precharge system of the divided bit line types for a SRAM (Static Random Access Memory) reduces the active current consumption and bit line peak current by decreasing the number of bit lines to be precharged at any one time during a precharge cycle. For this, the system has a block selection signal generator that responds to certain column addresses with a block selection signal. A sub-block selection signal generator responds

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to certain addresses among the remaining column addresses with a sub-block selection signal.

A precharge decoder responds to pulses from the pulse generator and the block selection signal with a block selection precharge signal. A divided bit line precharge decoder responds to the sub-block selection signal and block selection precharge signal with a pulse for precharging only a certain sub-block of a certain block of the array of memory cells of the SRAM. A column predecoder responds to the block and sub-block selection signals with a block selecting pulse, and a column decoder responds to the block selecting pulse and the remaining column addresses to connect certain bit lines of the sub-block with a data line.

The advantages of this are to reduce the power consumption of such a SRAM chip, and the noise in its power supply voltage, by precharging of only a portion of the whole number of bit lines at any one time.

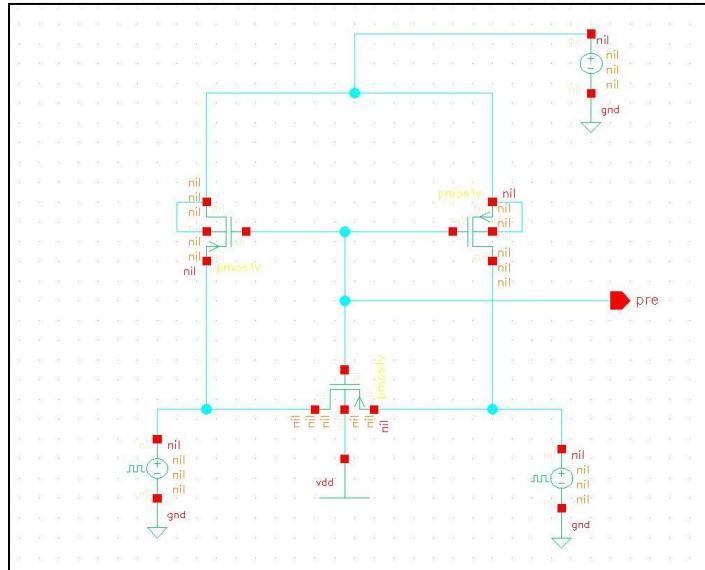


Fig.4.11 Pre-charge circuit Schematic

4.5.4 Sense Amplifier

The sense amplifier is an important circuit to regenerate the bit-line signals in a memory design. The sense amplifier can be also applied to the receiving of long interconnection signal with large RC delay and large capacitive load signal. Moreover, the complexity of the differential logic circuit can be enhanced by combining the sense amplifier with differential logic networks to reduce the delay time.

Due to large arrays of SRAM cells, the resulting signal, in the event of a Read operation, has a much lower voltage swing. To compensate for that swing a sense amplifier is used to amplify voltage coming off Bit Line and Bit bar Line.

In order to read out the value of a given bit of a word in this type of memory, the bit-cell voltage, or the magnitude of its charge, needs to be sensed, and the results of this sense operation must be delivered to the rest of the circuit.

In modern computer memory, a sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit); the term itself dates back to the era of magnetic core memory. A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a *bitline* that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

Modern sense-amplifier circuits consist of two to six (usually four) transistors, while early sense amplifiers for core memory sometimes contained as many as 13 transistors. There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. As such, sense amplifiers are one of the few remaining analog circuits in a computer's memory subsystem.

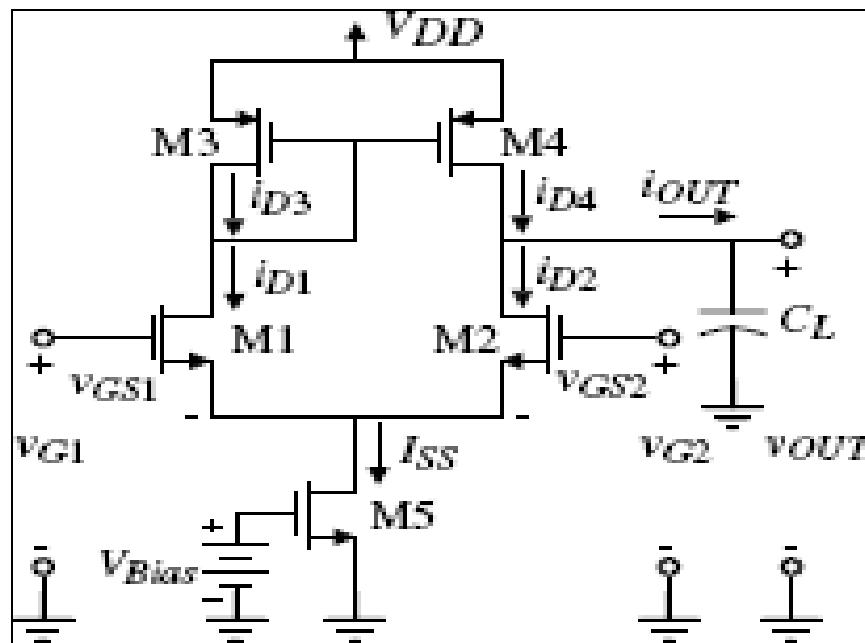


Fig.4.12 Sense Amplifier

Sense Amplifiers: Sense amplifiers are the most essential circuit of SRAM which detect the voltage difference between the bit-lines and show which data value is stored in the memory cell. In this paper we discuss two type of sense amplifiers i.e. Voltage Mode sense amplifiers and Charge Transfer sense amplifiers.

Voltage mode Sense Amplifier: The operation of voltage mode sense amplifier is based on the differential voltage developed by the bit-lines. The circuit consists of cross coupled inverters that convert the bit-line voltage difference at their input to full swing output. Figure shows the voltage mode sense amplifier circuit implementation. BL and BLB inputs are coupled to the column bit-lines of the cell. The inverters are formed by P6-N1 and P7-N2 that convert the differential voltage on the bit-lines to a full swing at the output. The pre-charge circuitry is formed by P3, P4 and P5 which is used to pre-charge the internal nodes X, \bar{X} of this circuit through the bit-lines. The memory cell is connected to the sense amplifier by P1, P2 while to enable the sense amplifier N3 is used. The internal nodes of the sense amplifier are isolated from the external load by output inverters. The operation of the voltage mode sense amplifier is done in two phases. In the first phase i.e. pre charge phase, the PCH is kept active low so that bit-lines and the nodes X and \bar{X} are pre-charged high. During the evaluation phase, sense amplifier is connected

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to the memory cell by pulling down the select-line (SEL). A voltage difference is developed between bit-lines BL and BLB due to the stored data in the memory cell.

If the data stored in the memory cell is a ‘1’, voltage across BLB decreases slightly and if the data stored in memory cell a ‘0’, voltage across BL decreases slightly. Once the required differential voltage has been developed between bit-lines, EN is pulled high to enable the sense amplifier. Differential discharging of the bit-lines capacitance is used by the VMSA for sensing the voltage difference and converts this differential voltage at its inputs to a full swing at the outputs.

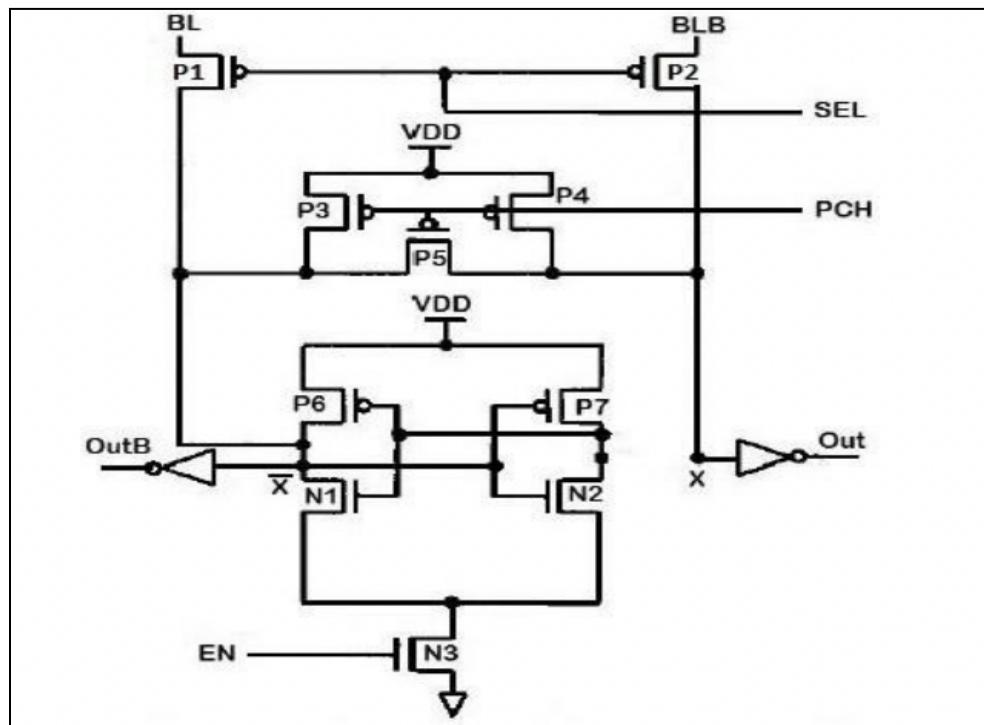


Fig.4.13 Voltage Mode Sense Amplifier

4.5.4.1 Charge Transfer Sense Amplifier

The basic function of Charge Transfer Sense Amplifier is depends upon the charge redistribution from high bit-line capacitance to the low capacitance of the nodes X and \bar{X} as shown in figure 3. The high speed operation of CTSA is due to this charger distribution. The circuit has two parts in which P6, P9, N1 & P7, P10, N2 form a

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common gate cascade with PMOS P6 and P7 biased at V_o . In the other part P12, P13, N3 and N4 form the cross coupled inverters[7]. CTSA is operated in two phase. In the pre-charge phase, high pre-charging of the bit-lines and all the intermediate nodes (A, B, C & D) is done. By keeping EN high the output of the common-gate amplifier (X and \bar{X}) is pre discharged low. In the evaluation phase, PCH is kept high and SEL input is grounded to select a column. By dragging EN low CTSA is enabled. Assume the bit-line BLB is going low. As the voltage of the BLB goes immediate $V_o + |VTP|$, P6 goes into sub-threshold region of operation avoiding the output node from getting charged. However, the other bit-line BL remains high and charges the output node X to high.

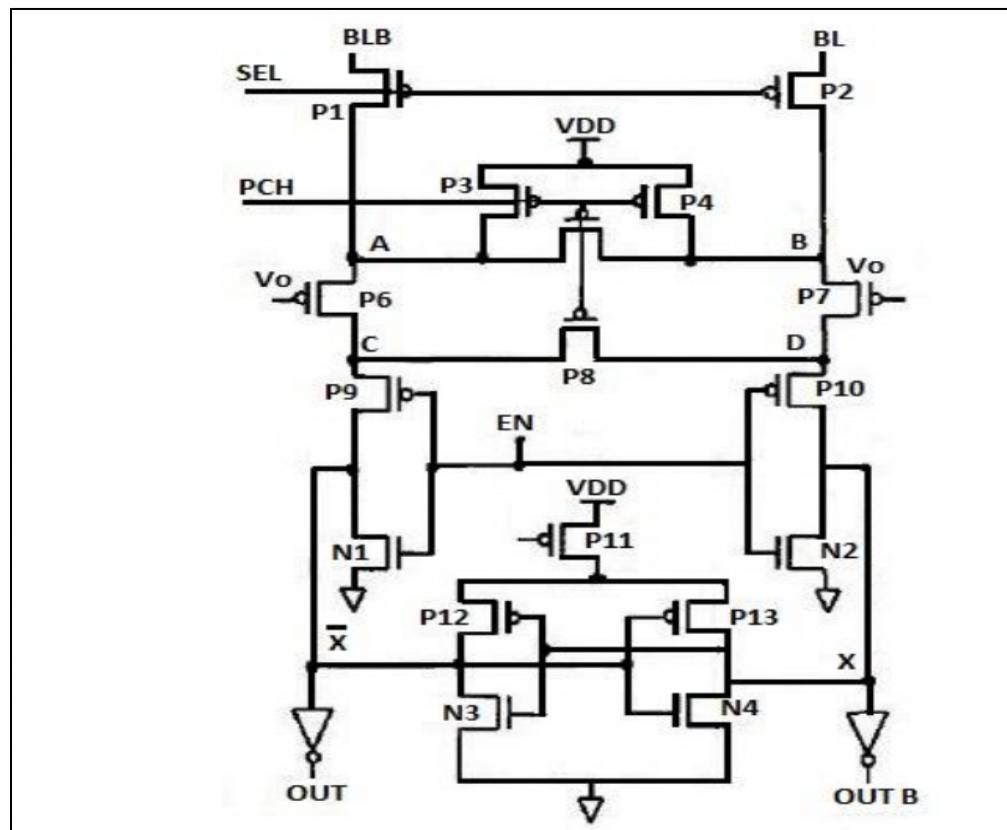


Fig.4.14 Charge Transfer Sense Amplifier

4.5.5 Write driver

The Write Driver is responsible for writing a specific value in the bit-cell. The circuit has the function of charging or discharging the bit lines to the desired bit be written in the memory cell. The circuit schematic of write driver designed in this work is presented in below figure. This circuit has two input signals, they are the signal representing the bit value to be written in the memory cell, and the control signal write enable (WE).

The control signal WE function is to allow or not the access to the bit lines by the Write Driver. When WE is on, the Write Driver imposes in the bit lines the required voltage values for writing the desired value in the Bit-Cell.

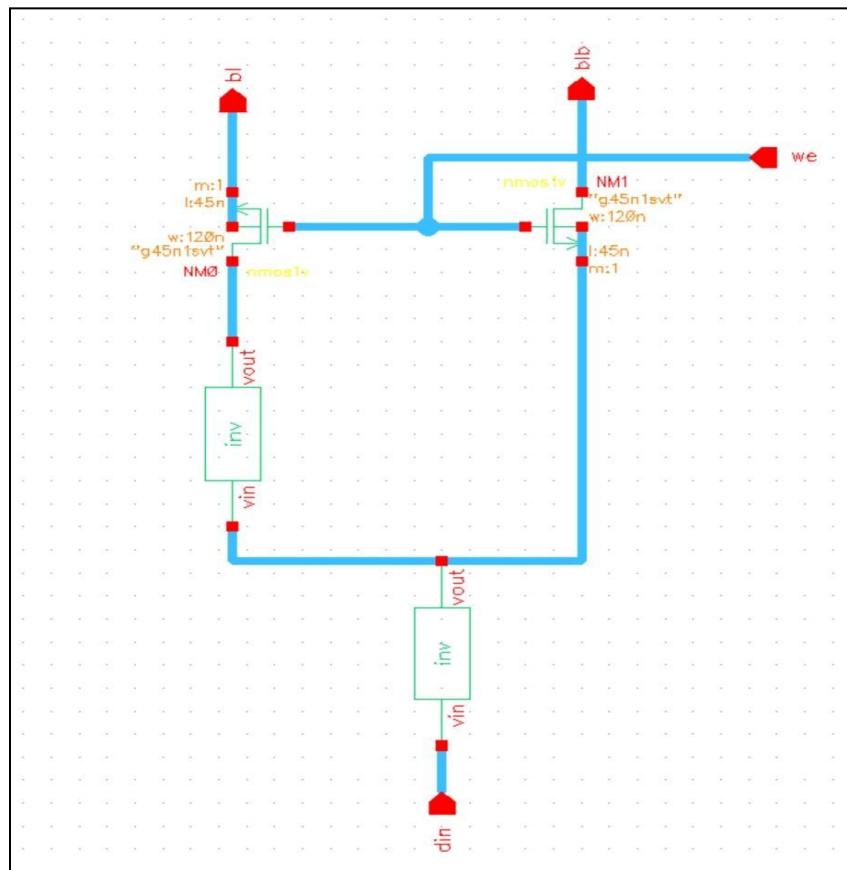


Fig.4.15 Write Driver

4.6 4X4 MEMORY ARRAY SRAM CELL SCHEMATIC

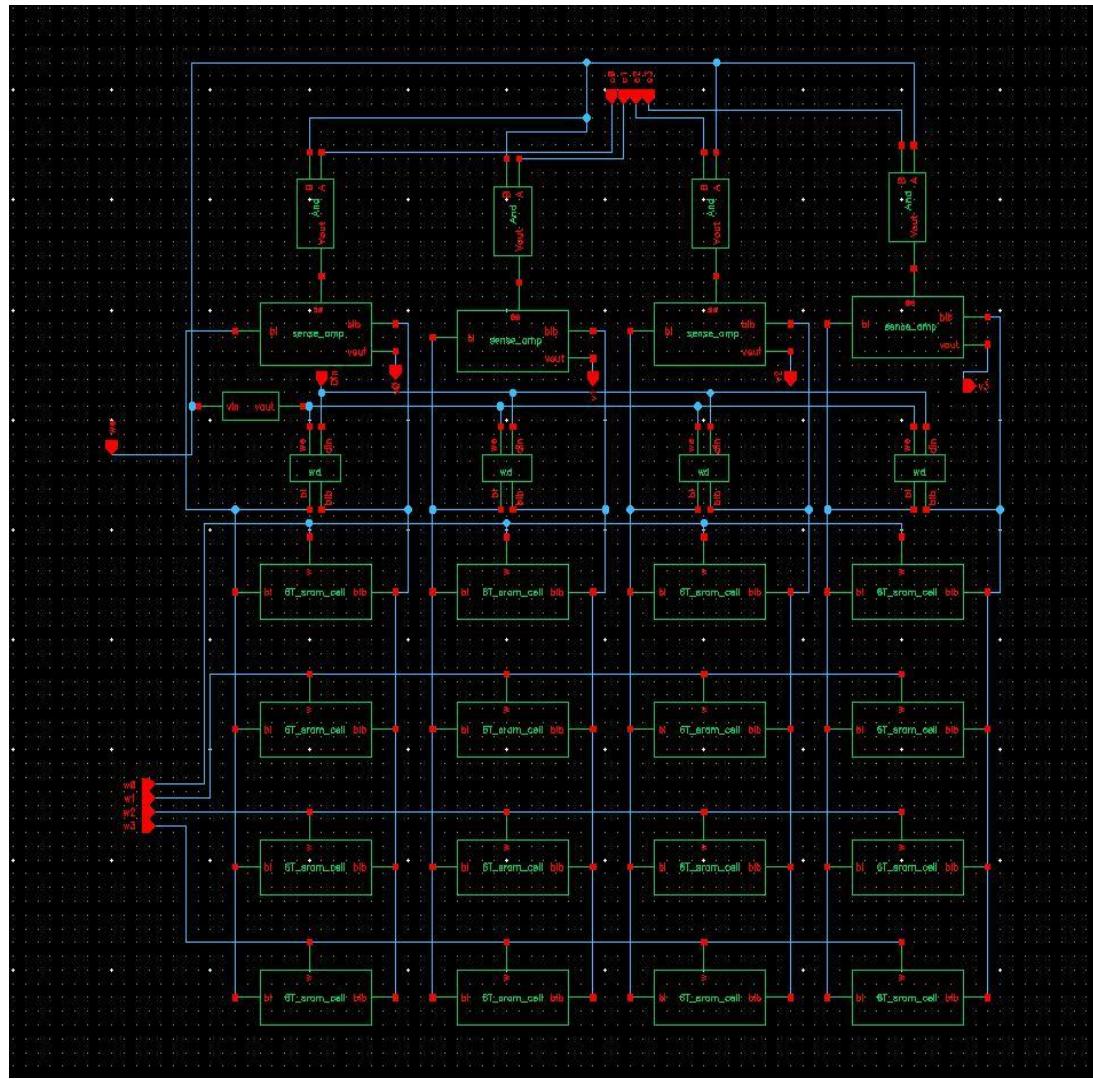


Fig.4.16 4X4 Memory array SRAM Cell Schematic

4.7 4X4 ADIABATIC MEMORY ARRAY SRAM CELL SCHEMATIC

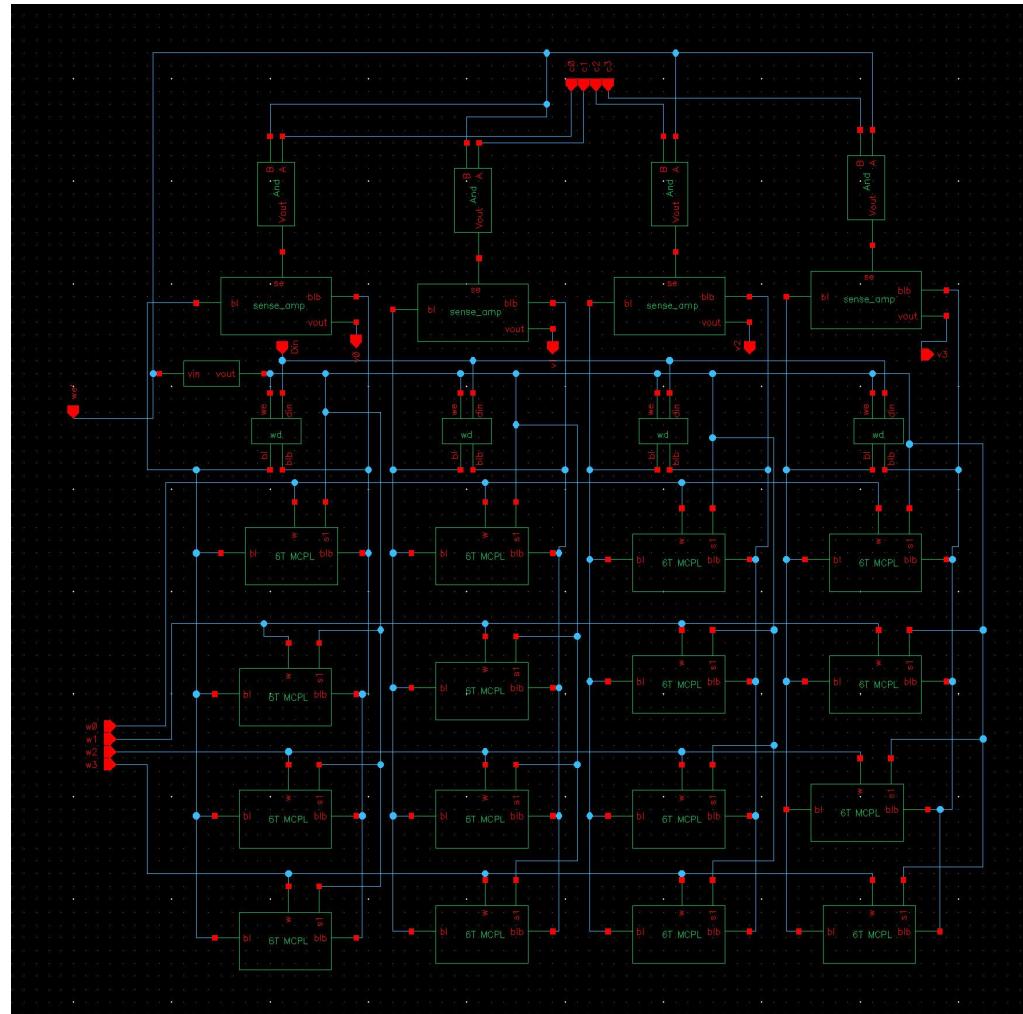


Fig.4.17 4X4 Adiabatic Memory array Sram Cell Schematic

CHAPTER-5

RESULTS

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

5.1 PMOS

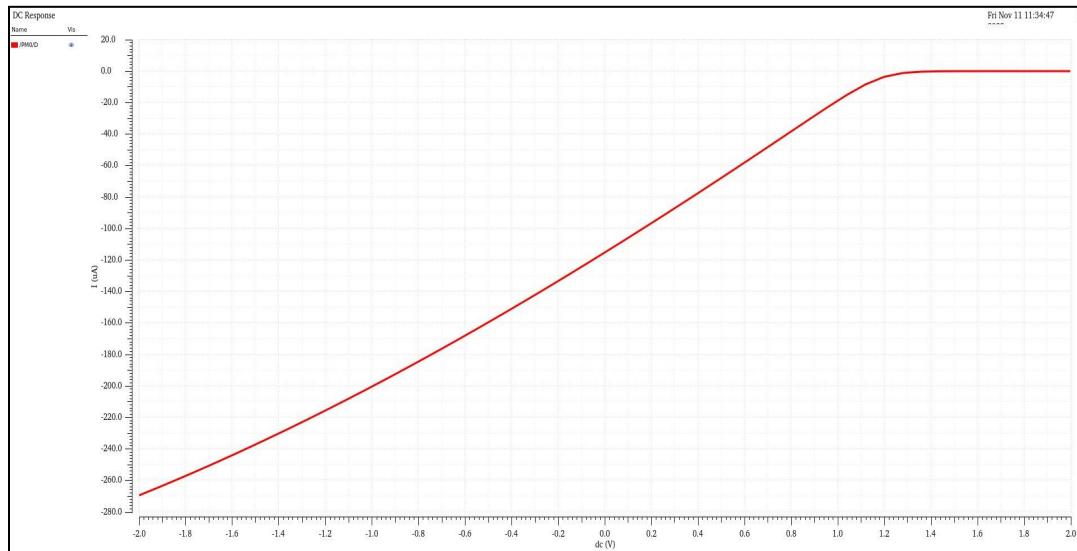


Fig.5.1 PMOS Drain current vs Gate voltage

5.2 NMOS

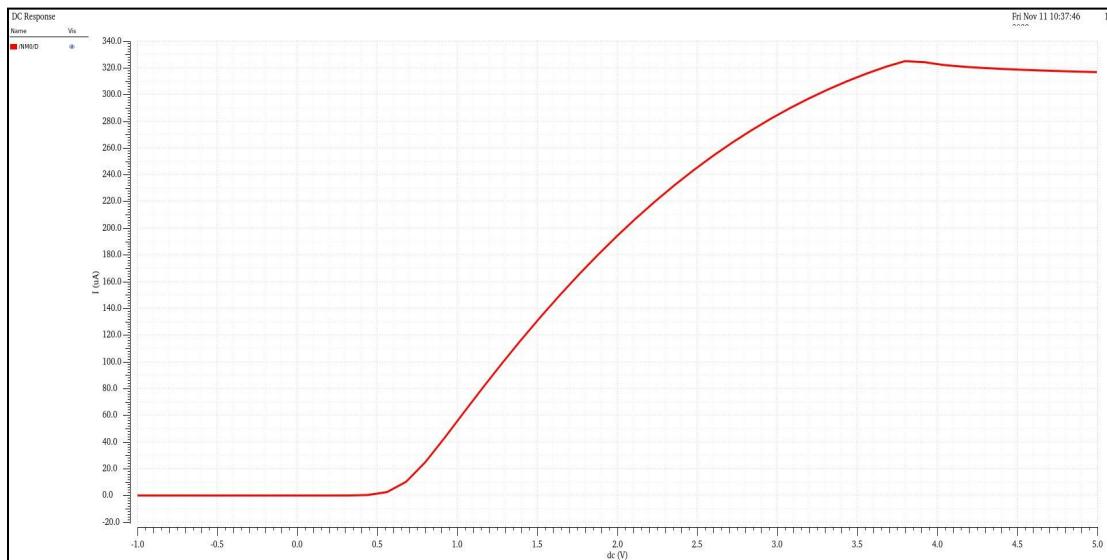


Fig.5.2 NMOS Drain current vs Gate voltage

5.3 INVERTER

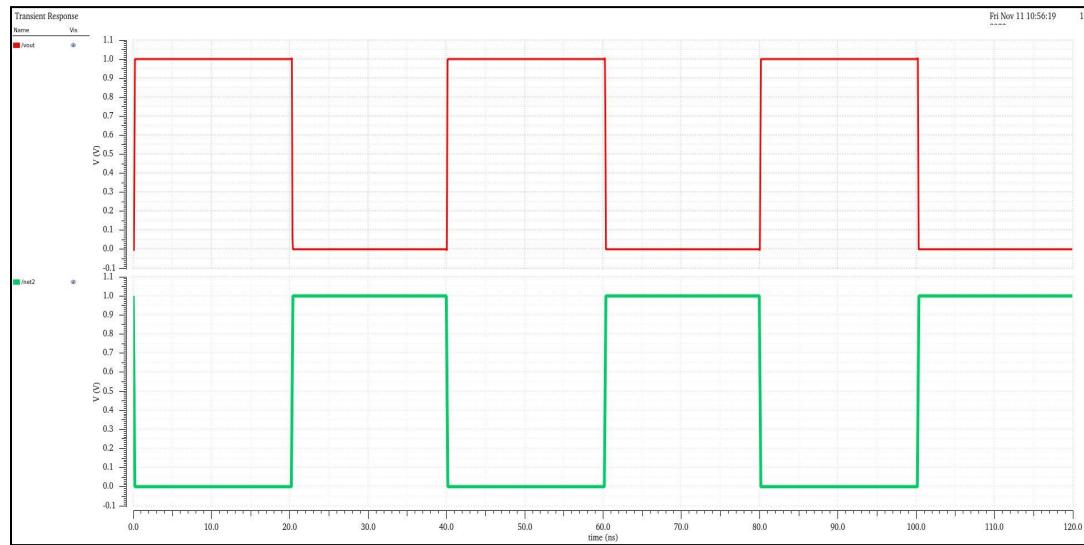


Fig.5.3 Inverter Vin & Vout vs TIme

5.4 SENSE AMPLIFIER

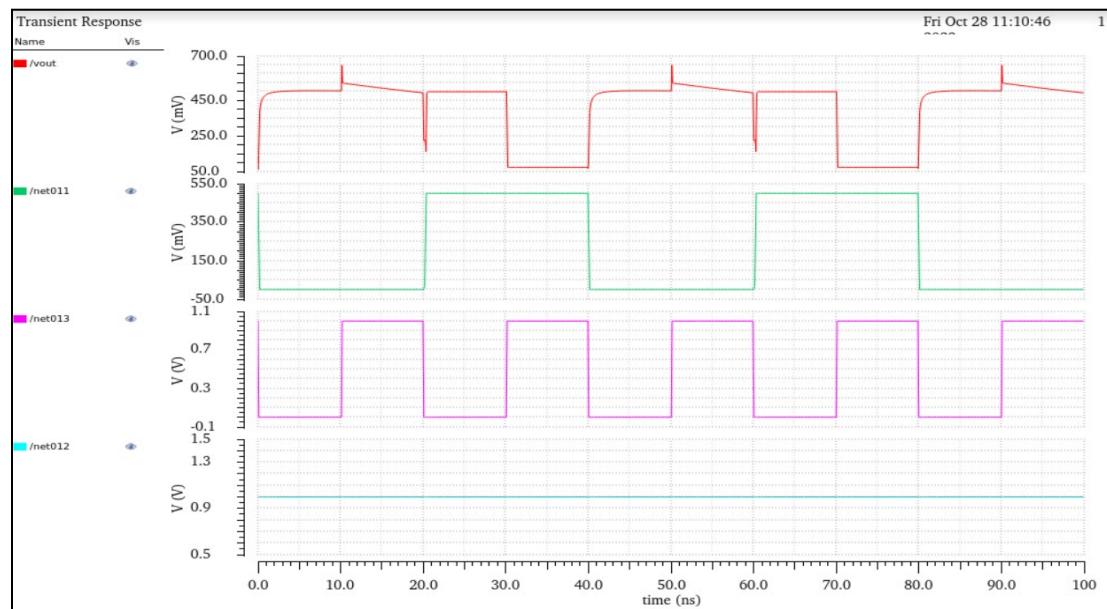


Fig.5.4 Initial Test Output 1

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

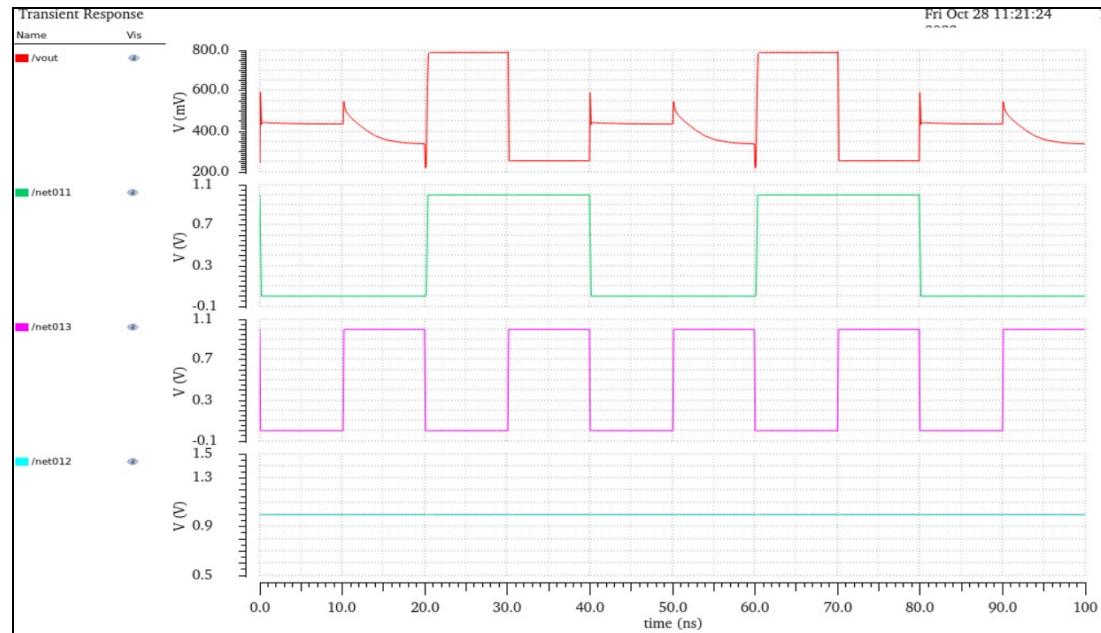


Fig.5.5 Initial Test Output 2



Fig.5.6 Sensing Vout 1v

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

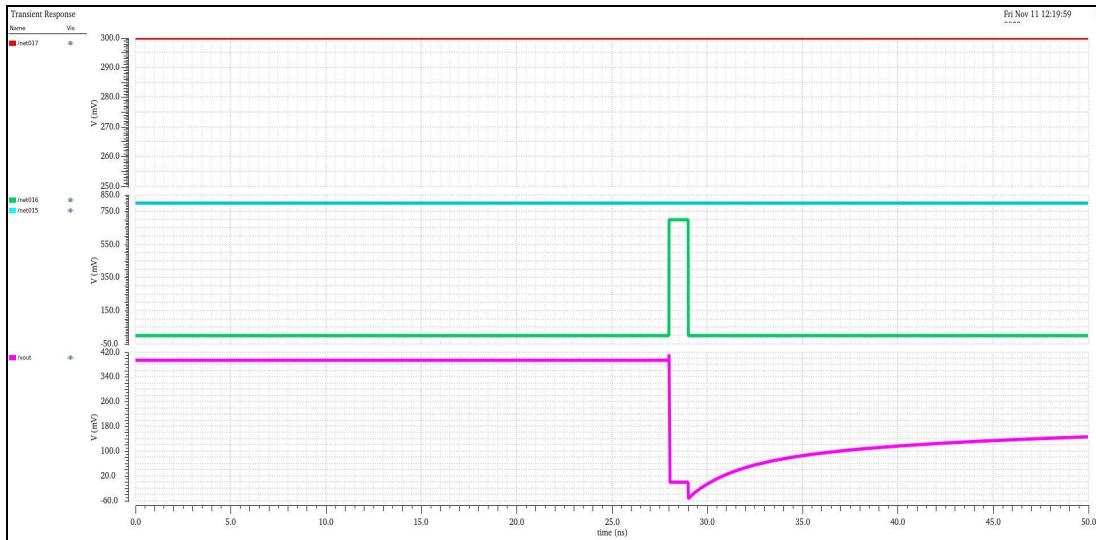


Fig.5.7 Sensing Vout 0v

5.5 1-BIT SRAM CELL READ-WRITE OPERATION

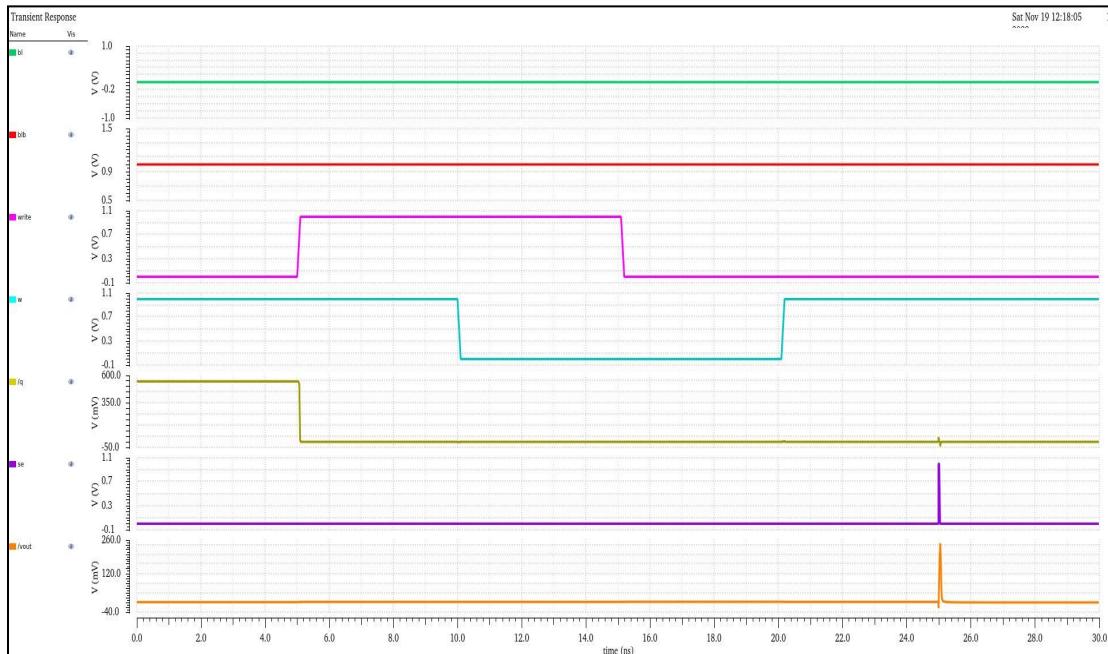


Fig.5.8 Writing and Reading Logic 0 of Conventional 6T

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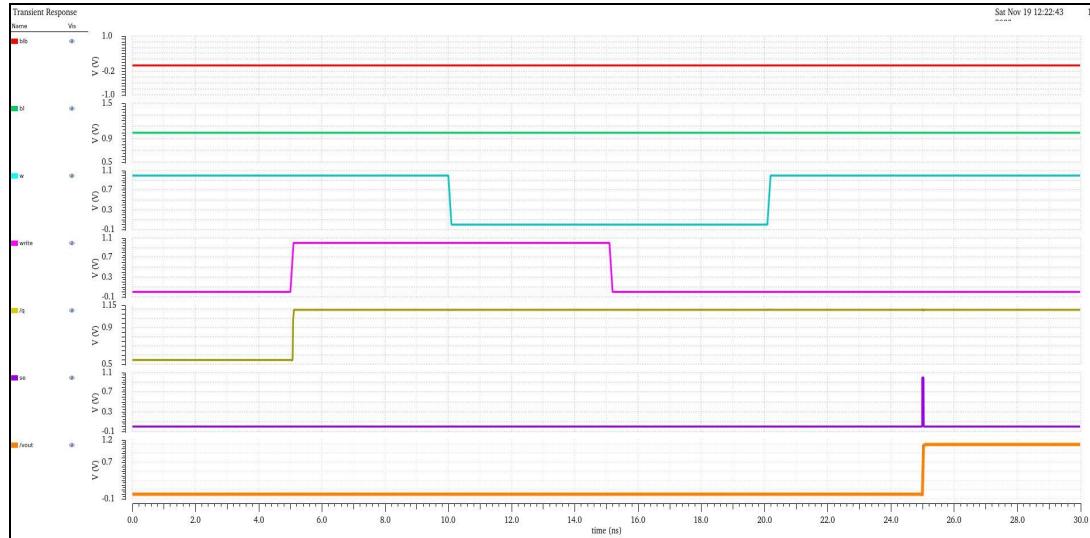


Fig.5.9 Writing and Reading Logic 1 in Conventional 6T

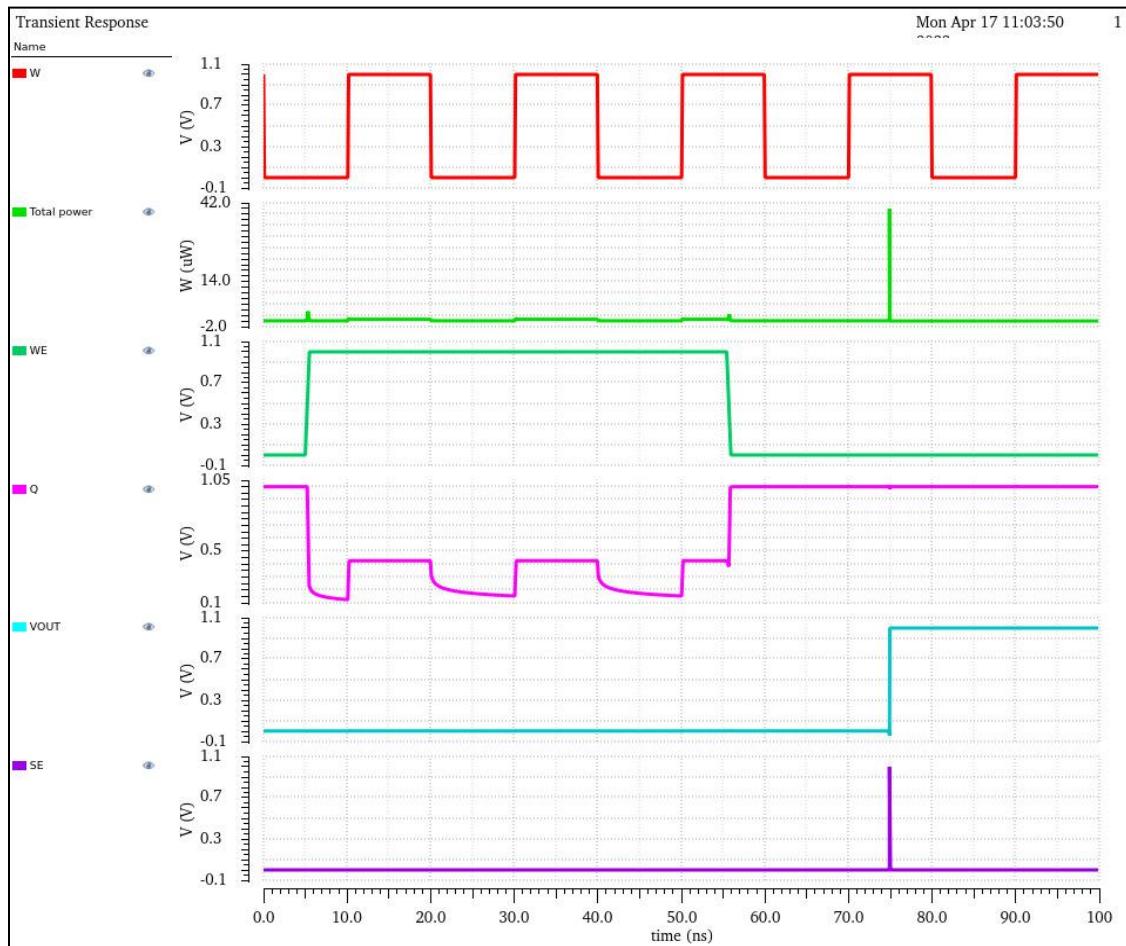


Fig.5.10 Writing and Reading Logic 1 in Adiabatic 6T

5.6 TEST CIRCUIT OF 4X4 SRAM MEMORY ARRAY

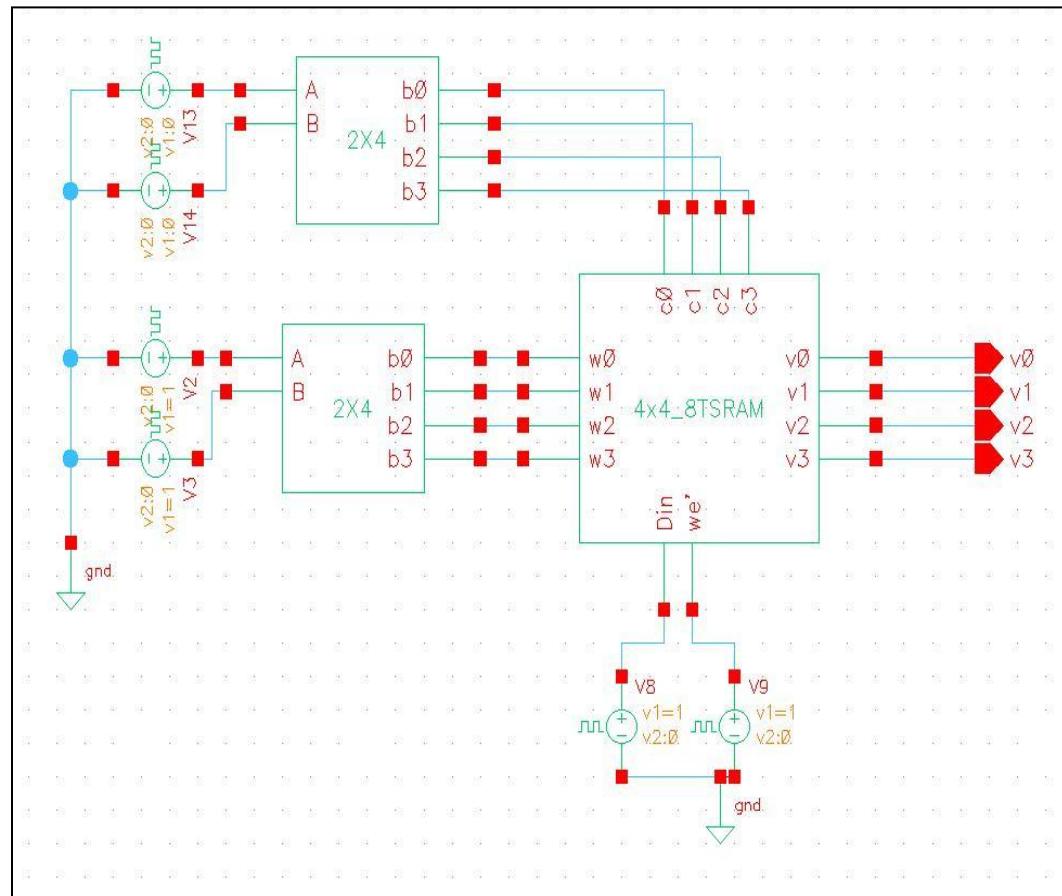


Fig.5.11 Test Circuit of 4x4 SRAM Memory Array

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

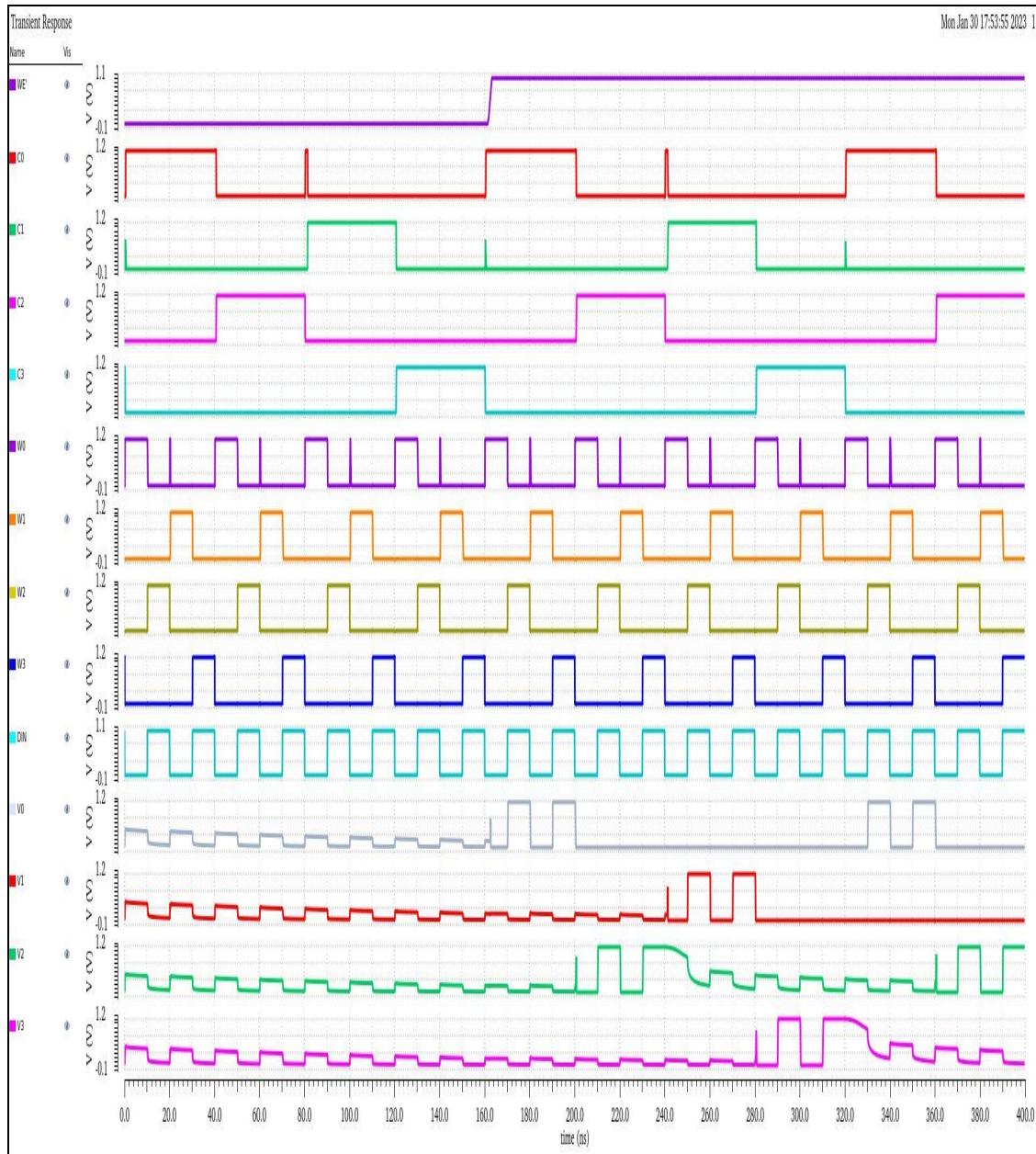


Fig.5.12 Output Waveform

5.7 POWER CONSUMPTIONS :

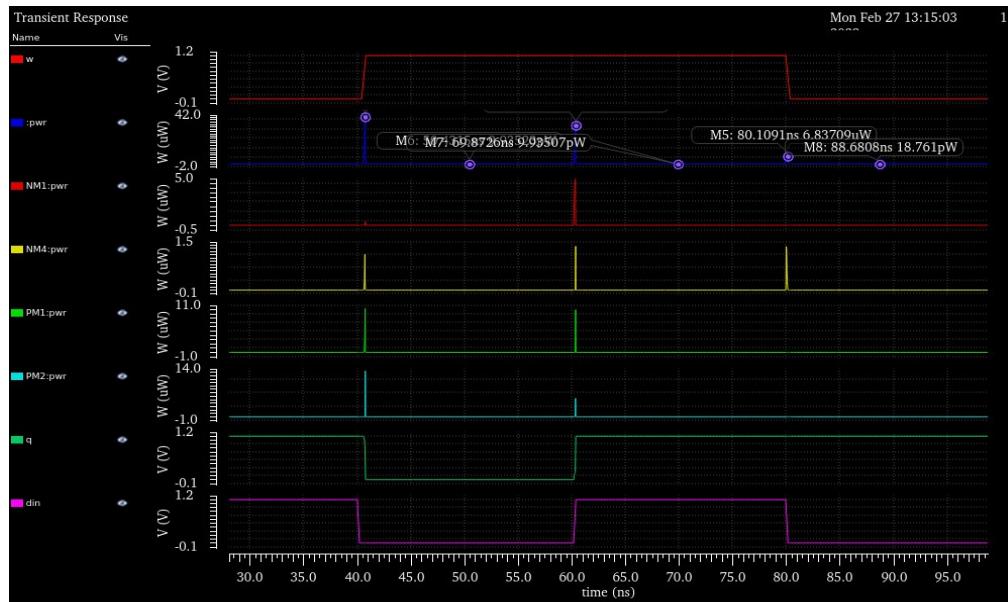


Fig.5.13 Power Graphs of Conventional Single 6T SRAM

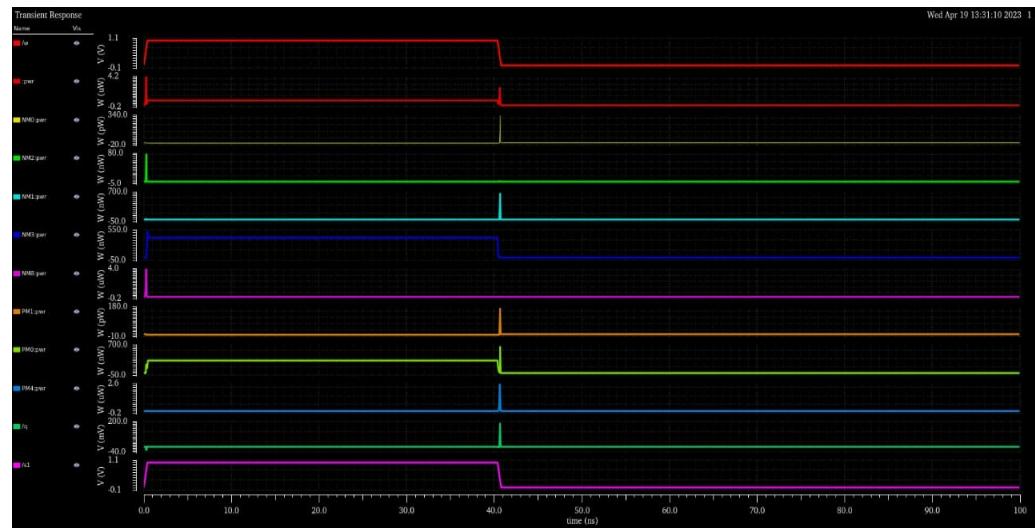


Fig.5.14 Power Graphs of Adiabatic Single 6T SRAM

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

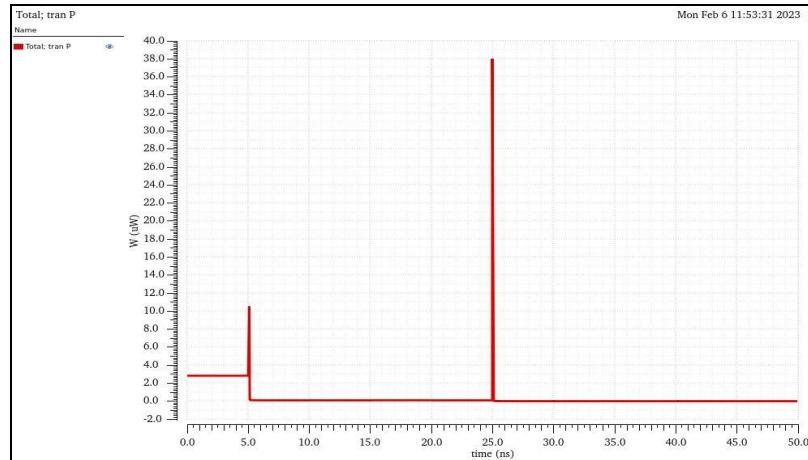


Fig.5.15 Write and read power in single 6T cell graph

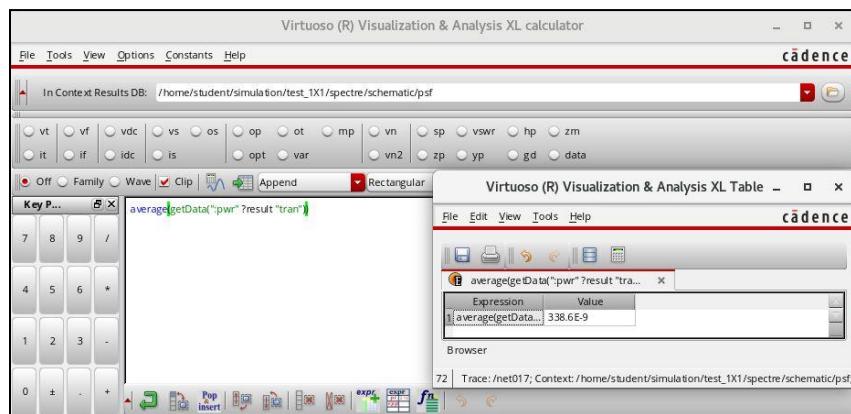


Fig.5.16 Write and read power in single 6T cell(338nw)

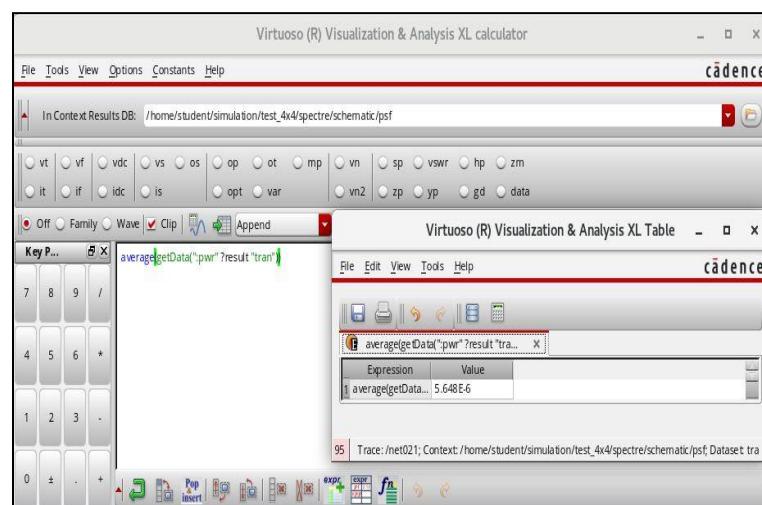


Fig.5.17 Write and Read power in 4X4 6T Array(5.6mw)

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

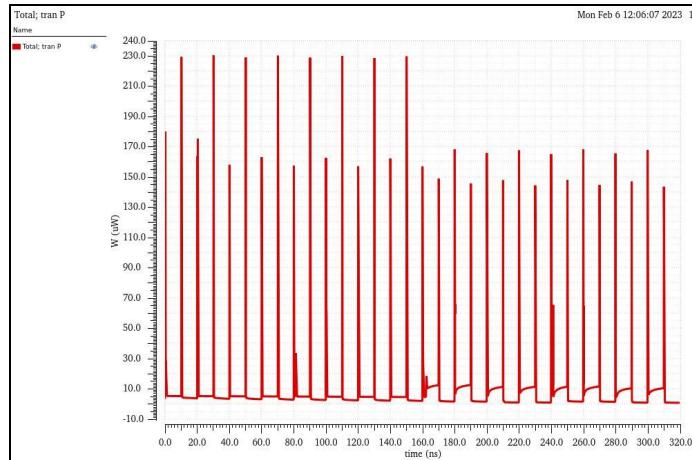


Fig.5.18 Write and Read power in 4X4 6T Array graph

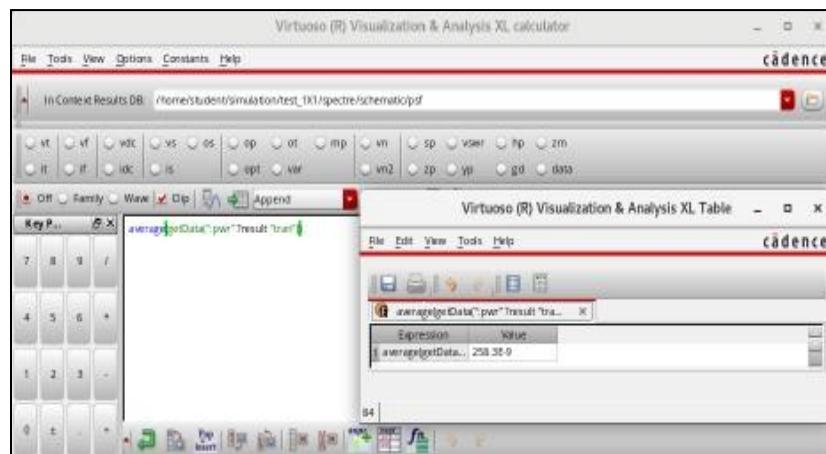


Fig.5.19 Write and read power in single 6T cell using adiabatic logic (258nw)

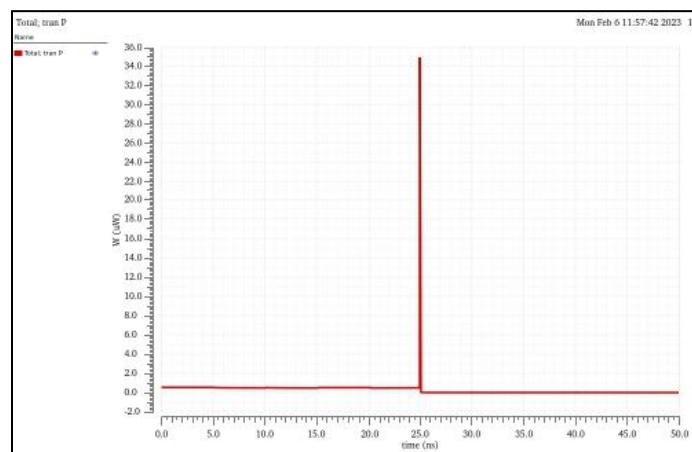


Fig.5.20 Write and read power in single 6T cell using adiabatic logic graph

DESIGN OF 6T SRAM USING ADIABATIC LOGIC

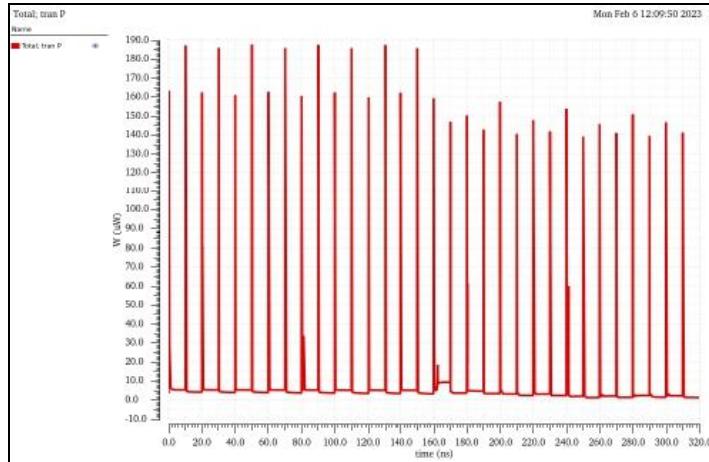


Fig.5.21 Write and Read power in 4X4 6T Array using Adiabatic logic graph

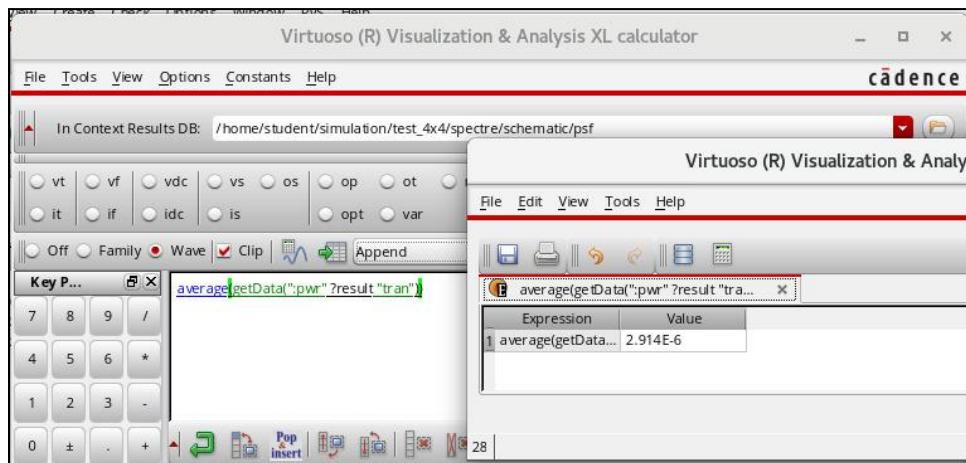


Fig.5.22 Write and Read power in 4X4 6T Array using Adiabatic logic(2.9mw)

CHAPTER-6

CONCLUSION AND

FUTURE SCOPE

6.1 CONCLUSION

In this paper, we presented the various structures of SRAM cell using adiabatic logic. With the help of adiabatic logic the power dissipation and energy is reduced. These structures are designed, simulated and results are taken from the cadence EDA tool. 91% of power reduction is achieved with the MCPL adiabatic logic from the conventional SRAM. Further in future new SRAM cell can be designed which will reduce the power dissipation and energy.

6.2 FUTURE SCOPE

Future scope of this project include further improvement in power in scaled down 45nm below fabrication technologies. By improving the design logic in the future projects we can get better stability and delays in read and write operation.

The Memory array can be designed for more RAM i.e 8*8 or 16*16 and can be implemented in physical form.

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