DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [INFORMATION TECHNOLOGY]
SUBJECT: (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: Online External Exam**	**Seat No.**	:
Date	**: 02/12/2020**	**Day**	: **Wednesday**
Time	**: 90 minutes**	**Max. Marks**	: **30**

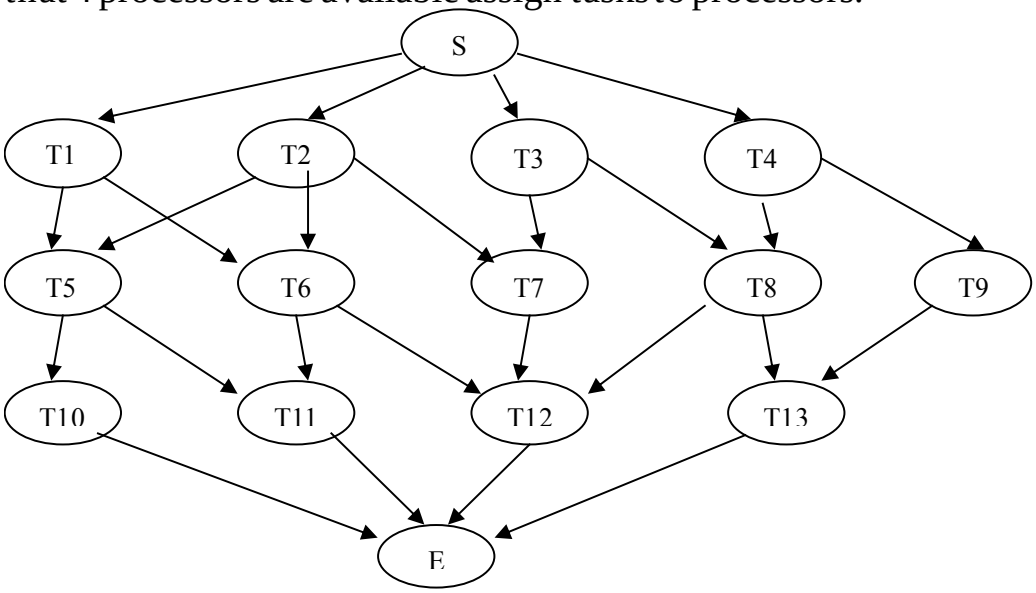
INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.
5. Scan your answer sheets properly and save as a single pdf file. Upload this pdf file to the google classroom.
6. PDF File Name Format is: **"B.Tech_5_IDNO_RollNO_IT506_AMP.pdf"**

SECTION - II

Q.2 Attempt Any Three from the following questions. **[12]**

(a) A Task graph with various tasks is given in Figure below. Assuming that 4 processors are available assign tasks to processors. **[4]**



T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
3	4	5	4	6	7	6	5	6	8	9	10	9

(b) Determine the addressing modes and write down the opcode (in HEX) for the following instructions. (Refer Table-1 and if require take D=1) **[4]**

1) MOV BL, [SI + 6AB7H]
2) MOV CX,97FFh [BP][SI]
3) MOV CS: [BX], DL
4) MOV SI, DI

TABLE-1: For Question 2(b)

Operands	Memory Operands			Register Operands
	No Displacement	Displacement 8 bits	Displacement 16 bits	
MOD	**00**	**01**	**10**	**11**
R/M				W=0 W=1
000	[BX]+[SI]	[BX]+[SI]+DISP8	[BX]+[SI]+DISP16	AL AX
001	[BX]+[DI]	[BX]+[DI] +DISP8	[BX]+[DI] +DISP16	CL CX
010	[BP]+[SI]	[BP]+[SI]+DISP8	[BP]+[SI]+DISP16	DL DX
011	[BP]+[DI]	[BP]+[DI]+DISP8	[BP]+[DI]+DISP16	BL BX
100	[SI]	[SI]+DISP8	[SI]+DISP16	AH SP
101	[DI]	[DI]+DISP8	[DI]+DISP16	CH BP
110	DATA 16 (DIRECTADDRESS)	[BP]+DISP8	[BP]+DISP16	DH SI
111	[BX]	[BX]+DISP8	[BX]+DISP16	BH DI

Q2 (C) Selector of the following descriptor must be loaded into which segment register of 80386 in PM and why? Which are all the checks 80386 will do and will there be exception(s) due to these checks? **[4]**

		Byte
06	8F	6
F1	3D	4
85	B2	2
FF	FF	0

Now if following instruction is executed in PM of 80386 :
MOV [0077FFFFh],57623A05h Will there be any exception? Justify your answer. If any exception, suggest the modification in the descriptor to avoid that exception.

(D) Shown below is a system with one-page directory PD and three-page tables PT0-PT3. CR3 register is initialized to the base address of PD. Determine the effective physical address for the following linear address: 00C029ABh. Describe every step. Bottom entry is the starting entry of each table. **[4]**

00160003h	0AB0003h	059000003h	780450003h	9AB00003h
00140003h	02500003h	02600003h	044A0003h	7FF00003h
00150003h	0A000003h	0B000003h	0B055003h	00570003h
00130003h	12000003h	22A00003h	2A100003h	97B00003h
Page Dir	**PT0**	**PT1**	**PT2**	**PT3**

(E) If a program has 15% conditional branch instructions and 8% unconditional branch instructions and if 20% of conditional branches are taken branches. The probability of branch instructions found in BTB is 0.92 and 85% cases the branch prediction base on BTB is correct. calculate the % loss in speedup for SMAC2P. **[4]**

Q.3 Attempt the following questions. **[18]**

Q.3 (a) An Examination paper has 5 questions to be answered and there are 2000 answer books. Each answer takes 10 minutes to correct. Consider 5 teachers are employed to correct the papers. Every question is not answered by all candidates. 10% candidates do not answer question-1, 15% candidates do not answer question-2, 20% candidates do not answer question-3, 25% candidates do not answer question-4. 5% candidates do not answer question-5. **[6]**

(I)If pipeline method is used to correct answer books What is the speed up and efficiency of this method?

(II)If Agenda parallelism method is used to correct answer books What is the speed up and efficiency of this method?

(III)What is the speedup of agenda parallelism method over pipeline method?

(b) If a far pointer of a user CALL instruction consists of 48-bit virtual address as 600800007F90h, what is the starting physical address of segment descriptor? The content of GDTR is 74DE261370FFh. If GDT contains following descriptor: **[6]**

		Byte
00 h	F0 h	6
AC h	79 h	4
CB h	D6 h	2
7F h	FF h	0

Describe above segment descriptor in detail. Will processor allow to execute the CALL instruction? Justify your answer. What is the starting physical address of the subroutine?

(c) Explain in detail the "Task switching" mechanism implemented in PM of 80386 and four ways to switch the task in detail. **[6]**

OR

Q.3 (a) I) For the given sequence of instruction develop superscalar pipeline execution diagram (Assume one floating point and two integer execution unit, register forwarding is also used). **[6]**

Instruction	Number of cycles needed	Arithmetic unit needed
R2←R2/R7	2	Floating point
R3←R2-R1	1	Integer

R1←R7+9	1	Integer
R8←R2 + R6	1	Integer
R4←R5*R8	2	Floating point
R7←R2+5	1	Integer
R2←R1-2	1	Integer
R9←R6*R8	2	Floating point

II) Is it possible to rename registers to reduce the number of execution cycles? If yes, list out renamed instructions for this instruction set. If no, justify your answer.

III)Reschedule instruction (if possible) to reduce the number of cycles needed to execute this set of instructions.

(b) If an interrupt comes on IR2 pin of 8259 and upper five bits of ICW2 contains $(00011)_B$ and IDTR=0050BC0000FFh, will there be any exception? If any exception, correct the content of IDTR. If no, Why? The following is the interrupt Gate descriptor whose content is as follows and it is accessed when interrupt is arrived on IR2 then what is physical address of this Interrupt Gate descriptor? **[6]**

		Byte
07FF h		6
FEh	00h	4
09A0h		2
1234h		0

Prove that it is a valid interrupt gate descriptor. Now if GDTR=00088990007Fh, selector of interrupt gate descriptor will generate any exception? If yes, do the correction in the above descriptor/GDTR such that there would not be any exception. If no, why?

(C) Write a main line program which calls the procedure Solve_Quadratic to get the value of Discriminant (Δ). A, B and C values have been passed on the stack by main line program and the procedure Solve_Quadratic returns the Discriminant (Δ) value in AX. Write main line and procedure program for turbo assembler. Write down steps to assemble and execute the program. Draw the stack frame neatly. **[6]**