# **High Performance Computing (HPC) MCQs** [set-9]

201. A processor performing fetch or decoding of different instruction during the		
execution of another instruction is called		
A. super-scaling		
B. pipe-lining		
C. parallel computation		
D. none of these Answer: B		
202. General MIMD configuration usually called		
A. a multiprocessor		
B. a vector processor		
C. array processor		
A. a multiprocessor B. a vector processor C. array processor D. none of the above.  Answer: A		
203. A Von Neumann computer uses which one of the following?		
A. sisd		
B. simd		
C. misd		
D. mimd. Answer: A		
204. MIMD stands for		
A. multiple instruction multiple data		
B. multiple instruction memory data		
C. memory instruction multiple data		
D. multiple information memory data  Answer: A		

## 205. MIPS stands for:

A. memory instruction per second

B. major instruction per secondC. main information per secondD. million instruction per second

Answer: D

### 206. M.J. Flynn's parallel processing classification is based on:

- A. multiple instructions
- B. multiple data
- C. both (a) and (b)
- D. none of the above

Answer: C

#### 207. VLIW stands for:

- A. vector large instruction word
- B. very long instruction word
- C. very large integrated word
- D. very low integrated word

Answer: B

## 208. The major disadvantage of pipeline is:

- A. high cost individual dedicated
- B. initial setup time
- C. if branch instruction is encountered the pipe has to be flushed
- D. all of the above

Answer: C

## 209. A topology that involves Tokens.

- A. star
- B. ring
- C. bus
- D. daisy chaining

Answer: B

## 210. multipoint topology is

- A. bus
- B. star
- C. mesh

D. ring Answer: A	
211. In super-scalar mode, all the similar instructions are gr	couped and executed
together.	
A. true	
B. false Answer: A	
212. Which mechanism performs an analysis on the code to	determine which data
items may become unsafe for caching, and they mark those	items accordingly?
A. directory protocol	
B. snoopy protocol	
C. server based cache coherence	
D. compiler based cache coherence Answer: D	
213. How many processors can be organized in 5-dimension	al binary hypercube
system?	
A. 25	
B. 10	
C. 32	
D. 20	
Answer: C	
214. Multiprocessors are classified as	
A. simd	
B. mimd	
C. sisd	
D. misd Answer: B	
215. Which of the following is not one of the interconnection	structures?
A. crossbar switch	
B. hypercube system	
C. single port memory	
D. time-shared common bus	
Answer: C	

216. Which combinational device is used in crossbar switch for selecting proper
memory from multiple addresses?
A. multiplexer
B. decoder
C. encoder
D. demultiplexer
Answer: A
217. How many switch points are there in crossbar switch network that connects 9
processors to 6 memory modules?
A. 50
B. 63
C. 60
D. 54 Answer: D
218. In a three-cube structure, node 101 cannot communicate directly with node?
A. 1
B. 11
C. 100
D. 111 Answer: B
219. Which method is used as an alternative way of snooping-based coherence
protocol?
A. directory protocol
B. memory protocol
C. compiler based protocol
D. none of above Answer: A
220. snoopy cache protocol are used inbased system
A. bus
B. mesh
C. star
D. hypercube Answer: A

221. superscalar architecture containsexecution units for instruction
execution
A. multiple
B. single
C. none of the above Answer: A
222. time taken by header of a message between two directly connected nodes is
called as
A. startup time
B. per hop time
C. per word transfer time
D. packaging time Answer: B
223. the number of switch requirement for a network with n input and n output is
A. n
B. n2
C. n3
D. n4
Answer: B
224. which of the following is not static network
A. bus
B. ring
C. mesh
D. crossbar switch Answer: D
225. In super-scalar processors, mode of execution is used.
A. in-order
B. post order
C. out of order
D. none of the mentioned  Answer: C