# High Performance Computing (HPC) MCQs [set-1]

**1. A CUDA program is comprised of two primary components: a host and a _____.**

A. gpu??kernel

B. cpu??kernel

C. os

D. none of above

Answer: A

**2. The kernel code is dentified by the _____qualifier with void return type**

A. _host_

B. __global__??

C. _device_

D. void

Answer: B

**3. The kernel code is only callable by the host**

A. true

B. false

Answer: A

**4. The kernel code is executable on the device and host**

A. true

B. false

Answer: B

**5. Calling a kernel is typically referred to as _____.**

A. kernel thread

B. kernel initialization

C. kernel termination

D. kernel invocation

Answer: D

## 6. Host codes in a CUDA application can Initialize a device

A. true

B. false

Answer: A

## 7. Host codes in a CUDA application can Allocate GPU memory

A. true

B. false

Answer: A

## 8. Host codes in a CUDA application can not Invoke kernels

A. true

B. false

Answer: B

## 9. CUDA offers the Chevron Syntax to configure and execute a kernel.

A. true

B. false

Answer: A

## 10. the BlockPerGrid and ThreadPerBlock parameters are related to the _____ model supported by CUDA.

A. host

B. kernel

C. thread??abstraction

D. none of above

Answer: C

## 11. _____ is Callable from the device only

A. _host_

B. __global__??

C. _device_

D. none of above

Answer: C

## 12. _____ is Callable from the host

A. _host_

B. __global__??

C. _device_

D. none of above

Answer: B

---

## 13. _____ is Callable from the host

A. _host_

B. __global__??

C. _device_

D. none of above

Answer: A

---

## 14. CUDA supports _____ in which code in a single thread is executed by all other threads.

A. tread division

B. tread termination

C. thread abstraction

D. none of above

Answer: C

---

## 15. In CUDA, a single invoked kernel is referred to as a _____.

A. block

B. tread

C. grid

D. none of above

Answer: C

---

## 16. A grid is comprised of _____ of threads.

A. block

B. bunch

C. host

D. none of above

Answer: A

---

## 17. A block is comprised of multiple _____.

A. treads

B. bunch

C. host

D. none of above

Answer: A

## 18. a solution of the problem in representing the parallelismin algorithm is

A. cud

B. pta

C. cda

D. cuda

Answer: D

## 19. Host codes in a CUDA application can not Reset a device

A. true

B. false

Answer: B

## 20. Host codes in a CUDA application can Transfer data to and from the device

A. true

B. false

Answer: A

## 21. Host codes in a CUDA application can not Deallocate memory on the GPU

A. true

B. false

Answer: B

## 22. Any condition that causes a processor to stall is called as _____.

A. hazard

B. page fault

C. system error

D. none of the above

Answer: A

## 23. The time lost due to branch instruction is often referred to as _____.

A. latency

B. delay

C. branch penalty

D. none of the above

Answer: C

**24.** _____ method is used in centralized systems to perform out of order execution.

A. scorecard

B. score boarding

C. optimizing

D. redundancy

Answer: B

**25.** The computer cluster architecture emerged as an alternative for _____.

A. isa

B. workstation

C. super computers

D. distributed systems

Answer: C