MINI-PROJECT Project Status			
Project File:	mini-project.ise	**Current State:**	Placed and Routed
Module Name:	tic_tac_toe	• **Errors:**	No Errors
Target Device:	xc5vlx110t-1ff1136	• **Warnings:**	3 Warnings
Product Version:	ISE 9.2i	• **Updated:**	Mon 22. Mar 19:06:17 2021

MINI-PROJECT Partition Summary
No partition information was found.

Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice LUTs	23	69,120	1%	
Number used as logic	23	69,120	1%	
Number using O6 output only	23			
Slice Logic Distribution				
Number of occupied Slices	11	17,280	1%	
Number of LUT Flip Flop pairs used	23			
Number with an unused Flip Flop	23	23	100%	
Number with an unused LUT	0	23	0%	
Number of fully used LUT-FF pairs	0	23	0%	
IO Utilization				
Number of bonded IOBs	73	640	11%	
Specific Feature Utilization				
Total equivalent gate count for design	161			
Additional JTAG gate count for IOBs	3,504			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints		

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon 22. Mar 19:05:00 2021	0	1 Warning	0
Translation Report	Current	Mon 22. Mar 19:05:30 2021	0	0	0
Map Report	Current	Mon 22. Mar 19:05:51 2021	0	2 Warnings	5 Infos
Place and Route Report	Current	Mon 22. Mar 19:06:05 2021	0	0	2 Infos
Static Timing Report	Current	Mon 22. Mar 19:06:15 2021	0	0	3 Infos
Bitgen Report	Out of Date	Sun 21. Mar 16:51:22 2021	0	0	0