```
Release 9.2i - xst J.36
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--> WARNING:Portability - The file path length of <D:/4th
Semester/CS250/CS422-Computer-Architecture-ComputerOrganizationAndDesign5thEdition2014.pdf/data/unsupported/CS422-
Computer-Architecture-ComputerOrganizationAndDesign5thEdition2014.pdf/data/CS422-Computer-Architecture-ComputerOrg
anizationAndDesign5thEdition2014.pdf.acd> exceeds the allowed maximum file path length [260]
Parameter TMPDIR set to ./xst/projnav.tmp
CPU : 0.00 / 0.31 s | Elapsed : 0.00 / 1.00 s

--> Parameter xsthdpdir set to ./xst
CPU : 0.00 / 0.31 s | Elapsed : 0.00 / 1.00 s

--> Reading design: tic_tac_toe.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "tic_tac_toe.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "tic_tac_toe"
Output Format                      : NGC
Target Device                      : xc5vlx110t-1-ff1136

---- Source Options
Top Module Name                    : tic_tac_toe
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : YES
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : YES
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Use DSP Block                      : auto
Automatic Register Balancing       : No
```

```
---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Library Search Order               : tic_tac_toe.lso
Keep Hierarchy                     : NO
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Compilation                              *
=========================================================================
Compiling verilog file "tic_tac_toe.v" in library work
Module <tic_tac_toe> compiled
No errors in compilation
Analysis of file <"tic_tac_toe.prj"> succeeded.


=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for module <tic_tac_toe> in library <work>.


=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing top module <tic_tac_toe>.
Module <tic_tac_toe> is correct for synthesis.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...
```

```
Synthesizing Unit <tic_tac_toe>.
    Related source file is "tic_tac_toe.v".
Unit <tic_tac_toe> synthesized.


=========================================================================
HDL Synthesis Report

Found no macro
=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================

Loading device for application Rf_Device from file '5vlx110t.nph' in environment D:\4th Semester\CS250.

=========================================================================
Advanced HDL Synthesis Report

Found no macro
=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <tic_tac_toe> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block tic_tac_toe, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                          Partition Report                             *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : tic_tac_toe.ngr
Top Level Output File Name         : tic_tac_toe
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : NO

Design Statistics
# IOs                              : 73
```

```
Cell Usage :
# BELS                          : 23
#      LUT3                     : 9
#      LUT5                     : 1
#      LUT6                     : 13
# IO Buffers                    : 73
#      IBUF                     : 72
#      OBUF                     : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 5vlx110tff1136-1


Slice Logic Utilization:
 Number of Slice LUTs:                  23  out of  69120     0%
    Number used as Logic:               23  out of  69120     0%

Slice Logic Distribution:
 Number of Bit Slices used:             23
   Number with an unused Flip Flop      23  out of     23   100%
   Number with an unused LUT:            0  out of     23     0%
   Number of fully used Bit Slices:      0  out of     23     0%

IO Utilization:
 Number of IOs:                         73
 Number of bonded IOBs:                 73  out of    640    11%

Specific Feature Utilization:

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -1

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 7.519ns
```

```
Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 200 / 1
-------------------------------------------------------------------------
Delay:               7.519ns (Levels of Logic = 7)
  Source:            X4<2> (PAD)
  Destination:       F (PAD)

  Data Path: X4<2> to F
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   0.818   0.710  X4_2_IBUF (X4_2_IBUF)
     LUT3:I0->O            1   0.094   0.480  X_four_SW0 (N18)
     LUT6:I5->O            3   0.094   0.984  X_four (X_four)
     LUT5:I0->O            1   0.094   0.480  F152 (F_map51)
     LUT6:I5->O            1   0.094   0.789  F180 (F_map53)
     LUT6:I2->O            1   0.094   0.336  F201 (F_OBUF)
     OBUF:I->O                 2.452          F_OBUF (F)
    ----------------------------------------
    Total                      7.519ns (3.740ns logic, 3.779ns route)
                                       (49.7% logic, 50.3% route)

=========================================================================
CPU : 13.07 / 13.42 s | Elapsed : 13.00 / 14.00 s

-->

Total memory usage is 388080 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    1 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```