Design of Digital Systems Laboratory (CS203)

Mini-Project

Group Number: 13

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Project Number: 13

Problem statement: Consider the Tic-Tac-Toe game:

- It is played on a 3-by-3 grid of squares (Fig-a). The players alternate turns. Each player chooses a square and places a mark in a square (one player uses X and the other O). The first player with three marks in a row, column, or diagonal wins the game.
- The circuit has 9 inputs (X1 to X9) and an output F (Fig-b). The F is '1' if a winning pattern is present and a 0 otherwise.

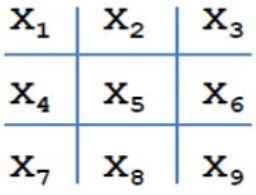


Fig-a

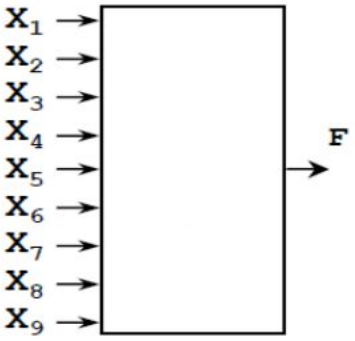


Fig-b

Assume the Boolean expression for F in the SOP form that must be in the row-major, column-major, and diagonal order.
Design, implement, and synthesize a logical circuit for the above electronic tic-tac-toe that indicates the presence of a winning pattern for a player.

Design Procedure: A 3-by-3 Tic-Tac-Toe game has 9 cells where each cell has either an 'X' or 'O' marked by respective participants in each turn. The problem statement is to design a circuit that predicts the presence of the winning pattern for a player. Thus, our digital circuit should take 9 inputs (one for every cell) denoted by X_1 to X_9, and should output F, which is 1 when a winning pattern is present and 0 otherwise.

To solve this problem, we need to consider three cases, which are, participant who marks 'X' wins, participant who marks 'O' wins or neither of them wins. Below is the grid representation of the 3-by-3 tic-tac-toe game,

X_1	X_2	X_3
X_4	X_5	X_6
X_7	X_8	X_9

A participant wins if all the consecutive entries in a row, a column or a diagonal have the character belonging to the participant. The participant who marks 'X' wins if any one of the following condition is met,

$X_1X_2X_3 = "XXX"$,
$X_4X_5X_6 = "XXX"$,
$X_7X_8X_9 = "XXX"$,
$X_1X_4X_7 = "XXX"$,
$X_2X_5X_8 = "XXX"$,
$X_3X_6X_9 = "XXX"$,
$X_1X_5X_9 = "XXX"$,
$X_3X_5X_7 = "XXX"$

Similarly, the participant who marks 'O' wins if any one of the following condition is met,

$X_1X_2X_3 = "OOO"$,
$X_4X_5X_6 = "OOO"$,

$X_7X_8X_9 = "OOO"$,
$X_1X_4X_7 = "OOO"$,
$X_2X_5X_8 = "OOO"$,
$X_3X_6X_9 = "OOO"$,
$X_1X_5X_9 = "OOO"$,
$X_3X_5X_7 = "OOO"$

In all of the above mentioned cases, a winning pattern is present as either of the participants wins and hence, our circuit should output F=1. In all other cases, there is no winning pattern and hence, our circuit should output F=0.

Our design makes use of nine wires (one for every input) that keep a track of whether the corresponding input is 'X' or 'O'. The value represented by the wire is 1 in case the corresponding input is 'X' and 0 in case the input is 'O'. Depending upon these values, the output F is determined by the following boolean expression,

$$F = ((X_1 \&\& X_2 \&\& X_3) \,||\, (X_4 \&\& X_5 \&\& X_6) \,||\, (X_7 \&\& X_8 \&\& X_9) \,||\, (\overline{X_1} \&\& \overline{X_2} \&\& \overline{X_3}) \,||\, (\overline{X_4} \&\& \overline{X_5} \&\& \overline{X_6}) \,||\, (\overline{X_7} \&\& \overline{X_8} \&\& \overline{X_9}) \,||\, (X_1 \&\& X_4 \&\& X_7) \,||\, (X_2 \&\& X_5 \&\& X_8) \,||\, (X_3 \&\& X_6 \&\& X_9) \,||\, (\overline{X_1} \&\& \overline{X_4} \&\& \overline{X_7}) \,||\, (\overline{X_2} \&\& \overline{X_5} \&\& \overline{X_8}) \,||\, (\overline{X_3} \&\& \overline{X_6} \&\& \overline{X_9}) \,||\, (X_1 \&\& X_5 \&\& X_9) \,||\, (X_3 \&\& X_5 \&\& X_7) \,||\, (\overline{X_1} \&\& \overline{X_5} \&\& \overline{X_9}) \,||\, (\overline{X_3} \&\& \overline{X_5} \&\& \overline{X_7}))$$

The terms with X_i in the uncomplemented form represent the winning conditions for the participant who marks 'X' and the terms with X_i in the complemented form represent the winning conditions for the participant who marks 'O'. If atleast one of the terms is 1, then F=1 as there is a winning pattern present, otherwise we get F=0.

Advantages: The advantages of our project are as follows,

- It makes accurate prediction of the presence of the winning pattern for a player in the 3-by-3 Tic-Tac-Toe game
- Takes the input of the grid values separately (i.e one input for every cell) there-by giving more freedom and clarity to the user using the circuit

Disadvantages: The Disadvantages of our project are as follows,

- Our project indicates the presence of the winning pattern for both the participants, and does not indicate which player won specifically. To counter this problem, two additional outputs can be implemented, that check the conditions for winning for each participant and output the result for every participant
- The digital circuit that we have implemented takes all the 9 inputs (one for every cell). Knowledge of all the cell entries is not needed every time, as a 3-by-3 Tic-Tac-Toe game can be won by marking less than 9 cells

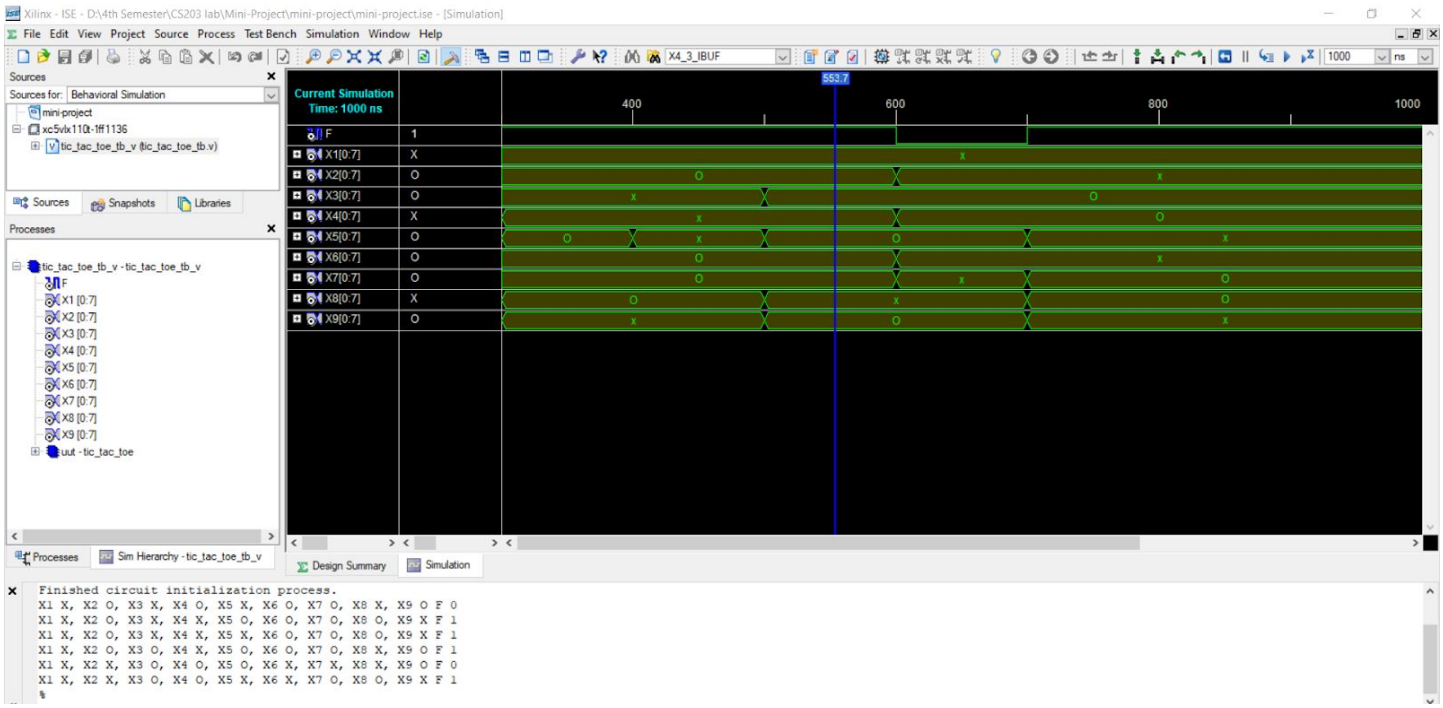
Simulation Procedure:

- The file tic_tac_toe.v contains the verilog code of the circuit that predicts the presence of a winning pattern of a 3-by-3 tic tac toe game. The file tic_tac_toe_tb.v is the test bench to test the working of the circuit.
- All of the following instructions are as per the xilinx 9.2i software
- Create a new project in verilog, and add the verilog module file tic_tac_toe.v and verilog test bench tic_tac_toe_tb.v.
- Synthesize the circuit to check the synthesis report and generate the post-synthesis simulation model
- Perform behavioural simulation to test the working of the circuit by using the test bench
- Implement the design (Translate, map, place & route). After implementing the design, power analysis can be made by selecting the 'Analyze power' option. To analyze the timings, select "Generate the post-place and route static timing".
- Generate the programming file

Simulation Results: Here are some of the snapshots indicating the various results of the simulation conducted of our circuit,

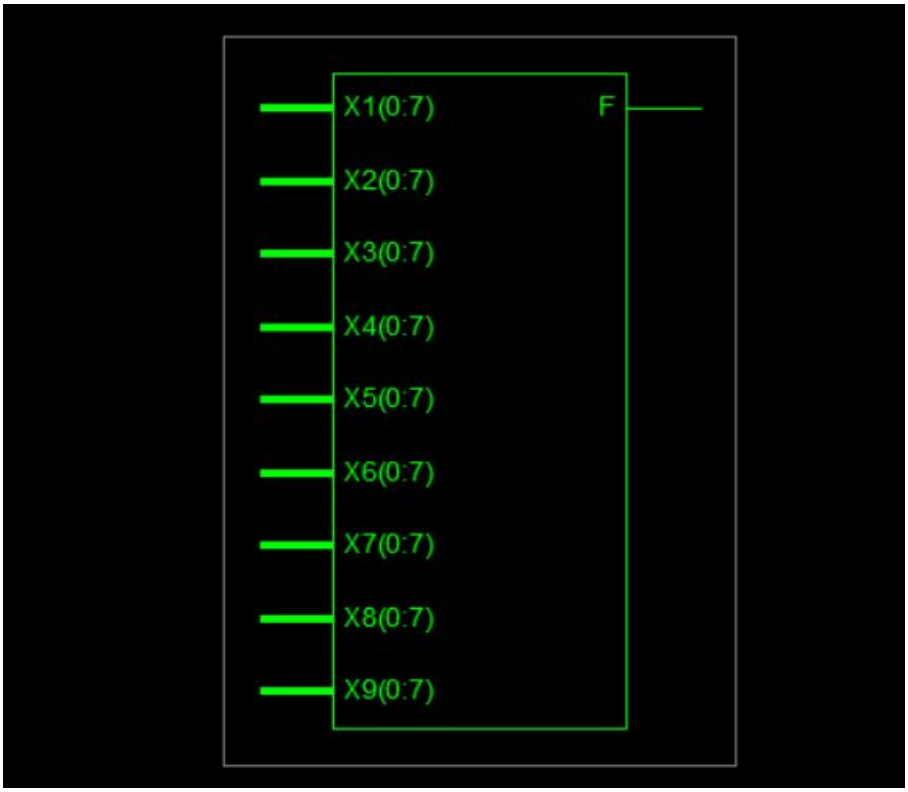
1) Timing diagram:

(Behavioural Implementation)

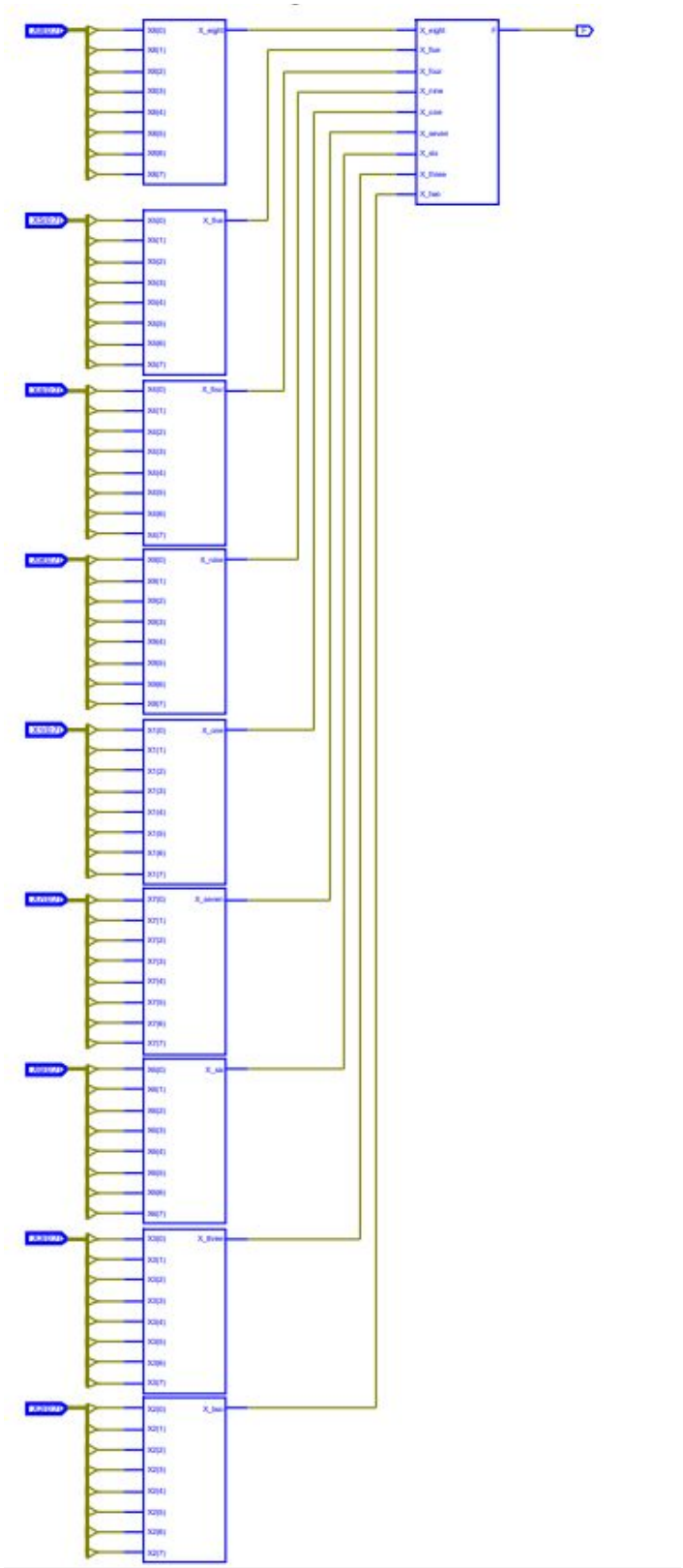


2) Logic Diagrams:

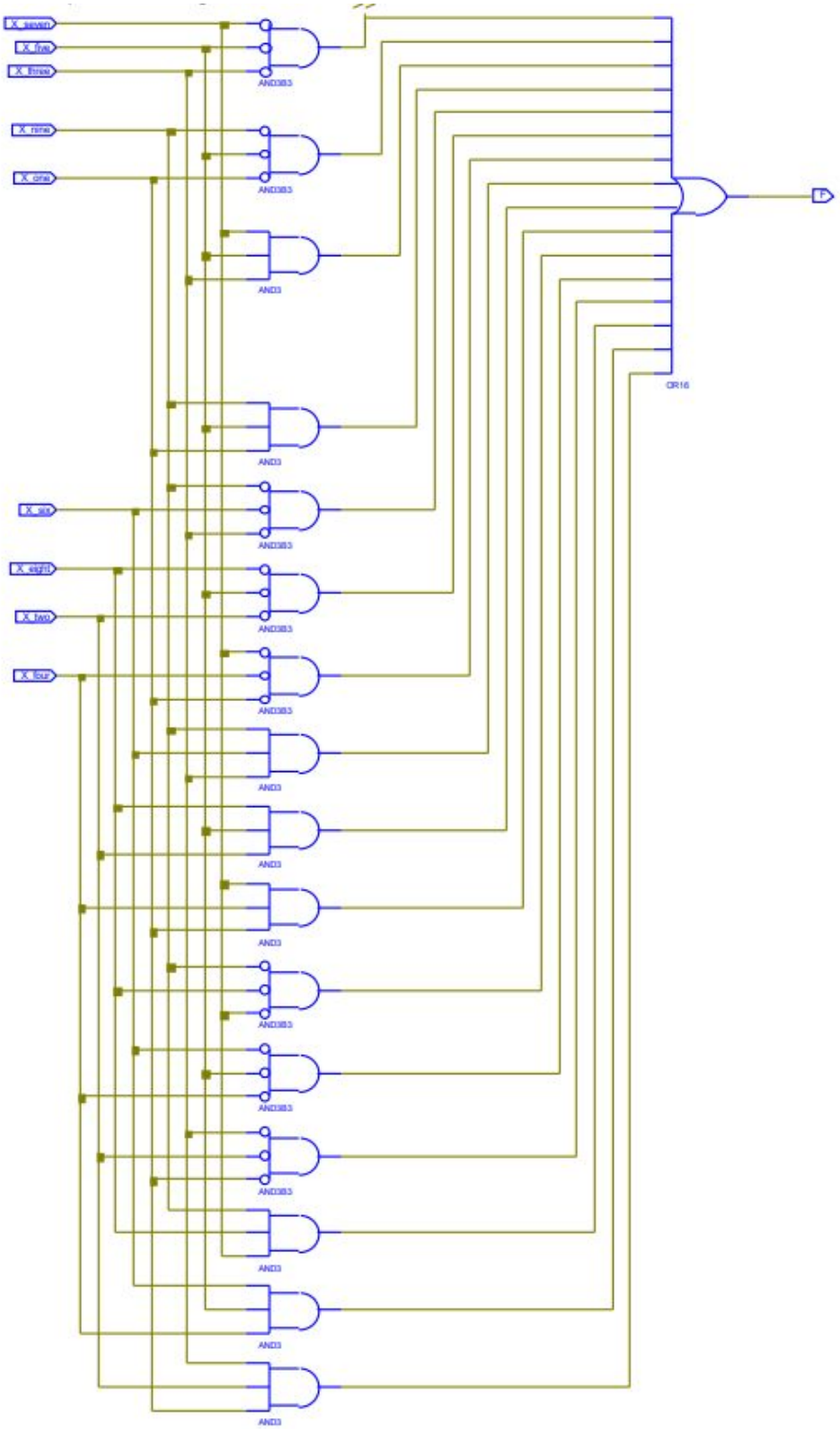
High level view of the circuit: $X_1 - X_9$ are the inputs and F is the output



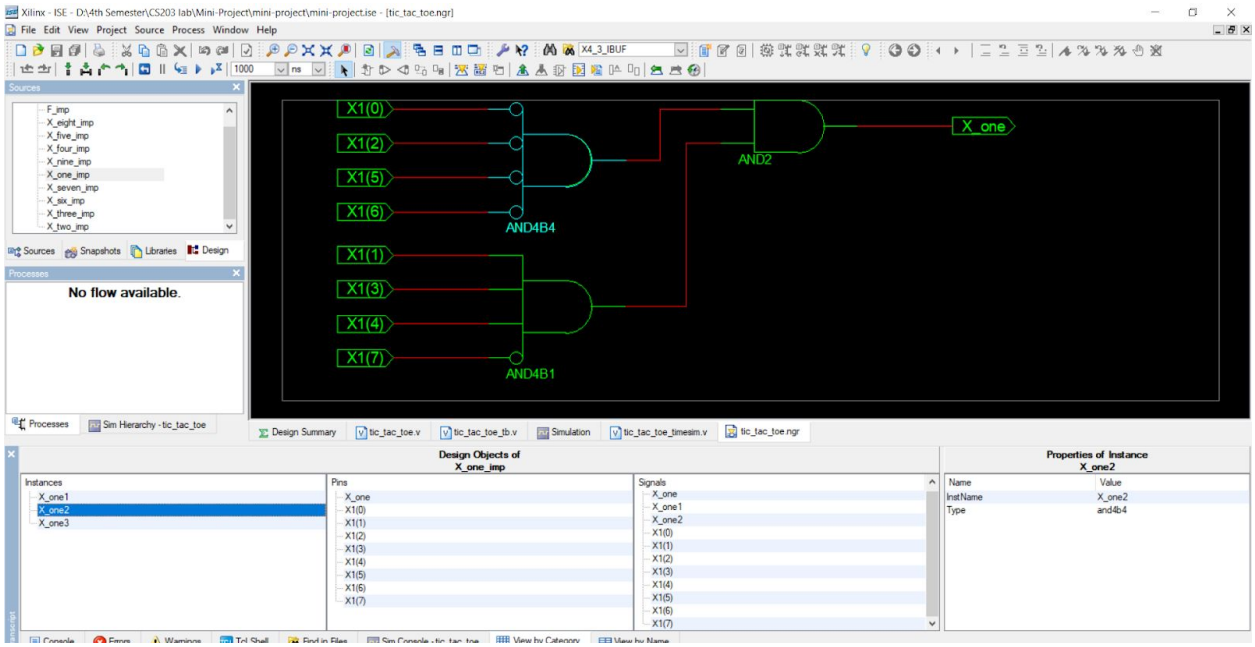
Each of the block on the left corresponds to each input, and the block on the right is same as that shown above



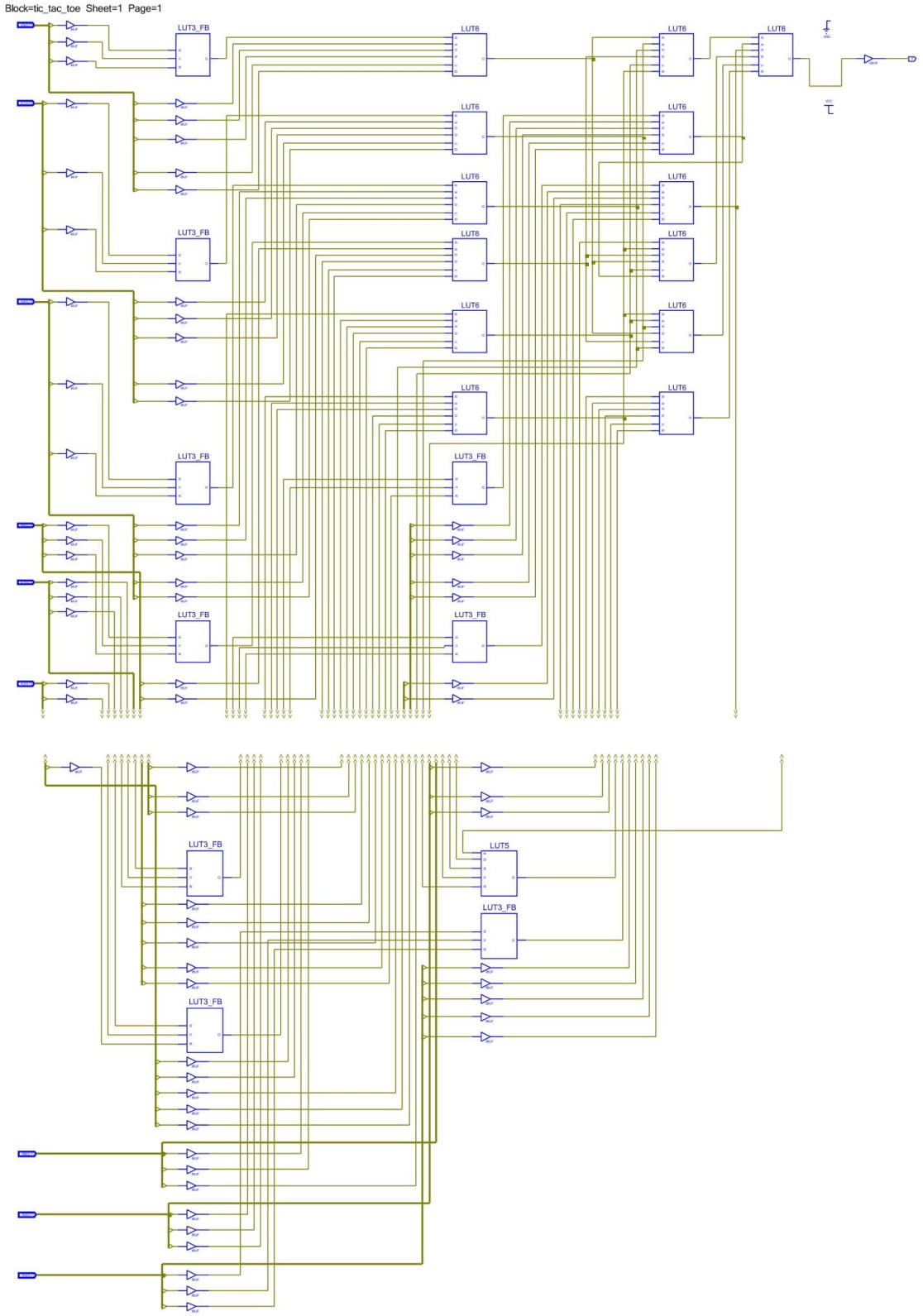
The diagram shown below represents the way boolean expression of F is expressed. There are in all 16 terms in the boolean expression of F.



The diagram shown below represents how the value for each of the X_i is dependent on the value of its 8 bits.



Detailed Technology schematic of the circuit: (The entire image of the circuit is divided into two halves because of the big image). The wires are correspondingly connected.



3) Result Table:

Design summary

MINI-PROJECT Project Status			
Project File:	mini-project.ise	**Current State:**	Placed and Routed
Module Name:	tic_tac_toe	• **Errors:**	No Errors
Target Device:	xc5vlx110t-1ff1136	• **Warnings:**	3 Warnings
Product Version:	ISE 9.2i	• **Updated:**	Mon 22. Mar 19:06:17 2021

MINI-PROJECT Partition Summary
No partition information was found.

Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice LUTs	23	69,120	1%	
Number used as logic	23	69,120	1%	
Number using O6 output only	23			
Slice Logic Distribution				
Number of occupied Slices	11	17,280	1%	
Number of LUT Flip Flop pairs used	23			
Number with an unused Flip Flop	23	23	100%	
Number with an unused LUT	0	23	0%	
Number of fully used LUT-FF pairs	0	23	0%	
IO Utilization				
Number of bonded IOBs	73	640	11%	
Specific Feature Utilization				
Total equivalent gate count for design	161			
Additional JTAG gate count for IOBs	3,504			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints		

Timing delays:

```
================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 200 / 1
--------------------------------------------------------------------------------
Delay:               7.519ns (Levels of Logic = 7)
  Source:            X4<2> (PAD)
  Destination:       F (PAD)

  Data Path: X4<2> to F
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   0.818   0.710  X4_2_IBUF (X4_2_IBUF)
     LUT3:I0->O            1   0.094   0.480  X_four_SW0 (N18)
     LUT6:I5->O            3   0.094   0.984  X_four (X_four)
     LUT5:I0->O            1   0.094   0.480  F152 (F_map51)
     LUT6:I5->O            1   0.094   0.789  F180 (F_map53)
     LUT6:I2->O            1   0.094   0.336  F201 (F_OBUF)
     OBUF:I->O                 2.452          F_OBUF (F)
    ----------------------------------------
    Total                      7.519ns (3.740ns logic, 3.779ns route)
                                       (49.7% logic, 50.3% route)

================================================================================
```

Timing delays for each pad of the input is included in the static timing report, present in the Reports folder.

Power consumption details:

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		818
Vccint 1.00V:	489	489
Vccaux 2.50V:	130	325
Vcco25 2.50V:	2	4
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0
Quiescent Vccint 1.00V:	489	489
Quiescent Vccaux 2.50V:	130	325
Quiescent Vcco25 2.50V:	2	4

Thermal summary:	
Estimated junction temperature:	33C
Ambient temp:	25C
Case temp:	33C
Theta J-A range:	10 - 10C/W

All the detailed reports are present in the Reports folder.