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Release 9.2i Map J.36
Xilinx Mapping Report File for Design 'tic_tac_toe'

Design Information
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Command Line   : D:\4th Semester\CS250\bin\nt\map.exe -ise D:/4th Semester/CS203
lab/Mini-Project/mini-project/mini-project.ise -intstyle ise -p
xc5vlx110t-ff1136-1 -w -logic_opt off -ol high -t 1 -cm area -k 6 -o
tic_tac_toe_map.ncd tic_tac_toe.ngd tic_tac_toe.pcf
Target Device  : xc5vlx110t
Target Package : ff1136
Target Speed   : -1
Mapper Version : virtex5 -- $Revision: 1.36 $
Mapped Date    : Mon Mar 22 19:05:34 2021

Design Summary
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Number of errors:      0
Number of warnings:    2
Slice Logic Utilization:
  Number of Slice LUTs:                        23 out of  69,120    1%
    Number used as logic:                      23 out of  69,120    1%
      Number using O6 output only:             23

Slice Logic Distribution:
  Number of occupied Slices:                   11 out of  17,280    1%
  Number of LUT Flip Flop pairs used:          23
    Number with an unused Flip Flop:           23 out of      23  100%
    Number with an unused LUT:                  0 out of      23    0%
    Number of fully used LUT-FF pairs:          0 out of      23    0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                       73 out of     640   11%

Specific Feature Utilization:

Total equivalent gate count for design:  161
Additional JTAG gate count for IOBs:  3,504
Peak Memory Usage:  452 MB
Total REAL time to MAP completion:  17 secs
Total CPU time to MAP completion:   14 secs

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Section 1 - Errors
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Section 2 - Warnings
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WARNING:LIT:243 - Logical network N187 has no load.
WARNING:LIT:395 - The above warning message base_net_load_rule is repeated 1
   more times for the following (max. 5 shown):
   N188
   To see the details of these warning messages, please use the -detail switch.

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs in the
   schematic.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to
   1.050 Volts)
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
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   2 block(s) removed
   2 signal(s) removed

Section 5 - Removed Logic
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The trimmed logic report below shows the logic removed from your design due to
sourceless or loadless signals, and VCC or ground connections.  If the removal
of a signal or symbol results in the subsequent removal of an additional signal
or symbol, the message explaining that second removal will be indented.  This
indentation will be repeated as a chain of related logic is removed.

To quickly locate the original cause for the removal of a chain of logic, look
above the place where that logic is listed in the trimming report, then locate
the lines that are least indented (begin at the leftmost edge).

The signal "N187" is loadless and has been removed.
 Loadless block "XST_VCC" (ONE) removed.
The signal "N188" is loadless and has been removed.
 Loadless block "XST_GND" (ZERO) removed.

Section 6 - IOB Properties
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| IOB Name                          | Type             | Direction | IO Standard | Drive    | Slew | Reg
(s)      | Resistor | IOB      |
|                                   |                  |           |             | Strength | Rate
|              |          | Delay    |
+-----------------------------------------------------------------------------------------------------------------------
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| F                                 | IOB              | OUTPUT    | LVCMOS25    | 12       | SLOW
|              |          |          |
| X1<0>                             | IOB              | INPUT     | LVCMOS25    |          |
|              |          |          |
| X1<1>                             | IOB              | INPUT     | LVCMOS25    |          |
|              |          |          |
| X1<2>                             | IOB              | INPUT     | LVCMOS25    |          |
|              |          |          |
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X1<3>	IOB	INPUT	LVCMOS25		
X1<4>	IOB	INPUT	LVCMOS25		
X1<5>	IOB	INPUT	LVCMOS25		
X1<6>	IOB	INPUT	LVCMOS25		
X1<7>	IOB	INPUT	LVCMOS25		
X2<0>	IOB	INPUT	LVCMOS25		
X2<1>	IOB	INPUT	LVCMOS25		
X2<2>	IOB	INPUT	LVCMOS25		
X2<3>	IOB	INPUT	LVCMOS25		
X2<4>	IOB	INPUT	LVCMOS25		
X2<5>	IOB	INPUT	LVCMOS25		
X2<6>	IOB	INPUT	LVCMOS25		
X2<7>	IOB	INPUT	LVCMOS25		
X3<0>	IOB	INPUT	LVCMOS25		
X3<1>	IOB	INPUT	LVCMOS25		
X3<2>	IOB	INPUT	LVCMOS25		
X3<3>	IOB	INPUT	LVCMOS25		
X3<4>	IOB	INPUT	LVCMOS25		
X3<5>	IOB	INPUT	LVCMOS25		
X3<6>	IOB	INPUT	LVCMOS25		
X3<7>	IOB	INPUT	LVCMOS25		
X4<0>	IOB	INPUT	LVCMOS25		
X4<1>	IOB	INPUT	LVCMOS25		
X4<2>	IOB	INPUT	LVCMOS25		
X4<3>	IOB	INPUT	LVCMOS25		
X4<4>	IOB	INPUT	LVCMOS25		
X4<5>	IOB	INPUT	LVCMOS25		
X4<6>	IOB	INPUT	LVCMOS25		
X4<7>	IOB	INPUT	LVCMOS25		
X5<0>	IOB	INPUT	LVCMOS25		
X5<1>	IOB	INPUT	LVCMOS25		
X5<2>	IOB	INPUT	LVCMOS25		
X5<3>	IOB	INPUT	LVCMOS25		

X5<4>			IOB	INPUT	LVCMOS25	
X5<5>			IOB	INPUT	LVCMOS25	
X5<6>			IOB	INPUT	LVCMOS25	
X5<7>			IOB	INPUT	LVCMOS25	
X6<0>			IOB	INPUT	LVCMOS25	
X6<1>			IOB	INPUT	LVCMOS25	
X6<2>			IOB	INPUT	LVCMOS25	
X6<3>			IOB	INPUT	LVCMOS25	
X6<4>			IOB	INPUT	LVCMOS25	
X6<5>			IOB	INPUT	LVCMOS25	
X6<6>			IOB	INPUT	LVCMOS25	
X6<7>			IOB	INPUT	LVCMOS25	
X7<0>			IOB	INPUT	LVCMOS25	
X7<1>			IOB	INPUT	LVCMOS25	
X7<2>			IOB	INPUT	LVCMOS25	
X7<3>			IOB	INPUT	LVCMOS25	
X7<4>			IOB	INPUT	LVCMOS25	
X7<5>			IOB	INPUT	LVCMOS25	
X7<6>			IOB	INPUT	LVCMOS25	
X7<7>			IOB	INPUT	LVCMOS25	
X8<0>			IOB	INPUT	LVCMOS25	
X8<1>			IOB	INPUT	LVCMOS25	
X8<2>			IOB	INPUT	LVCMOS25	
X8<3>			IOB	INPUT	LVCMOS25	
X8<4>			IOB	INPUT	LVCMOS25	
X8<5>			IOB	INPUT	LVCMOS25	
X8<6>			IOB	INPUT	LVCMOS25	
X8<7>			IOB	INPUT	LVCMOS25	
X9<0>			IOB	INPUT	LVCMOS25	
X9<1>			IOB	INPUT	LVCMOS25	
X9<2>			IOB	INPUT	LVCMOS25	
X9<3>			IOB	INPUT	LVCMOS25	

X9<4>	IOB	INPUT	LVCMOS25	
X9<5>	IOB	INPUT	LVCMOS25	
X9<6>	IOB	INPUT	LVCMOS25	
X9<7>	IOB	INPUT	LVCMOS25	
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Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

Section 10 - Modular Design Summary

Modular Design not used for this design.

Section 11 - Timing Report

Section 12 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 13 - Control Set Information

Use the "-detail" map option to print out Control Set Information.