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Release 9.2i par J.36
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LAPTOP-AVIS85FA::  Mon Mar 22 19:05:55 2021

par -w -intstyle ise -ol std -t 1 tic_tac_toe_map.ncd tic_tac_toe.ncd
tic_tac_toe.pcf


Constraints file: tic_tac_toe.pcf.
Loading device for application Rf_Device from file '5vlx110t.nph' in environment D:\4th Semester\CS250.
   "tic_tac_toe" is an NCD, version 3.1, device xc5vlx110t, package ff1136, speed -1

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 0.950 Volts. (default - Range: 0.950 to 1.050 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints
("par
   -x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
   internal clocks in this design. The PAR timing summary will list the performance achieved for each clock.
Note: For
   the fastest runtime, set the effort level to "std".  For best performance, set the effort level to "high".
For a
   balance between the fastest runtime and best performance, set the effort level to "med".

Device speed data version:  "PRELIMINARY 1.54 2007-04-25".


INFO:Par:253 - The Map -timing placement will be retained since it is likely to achieve better performance.

Device Utilization Summary:

   Number of External IOBs                  73 out of 640    11%
      Number of LOCed IOBs                  73 out of 73    100%

   Number of Slice Registers                 0 out of 69120   0%
      Number used as Flip Flops              0
      Number used as Latches                 0
      Number used as LatchThrus              0

   Number of Slice LUTS                     23 out of 69120   1%
   Number of Slice LUT-Flip Flop pairs      23 out of 69120   1%


Overall effort level (-ol):   Standard
Router effort level (-rl):    Standard

Starting Router

Phase 1: 111 unrouted;       REAL time: 9 secs

Phase 2: 111 unrouted;       REAL time: 9 secs

Phase 3: 70 unrouted;       REAL time: 9 secs

Phase 4: 70 unrouted; (0)      REAL time: 9 secs

Phase 5: 70 unrouted; (0)      REAL time: 9 secs

Phase 6: 0 unrouted; (0)      REAL time: 9 secs

Phase 7: 0 unrouted; (0)      REAL time: 9 secs

Phase 8: 0 unrouted; (0)      REAL time: 9 secs
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Total REAL time to Router completion: 9 secs
Total CPU time to Router completion: 9 secs

Partition Implementation Status
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  No Partitions were found in this design.

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Generating "PAR" statistics.


   The Delay Summary Report


The NUMBER OF SIGNALS NOT COMPLETELY ROUTED for this design is: 0

   The AVERAGE CONNECTION DELAY for this design is:        1.012
   The MAXIMUM PIN DELAY IS:                               1.562
   The AVERAGE CONNECTION DELAY on the 10 WORST NETS is:   1.470

   Listing Pin Delays by value: (nsec)

    d < 1.00   < d < 2.00  < d < 3.00  < d < 4.00  < d < 5.00  d >= 5.00
   ---------   ---------   ---------   ---------   ---------   ---------
          52          59           0           0           0           0

Timing Score: 0



Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 10 secs
Total CPU time to PAR completion: 10 secs

Peak Memory Usage:  369 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file tic_tac_toe.ncd



PAR done!
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