# SVR ENGINEERING COLLEGE

## PHYSICS OF ELECTRONIC MATERIALS AND DEVICES

**by**

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## 3. Physics of Semiconductor Devices

### Light Emitting Diode(LED) :

Introduction :

LEDs, or Light-Emitting Diodes, are semiconductor devices that convert electrical energy into light energy.

In 1962, Nick Holonyak has come up with the idea of a light-emitting diode, and he was working for the general electric company. The LED is a special type of diode and they have similar electrical characteristics to a PN junction diode. Hence the LED allows the flow of current in the forward direction and blocks the current in the reverse direction. The LED occupies a small area which is less than 1 $mm^2$.

Band Structure:

In a solid material, such as a semiconductor, the electrons occupy specific energy levels called bands. The two main bands relevant to LED operation are the valence band and the conduction band. The valence band contains electrons that are bound to atoms, while the conduction band contains electrons that are free to move.

The energy gap between the valence band and the conduction band is known as the band gap. In an LED, the semiconductor material is carefully chosen to have a specific band gap, which determines the color of light emitted by the LED.

PN junction :

A PN junction is a crucial component of a light-emitting diode (LED). An LED is a semiconductor device that emits light when current flows through it. The PN junction within an LED is responsible for the conversion of electrical energy into light energy.

The PN junction is formed by joining two types of semiconductors: P-type and N-type. The P-type region is doped with impurities that create an excess of positively charged "holes," while the N-type region is doped with impurities that create an excess of negatively charged electrons. When the P and N regions are brought together, the excess electrons from the N-type region migrate into the P-type region,

filling the holes. This migration of charges creates a region near the junction called the depletion zone.

The depletion zone is a thin region near the PN junction that lacks any mobile charge carriers. Within this zone, electrons from the N-type side combine with holes from the P-type side, resulting in the release of energy in the form of light. This process is known as recombination.

To facilitate efficient recombination and light emission, LED materials are typically chosen to have a wide band gap. The wider the band gap, the higher the energy of the emitted photons and the shorter the wavelength of light produced. Different semiconductor materials with varying band gaps are used to produce LEDs that emit different colors of light, such as red, green, blue, or other colors.

By applying a forward bias voltage to the PN junction (connecting the P-type side to the positive terminal and the N-type side to the negative terminal of a power supply), current flows through the PN junction, and recombination occurs, resulting in the emission of light. The intensity of light emitted by the LED is directly proportional to the current passing through it.

Typical Characteristics of LED under equilibrium & under bias :

Under equilibrium:

1.Energy Band Diagram: In the energy band diagram, under equilibrium conditions, the LED (Light-Emitting Diode) is in a non-conductive state, and the energy bands are separated by a band gap. The valence band is fully occupied by electrons, while the conduction band is empty.

2.No Current Flow: In the absence of an external bias, no current flows through the LED. The device is in a stable state with no net movement of charge carriers.

Under bias:

1.Forward Bias: When a forward bias is applied to an LED, the positive terminal of the power supply is connected to the p-type region, and the negative terminal is connected to the n-type region. This bias reduces the width of the depletion region.

2.Injection of Carriers: The forward bias allows the injection of minority carriers (electrons from the n-region and holes from the p-region) across the junction. Electrons move from the n-side to the p-side, while holes move from the p-side to the n-side.

3.Recombination: As electrons and holes are injected across the junction, they recombine in the active region of the LED, which is typically made of a

semiconductor material with a direct bandgap. This recombination process releases energy in the form of photons.

4.Photon Emission: The recombination of electrons and holes in the active region generates photons with a specific energy determined by the bandgap of the material. The photons are emitted as light, and their energy corresponds to the wavelength of the emitted light.

5.Light Output: The emitted photons pass through the transparent layers of the LED, resulting in the production of visible light. The color of the emitted light depends on the bandgap energy of the semiconductor material used in the LED.

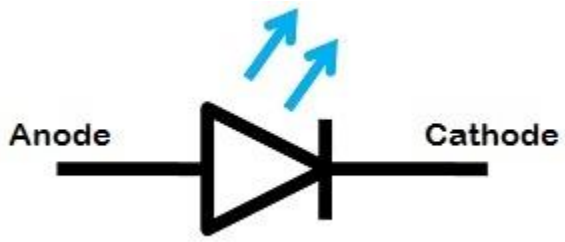
6.Current Flow: Under bias, a forward current flows through the LED, allowing the continuous injection and recombination of carriers, resulting in the sustained emission of light.

7.Efficiency: LEDs operate with high efficiency compared to traditional lighting sources since they primarily convert electrical energy into light energy rather than heat.

The above characteristics may vary depending on the specific design and materials used in an LED.

LED Symbol :

The LED symbol is similar to a diode symbol except for two small arrows that specify the emission of light, thus it is called LED (light-emitting diode). The LED includes two terminals namely anode (+) and the cathode (-). The LED symbol is shown below.




Construction & Working of LED :

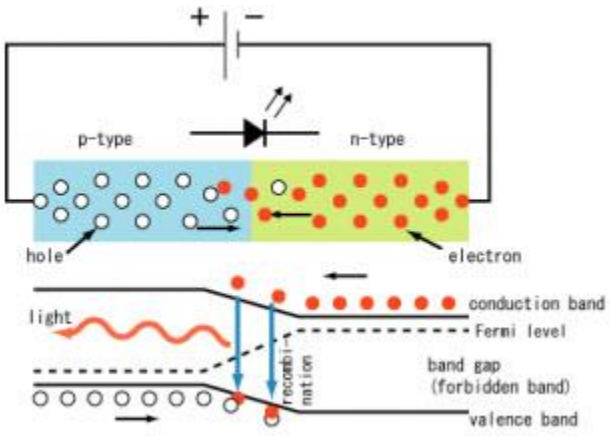
Construction :

The construction of LED is very simple because it is designed through the deposition of three semiconductor material layers over a substrate. These three layers are arranged one by one where the top region is a P-type region, the middle region is active and finally, the bottom region is N-type. The three regions of semiconductor

material can be observed in the construction. In the construction, the P-type region includes the holes; the N-type region includes electrons whereas the active region includes both holes and electrons.

When the voltage is not applied to the LED, then there is no flow of electrons and holes so they are stable. Once the voltage is applied then the LED will forward biased, so the electrons in the N-region and holes from P-region will move to the active region. This region is also known as the depletion region. Because the charge carriers like holes include a positive charge whereas electrons have a negative charge so the light can be generated through the recombination of polarity charges.

Working :




The light emitting diode simply, we know as a diode.

- The P- type silicon contains holes and n-type contains electrons.
- The power supply across the p-n junction makes the diode forward biased and pushing the electrons from n-type to p-type. Pushing the holes in the opposite direction.
- Electron and holes at the junction are combined.
- The photons are given off as the electrons and holes are recombined.
- When the diode is forward biased, then the electrons & holes are moving fast across the junction and they are combining constantly, removing one another out.
- Soon after the electrons are moving from the n-type to the p-type silicon, it combines with the holes, and then it disappears.
- Hence it makes the complete atom & more stable and it gives the little burst of energy in the form of a tiny packet or photon of light.

Advantages of LED :

1.Low power consumption.

2.Long life (about 50000 hours) if stable voltage source is used.

3.It starts quickly i.e. no warm up time is required.

4. Not affected by surrounding temperature.

5. Less self heating.

6. The light is directional so it can be focused onto working plane directly. Wastage of light is avoided.

7. It does not contain mercury and any other gases.

8. Color rendering is excellent.

9. Small in size and weight.

10. More energy efficient.

11. Not damaged due to external shock.

Disadvantages of LED **:**

1.Stable voltage source is required.

2.Life is affected due to voltage fluctuations.

3.Initial cost is more.

Applications of LED **:**

1.Indicating lamps.

2.Bi-color indicators.

3. Fault-indicators.

4. Display-boards.

5. Decorative lighting.

6. Wrist watches.

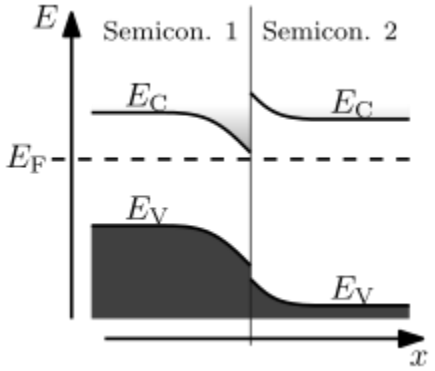
7. In automobile industries as electro-mechanical control.

8. In instrumentation.

**Heterojunctions :**

Heterojunctions play a crucial role in semiconductor devices and electronics. A heterojunction is formed when two different semiconductor materials with dissimilar bandgaps are brought into contact. The interface between these materials creates a junction that possesses unique properties not found in homogeneous materials. In a heterojunction, the properties of the materials on either side of the junction can differ significantly. This contrast gives rise to interesting electronic and optical phenomena, making heterojunctions essential in various semiconductor devices. These devices include transistors, light-emitting diodes (LEDs), solar cells, and laser diodes.

Here are some of the important roles and applications of heterojunctions in semiconductors:




1. Bandgap Engineering: Heterojunctions allow for precise control of the bandgap in a semiconductor device. By combining materials with different bandgaps, engineers can create a junction with a tailored bandgap. This enables the design of devices that can emit, detect, or modulate light at specific wavelengths, making them crucial in optoelectronic applications such as LEDs (light-emitting diodes) and laser diodes.

2.Carrier Confinement: Heterojunctions can confine charge carriers (electrons and holes) to specific regions within a semiconductor device. This confinement results in enhanced carrier mobility, reduced scattering, and improved device performance. For example, heterojunctions are used in high-electron-mobility transistors (HEMTs) to achieve high-speed and low-noise amplification.

3.Tunneling and Barrier Formation: Heterojunctions create energy barriers that can control the flow of charge carriers across the junction. This phenomenon is exploited in tunnel diodes, where the heterojunction enables the tunneling of charge carriers through the barrier, leading to unique properties like negative differential resistance.

4.Photovoltaic Devices: Heterojunctions are utilized in solar cells and photovoltaic devices. They help in efficient charge separation and collection, allowing for better conversion of light energy into electrical energy. Heterojunction solar cells, such as silicon-based heterojunction solar cells, have demonstrated high conversion efficiencies due to their superior electrical characteristics.

5.Integrated Circuits: Heterojunctions are essential for fabricating advanced integrated circuits. They enable the integration of different types of materials, such as III-V compound semiconductors and silicon, to combine their unique properties. This integration is important for the development of high-performance electronic devices, such as high-speed transistors and low-power logic circuits.

Heterojunctions can be created by growing or depositing one material on another using various techniques such as molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), or physical vapor deposition (PVD). The careful selection and combination of materials with different properties enable engineers and scientists to tailor the electronic and optical characteristics of the heterojunction for specific applications.

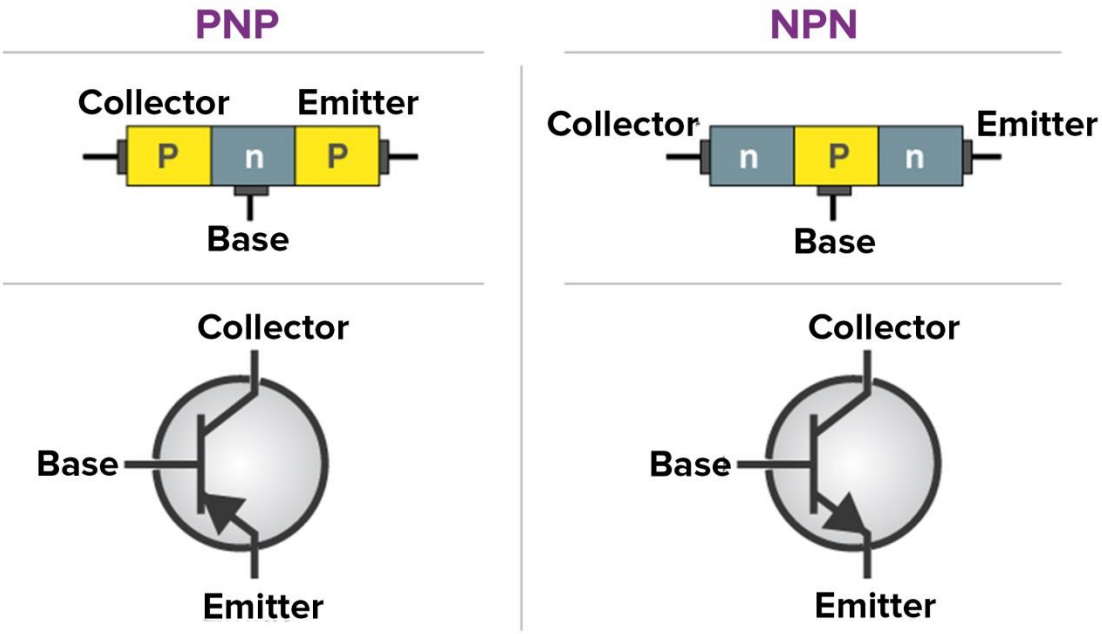
**Transistor :**

Definition: The transistor is a semiconductor device which transfers a weak signal from low resistance circuit to high resistance circuit. The words **trans** mean transfer property and **istor** mean resistance property offered to the junctions. In other words, it is a switching device which regulates and amplify the electrical signal likes voltage or current.

The transistor consists two PN diode connected back to back. It has three terminals namely emitter, base and collector. The base is the middle section which is made up of thin layers. These names are given as per the common terminal of the transistor. The emitter based junction of the transistor is connected to forward biased and the collector-base junction is connected in reverse bias which offers a high resistance.

Transistor Symbols:

There are two types of transistor, namely NPN transistor and PNP transistor. The transistor which has two blocks of n-type semiconductor material and one block of P-type semiconductor material is known as NPN transistor. Similarly, if the material has one layer of N-type material and two layers of P-type material then it is called PNP transistor. The symbol of NPN and PNP is shown in the figure below.




The arrow in the symbol indicates the direction of flow of conventional current in the emitter with forward biasing applied to the emitter-base junction. The only difference between the NPN and PNP transistor is in the direction of the current.

Transistor Terminals :

The transistor has three terminals namely, emitter, collector and base. The terminals of the diode are explained below in details.

**Emitter –** The section that supplies the large section of majority charge carrier is called emitter. The emitter is always connected in forward biased with respect to the base so that it supplies the majority charge carrier to the base. The emitter-base junction injects a large amount of majority charge carrier into the base because it is heavily doped and moderate in size.

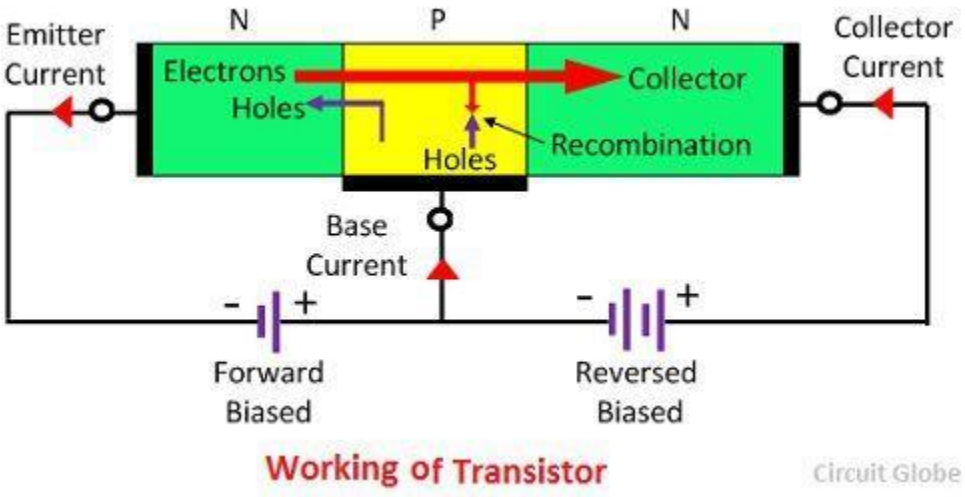
**Collector –** The section which collects the major portion of the majority charge carrier supplied by the emitter is called a collector. The collector-base junction is always in reverse bias. Its main function is to remove the majority charges from its junction with the base. The collector section of the transistor is moderately doped,

but larger in size so that it can collect most of the charge carrier supplied by the emitter.

**Base –** The middle section of the transistor is known as the base. The base forms two circuits, the input circuit with the emitter and the output circuit with the collector. The emitter-base circuit is in forward biased and offered the low resistance to the circuit. The collector-base junction is in reverse bias and offers the higher resistance to the circuit. The base of the transistor is lightly doped and very thin due to which it offers the majority charge carrier to the base.

Working of Transistor:

Usually, silicon is used for making the transistor because of their high voltage rating, greater current and less temperature sensitivity. The emitter-base section kept in forward biased constitutes the base current which flows through the base region. The magnitude of the base current is very small. The base current causes the electrons to move into the collector region or create a hole in the base region.




The base of the transistor is very thin and lightly doped because of which it has less number of electrons as compared to the emitter. The few electrons of the emitter are combined with the hole of the base region and the remaining electrons are moved towards the collector region and constitute the collector current. Thus we can say that the large collector current is obtained by varying the base region.

Advantages :

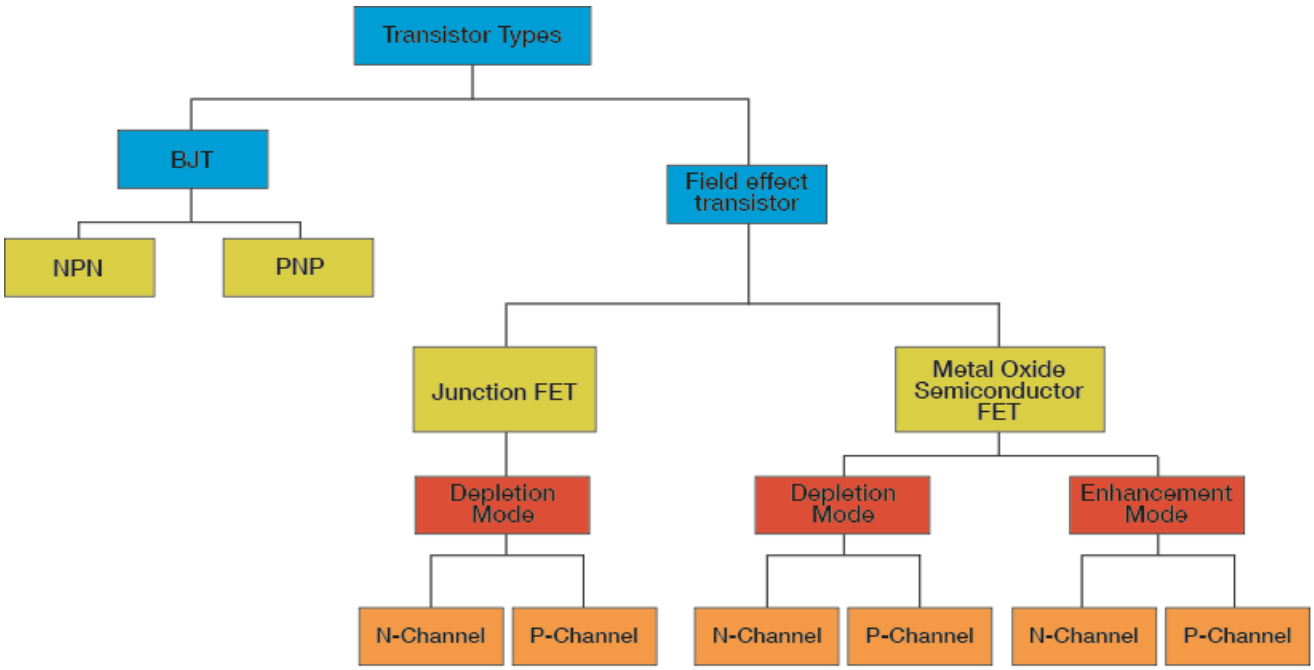
There are many advantages of a transistor such as −

- High voltage gain.

- Lower supply voltage is sufficient.
- Most suitable for low power applications.
- Smaller and lighter in weight.
- Mechanically stronger than vacuum tubes.
- No external heating required like vacuum tubes.
- Very suitable to integrate with resistors and diodes to produce ICs.

There are few disadvantages such as

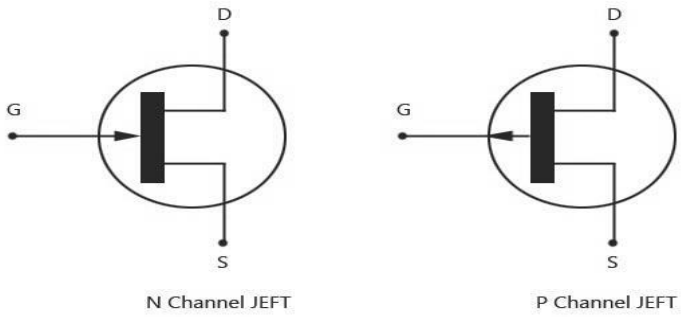
- They cannot be used for high power applications due to lower power dissipation.
- They have lower input impedance.
- They are temperature dependent.
- The manufacturing techniques of the transistors are much complex.



## FIELD EFFECT TRANSISTOR :

### JFET :

JFET is a unipolar-transistor, which acts as a voltage controlled current device and is a device in which current at two electrodes is controlled by the action of an electric field at a p-n junction.
A JFET, or junction field-effect transistor, is a FET in which the gate is created by reverse-biased.

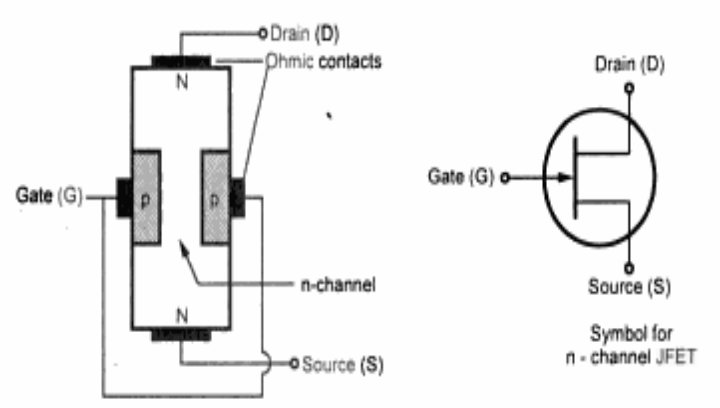



JFET-N-Channel and P-channel Schematic Symbol

Construction :

### n-channel JFET :

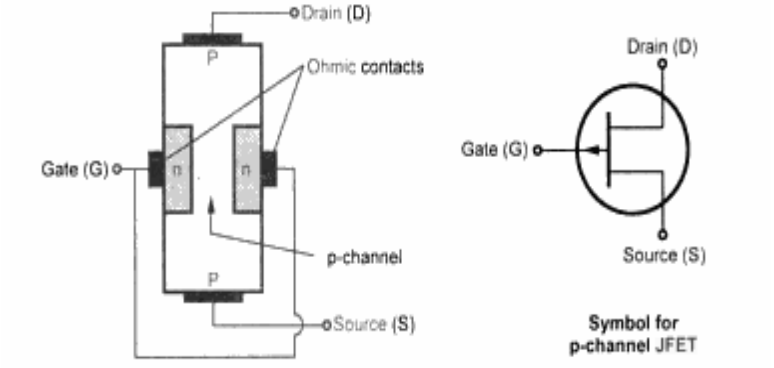
The figure shows construction and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and its two ends, two ohmic contacts are made which is the drain and source terminals of FET. Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the channel. Since this channel is in the n type bar, the FET is known as n-channel JFET.



The electrons enter the channel through the terminal called source and leave through the terminal called drain. The terminals taken out from heavily doped electronics of p type material are called gates. These electrodes are connected together and only one terminal is taken out, which is called gate, as shown in the figure.

**p-channel JFET :**

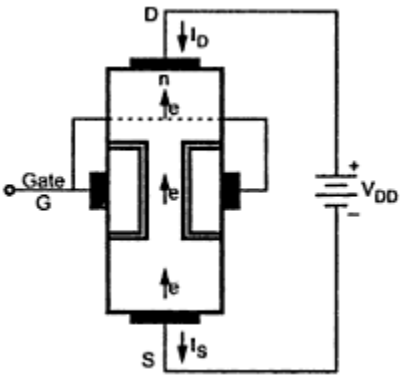
The device could be made of p type bar with two n type gates as shown in the figure. This will be p-channel JFET. The principle of working of n-channel JFET and p-channel JFET are similar. The only difference being that in n-channel JFET the current is carried by electrons while in p-channel JFET, it is carried by holes.



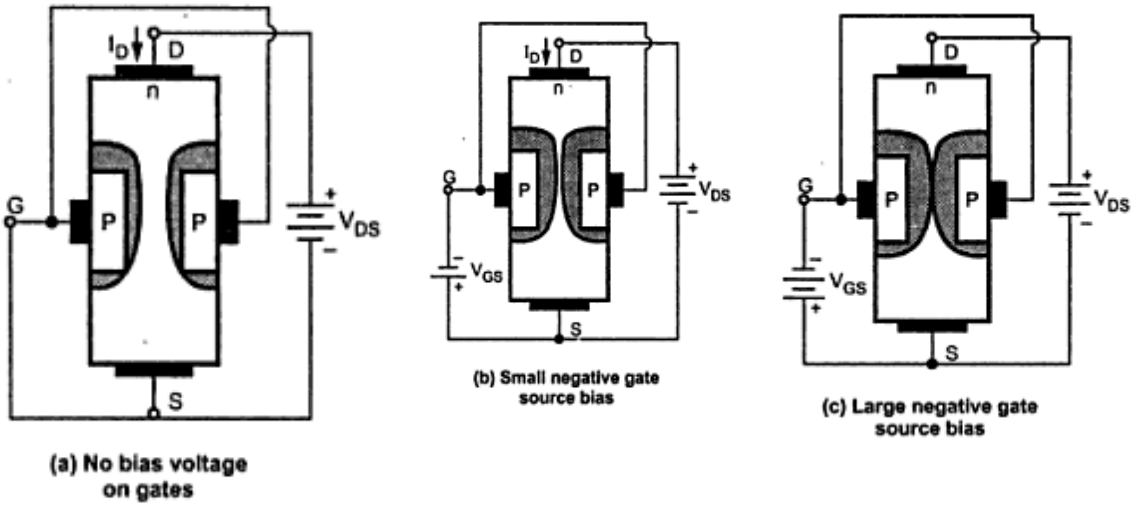

**Operation :**

In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero. The gate current in JFET is often neglected and assumed to be zero.

Let us consider the circuit in the figure, voltage VDD is applied between drain and source. Gate terminal is kept open. The bar is of n-type material. Due to the polarities of applied voltage as shown in the fig, the majority carriers i.e. the electrons start flowing from the source to the drain. The flow of electrons makes the drain current, ID.




The majority carriers move from source to drain through the space between the gate regions. The space is commonly known as **channel.** The width of this channel can be controlled by varying the gate voltage. To see the effect of gate voltage on channel-width and on drain current ID, consider the diagram below.




(a) No bias voltage on gates

(b) Small negative gate source bias

(c) Large negative gate source bias

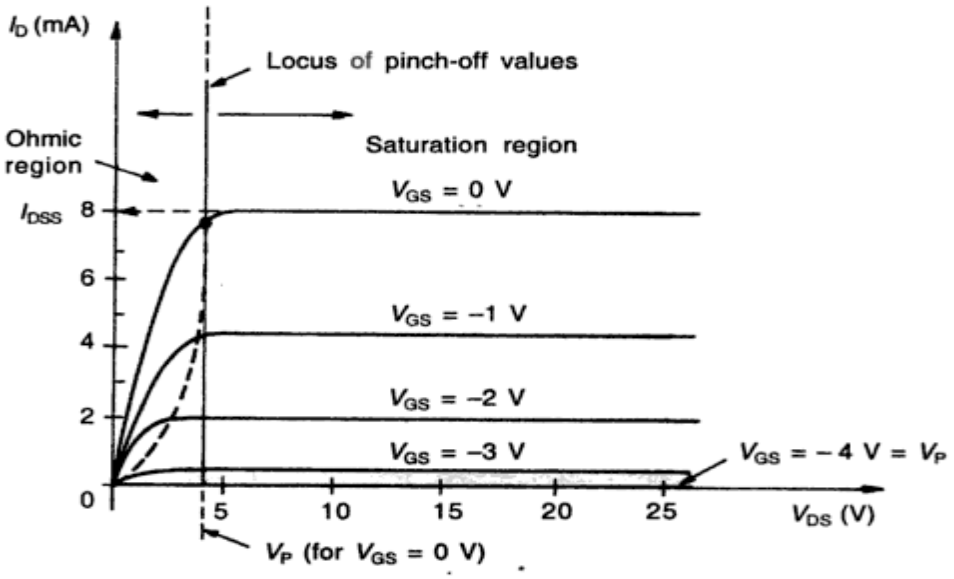
In the fig it can be observed that depletion region width is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that reverse bias is not uniform near the junction as it gradually increases from source side to drain side.
The depletion region does not contain charge carriers. The space between two depletion regions is available for conducting portion of the channel. When reverse bias voltage is applied externally to the gate, the reverse bias will increase and

hence increase the penetration of the depletion region which reduces the width of the conducting portion of the channel. When the width of the conducting portion of the channel reduces, the no. of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces.
When the external reverse bias voltage at the gate is increased as shown in fig (b) & (c) the depletion regions will increase more and at a particular stage the width of the depletion region will be equal to the original width of the depletion regions will increase more and more, and stage will come when the width of the depletion regions will be equal to the original width of the channel, leaving zero width for conducting portion of the channel, as shown in the fig (c). This will prevent any current flow from drain to source and this will cut off the drain current. The gate to source voltage that produces cutoff is known as cutoff voltage (VGS (OFF)).
When the gate is shorted to source, there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by IDSS and this is the possible drain current in JFET. It is clear that the gate to source voltage controls the current flowing through the channel and hence FET is also called **voltage controlled current source.**

**Characteristics :**

**Drain (or) current voltage characteristics of JFET :**
The current voltage characteristics of an n-channel JFET is shown in the figure. The drain current (ID) is plotted with VDS for different values of VGS. This characteristic is also known as drain characteristics of JFET. From the fig, we see that as the voltage increased from 0 to a few volts, the current increases as determined by ohm's law. The straight nature of the curve at low values for VDS reveals that for this region, the resistance is essentially constant for a fixed valued of VGS. But the slope of the ID –VDS curve near the origin is a function of the gate voltage. This region of operation is known as the linear region or ohmic region. As VDS increases and approaches a value VP (referred to as pinch – off voltage ), slope of the curve changes and the channel resistance increases. If VDS increases beyond pinch – off value, characteristics curve becomes more horizontal and ID maintains a saturation level. For VGS = 0v, the saturated value of ID is designated as IDSS, which is the drain – to –source current with source – gate Short circuit. Thus, IDSS is the maximum drain current for a JFET, obtained under the conditions VGS = 0V and VDS > |VP|. |. As the VDS increases beyond VP, the level of ID remains essentially the same and this region of the characteristics is known as saturation region. It may also be noted that once VDS > Vp, the JFET has the characteristics of a current source. Thus the current – voltage

characteristics displayed in fig can be divided into ohmic (linear) and saturation regions with the pinch-off conditions as the boundary.




As the negative bias of VGS increases, depletion region forms similar to those with VGS = 0 V but at a lower level of VDS. Thus, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of VDS, as shown in the fig it is seen that VGS = -VP, the saturation level of ID is essentially 0mA and the devices have been turned off.

The region of the right of the pinch-off locus in figure is normally employed in linear amplifiers. The region to the left of the pinch-off locus is referred to as *voltage controlled resistance region*, where the JFET can be used as voltage-controlled resistor. The channel resistance (RD) increases with increase of VGS values and empirical relation between the two is given by

$$R_D = \frac{R_0}{[1 - (V_{GS}/V_P)]^2}$$

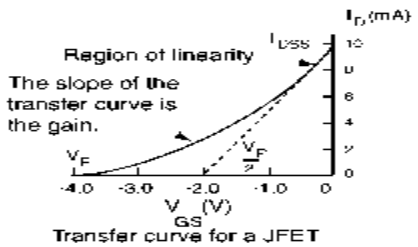
Where R0 is the resistance with VGS = 0. For an n-channel JFET with R0 = 10kΩ at VGS = -2V.
The drain currents suddenly rise in an unbounded manner at very high levels of VDS. The vertical rise in current is an indication that breakdown has occurred and the current through the channel is now limited solely by external circuit. In practical applications, the level of VDS is kept less than the breakdown voltages (VDSmax) that are mentioned in specification sheets of JFET.

Transfer characteristics :

The transfer characteristics of JFET is a plot of output (drain) current versus input controlling quantity (gate-source voltage) and is used extensively in JFET amplifiers. In contrast to linear input-output relationship of BJT, the input-output relationship of JFET is not linear. The relationship between ID and VGS is defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term on the right-hand side of the equation suggests that the relationship of $I_{DSS}$ $V_{GS}$ is nonlinear and exponential in nature. The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed. The transfer curve can be obtained using Shockley's equation or from the o/p characteristics.



Transfer curve for a JFET

**Expression for pinch off voltage and Drain Current:**

For the transfer characteristics,VDS is maintained constant at a suitable value greater than the pinch off voltage Vp.The gate voltage VGS is decreased from zero till ID is reduced to zero. The transfer characteristics ID versus VGS are shown in figure.

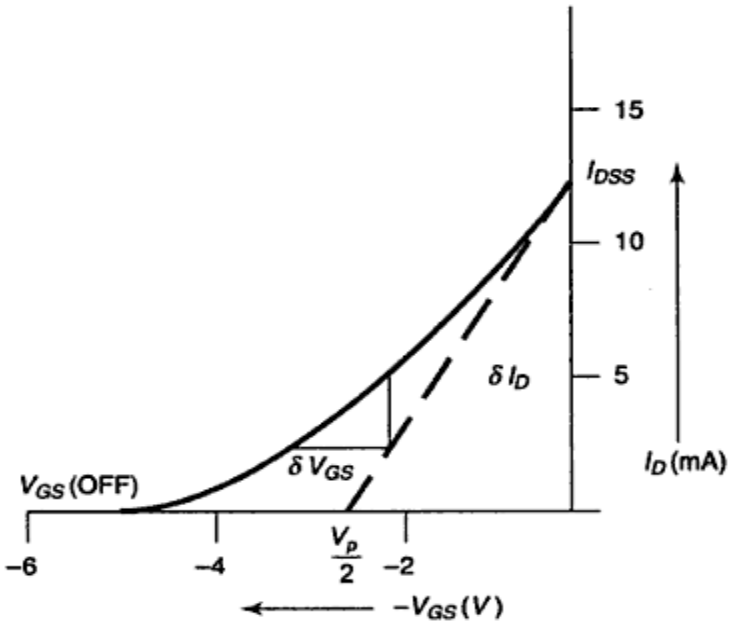



**Fig. 7.5** Transfer characteristics of JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where IDS is the saturation drain current, IDSS is the value of IDS when VGS=0 and VP is the pinch off voltage

Differentiating eqn (1) with respect to VGS we obtain the expression of gm

$$g_m = -2I_{DSS}/Vp(1-V_{Gs}/Vp) \quad (2)$$

From eqn (1)

$$(1-V_{GS}/Vp) = (I_{DS}/I_{DSS})_{1/2} \quad (3)$$

Suppose $g_m = g_{m0}$ when $V_{GS} = 0$

$$g_{m0} = -2I_{DSS}/Vp \quad (4)$$

Therefore from eqn (2) and (4)

$$\mathbf{g_m = g_{m0}(1-V_{GS}/Vp)}$$

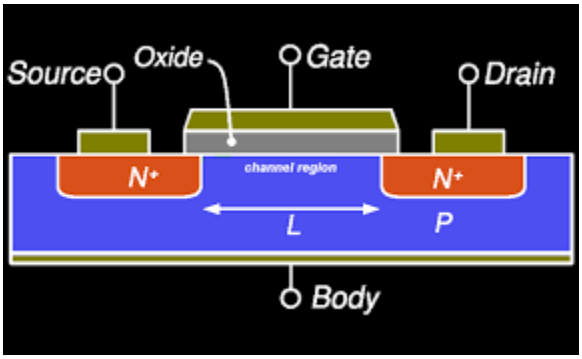
**MOSFET :**

MOSFET stands for metal oxide semiconductor field effect transistor. It is capable of voltage gain and signal power gain. The MOSFET is the core of integrated circuit designed as thousands of these can be fabricated in a single chip because of its very small size. Every modern electronic system consists of VLSI technology and without MOSFET, large scale integration is impossible.

It is a four terminals device. The drain and source terminals are connected to the heavily doped regions. The gate terminal is connected top on the oxide layer and the substrate or body terminal is connected to the intrinsic semiconductor.

MOSFET has four terminals, they are gate, source drain and substrate or body. MOS capacity present in the device is the main part. The conduction and valance bands are position relative to the Fermi level at the surface is a function of MOS capacitor voltage. The metal of the gate terminal and the source acts as the parallel and the oxide layer acts as insulator of the state MOS capacitor. Between the drain and source terminal inversion layer is formed and due to the flow of carriers in it, the current flows in MOSFET the inversion layer properties are controlled by gate voltage. Thus it is a voltage controlled device.

Two basic types of MOSFET are n channel and p channel MOSFETs. In n channel MOSFET, the current is due to the flow of electrons in inversion layer and in p channel current is due to the flow of holes




**Working Principle of MOSFET :**

The working principle of MOSFET depends up on the MOS capacitor. The MOS capacitor is the main part. The semiconductor surface at below the oxide layer and between the drain and source terminal can be inverted from p-type to n-type by applying a positive or negative gate voltages respectively. When we apply positive gate voltage the holes present beneath the oxide layer experience repulsive force and the holes are pushed downward with the substrate. The depletion region is populated by the bound negative charges, which are associated with the acceptor atoms. The positive voltage also attracts electrons from the n+ source and drain regions in to the channel. The electron reach channel is formed. Now, if a voltage

is applied between the source and the drain, current flows freely between the source and drain gate voltage controls the electrons concentration the channel. Instead of positive if apply negative voltage a hole channel will be formed beneath the oxide layer.

Now, the controlling of source to gate voltage is responsible for the conduction of current between source and the drain. If the gate voltage exceeds a given value, called the three voltage only then the conduction begins.

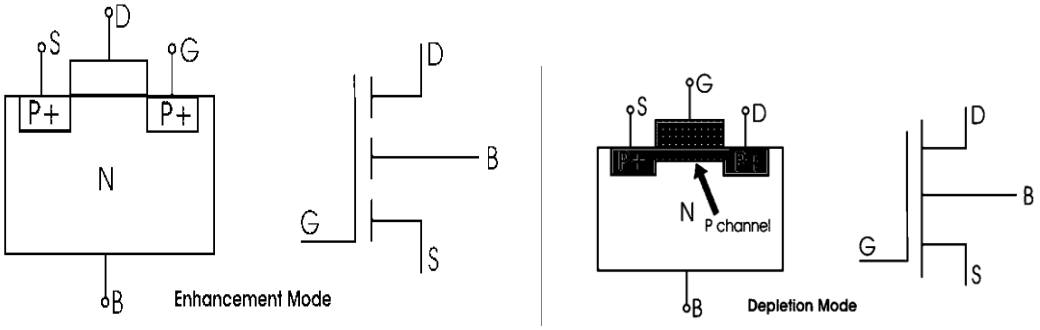
The current equation of MOSFET in triode region is –

$$I_D = u_n C_{ox} \frac{W}{2}[ (V_{GS} - V_{TH} )V_{DS} - \frac{1}{2}V^2_{DS}]$$

Where, $u_n$ = Mobility of the electrons $C_{ox}$ = Capacitance of the oxide layer W = Width of the gate area L = Length of the channel $V_{GS}$ = Gate to Source voltage $V_{TH}$ = Threshold voltage $V_{DS}$ = Drain to Source voltage.

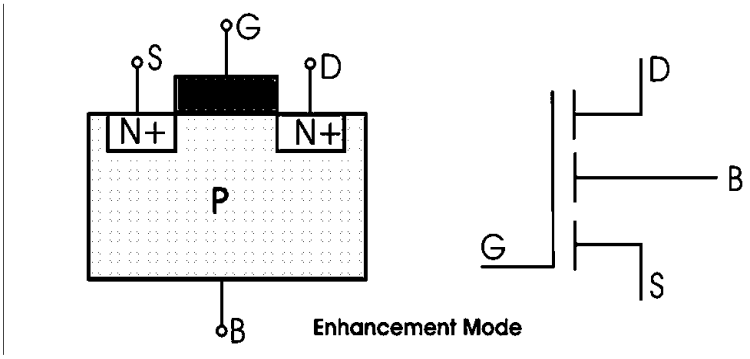
## P-Channel MOSFET :

MOSFET which has p - channel region between source and gate is known as **p - channel MOSFET**. It is a four terminals device, the terminals are gate, drain, source and substrate or body. The drain and source are heavily doped p+ region and the substrate is in n-type. The current flows due to the flow of positively charged holes that's why it is known as p-channel MOSFET. When we apply negative gate voltage, the electrons present beneath the oxide layer, experiences repulsive force and they are pushed downward in to the substrate, the depletion region is populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage also attracts holes from p+ source and drain region in to the channel region. Thus hole in which channel is formed, now if a voltage between the source and the drain is applied current flows. The gate voltage controls the hole concentration of the channel. The diagram of p- channel enhancement and depletion MOSFET are given below -

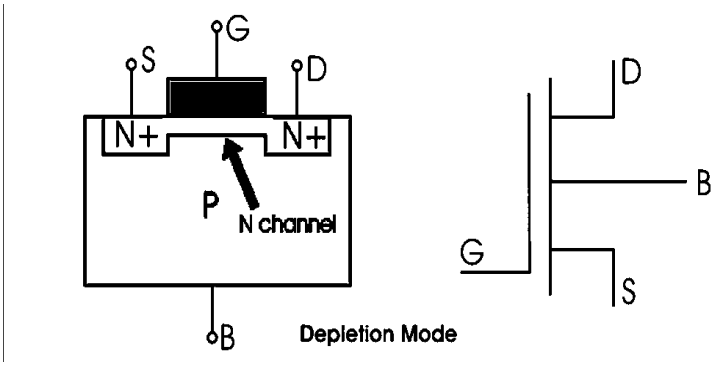


**N-Channel MOSFET :**

MOSFET having n-channel region between source and drain is known as **n-channel MOSFET** . It is a four terminal device, the terminals are gate, drain and source and substrate or body. The drain and source are heavily doped n+ region and the substrate is p-type. The current flows due to flow of the negatively charged electrons, that's why it is known as n- channel MOSFET. When we apply the positive gate voltage the holes present beneath the oxide layer experiences repulsive force and the holes are pushed downwards in to the bound negative charges which are associated with the acceptor atoms. The positive gate voltage also attracts electrons from n+ source and drain region in to the channel thus an electron reach channel is formed if a voltage is applied between the source and drain. The gate voltage controls the electron concentration in the n-channel MOSFET over p-channel MOSFET as the mobility of electrons are higher than holes. The diagrams of enhancements mode and depletion mode are given



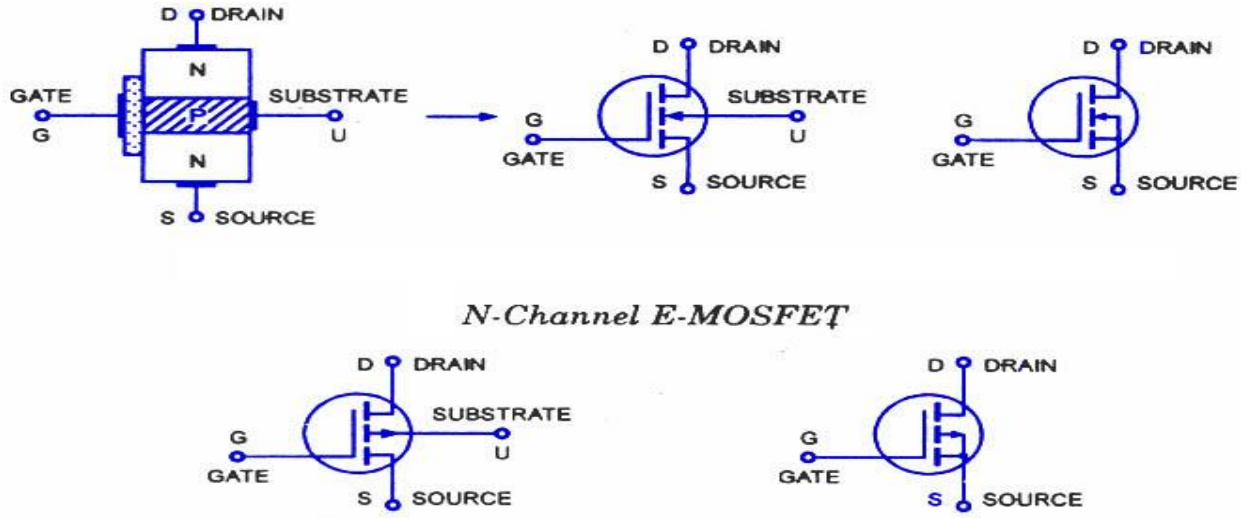
Enhancement Mode



Depletion Mode

**Enhancement and Depletion Mode MOSFET :**

**EMOSFET :**

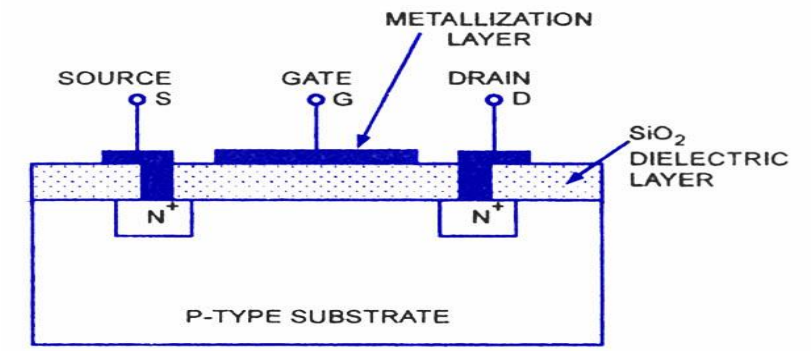



*N-Channel E-MOSFET*




*P-Channel E-MOSFET*
*Schematic Symbols For E-MOSFETs*

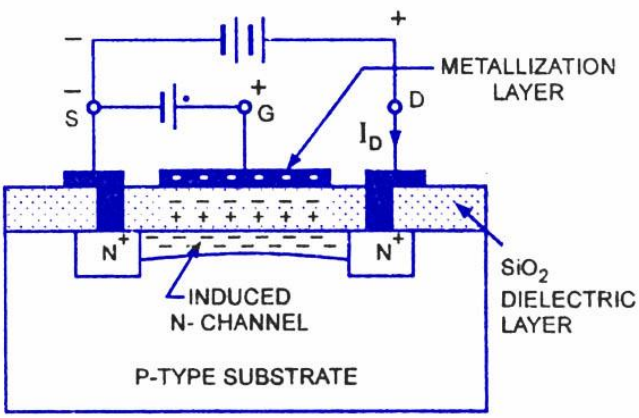
**Construction:**




*N-Channel E-MOSFET Structure*

Figure shows the construction of an N-channel E-MOSFET. The main difference between the construction of D-MOSFET and that of E-MOSFET, as we see from the figures given below the E-MOSFET substrate extends all the way to the silicon dioxide (SiO2) and no channels are doped between the source and the drain. Channels are electrically induced in these MOSFETs, when a positive gate-source voltage VGS is applied to it.

**Operation:**




*Operation of N-Channel E-MOSFET*

As its name indicates, this MOSFET operates only in the enhancement mode and has no depletion mode. It operates with large positive gate voltage only. It does not conduct when the gate-source voltage VGS = 0. This is the reason that it is called normally-off MOSFET. In these MOSFET's drain current ID flows only when VGS exceeds VGST [gate-to-source threshold voltage].

When drain is applied with positive voltage with respect to source and no potential is applied to the gate two N-regions and one P-substrate from two P-N junctions connected back to back with a resistance of the P-substrate. So a very small drain current that is, reverses leakage current flows. If the P-type substrate is now connected to the source terminal, there is zero voltage across the source substrate junction, and the–drain-substrate junction remains reverse biased.

When the gate is made positive with respect to the source and the substrate, negative (i.e. minority) charge carriers within the substrate are attracted to the positive gate and accumulate close to the-surface of the substrate. As the gate voltage is increased, more and more electrons accumulate under the gate. Since these electrons cannot flow across the insulated layer of silicon dioxide to the gate, they accumulate at the surface of the substrate just below the gate. These accumulated minority charge carriers N -type channel stretching from drain to source. When this occurs, a channel is induced by forming what is termed an inversion layer (N-type). Now a drain current starts flowing. The strength of the drain current depends upon the channel resistance which, in turn, depends upon the number of charge carriers attracted to the positive gate. Thus drain current is controlled by the gate potential.

Since the conductivity of the channel is enhanced by the positive bias on the gate so this device is also called the enhancement MOSFET or E- MOSFET.

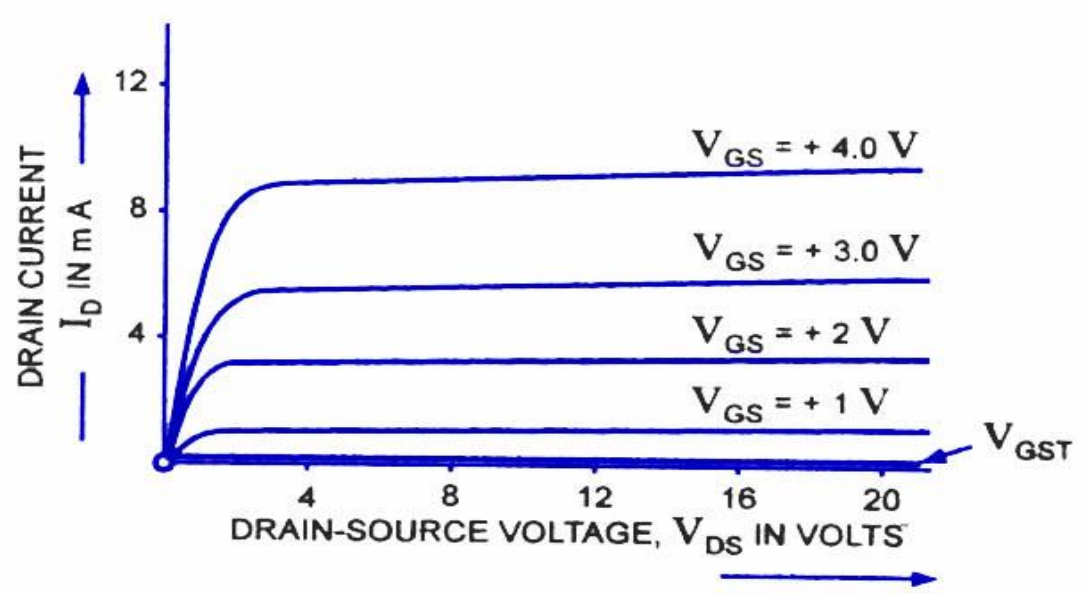
The minimum value of gate-to-source voltage VGS that is required to form the inversion layer (N-type) is termed the gate-to-source threshold voltage VGST. For VGS below VGST, the drain current ID = 0. But for VGS exceeding VGST an N-type inversion layer connects the source to drain and the drain current ID is large. Depending upon the device being used, VGST may vary from less than 1 V to more than 5 V.

JFETs and D-MOSFETs are classified as the depletion-mode devices because their conductivity depends on the action of depletion layers. E-MOSFET is classified as an enhancement-mode device because its conductivity depends on the action of the inversion layer. Depletion-mode devices are normally ON when the gate-source voltage VGS = 0, whereas the enhancement-mode devices are normally OFF when VGS = 0.

**Characteristics :**

**Drain Characteristics :**

Drain characteristics of an N-channel E-MOSFET are shown in figure. The lowest curve is the VGST curve. When VGS is lesser than VGST, ID is approximately zero. When VGS is greater than VGST, the device turns- on and the drain current ID is controlled by the gate voltage. The characteristic curves have almost vertical and horizontal parts.




*Drain Characteristics*

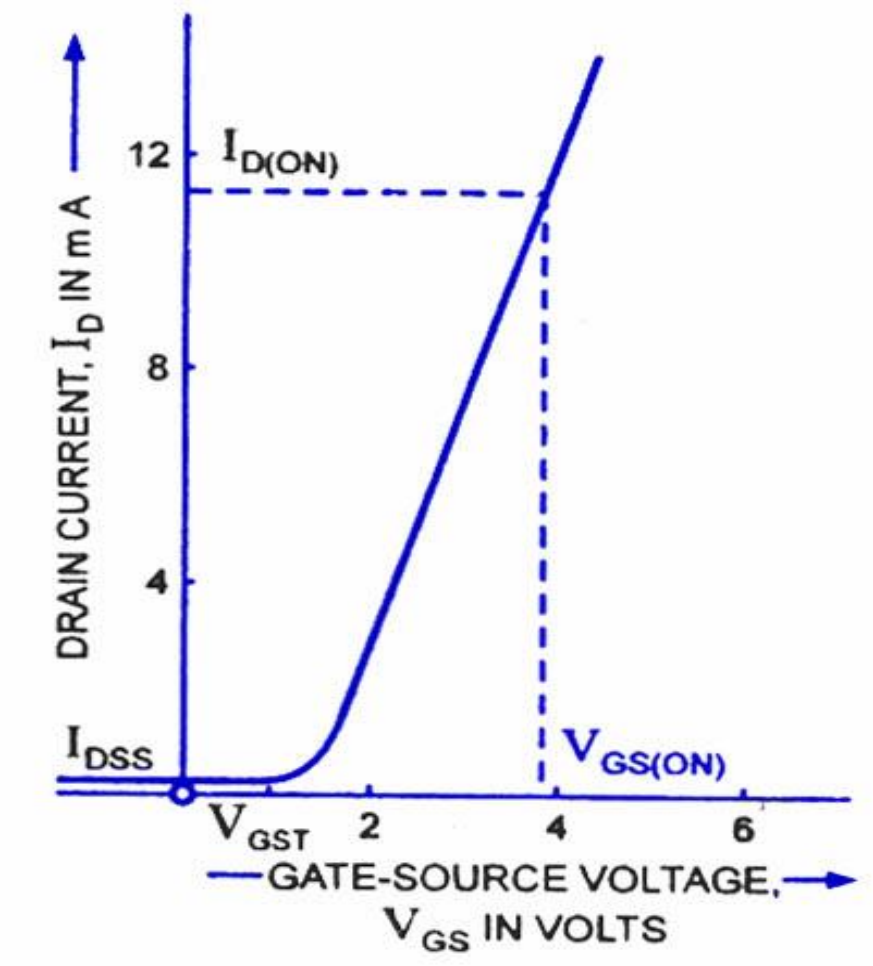
The almost vertical components of the curves correspond to the ohmic region, and the horizontal components correspond to the constant current region. Thus E-MOSFET can be operated in either of these regions *i.e.* it can be used as a variable-voltage resistor (WR) or as a constant current source.

**Transfer Characteristics :**

Figure shows a typical transconductance curve. The current IDSS at VGS <=0 is very small, being of the order of a few nano-amperes. When the VGS is made positive, the drain current ID increases slowly at first, and then much more rapidly with an increase in VGS. The manufacturer sometimes indicates the *gate-source threshold voltage* VGST at which the drain current ID attains some defined small value, say 10 A.

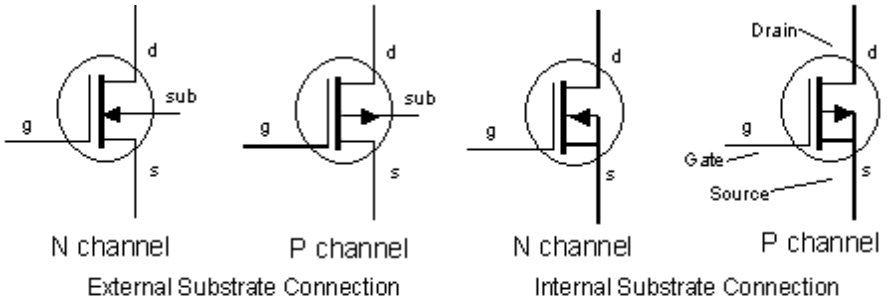
The equation for the transfer characteristic does not obey equation. However it does follow a similar "square law type" of relationship. The equation for the transfer characteristic of E-MOSFETs is given as:

$$\mathbf{I_D=K(VGS-VGST)^2}$$

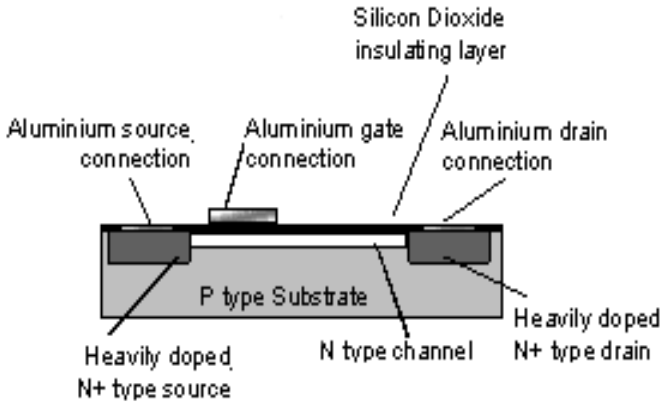



*Transfer Characteristic*

**Depletion Mode MOSFET :**
**Symbol :**




**Construction :**




**Depletion Mode N Channel MOSFET**

The depletion mode MOSFET shown as a N channel device (P channel is also available) in Fig, is more usually made as a discrete component, i.e. a single transistor rather than IC form. In this device a thin layer of N type silicon is deposited just below the gate−insulating layer, and forms a conducting channel between source and drain.

Therefore when the gate source voltage VGS is zero, current (in the form of free electrons) can flow between source and drain. Note that the gate is totally insulated from the channel by the layer of silicon dioxide. Now that a conducting channel is present the gate does not need to cover the full width between source and drain. Because the gate is totally insulated from the rest of the transistor this device, like other IGFETs, has a very high input resistance.

**Operation :**

In the N channel device, shown in Fig, the gate is made negative with respect to the source, which has the effect of creating a depletion area, free from charge carriers, beneath the gate. This restricts the depth of the conducting channel, so

increasing channel resistance and reducing current flow through the device. Depletion mode MOSFETS are also available in which the gate extends the full width of the channel(from source to drain). In this case it is also possible to operate the transistor in enhancement mode. This is done by making the gate positive instead of negative.

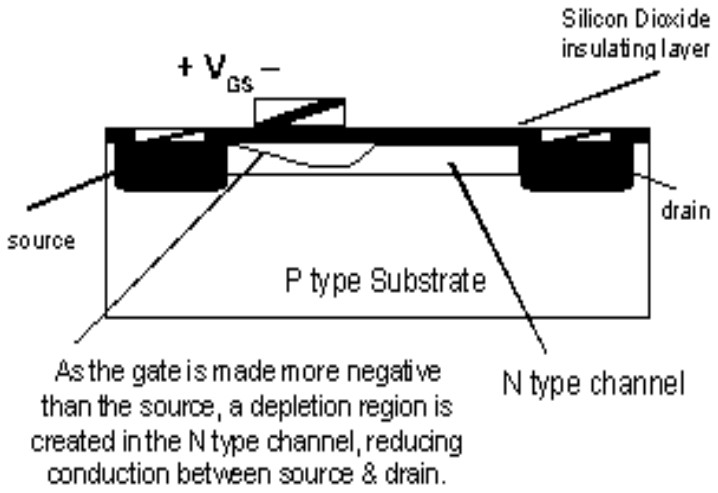



**Fig : Operation of a Depletion Mode MOSFET**

The positive voltage on the gate attracts more free electrons into the conducing channel, while at the same time repelling holes down into the P type substrate. The more positive the gate potential, the deeper, and lower resistance is the channel. Increasing positive bias therefore increases current flow. This useful depletion/enhancement version has the disadvantage that, as the gate area is increased, the gate capacitance is also larger than true depletion types. This can present difficulties at higher frequencies.

## Comparison of MOSFET and JFET :

1. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.
2. The gate leakage current in a MOSFET is of the order of 10-12A.Hence the input resistance of a MOSFET is very high in the order of 1010 to 1015 ohm. The gate leakage current of a JFET is of the order of 10-9A and its input resistance is of the order of 108 ohm.

3. The output characteristics of the JFET are flatter than those of the MOSFET and hence, the drain resistance of a JFET(0.1 to 1Mohm) is much higher than that of a MOSFET(1 to 50 K ohm)

4. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.

5. Comparing to JFET, MOSFETs are easier to fabricate.

6. MOSFET is very susceptible to overload voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.

7. MOSFET has zero offset voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.

8. Special digital CMOS circuits are available which involves near –zero power dissipation and very low voltage and current requirements. This makes them most suitable for portable systems.