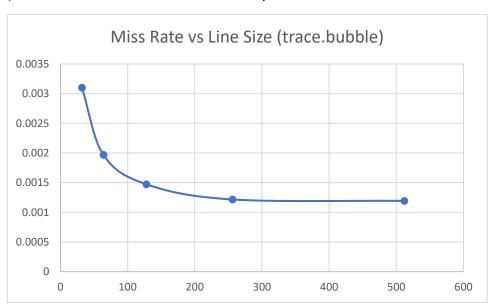
Cache Simulator Summary Report

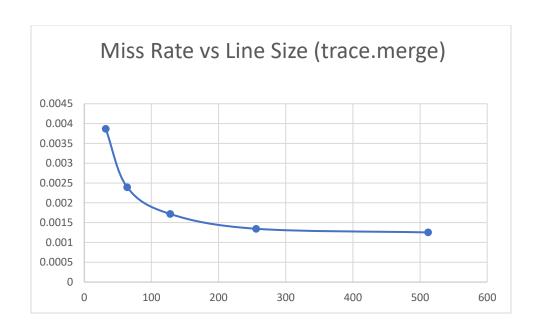
Praneeth Eddu

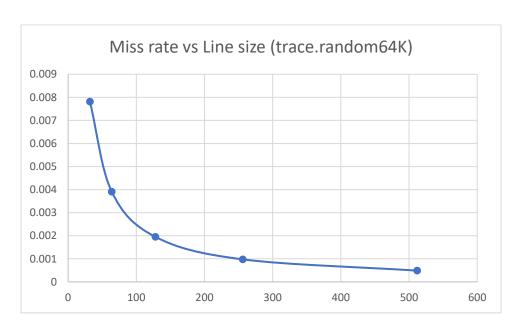
a. For the cache itself, I created an array of structs that are memory allocated by the number of sets (2^k) and that array consists of cache characteristics such as valid bit, dirty bit, LRU counter, and tag. Each cache characteristics array is memory allocated by the number of associations present. The number of bits for tag, index, and offset are calculated in the initializer function and are used to Cache characteristics array keeps track of whether the bit is valid, dirty, and keeps track of tag and manages the LRU when needed. LRU is incremented every time the cachesim_access() is called. The LRU is set to 0 when the cache line is brought into an invalid set or when the cache is full, and a new line needs to be replaced.

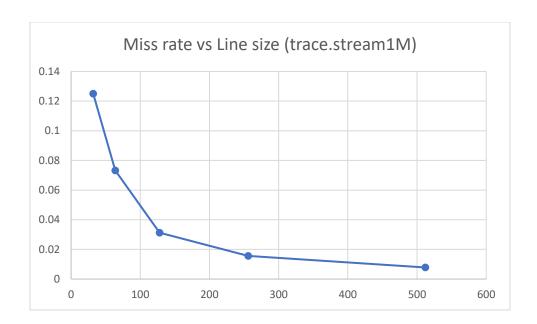
b.

1) Plots for miss rate vs line size for every trace:









2) Comparing from the plots, the best configuration to achieve a lower miss rate seems to be the cache with 512 block sizes, 64K cache size, 8 associativity.

Trace name	Overall miss rate	Read miss rate	Write miss rate
Trace.bubble	0.001048	0.9067	0.0933
Trace.merge	0.0011346	0.8822	0.1177
Trace.random64k	0.0004883	1	0
Trace.stream1M	0.00781	1	0

3) Write back traffic also seems to work the best when the cache has the highest configurations which 512 block size, 64K cache size, 8 associativity.

Trace name	Writeback value	Writeback traffic
Trace.bubble	5272	2699264
Trace.merge	7387	3782144
Trace.random64K	0	0
Trace.stream1M	0	0

4) The same trends follow for choosing the cache configurations (blocksize = 512, associativity = 8, cache size = 64K) for computing total memory access volume.

Trace name	Total memory	Total bytes	Memory access
	access volume	fetched (bytes)	volume saved
	(bytes)		(bytes)
Trace.bubble	3392512	3237039616	3233647104
Trace.merge	4460544	3931356160	3926895616
Trace.random64K	65536	134217728	134152192
Trace.stream1M	1048676	134217728	133169152