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ECE 3056

12/3/18

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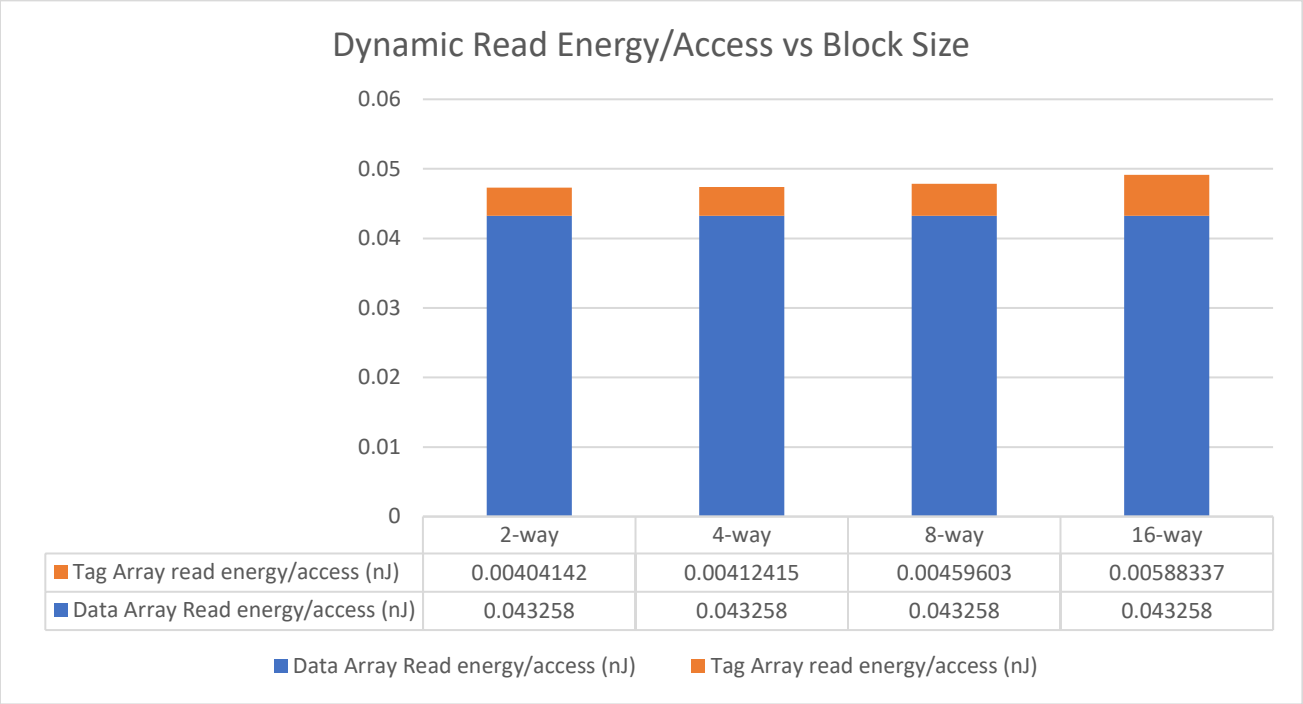
Assignment 5 – Energy

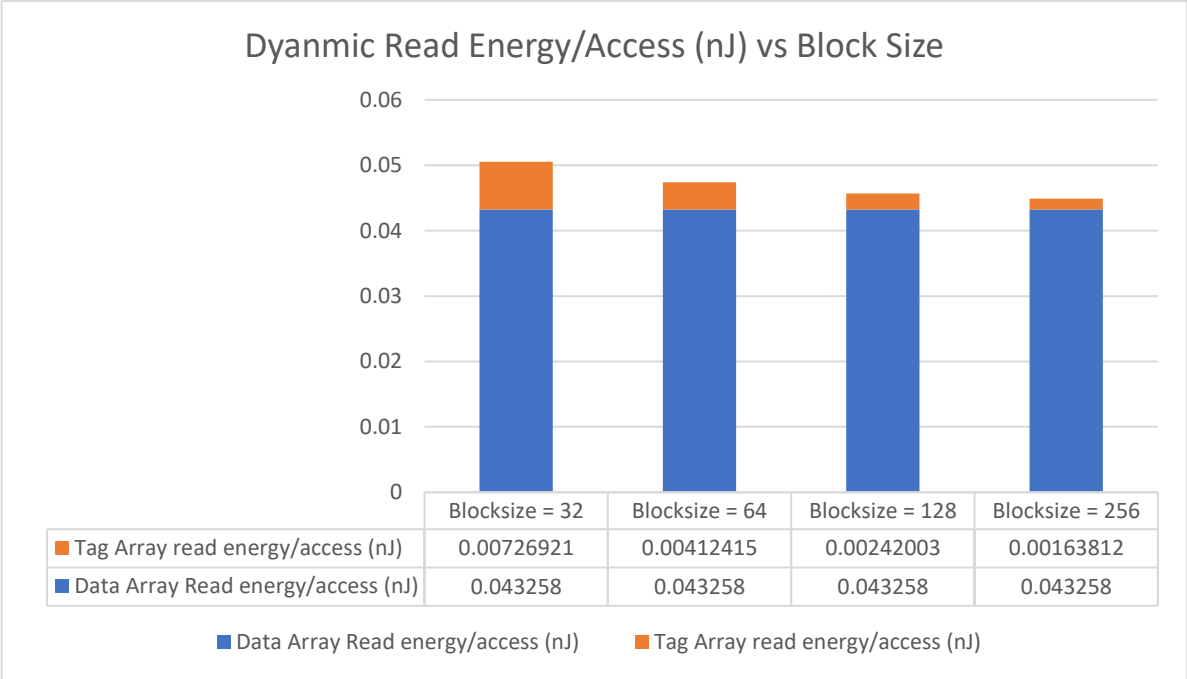
1a.



Analysis:

The dynamic read access time for data array remains the same for all the associativity cases since the cache only retrieves from the data from the data array. However, the set associativity breaks up the tag array into n data paths which in turn increases the number of gates introduced in the architecture. This causes an increase in the transistor switching which leads to an increased the dynamic energy. Hence, the dynamic read energy/access increases as the associativity increases.

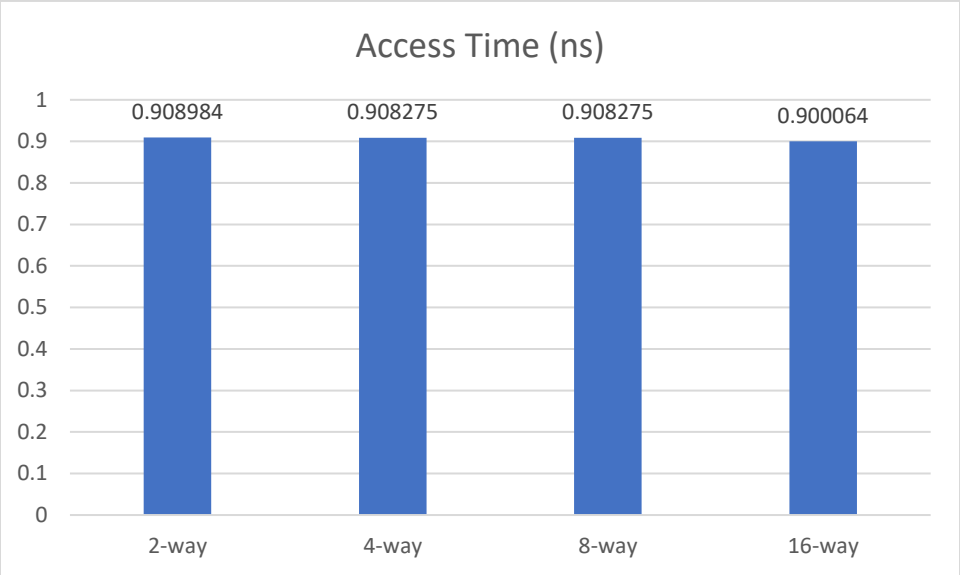
1c.



Analysis:

Increase in block size decreases the tag bits that are needed to be compared for hits/misses. Hence, this decreases the transistor switching and decreases the dynamic energy. Hence the Dynamic Read energy/access decreases as the block size increases.

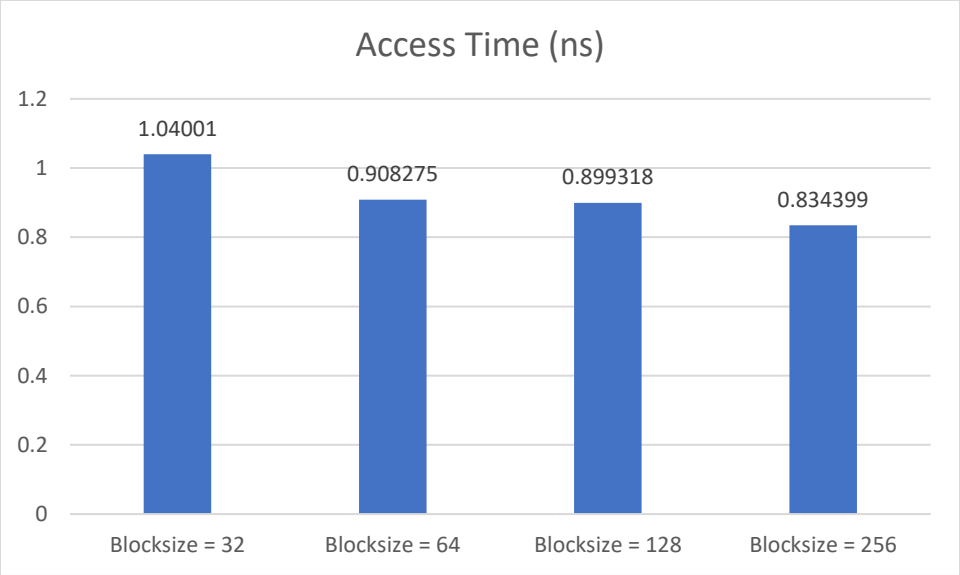
2a.



Analysis:

As mentioned in part 1a. the dynamic power increases as the associativity increases due to higher transistor switching. Theoretically, lower delays are caused by dynamic higher energy. Hence, the access time decreases as the associativity increases. Also, the number of tags bits needed to be compared are reduced with higher associativity which can also cause the reduction in access time.

2b.



Analysis:

As mentioned in part 1c. the increase in block size reduces the tag bits required to be compared which leads to reduced amounts of transistor switching. The lower the transistor switching, the lower the delay. Hence, the access time decreases as the block size increases.

3. The best cache configuration for 256 KB cache that fits closely within 1 mm^2 area and has the minimum energy-delay product is:

Block Size = 256 Bytes, Associativity = 2 (chosen from the scope of the above problems).

Block Size = 8192 Bytes, Associativity = 2 (chosen from all configurations possible)

From the above problems, the lower the associativity, the lower combined dynamic read access energy has been dispersed. Consecutively, higher the Block Size means lower access time. Hence, the parameters for the minimum energy-delay product have been chosen by picking lowest possible associativity (n = 2) and highest possible block size (256 Bytes or 8192 bytes) which meets the area requirements.