Research Article

Efficient circuit design for content-addressable memory in quantum-dot cellular automata technology

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Abstract

Quantum-dot cellular automata (QCA) technology is a kind of nanotechnology utilized for building computational circuits. It can be a good technology for overcome CMOS drawbacks at nano-scale due to its low delay and area. The Content-Addressable Memory (CAM) is a very fast memory that can perform search operations in a very short time. This feature makes the relative popularity of these memories and many applications for them, especially in network routing and processors. In this study, a novel loop-based circuit is designed for the QCA memory unit, which reduces area, cell count, latency, and cost. The obtained results using QCADesigner tool version 2.0.3 demonstrate that the designed QCA memory unit utilizes 16 cells, 0.01 μm^2 area, and 0.25 clock cycles and has a reduction of 33% in the number of cells, 50% in area, 50% in latency, and 75% in cost compared to existing works. Then, this memory unit is utilized to design an efficient structure for CAM circuit. The results show that the developed structure for CAM circuit has 0.75 clock cycles, 32 cells, and 0.03 μm^2 area, and it has a reduction of 20% in the number of cells, 25% in area, 40% in latency, and 75% in cost compared to existing works.

Article Highlights

- An efficient Content-Addressable Memory (CAM) circuit is designed using a novel QCA memory unit.
- The proposed QCA memory unit and CAM circuit have reduced cell count, area, latency, and cost.
- The QCADesigner tool version 2.0.3 is utilized to evaluate the developed circuits.

1 Introduction

The CMOS technology is a dominate technology for digital circuits design, but this technology has several concerns at nano-scale including short channel effects. The Quantum-dot Cellular Automata (QCA) technology is a significant kind of nanotechnology for the implementation of digital circuits such as full adder, comparator, shift register, counter, multiplier, and memory [1–8]. This kind of nanotechnology has significantly low delay and area compared to CMOS technology [3, 9]. So, it can significantly improve the design performance of logical circuits. The fundamental element in the QCA technology is named cell that is composed of two electrons and four dots. The electrons

of each cell can move across the dots. Thus, there are two stable states in each cell based on coulombic repulsion. These stable states are equal to logics "0" and "1" in digital circuits [1, 10, 11].

One of the most important elements in digital circuits design is memory [12]. There are two well-known kinds of memory, Content-Addressable Memory (CAM) and Random Access Memory (RAM). The CAM is a very fast memory that can perform search operations in a very short time [13–18]. The CAM circuit is accessed in parallel and simultaneously based on the content of the data rather than the specific location or address. The CAM circuit is especially suitable for parallel searches based on data due to its internal organization. This type of memory can be used in the Central Processing Unit (CPU) of computers. Therefore, many researchers [5–7, 12, 15, 17, 19–21] tried to improve the performance of memory circuits, especially CAM circuit.

In this study, a new structure is designed for 1-bit CAM circuit. Since the CAM circuit is composed of two main components: (a) memory unit and (b) identity gate; developing efficient circuits for these components can lead to increase the performance of the CAM circuit. For this purpose, an efficient 1-bit loop-based memory unit is developed as building block in this paper. This building block is composed of a MUX gate, which is constructed based on Majority Gates (MGs) and a feedback. In addition, we propose a new CAM circuit using this memory unit. The QCADesigner tool version 2.0.3 is employed for functionality verification of the developed circuits. The obtained results indicate that this new circuit for the memory unit has 0.01 µm^2, 16 cells, and 0.25 clock cycles. The developed CAM circuit has 0.03 µm^2, 32 cells, and 0.75 clock cycles. The designed circuits have many advantages with regard to area, cell count, latency, and cost.

The rest of this study is organized as follows: An overview of QCA concepts and structures is presented in Sect. 2. The developed circuits are presented in Sect. 3. The results and their comparison will be introduced in Sect. 4. Finally, we will conclude this study in Sect. 5.

2 Background

This section introduces the basic elements of the QCA technology.

2.1 QCA cell

The fundamental element in the QCA technology is a square cell that has two electrons in four dots. These electrons can freely tunnel between dots, but they cannot tunnel out of the cell [11]. So, there are two stable states
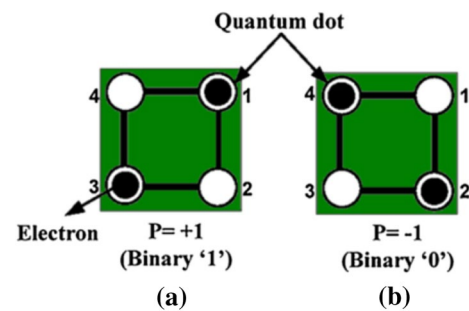

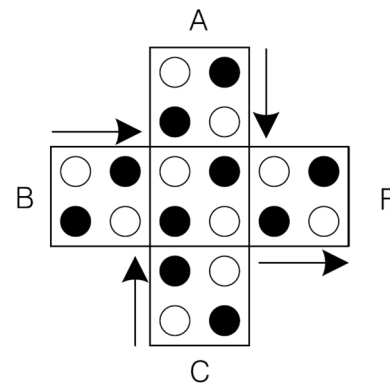**Fig. 1** The polarization of the QCA cell **a** $P = +1$ and **b** $P = -1$ [25]

Fig. 2 The QCA implementation of three-input majority gate [8]

that creates two polarizations, $P = -1$ and $P = +1$. These two polarizations are related to digital values "0" and "1" [22–24]. The QCA cell polarization is displayed in Fig. 1 [25].

2.2 QCA gates

There are two important QCA gates, (a) the majority gate and (b) inverter gate.

The majority gate with 3 inputs plays a vital role in digital circuits design in the QCA technology. Figure 2 displays this gate. If the majority gate inputs are shown by A, B, and C, the output of this gate is denoted as follows [2, 8]:

$$F = MG(A, B, C) = CB + CA + BA \qquad (1)$$

Additionally, if the constant values "1" and "0" are assigned to the input C, the MG will function as AND gate and OR gate, respectively [2, 8].

The inverter output will be the inverse of its input. Figure 3 displays the inverter gate [8]. Figure 3a displays the complex inverter gate in which the output has no noise. Figure 3b displays the simple inverter gate that can be designed using two QCA cells [8].

Fig. 3 The QCA inverter gate; **a** complex gate and **b** simple gate [8]

(a)   (b)
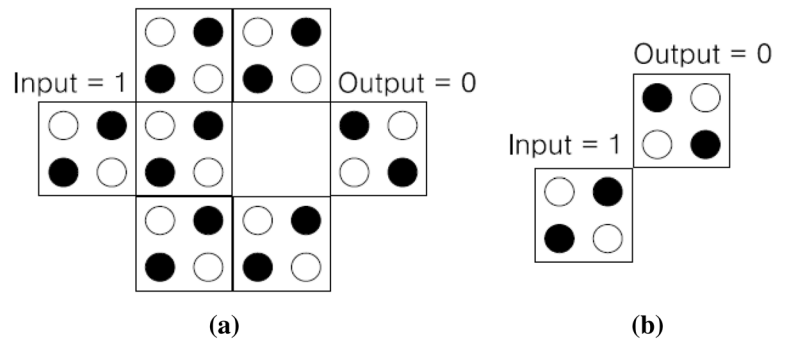
Fig. 4 The developed 1-bit QCA RAM circuit in [15]
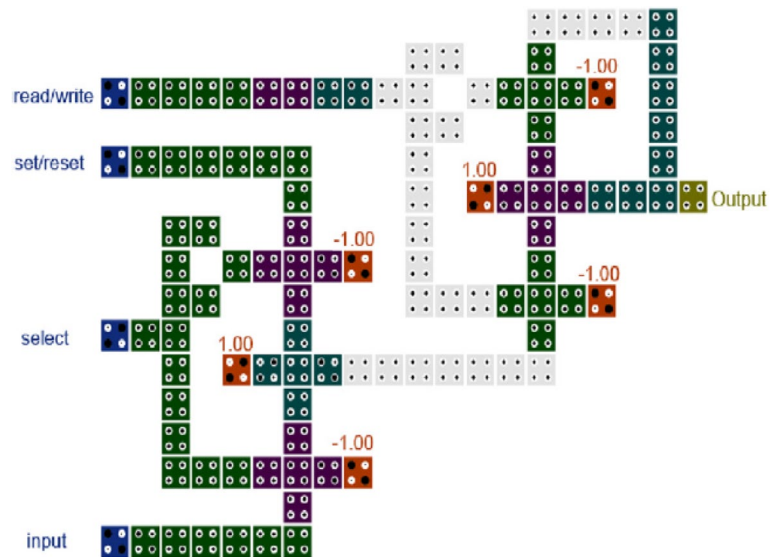
These two basic gates are utilized to implement QCA digital circuits such as memory.

2.3 The CAM circuit

The CAM circuit is a very fast memory that can perform search operations in a very short time [13–18]. So, many researches have been done to increase the performance of the memory circuits, especially CAM circuit in recent years.

Hashemi and Navi [15] have offered a 1-bit RAM circuit using a robust MUX gate that has set and reset ability. In this circuit, an extra clocking zone is added to read/write signal to synchronize the input signals. This structure is displayed in Fig. 4.

This RAM circuit has 109 cells, 1.75 clock cycles, and 0.13 μm^2 area.

Angizi et al. [19] have offered a 5-input majority gate. Then, they have offered a 1-bit RAM circuit using this 5-input MG and 3-input MG that is shown in Fig. 5. This memory circuit has set and reset ability, which are used to control the output.
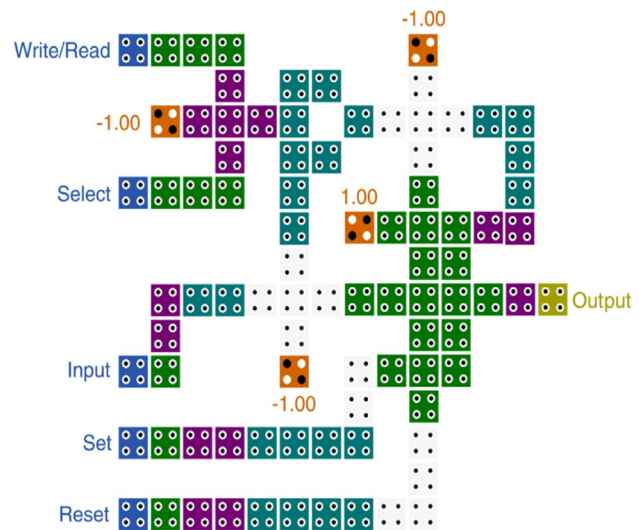
Fig. 5 The developed 1-bit RAM circuit in [19]

This RAM circuit requires 88 cells, 1.5 clock cycles, and 0.08 µm² area.

Mubarakali et al. [12] have offered a 1-bit RAM circuit, which has select ability. The designed memory circuit is constructed of a MUX gate, an inverter gate, and five 3-input MG. Figure 6 displays the designed RAM in [12].

This RAM circuit requires 87 cells, 1.5 clock cycles, and 0.13 µm² area.

Song et al. [7] have designed a novel loop-based RAM circuit using the developed 2–1 multiplexer and D-latch circuits. The half-cell misplacement method is utilized for the implementation of inverse operation in the developed multiplexer circuit. The developed 1-bit RAM circuit has synchronous set and reset, which has the 3-input MG advantages. Figure 7 displays the designed 1-bit RAM circuit in [7].

This RAM circuit has 26 cells, 1 clock cycles, and 0.026 µm² area.

Rasouli Heikalabad et al. [20] have offered a 5-input MG. Then, they have designed a 1-bit CAM circuit based on this offered 5-input MG. Figure 8 displays the designed CAM circuit in [20].

This CAM circuit requires 100 cells, 0.14 µm² area, and 2 clock cycles.

Park et al. [6] have offered a 1-bit CAM circuit in three-layer. The developed CAM circuit is illustrated in Fig. 9.

This CAM circuit requires 89 cells, 0.09 µm² area, and 2 clock cycles latency.
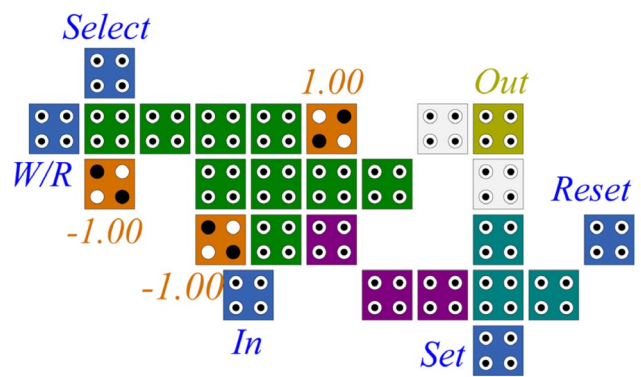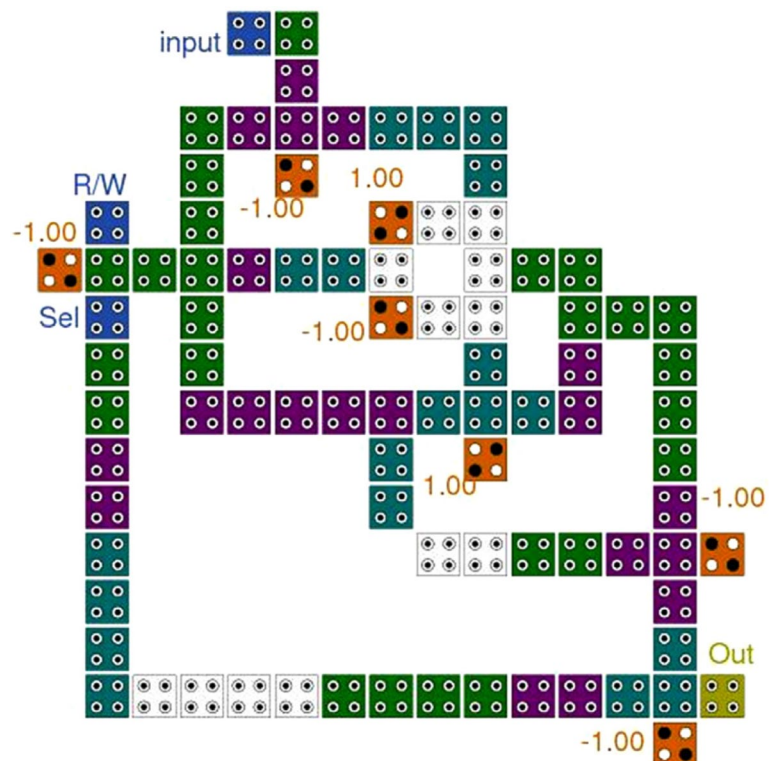

Fig. 7 The developed 1-bit RAM circuit in [7]

Hussien et al. [5] have offered a 5-input MG to increase the performance of the developed circuits in [20]. Then, they have designed a 1-bit CAM circuit based on this designed 5-input MG. Figure 10 displays the designed CAM circuit in [5]

This memory circuit requires 87 cells, 2 clock cycles, and 0.11 µm² area.

Sadoghifar and Rasouli Heikalabad [17] have designed a unique gate structure using an XOR gate and a 3-input MG. Then, they have designed a 1-bit CAM circuit based on this developed unique gate and memory unit. Figure 11 displays the developed 1-bit CAM circuit in [17].

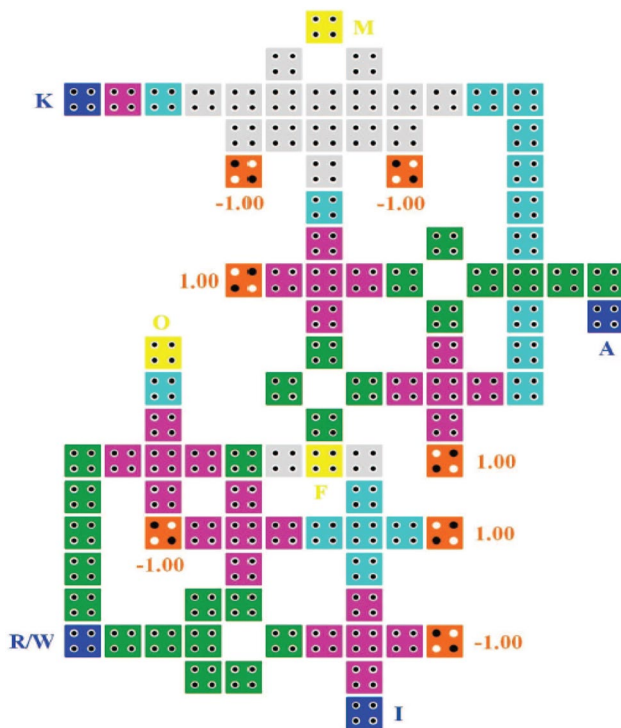**Fig. 6** The designed 1-bit RAM circuit in [12]

Fig. 8 The developed 1-bit CAM circuit in [20]

This memory circuit requires 46 cells, 1.25 clock cycles, and 0.04 μm² area.

Majeed et al. [21] have designed an optimal unique block using 2-input XOR gate and 3-input MG. Then, they utilize the developed optimal unique block for building a novel CAM circuit. The developed CAM circuit is shown in Fig. 12.

This memory circuit requires 40 cells, 1.25 clock cycles, and 0.04 μm² area.

Although these memory circuits have a suitable performance, the performance of the QCA memory circuits can be increased as described in next section.

3 The proposed circuits

This section presents the proposed structure for the CAM circuit. The proposed structure for the CAM circuit composed of two components: (a) the developed memory unit as building block and (b) identity gate. In the memory unit, the read and write operations are controlled using control signal. The output in this unit is used as the input of the identity gate. The identity gate has the task of matching the memory unit's output to the desired data. This section outlines the developed structures for memory unit and content-addressable memory.

3.1 The proposed memory unit

The proposed structure for the memory unit in the developed CAM circuit is based on the following equation:

$$M = \overline{(R/W)}IN + (R/W)M \qquad (2)$$

Based on Eq. (2), if R/W is "0", the input signal IN will be displayed in the output M. Whenever R/W is "1", the previous value will be hold in the output M regardless of the input IN. The memory unit proposed in this work is consists of a multiplexer 2 to 1 and negative feedback. The feedback loop is implemented by connecting the output M to the input port that is active when R/W is equal to "1". The proposed QCA structure for the implementation of the memory unit is displayed in Fig. 13. Table 1 shows the correctness of the developed structure for the implementation of memory unit based on Eq. (2).

Our new structure for the memory has 0.01 μm² area, 0.25 clock cycles, and 16 cells. This new structure will be utilized to develop a CAM circuit.

3.2 The proposed content-addressable memory

The proposed structure for the developed CAM circuit is based on the following equation:

$$Q = (A \ XNOR \ M) + S \qquad (3)$$

Figure 14 displays the developed structure for the CAM circuit.

The developed structure for the CAM circuit requires 0.03 μm² area, 0.75 clock cycles, and 32 cells. Recall that the proposed structure composed of two components: the developed memory unit as building block and identity gate. In the memory unit, the read and write operations are controlled using control signal that is shown by R/W. The output in this unit is shown by M that is the input of the identity gate. In addition, the identity gate has two other inputs named A and S. The output of the developed CAM circuit that is also output of the identity gate is shown by Q. Table 2 displays the correctness table for the proposed structure for the QCA CAM circuit based on Eq. (3). In accordance with Eq. (3), when the R/W value of the memory unit of the proposed CAM circuit is set to "0", the output of memory unit will be equal to the input IN. This means writing operation is performed. On the other hand, when the R/W value of the memory unit of the proposed CAM circuit is set to "1", the output of the memory unit is the previous value, that means the read operation is performed. Moreover, when the S value is set to "1", the output Q is "1" and when the S value is set to "0", the output Q is determined based on the inputs A and M.
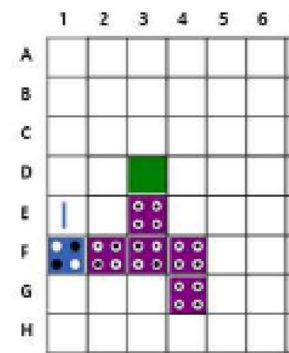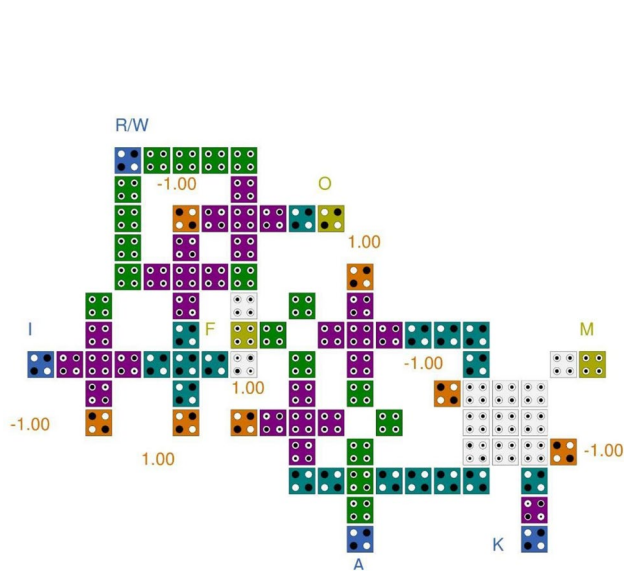
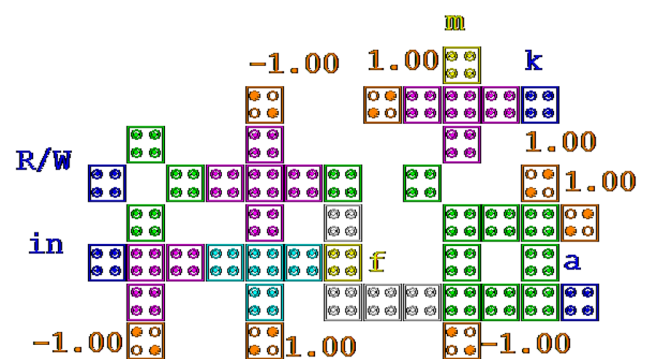**Fig. 9** The designed 1-bit CAM circuit in [6]
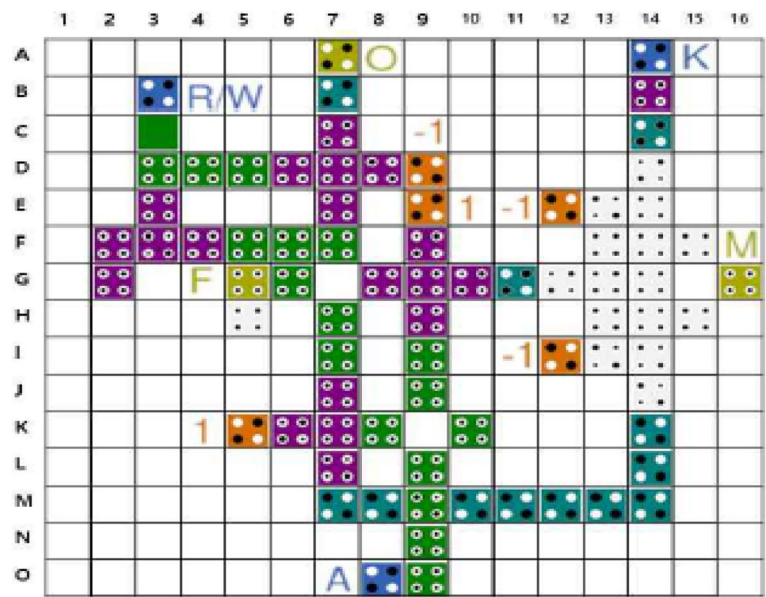
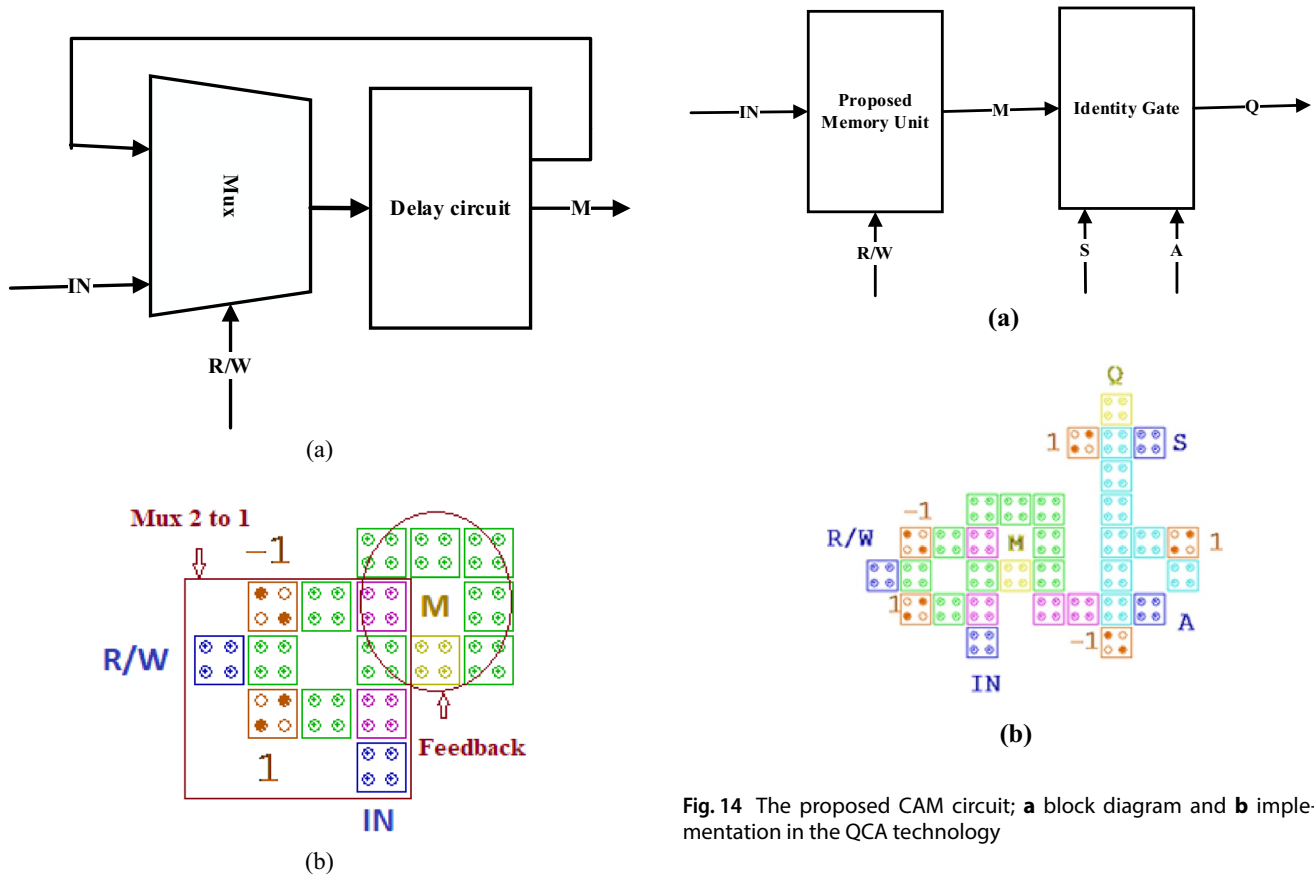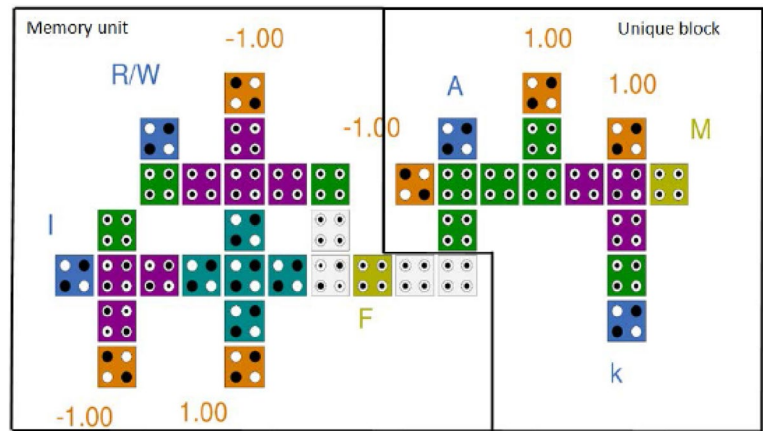**(a)** layer 1
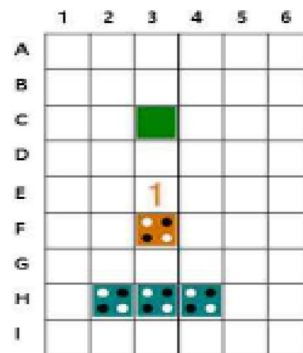
(b) layer 2   **(c)** layer 3

Fig. 11 The designed 1-bit CAM circuit in [17]

4 The results and comparison

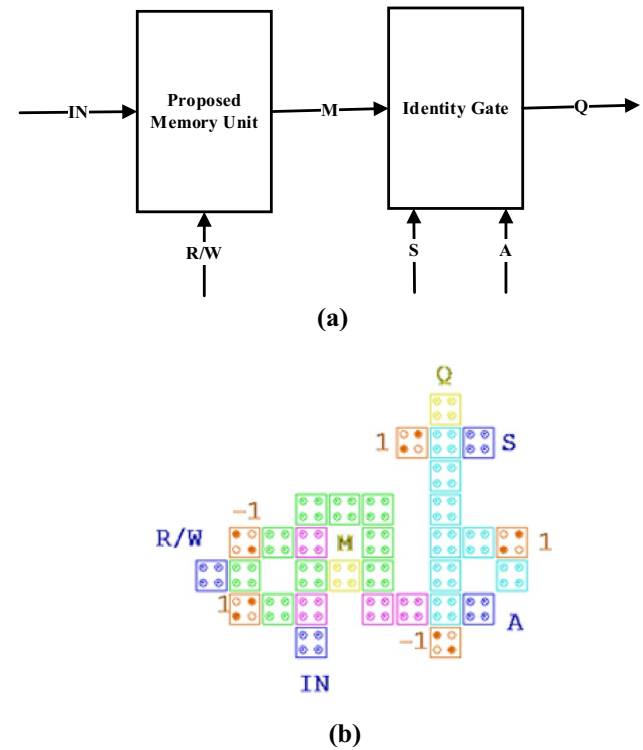This section outlines the simulation results and comparison the obtained results from the proposed structures for

Fig. 10 The designed 1-bit CAM circuit in [5]

Fig. 12 The designed 1-bit CAM circuit in [21]

(a)

(a)

(b)

Fig. 13 The proposed memory unit; **a** block diagram and **b** implementation in the QCA technology

(b)

Fig. 14 The proposed CAM circuit; **a** block diagram and **b** implementation in the QCA technology

memory unit and content-addressable memory with the simulation results that are reported in other works. The developed structures are simulated by using QCADesigner tool version 2.0.3.

4.1 The proposed memory unit

Figure 15 displays the simulation results of the designed memory unit, where the Bistable approximation engine is used for implementation. The simulation results verify the functionality of the designed memory unit. In addition,

Table 1 The truth table for the developed memory unit

R/W	IN	M
0	0	0
0	1	1
1	0	1
1	1	1

Table 2 The truth table for the proposed CAM circuit

| S	R/W	IN	A	M = (IN + R/W)	Q = (A XNOR M) + S
0	0	0	0	0	1
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	1	0
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

these results denote that our structure has 0.25 clock cycles delay. Table 3 displays the results of the deigned structure and its comparison with another circuit in [21].

Based on these results that are shown in the Figs. 13, 15 and Table 3, our proposed memory unit provides advantages compared with [21] with regard to cell count, area, latency, and cost. Accordingly, the designed structure has improved compared with that design in [21] by about 50%, 33%, 50%, and 75% with regard to area, cell count, latency, and cost, respectively, due to the use of the proposed structure for the memory unit.

4.2 The proposed content-addressable memory

Figure 16 illustrates the results of the developed CAM circuit. The simulation results verify the functionality of the designed content-addressable memory. In addition, these results denote that our structure has 0.75 clock cycles delay. Table 4 summarizes the results of the simulation in comparison with previous works in [5, 6, 12, 15, 17, 19–21].

Based on these results that are shown in Figs. 14, 16 and Table 4, our proposed CAM circuit has advantages compared with [5, 6, 12, 15, 17, 19–21] with regard to cell count, area, and cost. The proposed CAM circuit has improved in comparison with that design in [21] by about 25%, 20%, 40%, and 60% with regard to area, cell count,
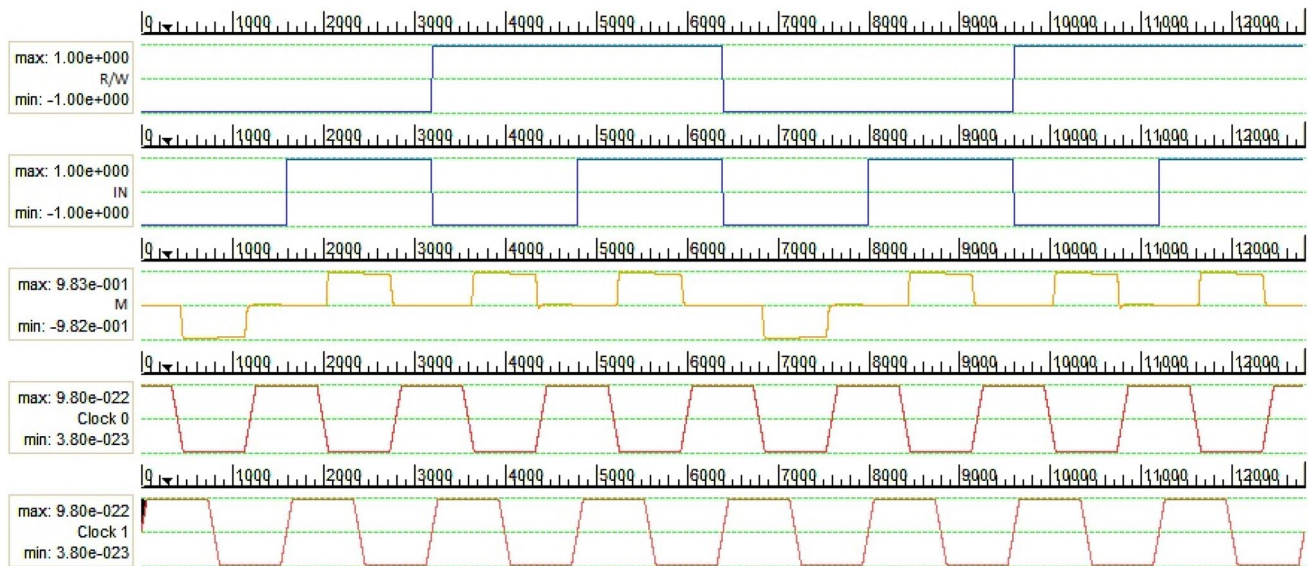
Fig. 15 The results of the developed memory unit

Table 3 The comparative table for the memory units

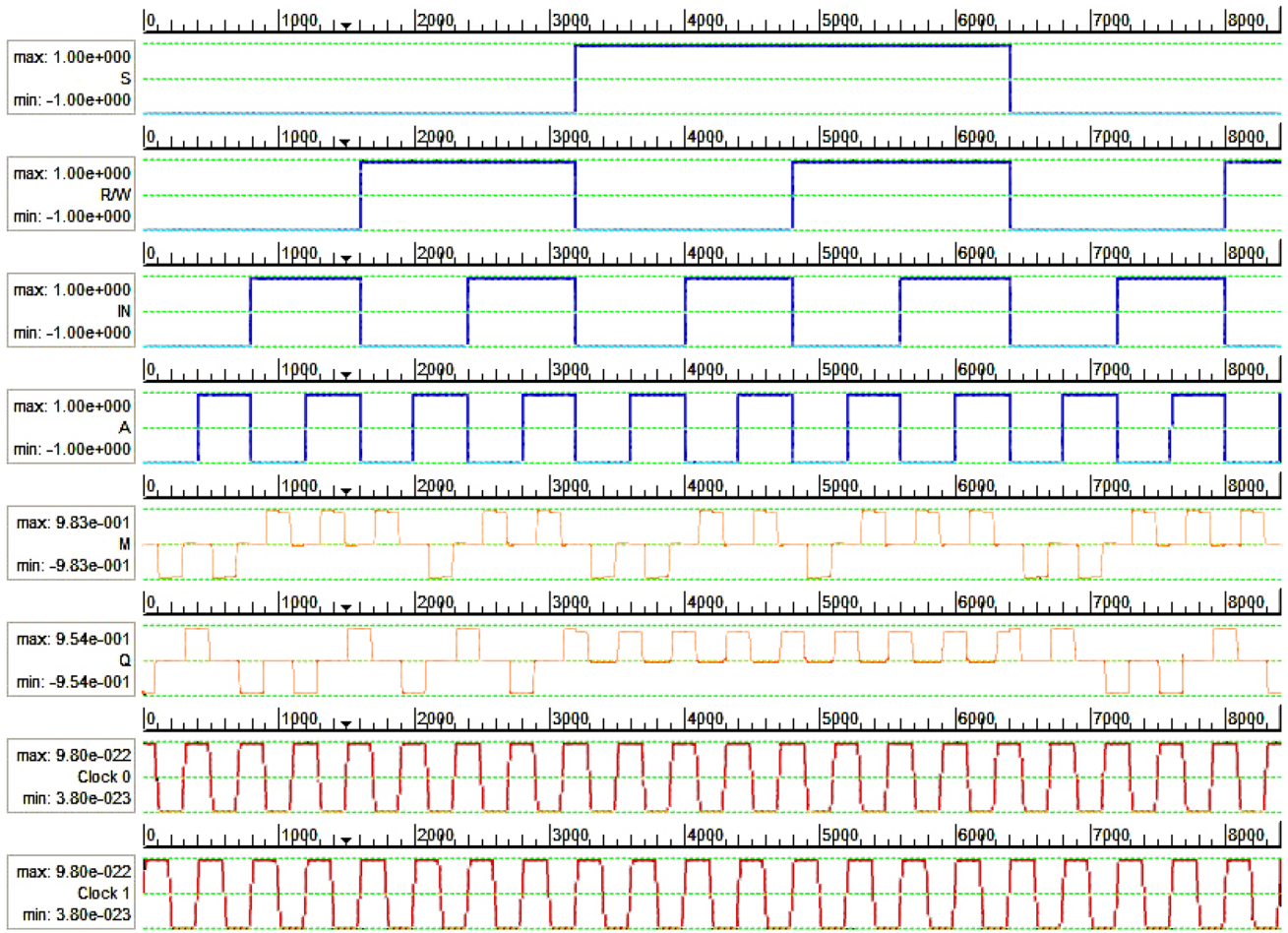| Reference	Cell count	Area (μm²)	Latency (clock cycle)	Cost = Area * Latency (clock cycle)
[21]	24	0.02	0.5	0.01
This paper	16	0.01	0.25	0.0025

Fig. 16 The results of the designed content-addressable memory circuit

Table 4 The comparative table for the CAM circuits

References	Cell count	Area (µm²)	Latency (clock cycle)	Cost = Area * Latency (clock cycle)
[15] (RAM)	109	0.13	1.75	0.227
[19] (RAM)	88	0.08	1.5	0.12
[12] (RAM)	87	0.13	1.5	0.195
[7] (RAM)	26	0.026	1	0.026
[20] (CAM)	100	0.14	2	0.28
[6] (CAM)	89	0.09	2	0.37
[5] (CAM)	87	0.11	2	0.22
[17] (CAM)	46	0.04	1.25	0.05
[21] (CAM)	40	0.04	1.25	0.05
This paper (CAM)	32	0.03	0.75	0.02

latency, and cost, respectively, due to the use of the developed memory unit and efficient design if CAM circuit.

5 Conclusions

The QCA technology is one of the novel kind of nanotechnologies that has been able to replace the CMOS by relying on its superior capabilities such as speed and area. The CAM circuit is a type of memory circuits that is mostly utilized in high-speed systems. In this paper, a new circuit was developed for the memory unit. Subsequently, this new memory unit was utilized to developed CAM circuit in the QCA technology. The results are obtained using QCADesigner tool version 2.0.3. The proposed circuit for the CAM circuit requires $0.03 \ \mu m^2$ area, 32 cells, and 0.75 clock cycles delay. The simulation results indicate improvements in the proposed circuit compared with other circuits. The proposed CAM circuit has been improved compared to recently designed CAM circuit by about 25%, 20%, 40%, and 60% with regard to area, cell count, latency, and cost, respectively.

Declaration

Conflict of interest The authors state that there is no conflict of interest.

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