**THESIS:**

1. Designing and verifying the Random-Access memory cell in Quantum dot cellular Automata.
2. Designing and verifying the Content-Addressable memory cell in Quantum dot cellular Automata.

**ABSTRACT:**

Memory is crucial for system functionality, with Content-Addressable Memory (CAM) and Random-Access Memory (RAM) offering distinct data access methods. Various searching algorithms optimize this process, each with specific complexities and trade-offs. QCA Designer software is employed for designing, simulating, and verifying CAM and RAM memory cells, leveraging Quantum-dot Cellular Automata (QCA) technology. The focus on efficient searching algorithms highlights the need to balance computational intricacies with practical advantages in memory design.

**INTRODUCTION TO QCA:**

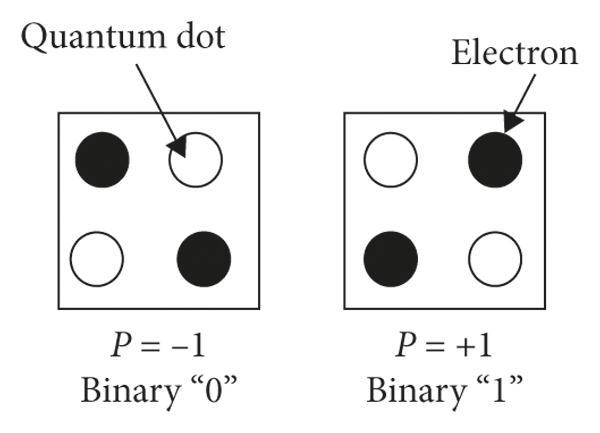
Quantum-dot Cellular Automata (QCA) is an innovative nanotechnology that leverages quantum effects to perform computation and store information. In QCA, binary data is represented using the polarization of electron spins within quantum dots. Unlike traditional electronic systems that use electrical currents, QCA operates based on the Coulombic interaction between neighboring quantum dots. This results in potential advantages such as ultra-low power consumption, high-speed operation, and a compact physical footprint. QCA has shown promise for applications in digital logic, memory design, and nanoscale computing due to its potential to overcome some of the limitations associated with conventional technologies. The unique properties of QCA make it an area of active research for developing next-generation computing architectures.

**Cell Orientations:**

1. In a 90-degree QCA cell, extra electrons occupy dots diagonally across from each other.
2. In a 45-degree QCA cell, extra electrons occupy dots vertically or horizontally across from each other.

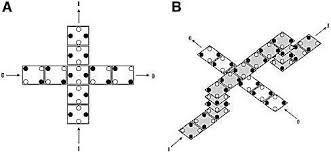
**Cell Polarizations (P):**

1. The extra electrons form distinct cell polarizations, denoted as P.
2. In a 90-degree cell, P can be -1 or +1, representing binary states 0 and 1.
3. In a 45-degree cell, similar binary information is encoded using P values.



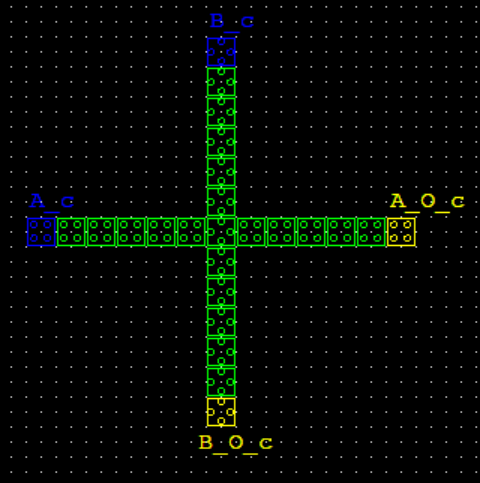
**SINGLE LAYER vs MULTILAYER DESIGN:**

Multilayer QCA design is adopted when the one cell train is required to be bypassed by another without connection. Multilayer design is simply a multi plane design. First Design below is single layer whereas second design is multilayer.

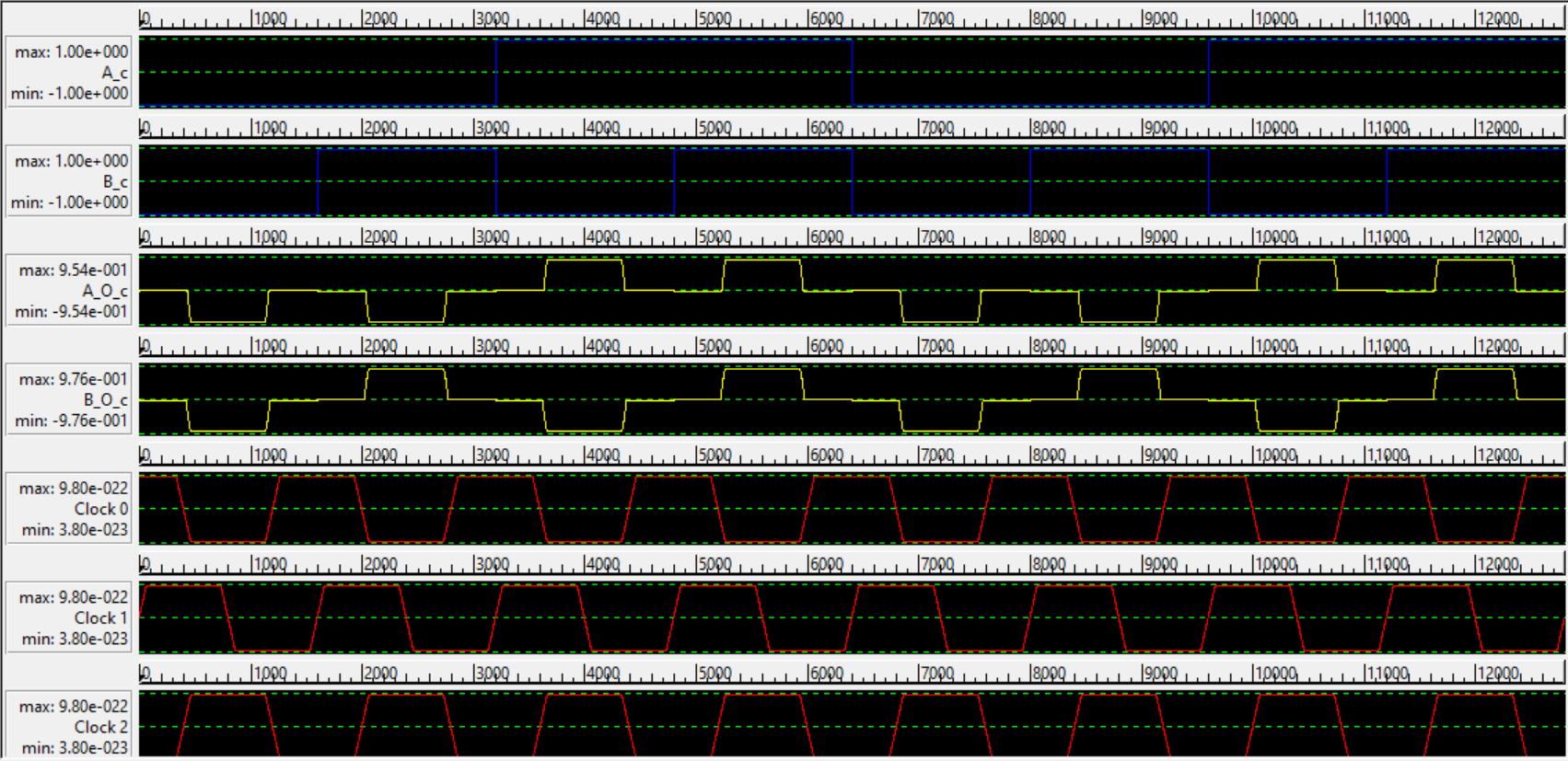


Multi-layer design for the same CAM cell is also tried by us but the simulation results we got are different from the simulation results we got from single layer design.

So we come up with the conclusion that the CAM Cell design provided to us may be specially designed for single layer keeping in mind the effects of single layer on design which are absent in multilayer design that is why different outputs are obtained.

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**COPLANAR**

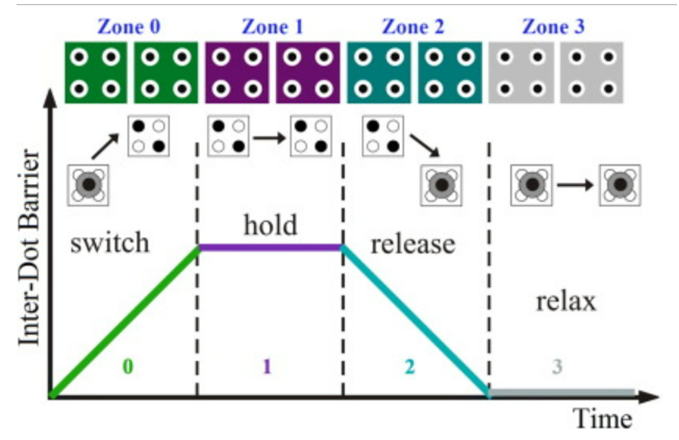
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**COPLANAR RESULT**

**QCA SIMULATION RESULTS OF BASIC GATES:**

**CLOCK PULSE :**

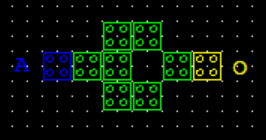
The clocking of QCA can be accomplished by controlling the potential barriers between adjacent quantum-dots. The clock used in QCA consists of four phases: hold, release, relax, and switch. It is considered that the lag between adjacent phases is 90°



**NOT GATE:**

No. of Cells=9

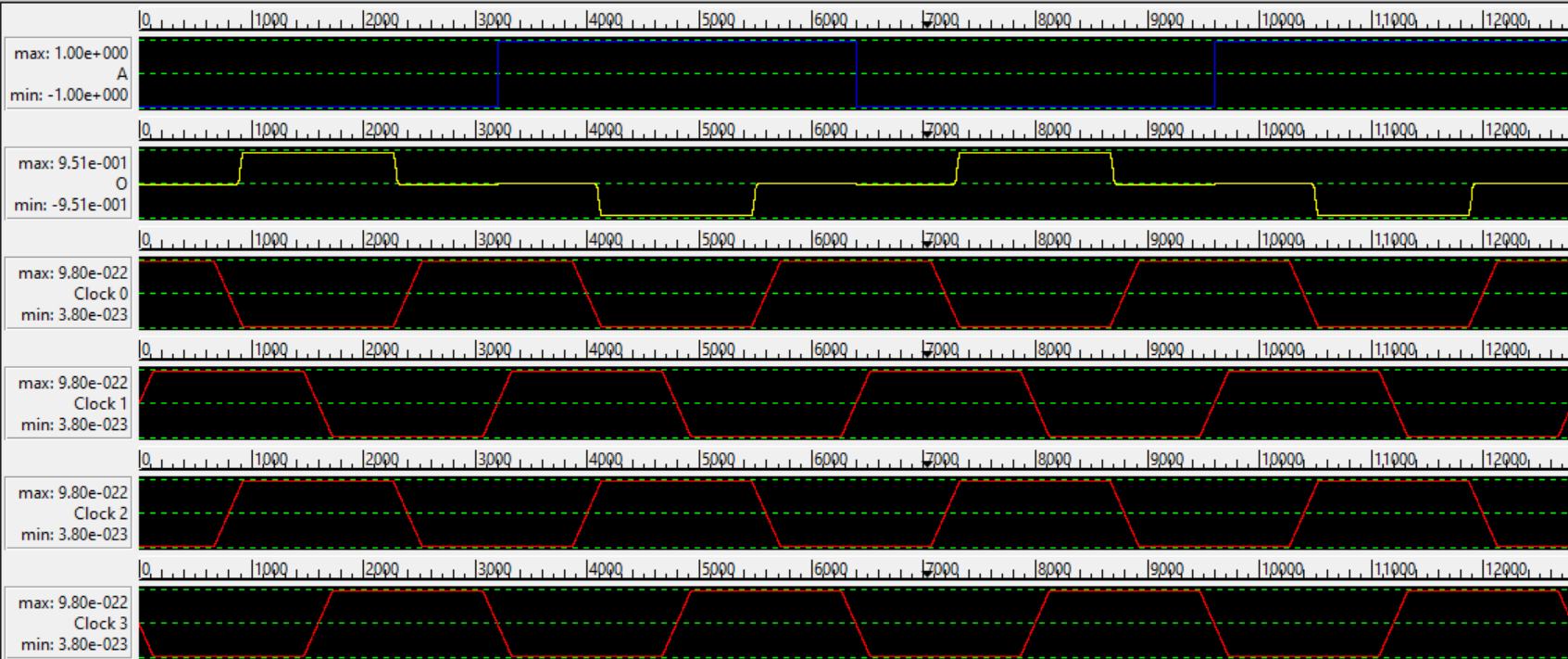
Area Occupied=6117 nm^2



**NOT Gate QCA Circuit**

**SIMULATION RESULT**

Output Figure showing the nature of NOT Gate logic.

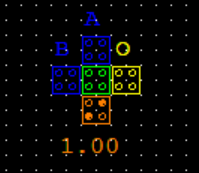


**NOT GATE RESULT**

**OR GATE:**

No. of Cells=5

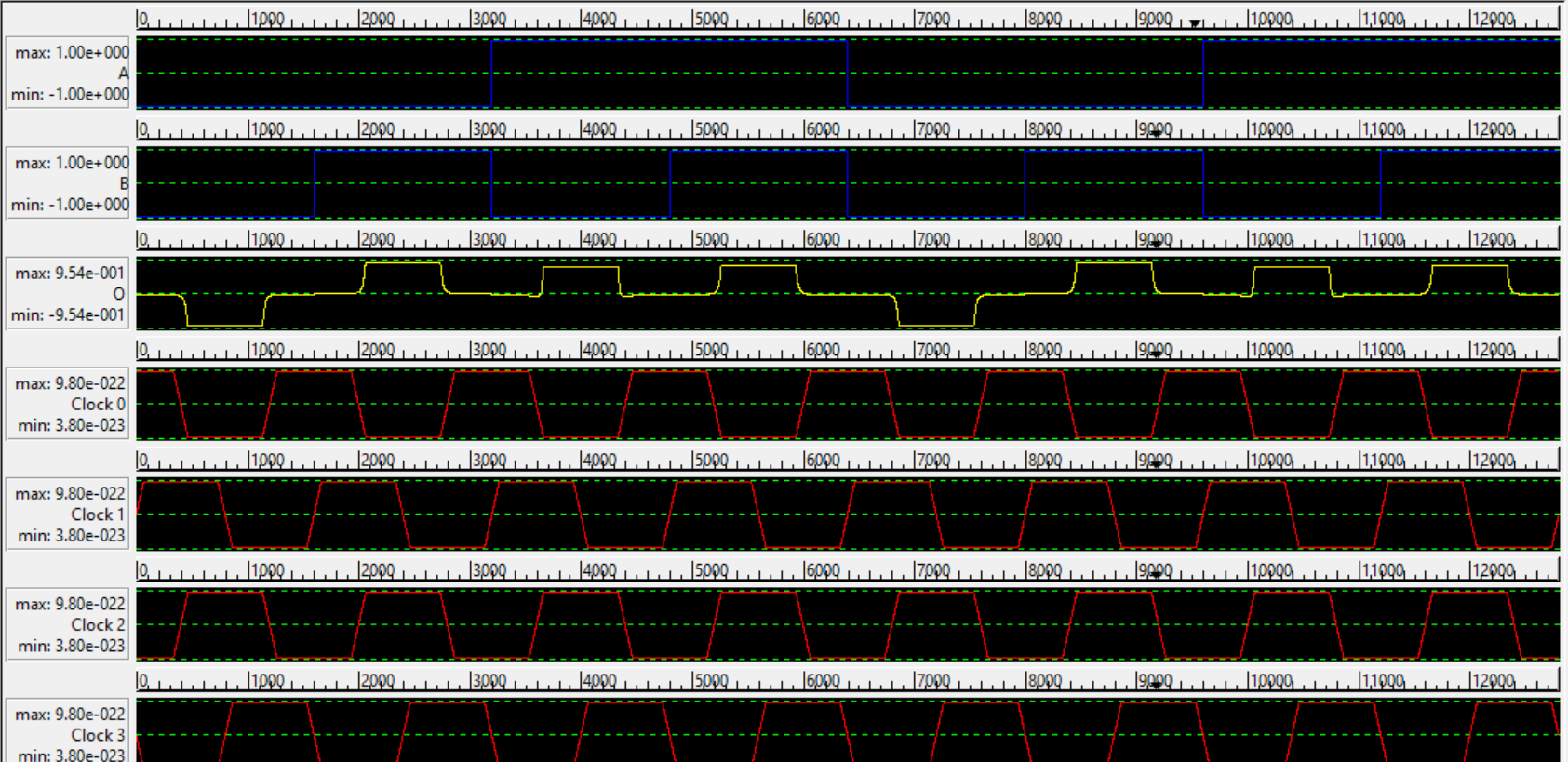
Area Occupied=0.01 um^2



**OR GATE**

**SIMULATION RESULT**

Figure showing the nature of OR Gate logic.

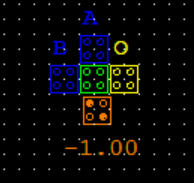


**OR GATE RESULT**

**AND GATE:**

No. of Cells=5

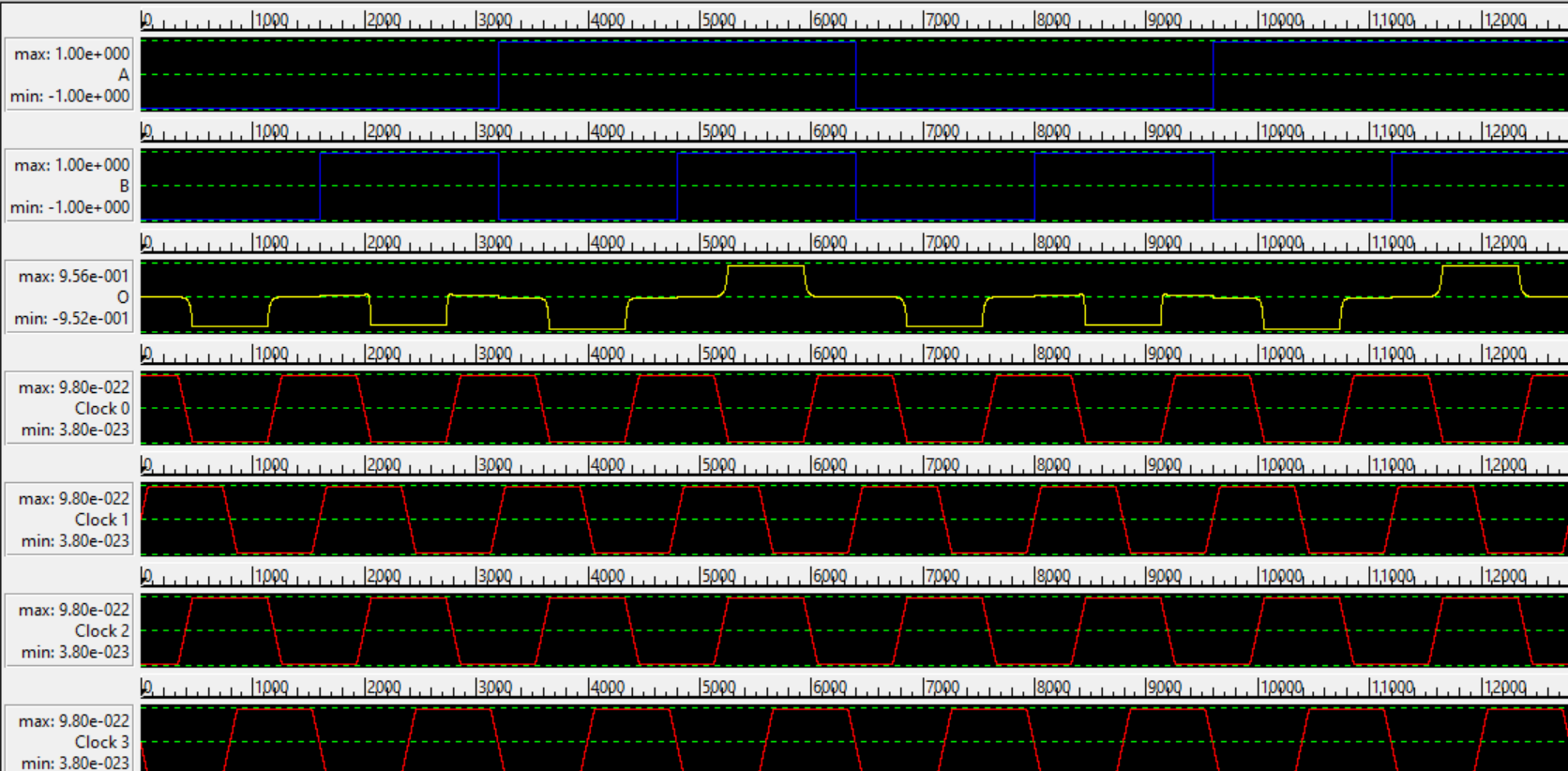
Area Occupied=0.01 um^2



**AND GATE**

**SIMULATION RESULT**

Figure showing the nature of AND Gate logic.



**AND GATE RESULT**

**NAND GATE:**

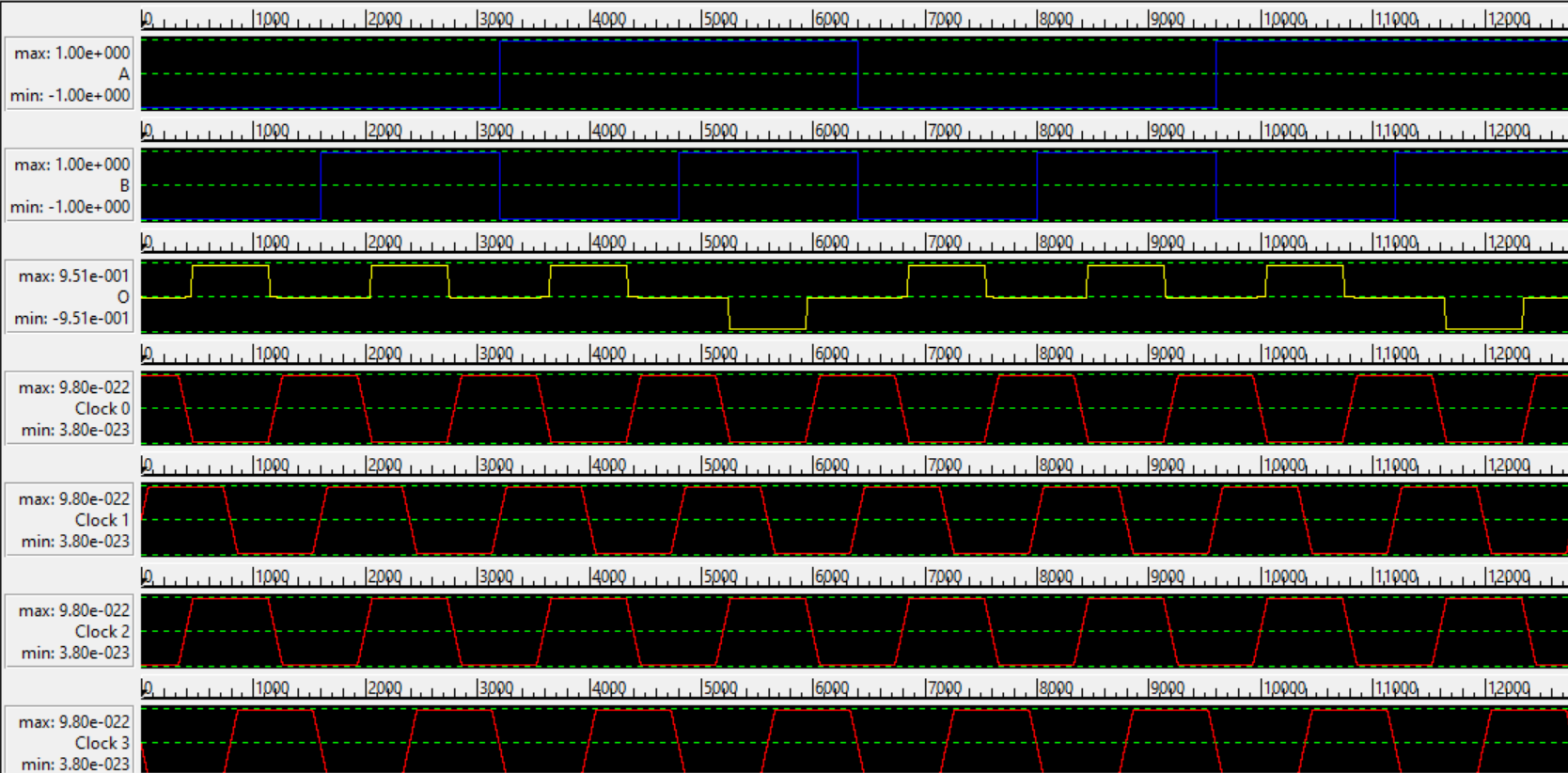
No. of Cells=12



**NAND GATE**

**SIMULATION RESULT**

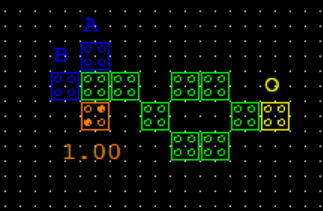
Figure showing the nature of NAND Gate logic.



**NAND GATE RESULT**

**NOR GATE:**

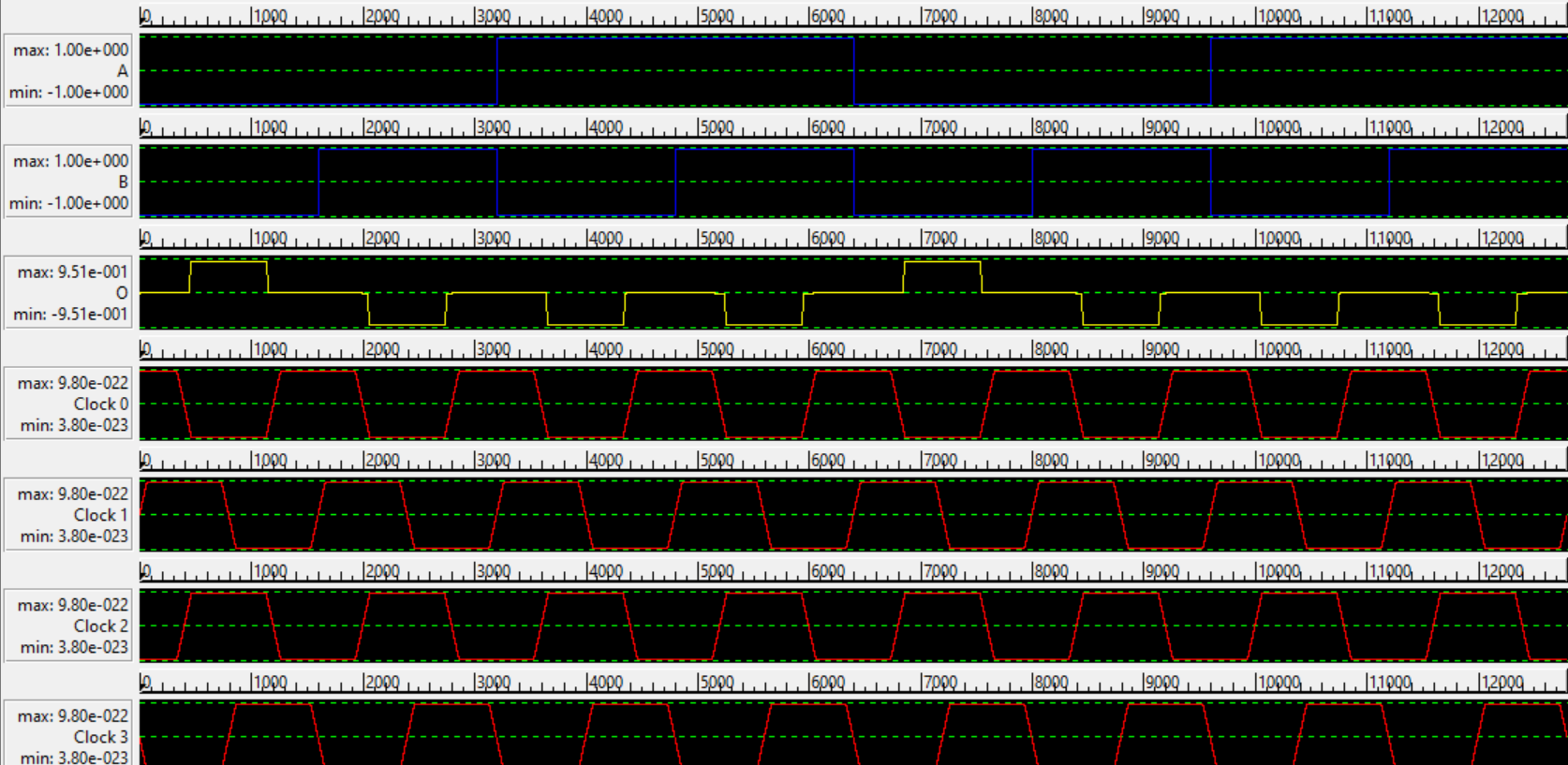
No. of Cells=12



**NOR GATE**

**SIMULATION RESULT**

Figure showing the nature of NOR Gate logic.



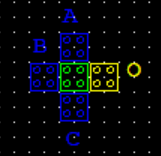
**NOR GATE RESULT**

**3-INPUT MAJORITY GATE:**

Maj (A, B, C) = AB + BC + CA

No. of Cells=5

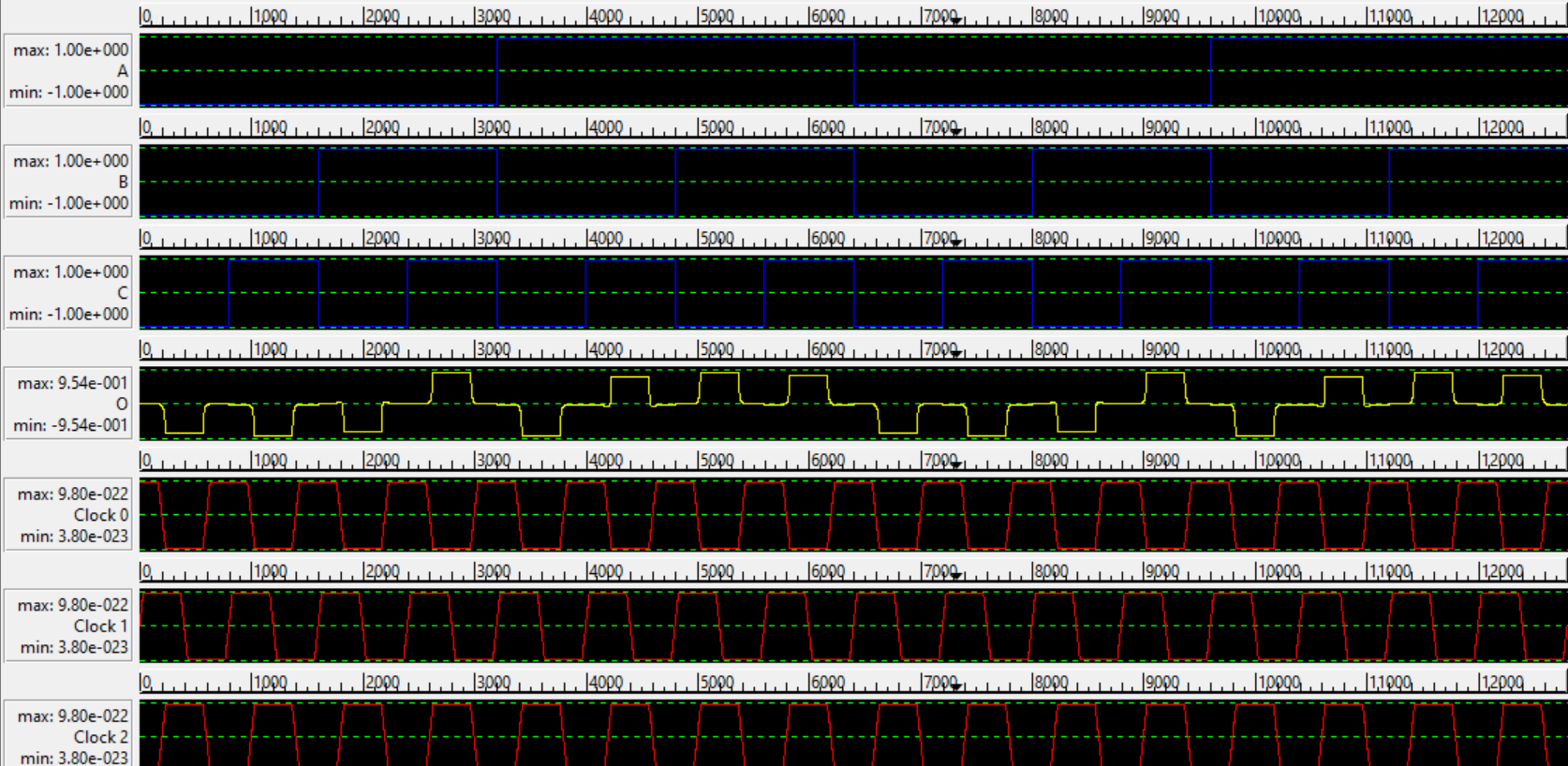
Area Occupied=0.01 um^2



**3 INPUT MAJORITY GATE**

**SIMULATION RESULT**

Figure showing the nature of 3 input Majority Gate logic.



**3 INPUT MAJORITY GATE RESULT**

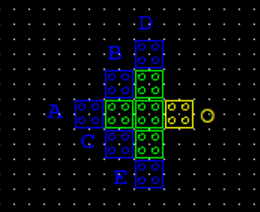
3 Input Majority gate functionality acts like a two-input AND or OR gate by setting the polarization of one input cell to a constant value of -1 or +1, respectively.

**5-INPUT MAJORITY GATE:**

Maj (A, B, C, D, E) = (ABC + ABD + ABE + ACD +ACE +ADE + BCD + BCE + BDE + CDE)

No. of Cells=10

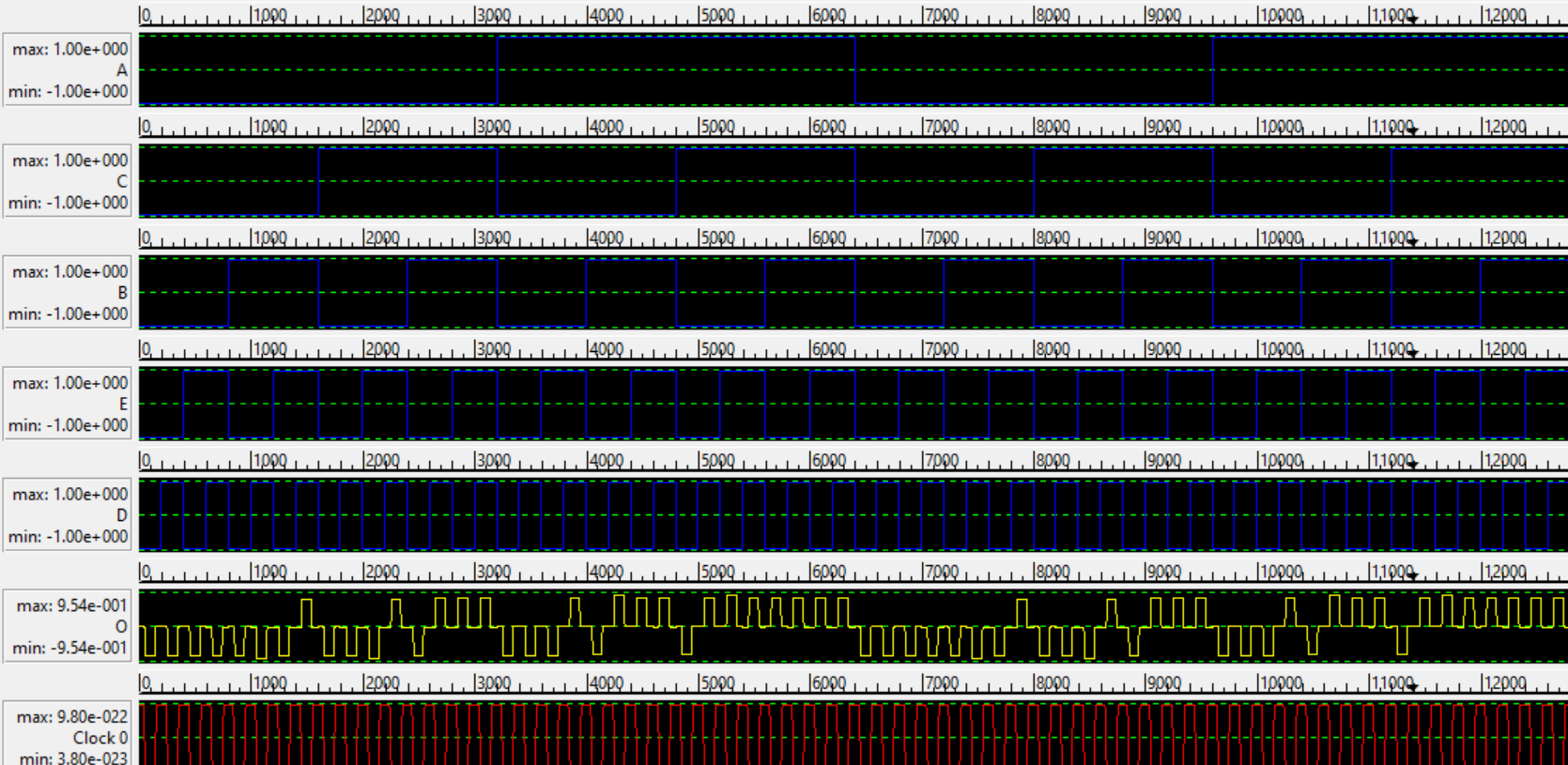
Area Occupied=0.01 um^2



**5 INPUT MAJORITY GATE**

**SIMULATION RESULT**

Figure showing the nature of 5 i/p Majority Gate logic.



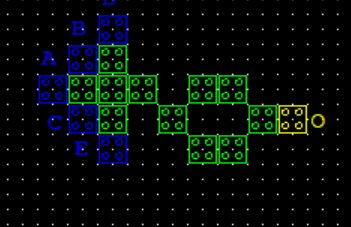
**5 INPUT MAJORITY GATE RESULT**

A 3 i/p NAND Gate and 3 i/p NOR Gate can be Obtained by taking the polarization of 2 of the 5 i/p of 5 i/p majority gate as -1 and 1 respectively.

**5-INPUT MINORITY GATE:**

Min (A, B, C, D, E) = {Maj (A, B, C, D, E)}’

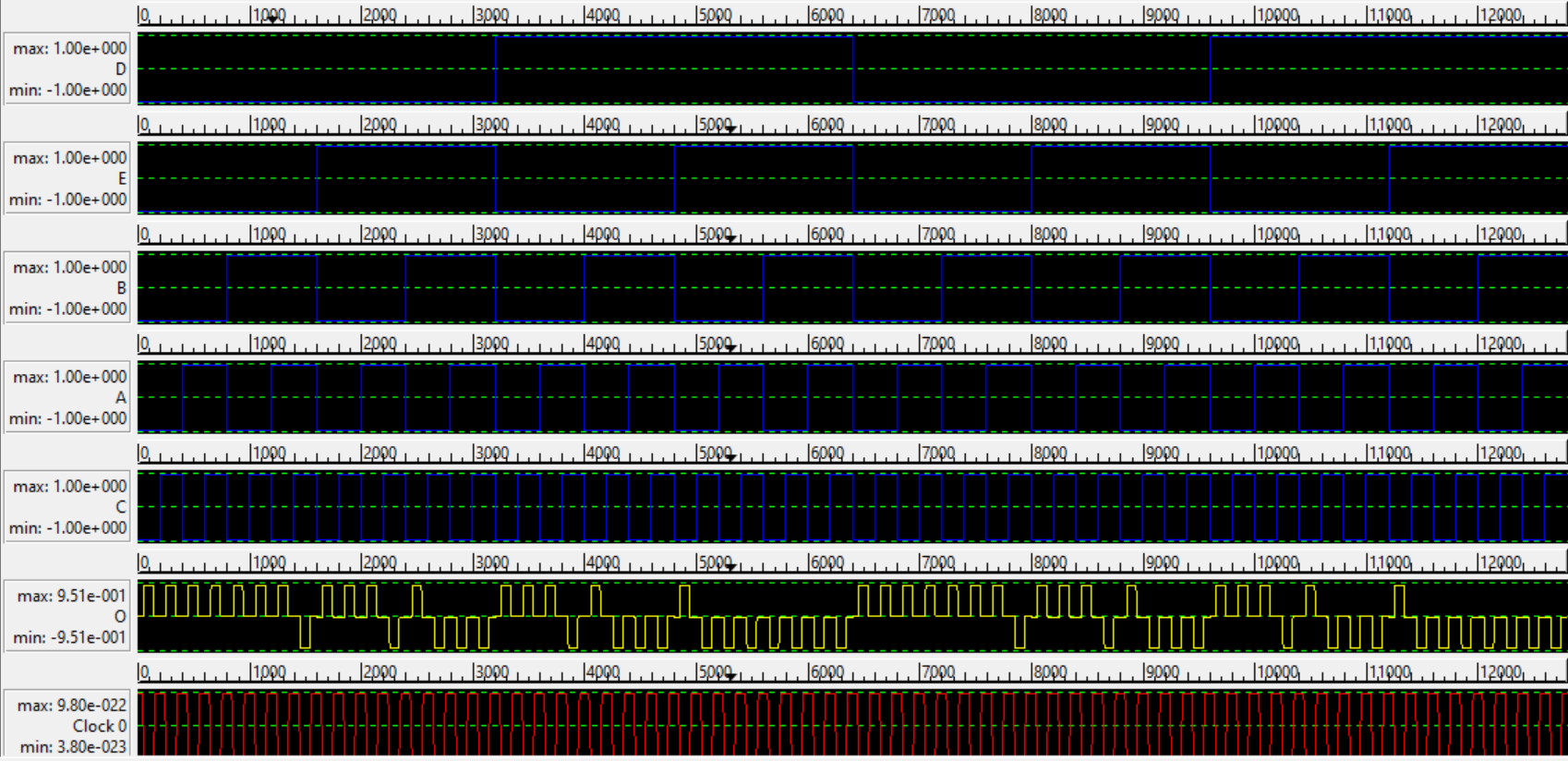
No. of Cells=17



**5 INPUT MINORITY GATE**

**SIMULATION RESULT**

Figure showing the nature of 5 i/p Minority Gate logic.



**5 INPUT MINORITY GATE RESULT**

**RAM:**

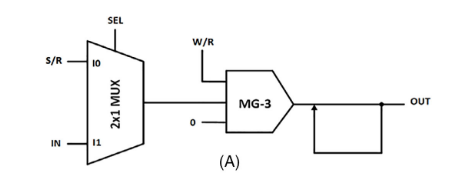
In RAM memory cell store data is searched using the memory location of that data. It is a less effective memory cell as compared to CAM Cell.

There are 4 latching clocking zones that follow one another within the memory loop. The looping of the stored memory continues until the memory is altered as a result of a write operation. No read operation modifies the memory in any way.

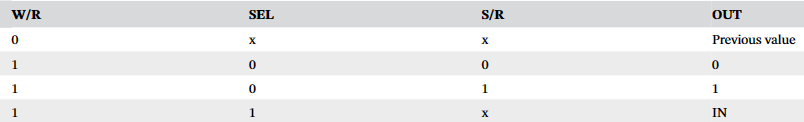
**PROPOSED RANDOM ACCESS MEMORY:**

cell area of 0.0078μm2, total area of 0.021μm2and having a latency of 0.75 clock cycles. The proposed design con-sists of four inputs; select (SEL), set/reset (S/R), input (IN), and write/read (W/R). The set/reset and input lines act as inputs to the 21 multiplexer used in the RAM cell and the select line is used to select the input. The 2:1 MUX pro-posed has been optimized to provide the desired functionality.When both the select line and W/R line are set to“1”then independent of the value of set/reset line, the output is equal to the value of input line which is the write operation. When the write/read line is set to“0”then the output is equal to the previous output and thus the read operation is performed. When W/R is set to“1”and the select line is set to“0,”the output is equal to the value of the set/reset line and accordingly the RAM cell performs Set and Reset Operations. The truth table of the proposed RAM cell is depicted in Table

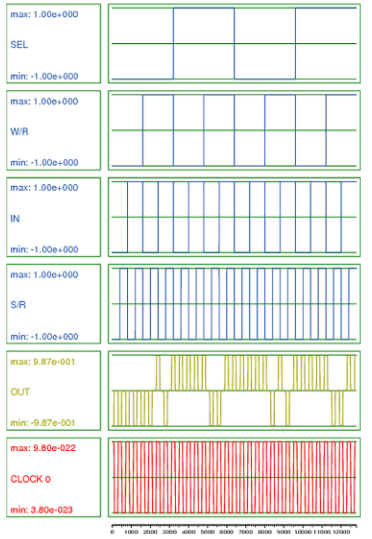
**CIRCUIT DIAGRAM:**



**TRUTH TABLE OF RAM CELL:**



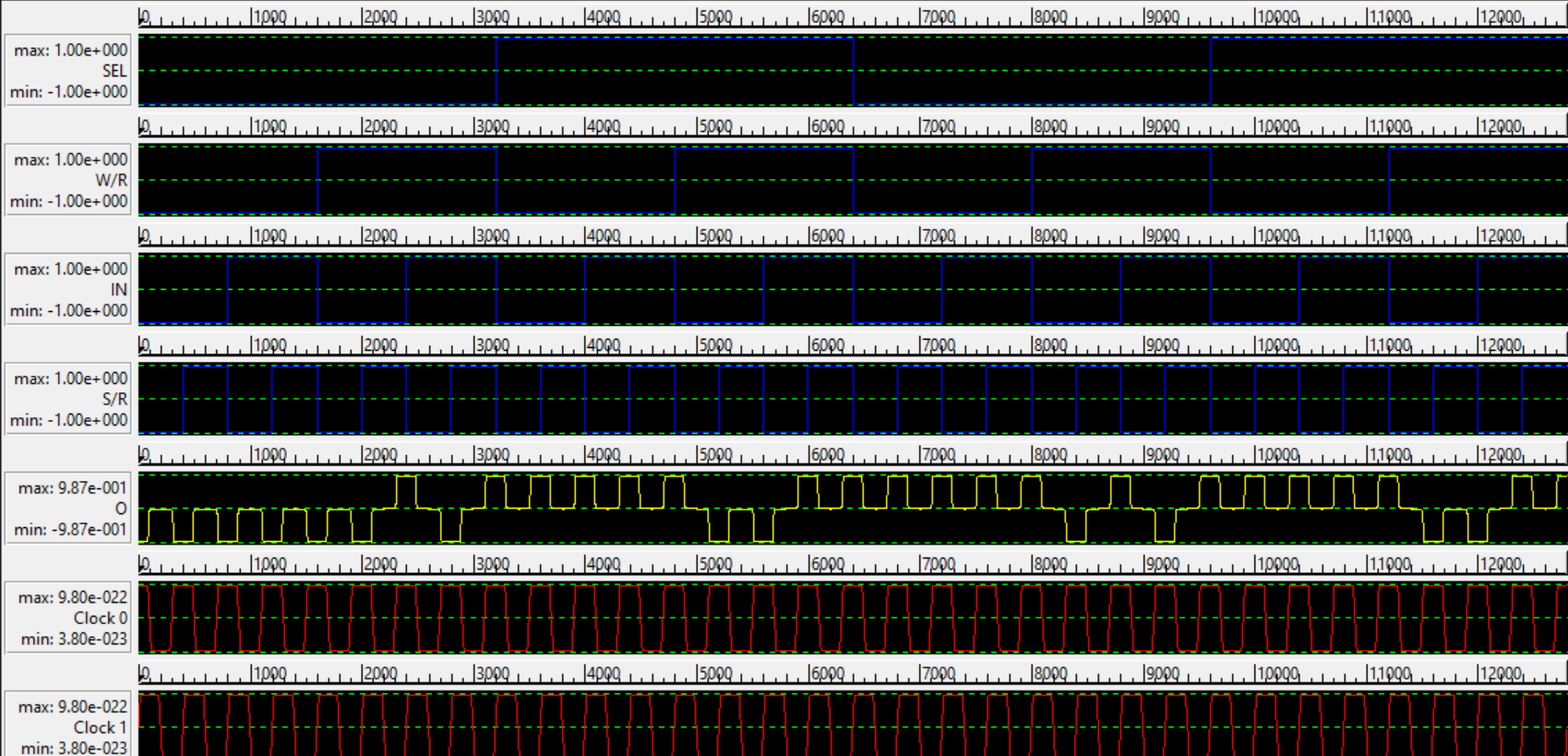
**ACTUAL** **OUTPUT FOR PROPOSED RAM CELL:**

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**RAM:**



**RAM OUTPUT:**

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**CAM:**

Content addressable memory (CAM) is a data storage device that stores memory in cells. When any aspect of the memory is entered, the CAM compares the input with all the stored data. It is a high-speed technology. In CAM memories are not arranged in chronological order and are not packed in isolated modules.

The developed structure for the CAM circuit requires 0.03 µm2 area, 0.75 clock cycles, and 32 cells.

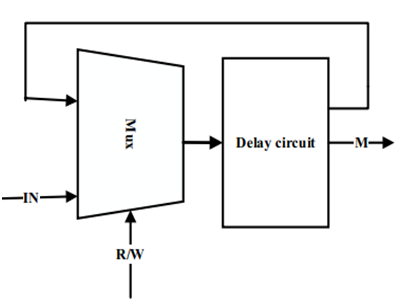
In the memory unit, the read and write operations are controlled using a control signal that is shown by R/W. The output in this unit is shown by M that is the input of

The gate has two other inputs named A and S. The output of the developed CAM circuit that is also the output of the identity gate is shown by Q.

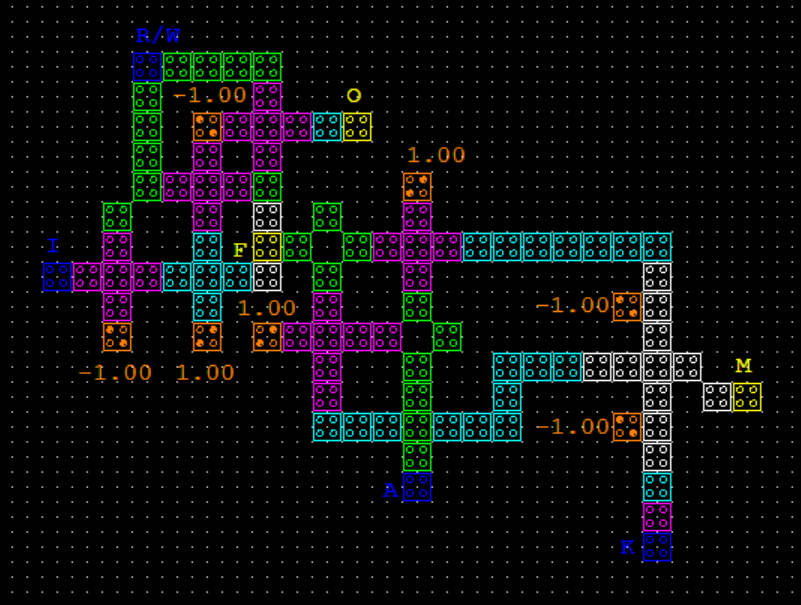
when the R/W value of the memory unit of the proposed CAM circuit is set to “0”, the output of the memory unit will be equal to the input IN. This means a writing operation is performed. On the other hand, when the R/W value of the

The memory unit of the proposed CAM circuit is set to “1”, the output of the memory unit is the previous value, that means the read operation is performed. Moreover, when the S value is set to “1”, the output Q is “1” and when the S value is set to “0”, the output Q is z

**MEMORY UNIT IN CAM CIRCUIT:**

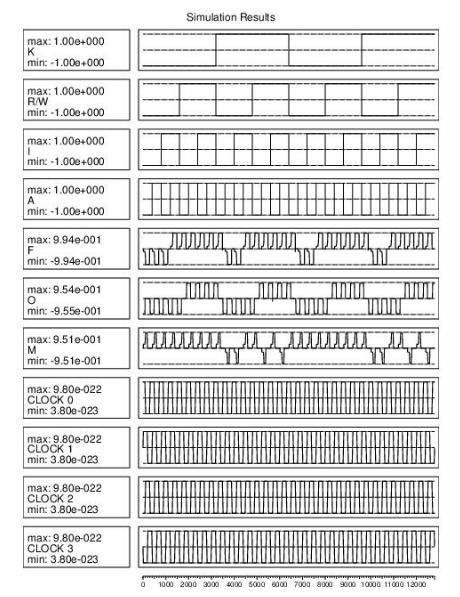


**CAM REFERENCE:**

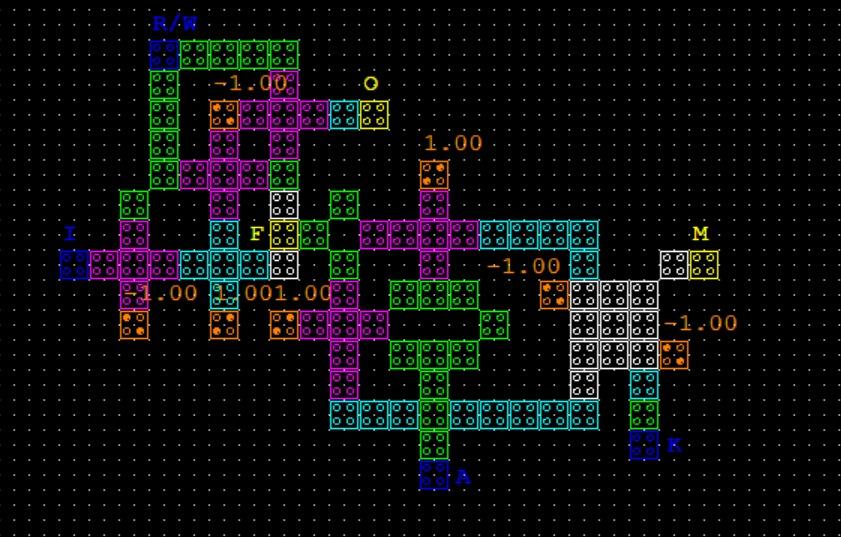


**CAM SIMULATION RESULTS:**

**ACTUAL OUTPUT:**

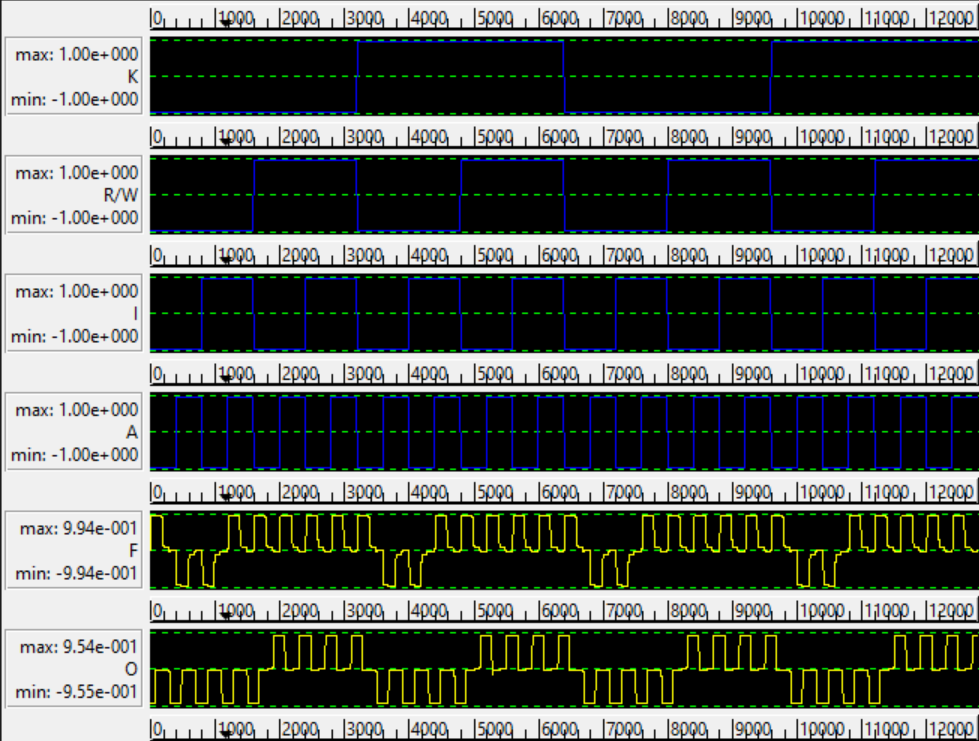
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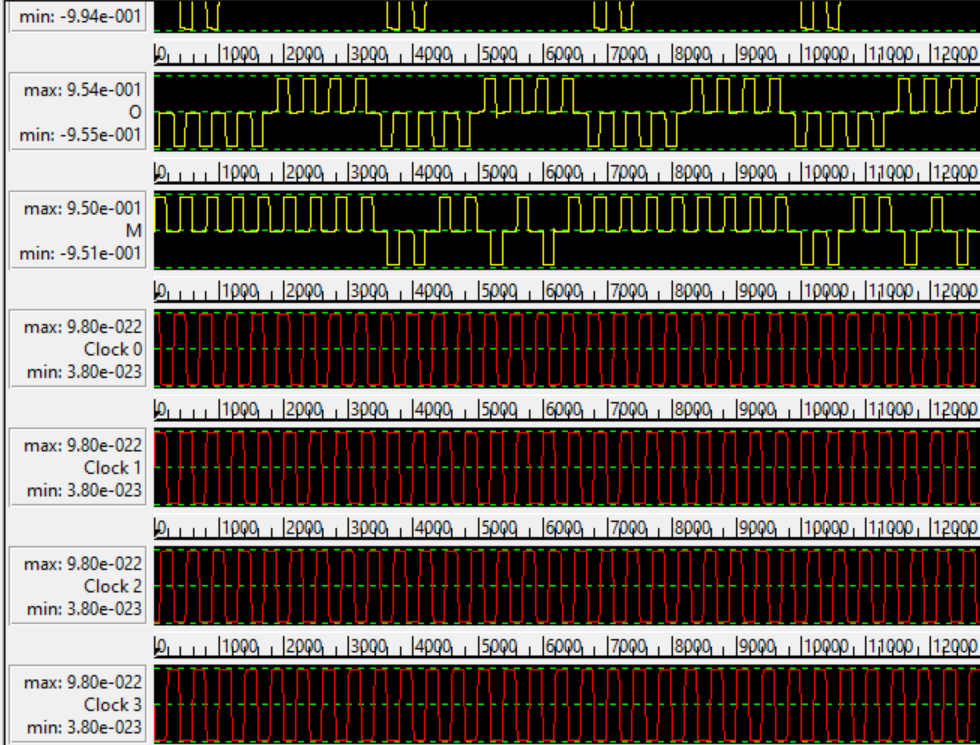
**PROPOSED CAM:**



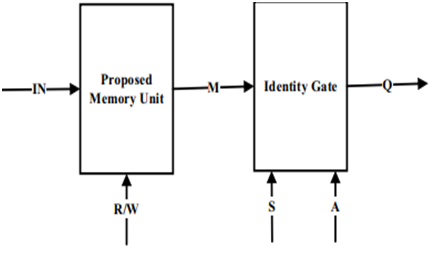
**OBTAINED RESULTS:**

**(PROPOSED CAM)**

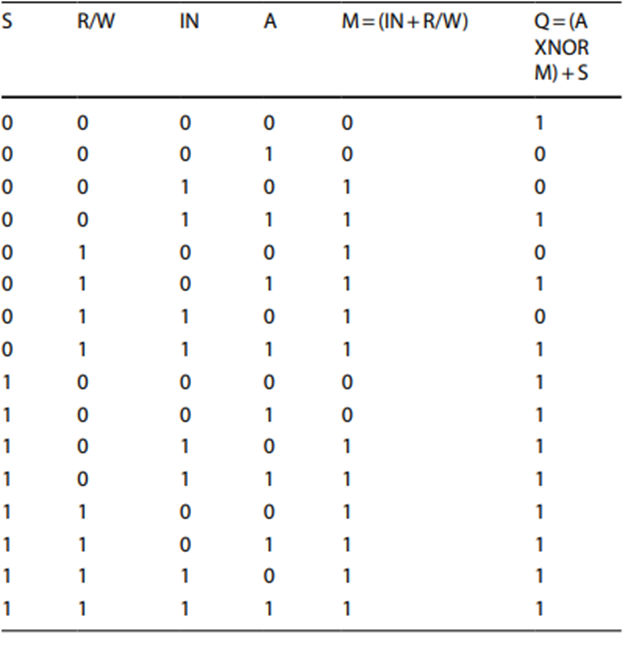




**BLOCK DIAGRAM :**



**TRUTH TABLE:**



**REFERENCES:**

**For RAM cell:**

<https://onlinelibrary.wiley.com/doi/epdf/10.1002/jnm.2946>

**For CAM cell:**

Reference pdf

**CONCLUSION:**

Hence, we have verified and acknowledged the working of QCA cells and made basic circuits using QCA cells in QCA designer app

Also, we have designed RAM cell and CAM cell using basic gates and verified the obtained results with the references provided.