Analog to Digital and Digital to Analog Conversion

- The most naturally occurring phenomena are analog in nature. Analog quantities are continuous functions of time and most transducers give an analog output.
- Digital to analog converters are used in computer driven CRT displays, digital generation of analog waveforms, and digital control of automatic process control systems.
- Moreover, some popular A/D conversion techniques use D/A converters for functioning.

General Considerations of Analog to Digital and Digital to Analog Conversion

For an n-bit system, a number can be represented by

$$d_{(n-1)}2^{(n-1)} + d_{(n-2)}\,2^{(n-2)} + \ldots\ldots\ldots\ldots + d_1 2^1 + d_0\,2^0$$

Consider a 4-bit system having full range E_R. Then, for different combination of digital input, analog voltage is given by

Table 5.1 Equivalent analog voltage for digital input

Digital input	Analog voltage
1000	$E_R/2$
0100	$E_R/2^2$
0010	$E_R/2^3$
0001	$E_R/2^4$

Thus, for an n-bit system having full range E_R,

$$\text{weight or range of MSB} = \frac{E_R}{2}$$

$$\text{weight or range of LSB} = \frac{E_R}{2^n}$$

Consider the 4-bit system explained above. Then, the analog output for a digital input having all bits high i.e., input = 1111 can be obtained superimposing all the values given in above table.

$$E_o = \frac{E_R}{2} + \frac{E_R}{2^2} + \frac{E_R}{2^3} + \frac{E_R}{2^4}$$

$$\text{or, } E_o = E_R\,[1\times 2^{-1} + 1\times 2^{-2} + 1\times 2^{-3} + 1\times 2^{-4}]$$

$$\text{or, } E_o = E_R\,[d_3 2^{-1} + d_2 2^{-2} + d_1 2^{-3} + d_0 2^{-4}]$$

$$\text{or, } E_o = \frac{E_R}{2^4}\,[d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0]$$

Thus, for an n-bit system, the analog voltage is given by

$$E_o = \frac{E_R}{2^n}\,[d_{(n-1)}\,2^{(n-1)} + d_{(n-2)}\,2^{(n-2)} + \ldots\ldots\ldots + d_1 2^1 + d_0 2^0]$$

Digital to Analog Converter (DAC)

Following are the types of DAC:

- Weighted Resistor Network (WRN) DAC
- R:2R Ladder Network DAC
- **Weighted Resistor Network**

In WRN DAC, the resistor is weighted reverse of the binary system i.e., resistance associated with MSB has the least value and as we move from MSB to LSB, the resistance value increases with a factor 2 as given in the following table.

For 4-bit system,

Bit	d_3	d_2	d_1	d_0
Binary weight	2^3	2^2	2^1	2^0
Resistance weight or value	2^0R	2^1R	2^2R	2^3R

Thus for an n-bit system (converter),

Weight or value of the resistance in MSB = 2^0R

Weight or value of the resistance in LSB = $2^{(n-1)}R$

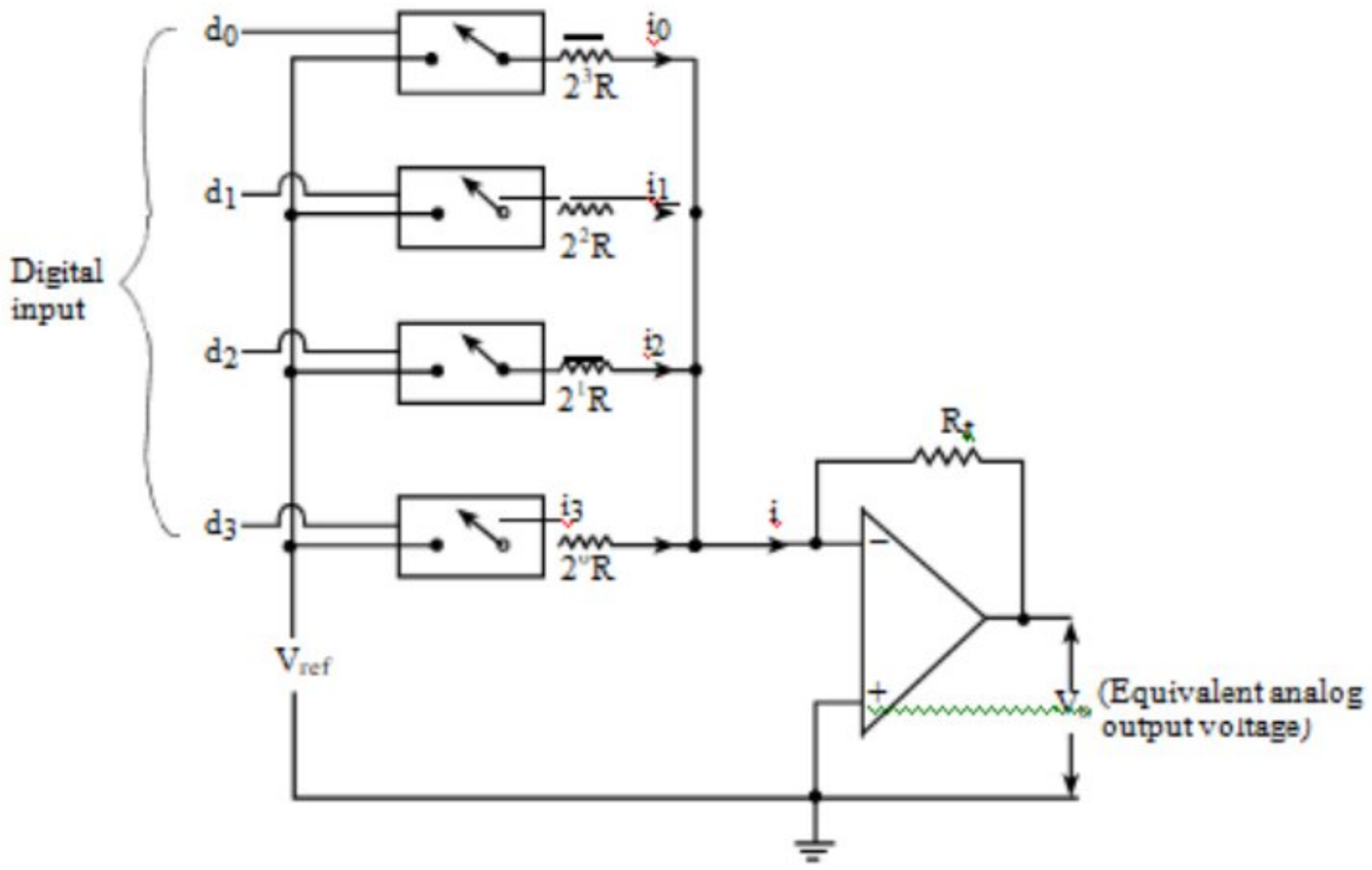


***Figure 5.1** 4-bit WRN DAC*

A reference voltage V_{ref} is applied to all the resistors through the switches. This switch responds to only binary digit 1 i.e., an input of 1001 will close the switch associated with MSB and LSB. For different combination of digital input, analog value of the current is given in Table 5.2.

Table 5.2 Analog value of current for different digital input

Digital input	Analog output (current)
1000	$i_3 = \frac{V_{ref}}{2^0R}$
0100	$i_2 = \frac{V_{ref}}{2^1R}$
0010	$i_1 = \frac{V_{ref}}{2^2R}$
0001	$i_0 = \frac{V_{ref}}{2^3R}$

If all the bits of digital input are high i.e., input = 1111, then the resultant current can be obtained by superimposing all the results given in the above table.

$i = i_3 + i_2 + i_1 + i_0$

or, $i = \frac{V_{ref}}{2^0R} + \frac{V_{ref}}{2^1R} + \frac{V_{ref}}{2^2R} + \frac{V_{ref}}{2^3R}$

If all the bits of digital input are high i.e., input = 1111, then the resultant current can be obtained by superimposing all the results given in the above table.

$i = i_3 + i_2 + i_1 + i_0$

$$\text{or, } i = \frac{V_{ref}}{2^0R} + \frac{V_{ref}}{2^1R} + \frac{V_{ref}}{2^2R} + \frac{V_{ref}}{2^3R}$$

$$\text{or, } i = \frac{V_{ref}}{R}\left[1\times 2^0 + 1\times 2^{-1} + 1\times 2^{-2} + 1\times 2^{-3}\right]$$

$$\text{or, } i = \frac{V_{ref}}{R}\left[d_3 2^0 + d_2 2^{-1} + d_1 2^{-2} + d_0 2^{-3}\right]$$

$$\text{or, } i = \frac{V_{ref}}{2^3R}\left[d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0\right]$$

Thus, for an n-bit converter, the resultant current is given by

$$i = \frac{V_{ref}}{2^{(n-1)}R}\left[d_{(n-1)}2^{(n-1)} + d_{(n-2)}2^{(n-2)} + \ldots\ldots + d_0 2^0\right]$$

Equivalent analog output voltage is given by

$V_o = -\,i\,R_f$

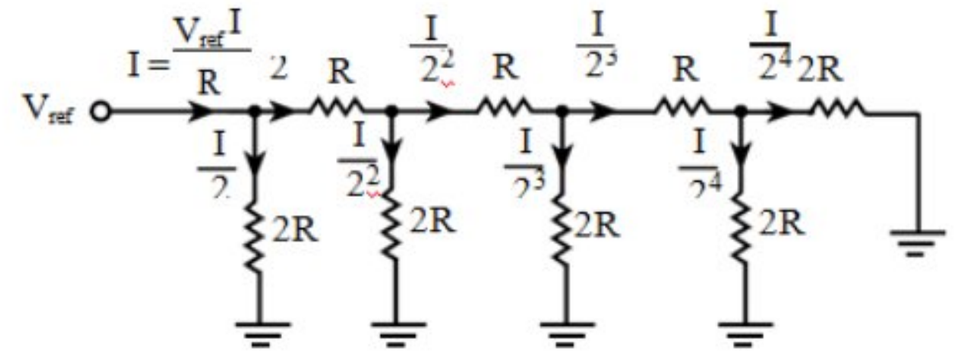
$$\therefore V_o = \frac{-V_{ref}R_f}{2^{(n-1)}R}\left[d_{(n-1)}2^{(n-1)} + d_{(n-2)}2^{(n-2)} + \ldots\ldots + d_1 2^1 + d_0 2^0\right]$$

Drawbacks of the WRN network DAC:

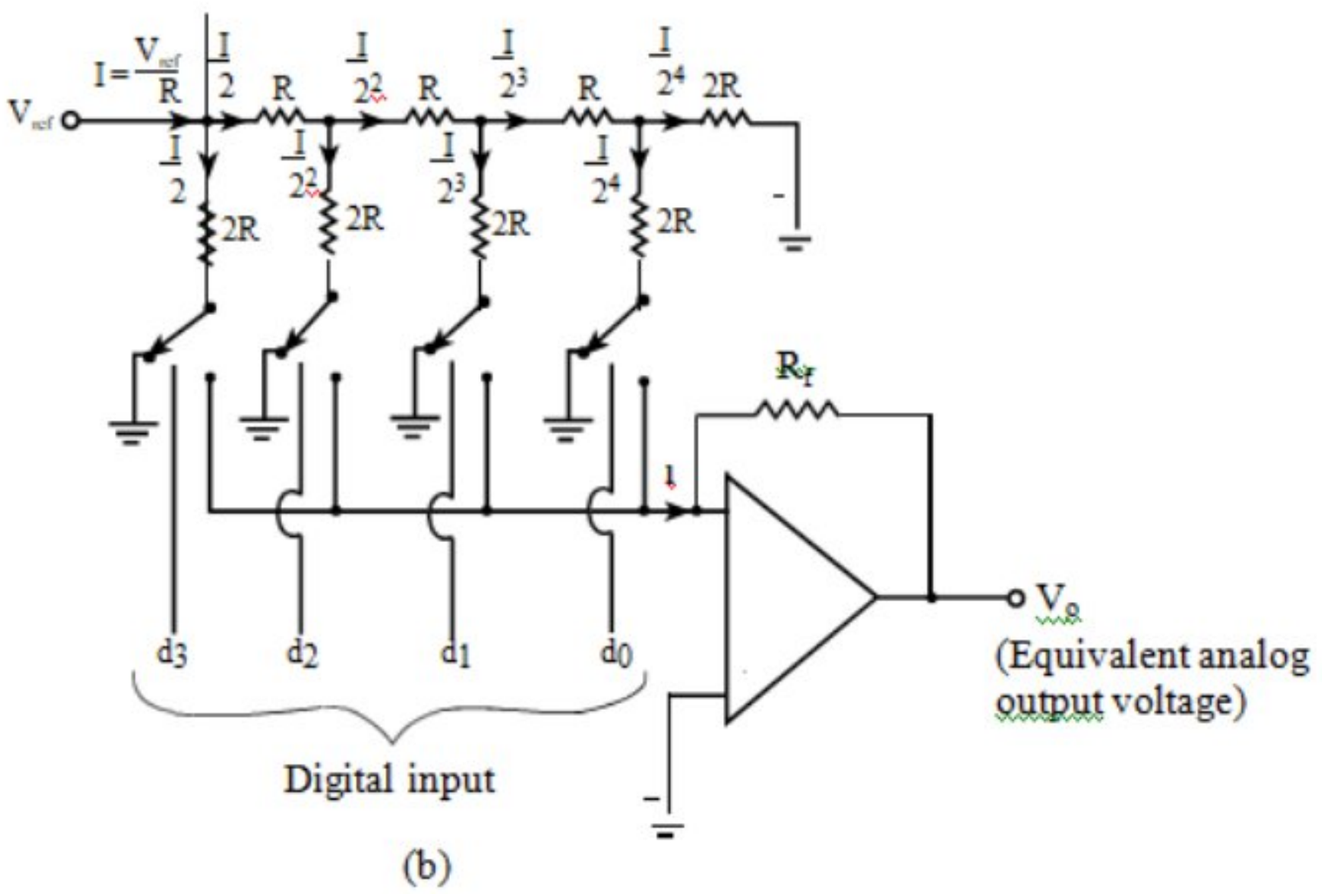
1. As the no. of bit increases, the resistance value also increases. Thus, for higher bit converter, the range of resistor becomes very high and it becomes difficult to fabricate all the resistors in the same IC.
2. For higher bit converter, the tolerance value of resistance in LSB becomes much greater than actual value in the MSB.

R:2R Ladder Network DAC

- The two drawbacks of weighted resistor network can be overcome using R:2R ladder network, as in this DAC, only two value resistors are used.



(a)



(b)

Figure 5.2 *(a) Resistive ladder network (b) 4-bit R:2R ladder network digital to analog converter.*

- Right hand side of each node of Figure 5.2 (a) has two equal resistors each having resistance 2R connected in parallel. So, the current reaching to any node will be divided into two equal parts. The current will be divided according to the expression below.

- Thus, the resistive ladder network of Figure 5.2 (a) generates a binary sequence of the current. If all the bits of digital inputs of Figure 5.2 (b) are high i.e., input equals 1111, then the resultant current is given by

$$i = \frac{I}{2^1} + \frac{I}{2^2} + \frac{I}{2^3} + \frac{I}{2^4}$$

$$\text{or, } i = I\,(1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 1\times2^{-4})$$

$$\text{or, } i = \frac{V_{ref}}{R}\,[\,1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}\,]$$

$$\text{or, } i = \frac{V_{ref}}{R}\,[d_3 2^{-1} + d_2 2^{-2} + d_1 2^{-3} + d_0 2^{-4}]$$

$$\text{or, } i = \frac{V_{ref}}{2^4 R}\,[d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0]$$

For an n-bit system,

$$i = \frac{V_{ref}}{2^n R}\,[d_{(n-1)}\,2^{(n-1)} + d_{(n-2)}\,2^{(n-2)} + \ldots\ldots\ldots + d_1 2^1 + d_0 2^0]$$

Thus, equivalent analog output voltage is given by

$$V_o = -\,i\,R_f$$

$$\therefore\ V_o = \frac{-V_{ref} R_f}{2^n R}\,[d_{(n-1)}2^{(n-1)} + d_{(n-2)}2^{(n-2)} + \ldots\ldots\ldots + d_1 2^1 + d_0 2^0]$$

Analog to Digital Converter (ADC)

Analog to digital converters are of following types:

1. Successive Approximation (SA) ADC
2. Ramp ADC
3. Dual Ramp ADC (Dual Slope ADC)
4. Flash ADC (or Parallel ADC)

Successive Approximation (SA) ADC:

- Successive approximation ADC is probably the most commonly used analog-to-digital converter.
- This method is based on comparing the input analog voltage with another analog voltage until the two are equal or as close as it is possible to set them.
- Figure 5.3 illustrates the subsystems involved.

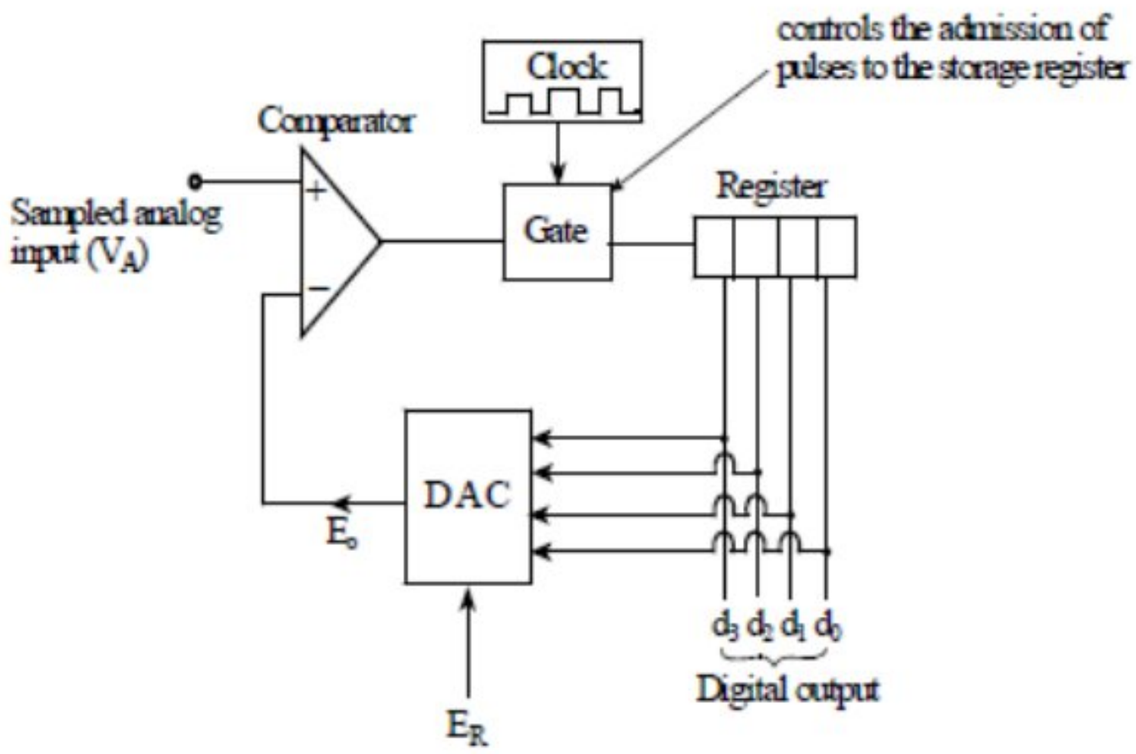


Figure 5.3 4-bit successive approximation ADC

$$E_o = \frac{E_R}{2^n}\,(d_{n-1}2^{n-1} + \ldots\ldots\ldots + d_0 2^0)$$

$$E_o = \frac{E_R}{2^4}\,(d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0)$$

1st approximation:

Input to DAC = 1000

Output from DAC = $E_o = \frac{8}{16} E_R$

If $E_o < V_A$, then, the comparator output will be high and the gate opens. So, the bit d_3 remains at 1 and next bit d_2 is set to 1.

2rd approximation:

Input to DAC = 1100

Output from DAC = $E_o = \frac{12}{16} E_R$

If $E_o > V_A$, then, the comparator output will be low and the gate closes. So, the bit d_2 is reset to 0 and next bit d_1 is set to 1.

3rd approximation:

Input to DAC = 1010

Output from DAC = $E_o = \frac{10}{16} E_R$

If $E_o < V_A$, then, the comparator output will be high and the gate opens. So, the bit d_1 remains at 1 and next bit d_0 is set to 1.

4th approximation:

Input to DAC = 1011

Output from DAC = $E_o = \frac{11}{16} E_R$

If $E_o > V_A$, then, the comparator output will be low and the gate closes. So, the bit d_0 is reset to 0. The nearest digital output for analog input will be 1010.

The flowchart of successive approximation ADC is shown below.

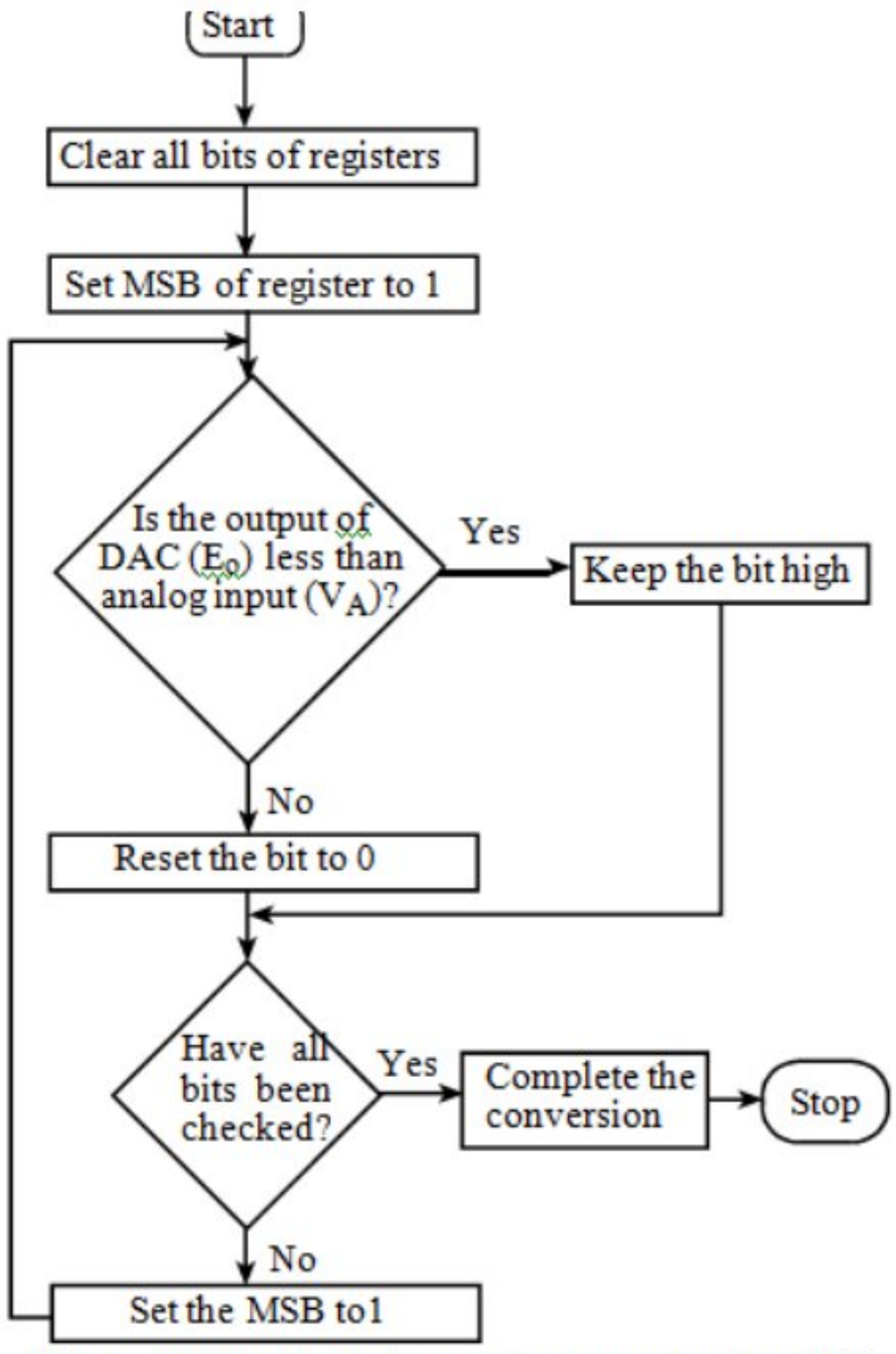


Figure 5.4 *Flowchart of successive approximation ADC*

- Successive approximation principle can be easily understood using a simple example; the determination of the weight of an object.
- By using a balance and placing the object on one side and an approximate weight on the other side, the weight of the object is determined.
- If the weight placed is more than the unknown weight, the weight is removed and another weight of smaller value is placed and again the measurement is performed.
- Now if it is found that the weight placed is less than that of the object, another weight of smaller value is added to the weight already present, and the measurement is performed.
- If it is found to be greater than the unknown weight, the added weight is removed and another weight of smaller value is
  added.
- In this manner by adding and removing the appropriate weight, the weight of the unknown object is determined.

Ramp ADC

- The *ramp* form of analog-to-digital converter involves an analog voltage which is increased at a constant rate, a so-called ramp voltage.
- This ramp voltage is generated by a capacitor being charged from a constant current source.
- The time taken for the ramp voltage to increase to the value of the input analog voltage will depend on the size of the sampled analog voltage.
- Figure 5.5 indicates the subsystems involved in the ramp form of analog-to-digital converter. Ramp ADCs are cheap but relatively slow.

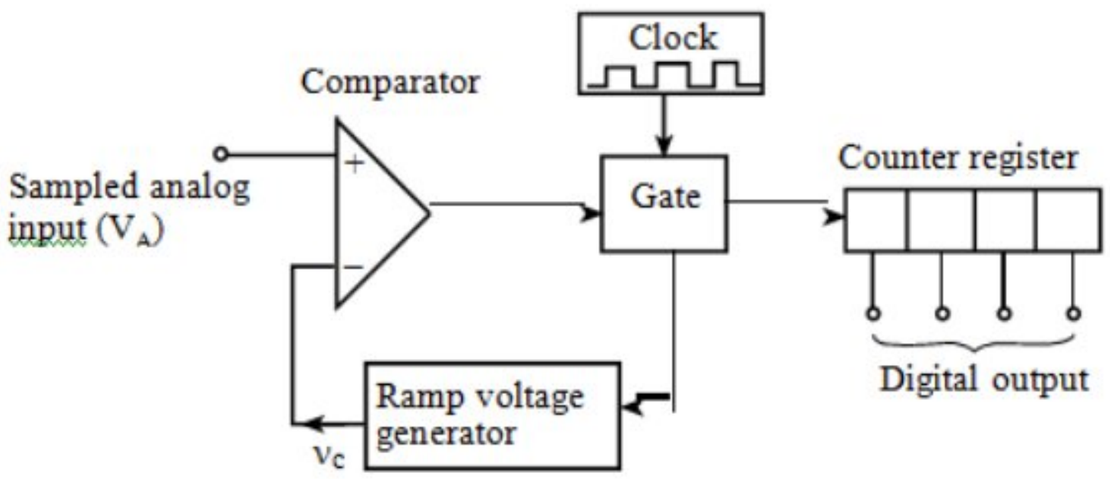


***Figure 5.5** Ramp ADC*

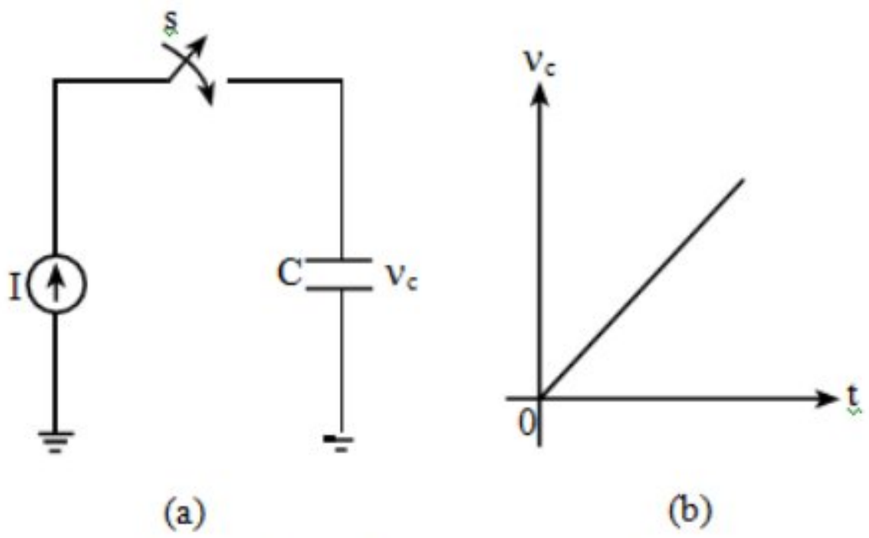


***Figure 5.6** (a) Ramp generator (b) ramp voltage*

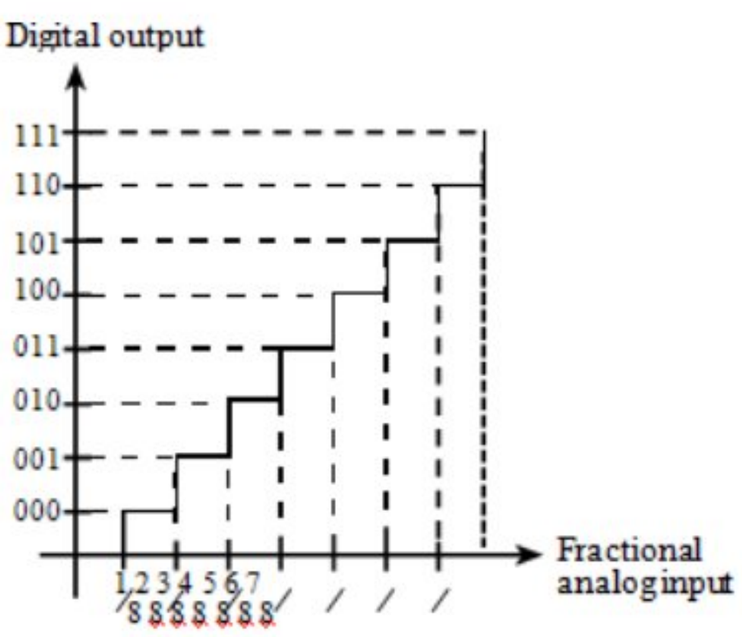


***Figure 5.7** 3-bit digital output*

Dual Ramp ADC (Dual Slope ADC)

- The accuracy of the single ramp ADC can be improved by using the *dual ramp ADC*.

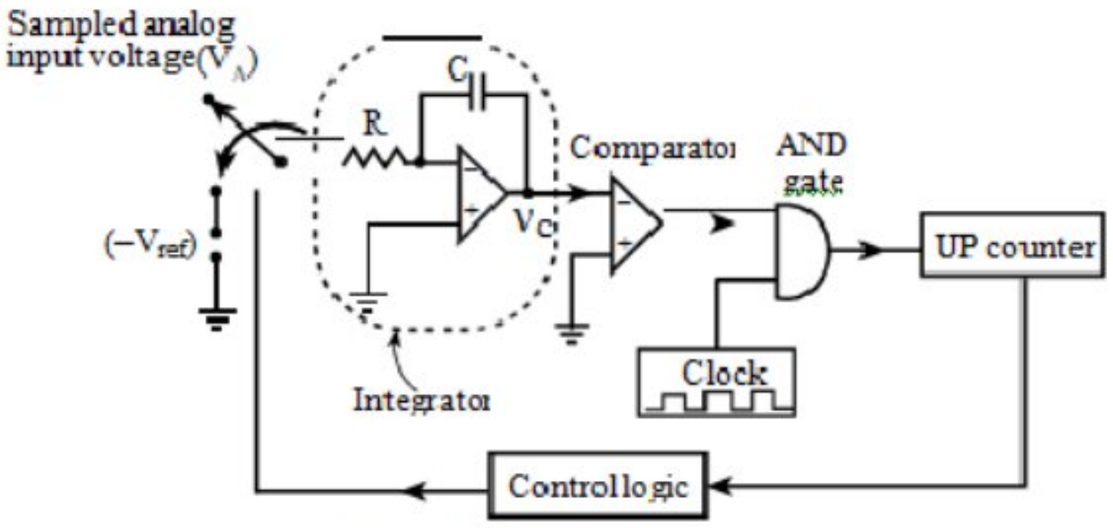


Figure 5.8 *Dual ramp ADC*

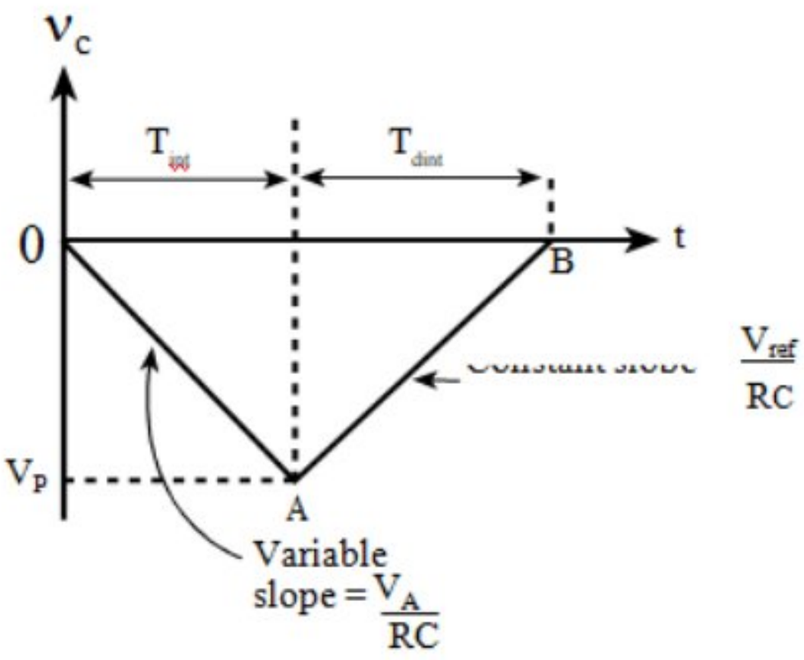
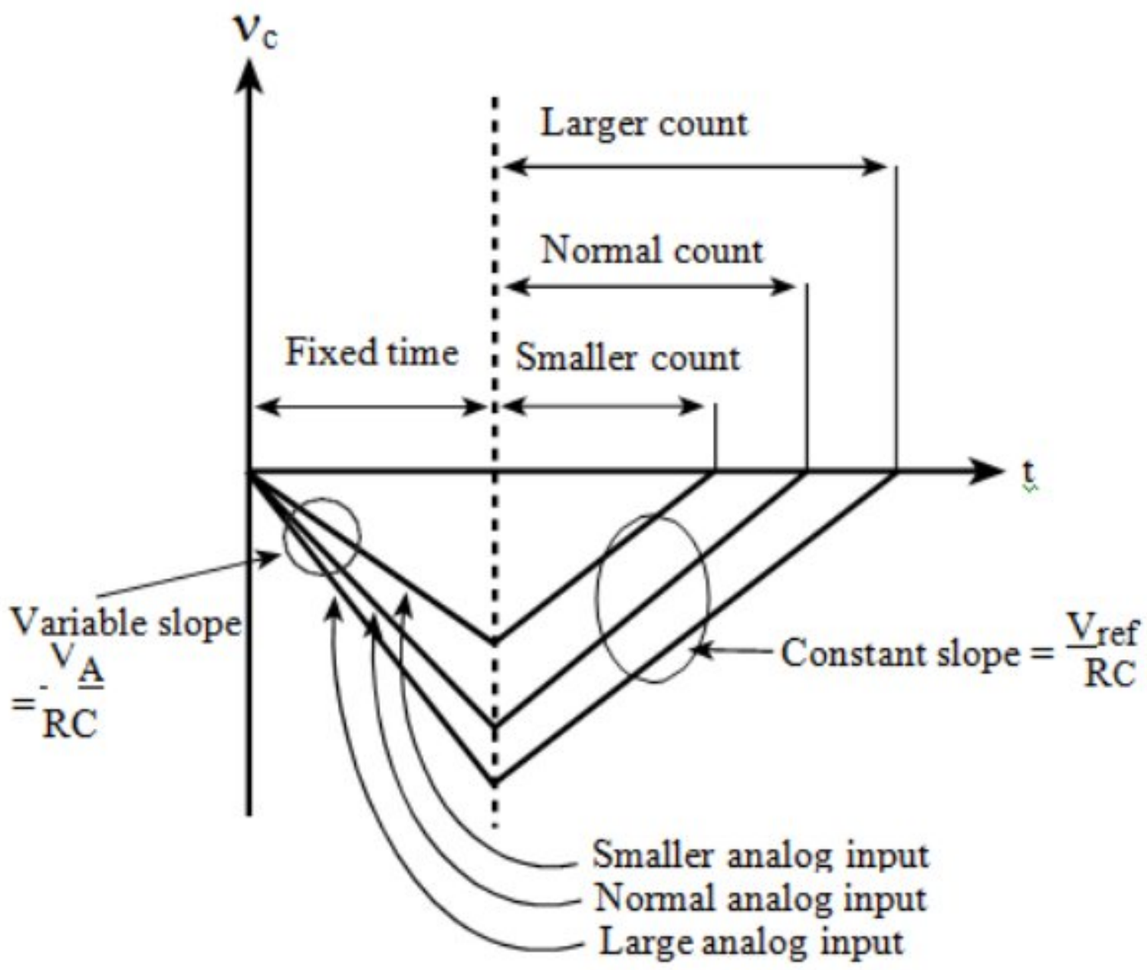


Figure 5.9 *Variation of voltage across capacitor with time in dual ramp ADC.*



(a)

- Figure 5.8 shows the different components of dual ramp ADC.
- It consists of an integrator which produces a ramp signal (n_c) from constant sampled analog input (V_A).
- Then, there is a comparator to drive the AND gate whose another input is clock pulse of certain frequency.
- The gate drives an up counter which on certain condition sends the signal to control logic to switch the input from V_A to $-V_{ref}$. When V_A is a applied to the integrator, it produces a ramp signal whose slope is equal to
- Then, the gate opens.

Considering Figure 5.9 (b), the slope of line OA is given by

$$\frac{V_P}{T_{int}} = \frac{V_A}{RC} \qquad \text{.....(1)}$$

The slope of line AB is given by

$$\frac{V_P}{T_{dint}} = \frac{V_{ref}}{RC} \qquad \text{.....(2)}$$

Dividing equation (1) by (2) gives

$$\frac{T_{dint}}{T_{int}} = \frac{V_A}{V_{ref}}$$

$$\text{or, } T_{dint} = \frac{V_A}{V_{ref}} T_{int} \qquad \text{.....(3)}$$

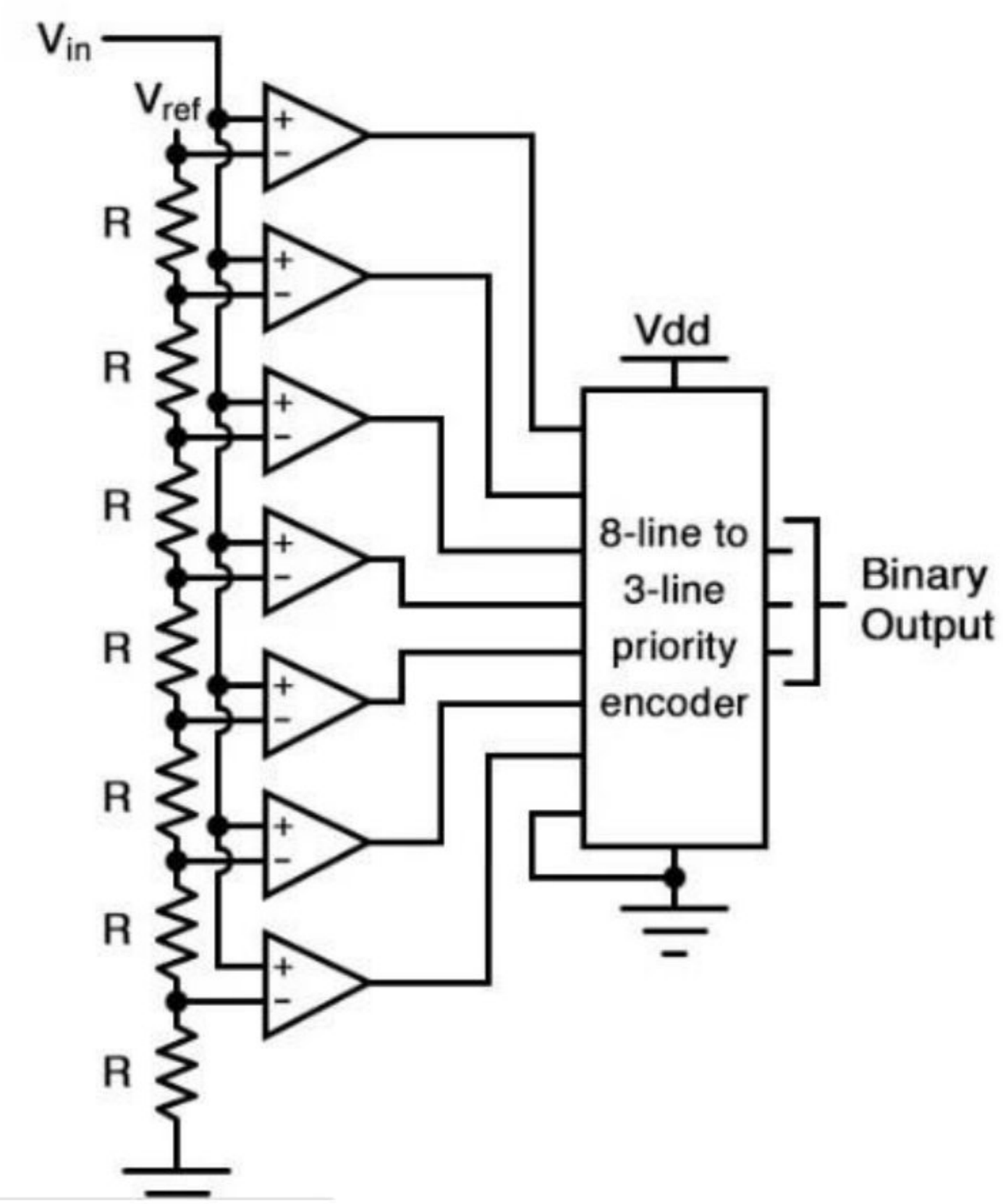
Total conversion time is given by

$$T_c = T_{int} + T_{dint}$$

$$\text{or, } T_c = T_{int} + \frac{V_A}{V_{ref}} T_{int}$$

$$\therefore T_c = T_{int}\left(1 + \frac{V_A}{V_{ref}}\right)$$

Flash ADC



- The flash analog-to-digital converter is a very fast, but more costly form of ADC.
- For an n-bit converter, 2^n -1 separate voltage comparators are used in parallel as shown in Figure