Design and Analysis of High swing Cascode Current Mirror

By – Pranjal Upadhyay
MTech-MVLSI
SR No.- 25912

GitHub project link : https://github.com/pranizuky-ux/High_swing_cascode_current_mirror

Node : 180 nm
VDD=1.8V

Design a high-swing current mirror using `pmos` transistor cells from the `gpdk180` library with $I_{ref} = 10\mu A$ and $I_{out} = 50\mu A$. Use V_{od} = 200mV for the mirror device M_1 and M_2. Use V_{od} = 50mV for the cascode devices M_3 and M_4.

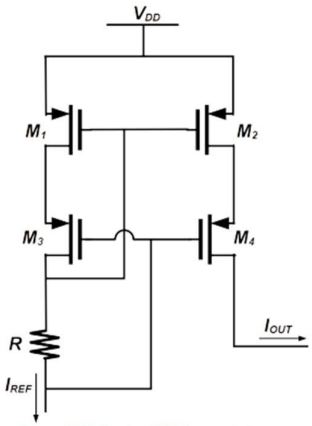


Figure 2: High swing PMOS current mirror

Characterize the following:

a. Perform a DC operating point simulation with $V_{out} = VDD/2$ at room temperature. Annotate the DC operating voltages. Calculate output impedance R_{out} from the DC operating point of the devices.

b. Output current vs. output voltage using a DC sweep of V_{out}. Plot I_{out} vs V_{out}. Calculate R_{out} from the I_{out} vs. V_{out} curve. Plot % error with respect to the ideal output vs. V_{out}.

c. Characterize output impedance R_{out} for $V_{out} = VDD/2$ using AC simulation. Compare with a) and b).

d. Perform a temperature sweep from -50C to 150C for $V_{out} = VDD/2$ and plot % error vs. temperature.

Design Procedure:

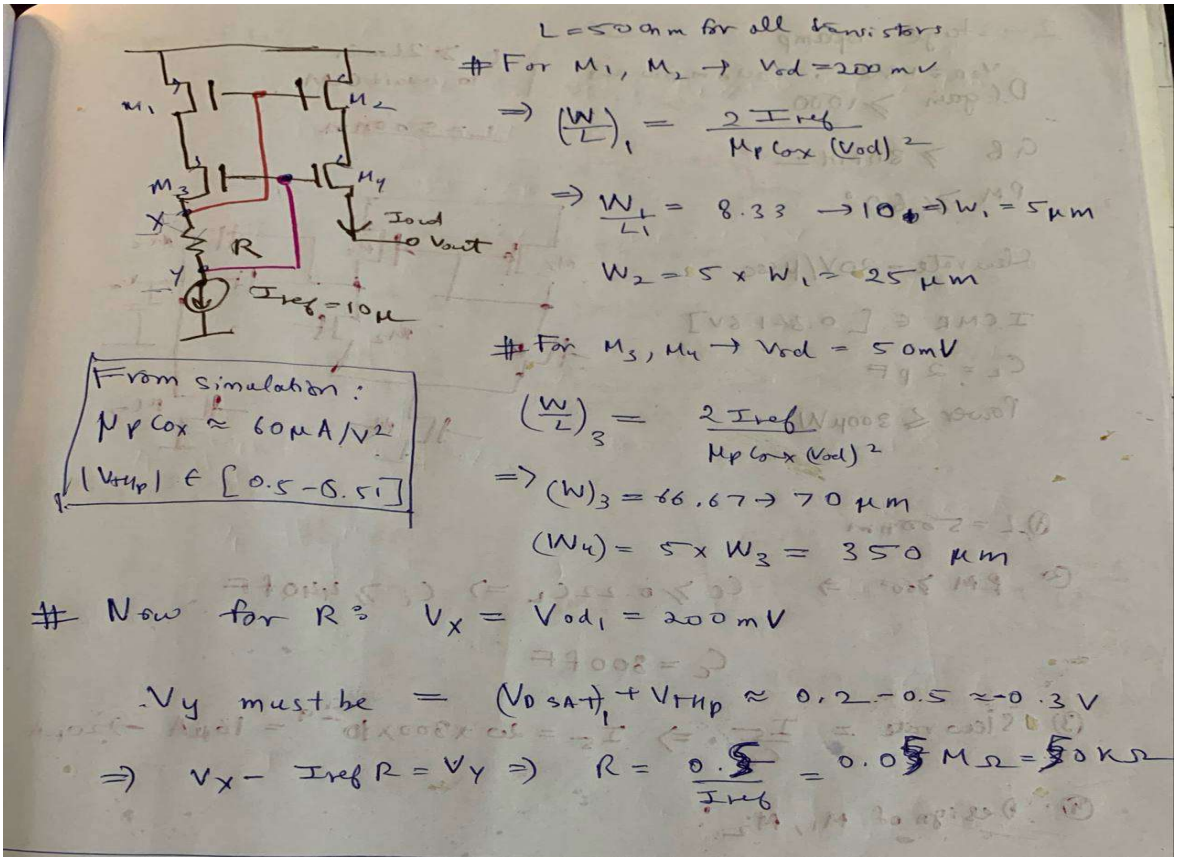
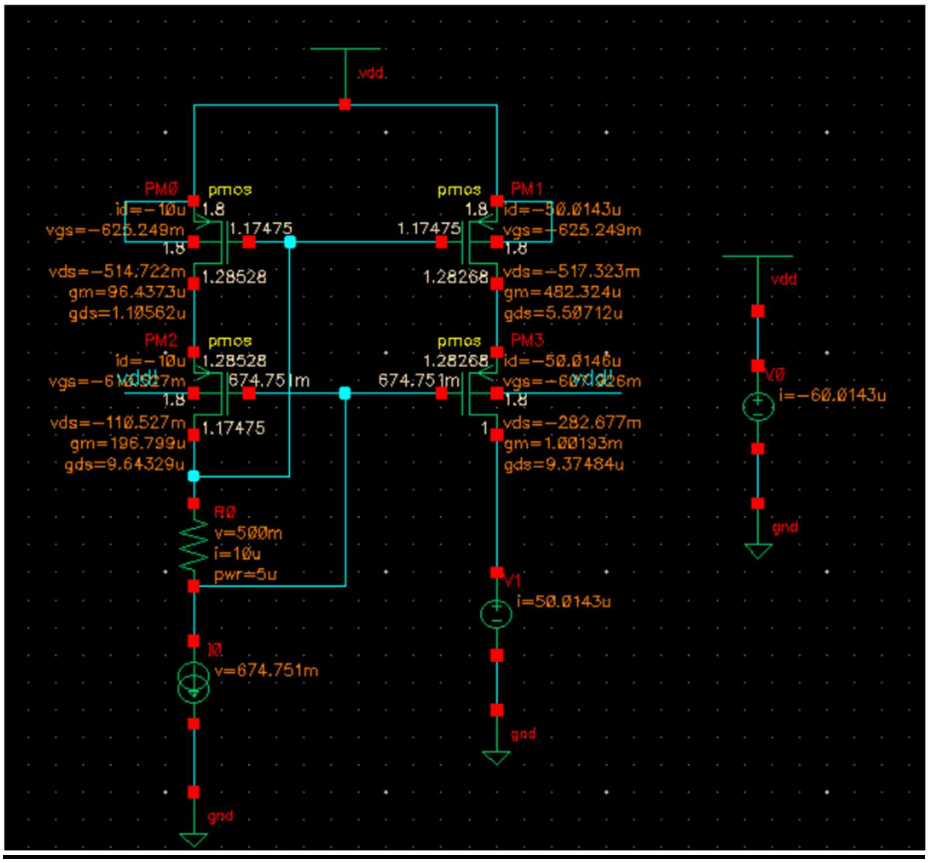


Table listing Mosfet sizing and R value:

M1	W = 5um	L = 500nm
M2	W = 25um	L = 500nm
M3	W = 70um	L = 500nm
M4	W=350um	L = 250nm
R	50kohm	-

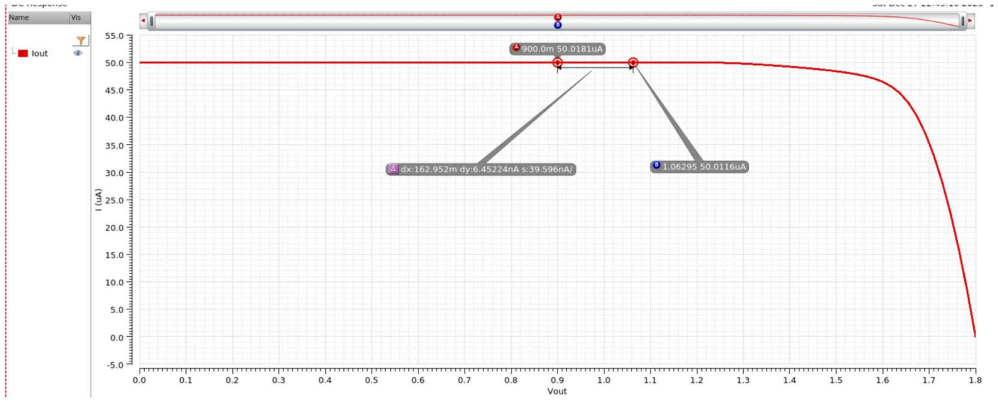
a)DC Analysis and Schematic:

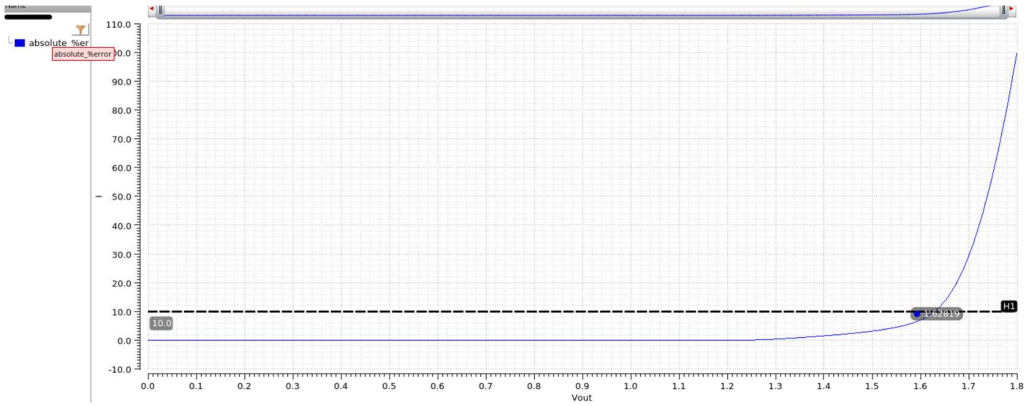


Rout=(1/gds4)+(1/gds2)+(gm4) (1/gds4)(1/gds2)=19.6Mohm

b) Iout vs Vout and Rout inference

from graph Rout approximately equals 28Mohm





The simulation shows that error is within 10 percent for Vout=1.62V

c) AC Simulation:

Source used for ac analysis: frequency = 1kHz

Vrms = 1mV

Current obtained = Irms = 48.6 pA

Rout = Vrms/ Irms = 100mV/ 48.6 pA =20.57Mohm

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d)%absolute error vs temperature