

Design and Stability Analysis of Two-Stage CMOS Opamp



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GitHub project link : https://github.com/pranizuky-ux/Two_stage_opamp

i) Phase Margin $\geq 60^\circ \Rightarrow C_c \geq 0.22 C_L$
 $\Rightarrow C_c \geq 440 \text{ fF}$
 I started with $C_c = 800 \text{ fF}$ (with simulation $C_c = 1 \text{ pF}$ for optimal PM)

ii) Slewrate $= 20 \text{ V}/\mu\text{s} = \frac{I_{\text{bias}}}{C_c}$
 $\Rightarrow I_{\text{bias}} = 20 \times 800 \times 10^{-9} = 16 \mu\text{A}$
 To account for inaccuracy due to square law model, $I_{\text{bias}} = 20 \mu\text{A}$

iii) Design of M_1, M_2 :
 $G_B = \frac{g_{m1}}{2\pi \times C_c} \Rightarrow g_{m1} = 150.79 \mu\text{A} \rightarrow 160 \mu\text{A}$
 $\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1}^2}{2\mu_n C_{ox} (I_{\text{bias}}/2)} \approx 4.22 \rightarrow 6$

again by simulation:
 $V_{\text{tran}} \in [0.47 - 0.58]$
 $V_{\text{thp}} \in [0.501 - 5.10 \text{ V}]$

iv) Design of M_3, M_4 :
 Let's assume $\rightarrow I_{\text{CMR}} \in [0.2 - 1.6 \text{ V}]$
 $\Rightarrow I_{\text{CMR}}^+ < V_{DD} - V_{\text{thp}} \left(\frac{I_{\text{bias}}}{2} \right) + V_{\text{thp}} \min$
 $\Rightarrow \left(\frac{W}{L}\right)_{3,4} \geq 13.1 \dots \rightarrow \left(\frac{W}{L}\right)_{3,4} = 14$

v) Design of M_5, M_6 :
 $I_{\text{CMR}}^- \geq V_{\text{thp}} \left(\frac{I_{\text{bias}}}{2} \right) + V_{\text{thp}} \max$
 $\rightarrow \left(\frac{W}{L}\right)_5 \leq 12.09 \rightarrow \left(\frac{W}{L}\right)_5 = 12 = \left(\frac{W}{L}\right)_2$

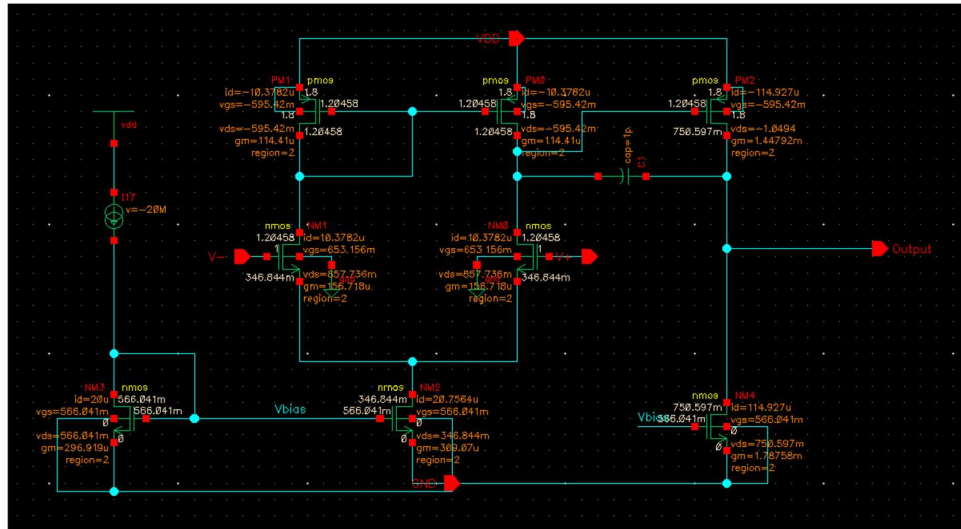
vi) Design of M_7 :
 for PM $\geq 60^\circ \rightarrow g_{m6} \geq 10 g_{m1} \rightarrow g_{m6} = 1600$
 also by design, it's fixed that
 $\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{I_6}{I_4} \Rightarrow \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{g_{m6}}{g_{m4}} \left[g_{m4} = 130 \mu\text{A} \right]$
 $\rightarrow \frac{g_{m6}}{g_{m4}} \times \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_6 = 173 \rightarrow 174$

vii) $\frac{I_6}{I_4} = \frac{174}{14} \Rightarrow I_6 \approx 125 \mu\text{A} \& \left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5} \times \left(\frac{W}{L}\right)_5$
 $\Rightarrow \left(\frac{W}{L}\right)_7 = 75$

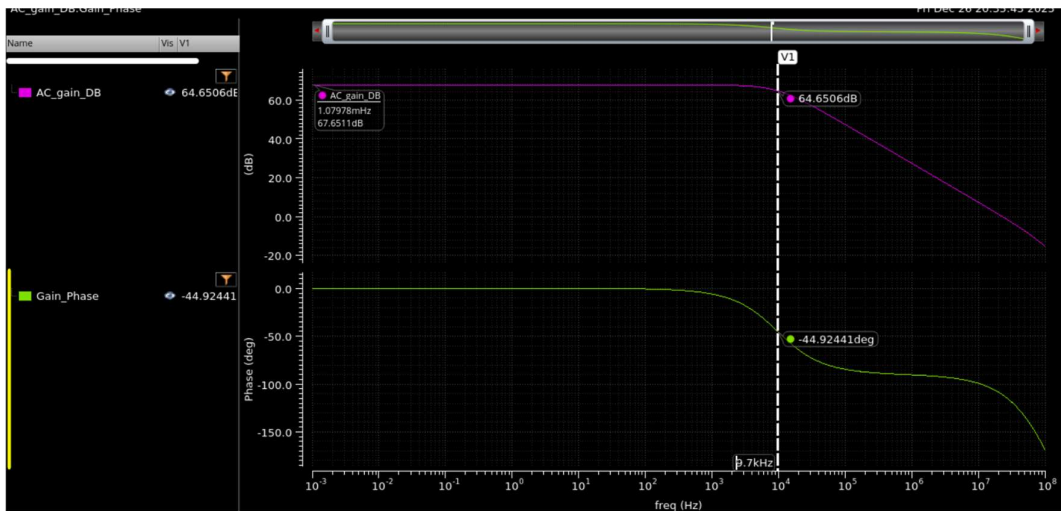
Table listing Mosfet sizing:

M1, M2	W = 3um	L = 500nm
M3, M4	W = 7um	L = 500nm
M5, M8	W = 6um	L = 500nm
M6	W=43.5um	L = 250nm
M7	W=18.75um	L = 250nm

DC Analysis and Schematic:

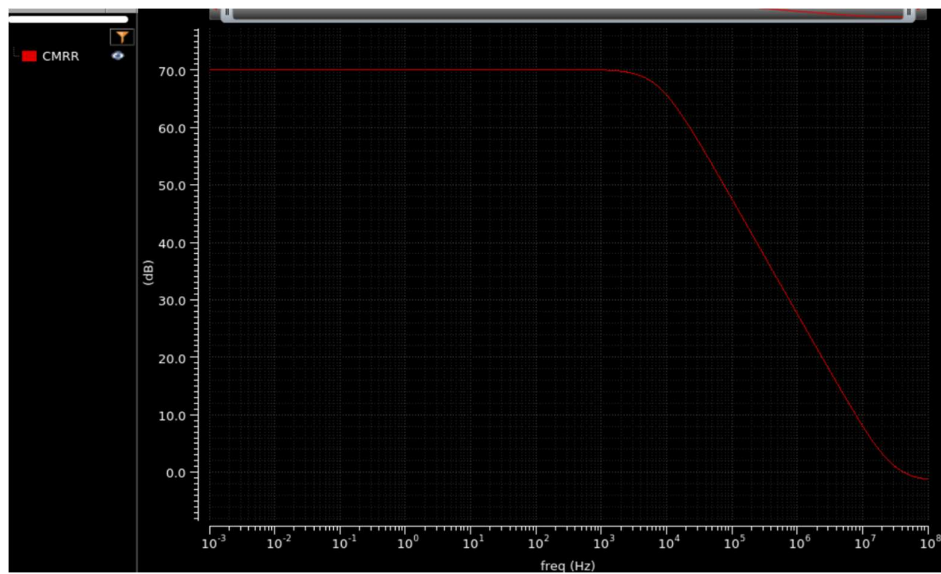


AC analysis

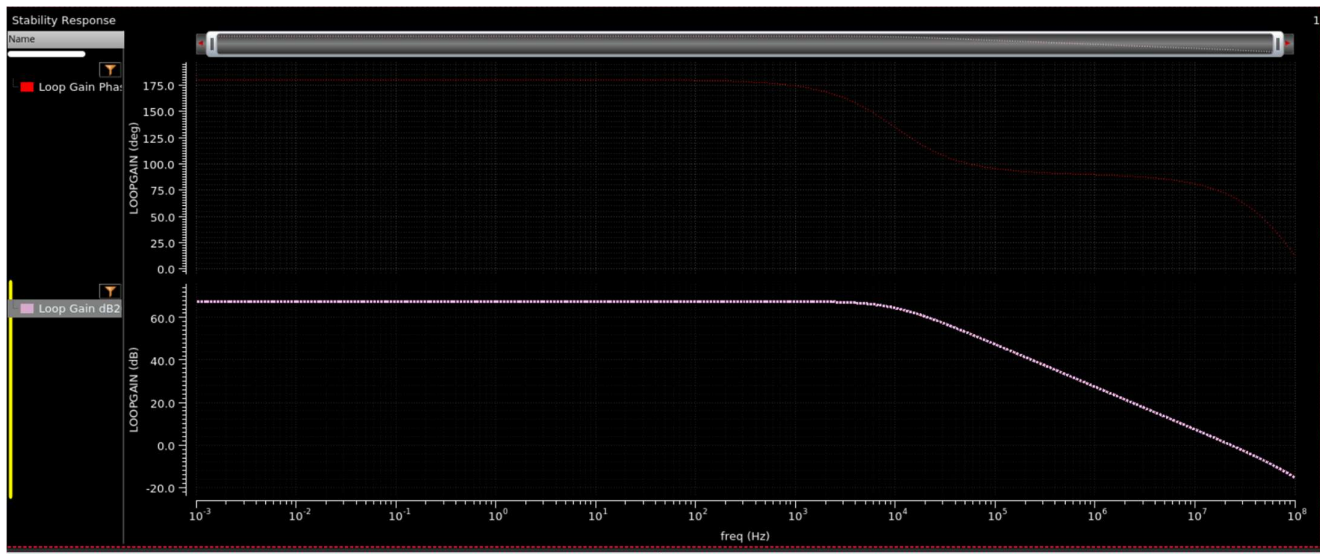


Outputs					
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	AC_gain_DB	wave	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
2	Bandwidth	9.70215K	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
3	Gain_Phase	wave	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
4	UGF	22.944M	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
5	PM	68.9624	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
6	PowerConsumption	255.552u	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

Plot after simulation:



Stability analysis



X
Direct Plot Form@QuClasSIC.c2sCAT1MEITY.ii...
X

Plotting Mode
Append

Analysis

☒ stb

Function

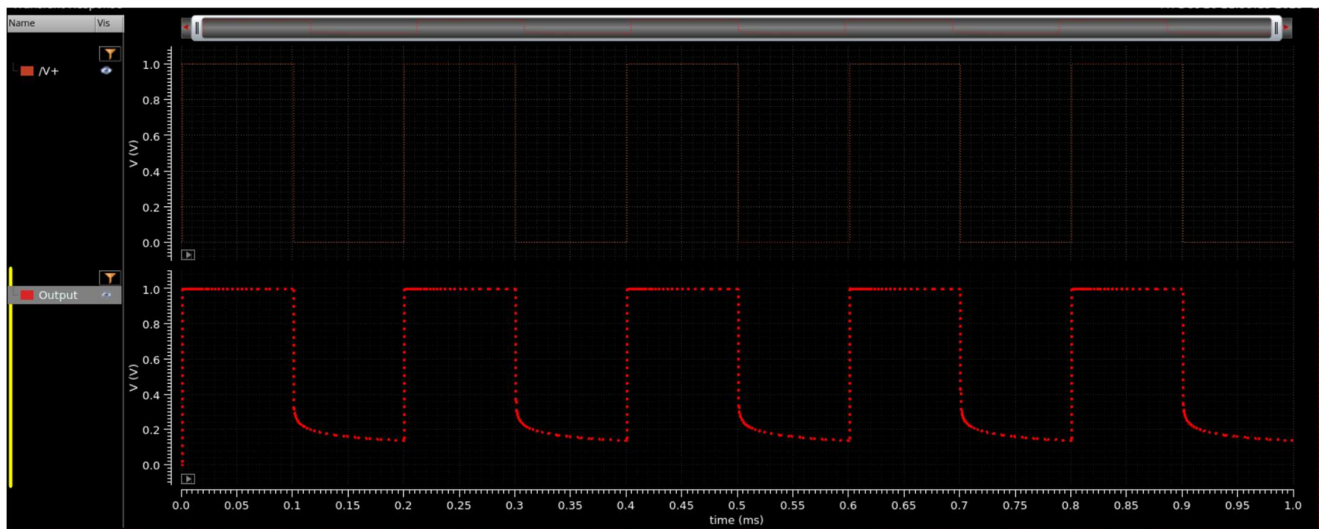
☐ Loop Gain
☒ Stability Summary

☐ Phase Margin
☐ Gain Margin

☐ PM Frequency
☐ GM Frequency

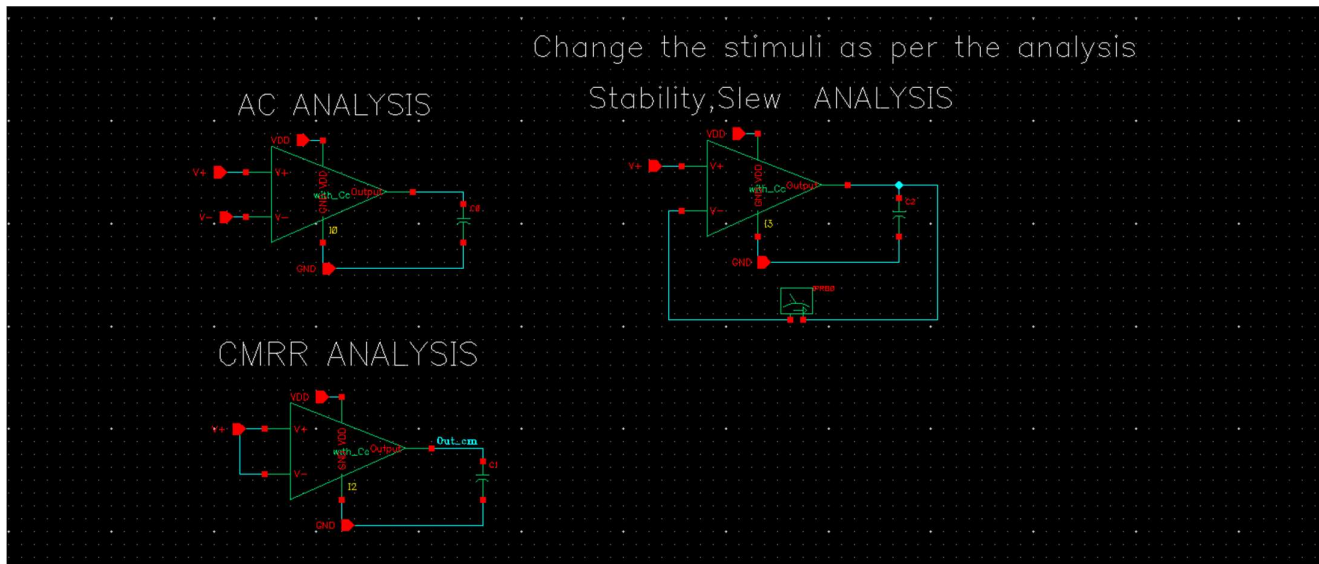
Phase Margin = 69.397 (Deg) @ freq = 22.9338M (Hz)

Transient analysis



6	SlewRate	19.5368M	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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Testbenches:



Finalized Design:

