Design and Stability Analysis of Two-Stage CMOS Opamp

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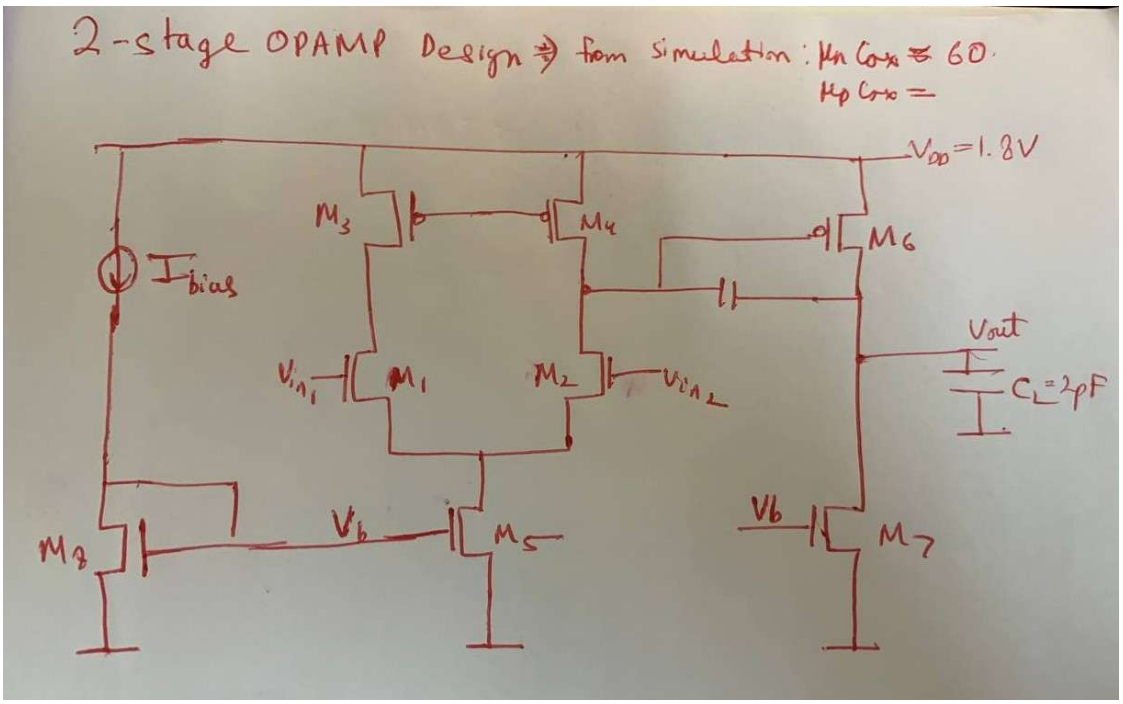
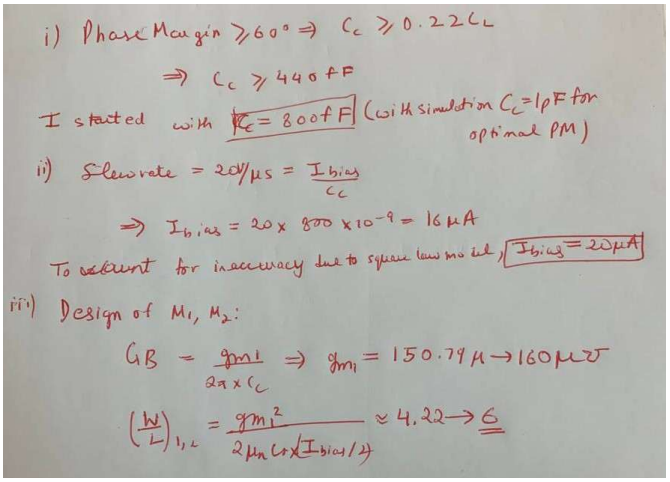
GitHub project link : https://github.com/pranizuky-ux/Two_stage_opamp

Parameter	Specification	Obtained
Open Loop, differential mode, DC Gain	≥ 60 dB	67.65 dB
CMRR	≥ 50 dB	80 dB
Unity Gain Band Width	≥ 20MHz	22.94 MHz
Phase Margin	≥ 60°	69.397°
Slew Rate	20V/µs	19.53V/µs
Power Dissipation	≤ 500 µW	255.552 µW

Node : 180 nm
VDD=1.8V
Load Capacitance= 2pF

Design Procedure:





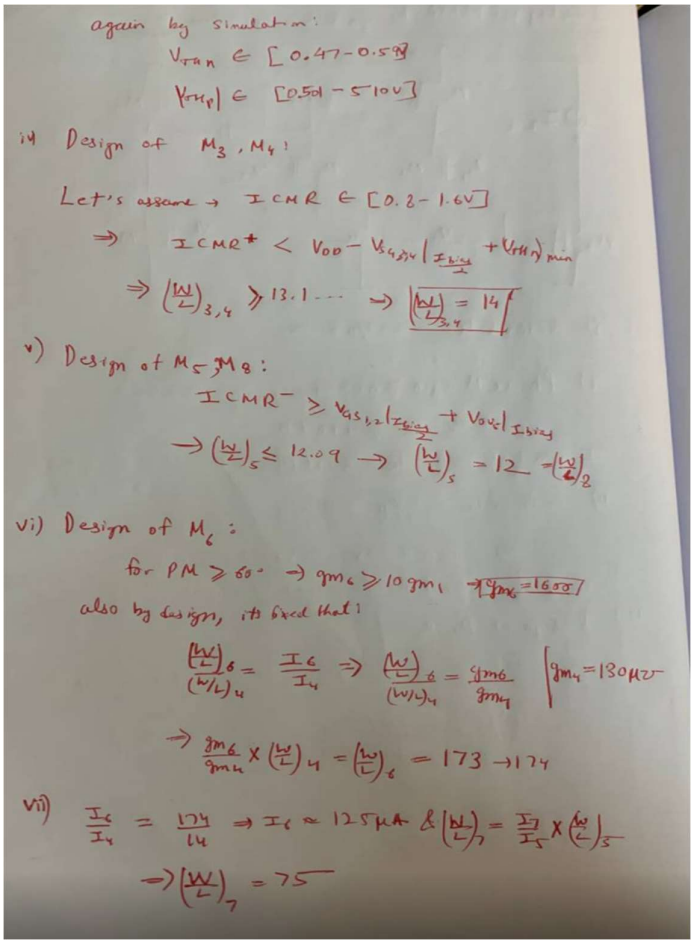
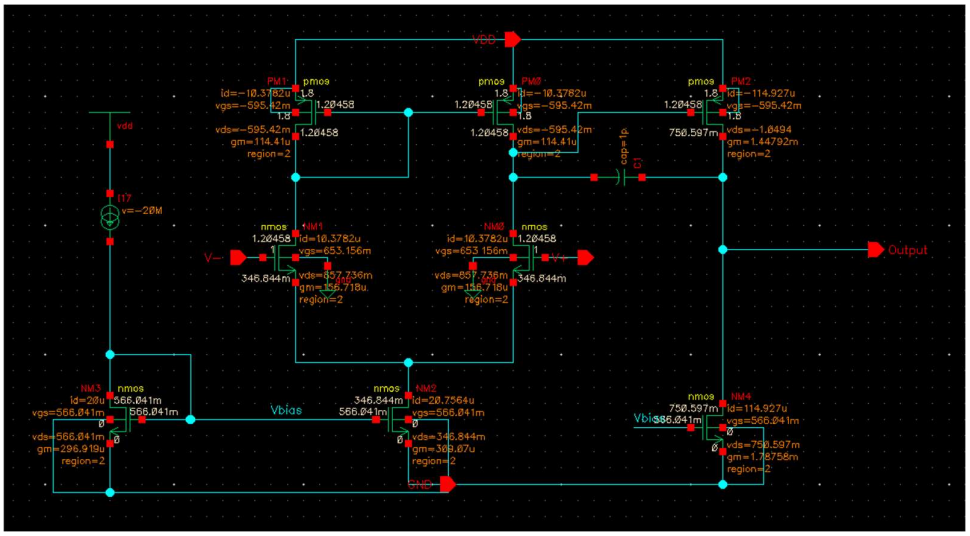


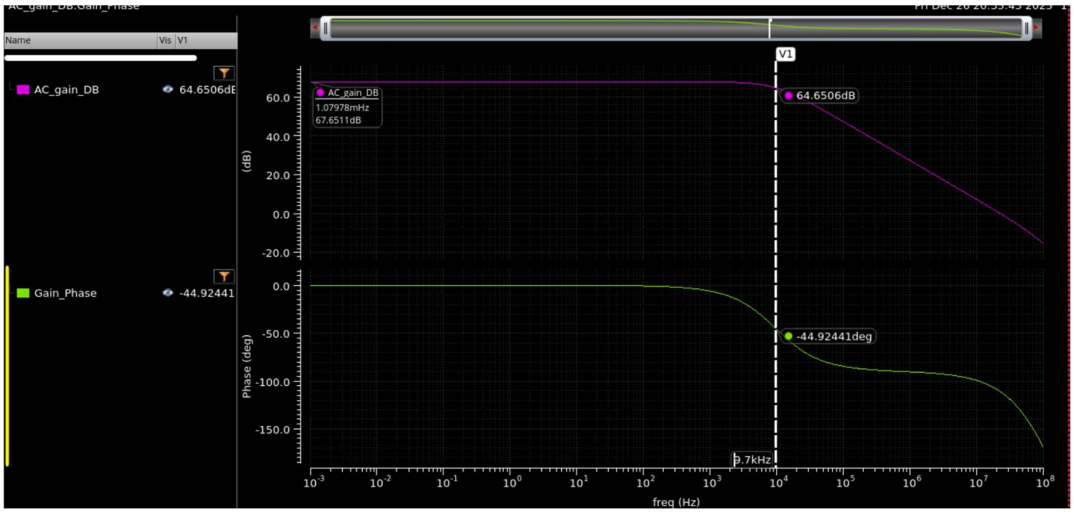
Table listing Mosfet sizing:

M1, M2	W = 3um	L = 500nm
M3, M4	W = 7um	L = 500nm
M5, M8	W = 6um	L = 500nm
M6	W=43.5um	L = 250nm
M7	W=18.75um	L = 250nm

DC Analysis and Schematic:



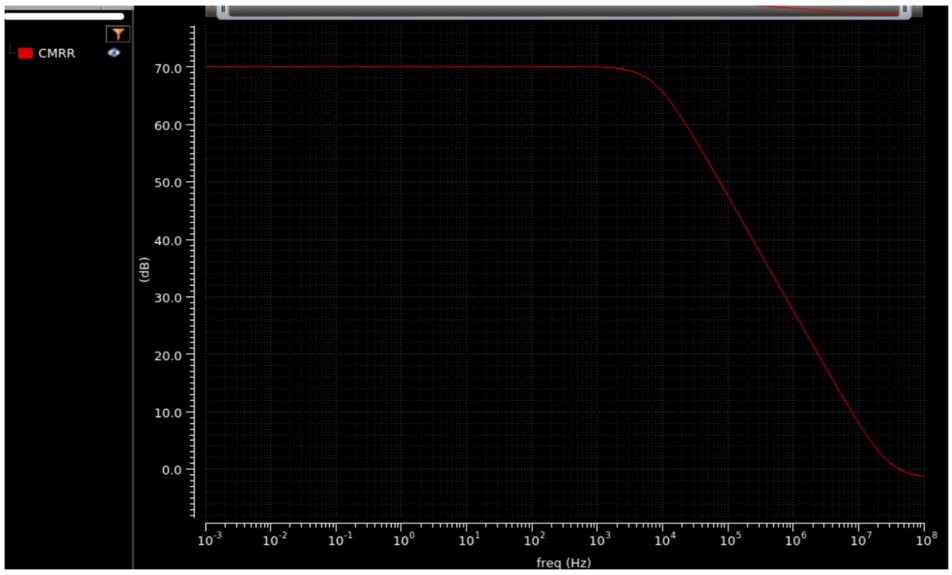
AC analysis



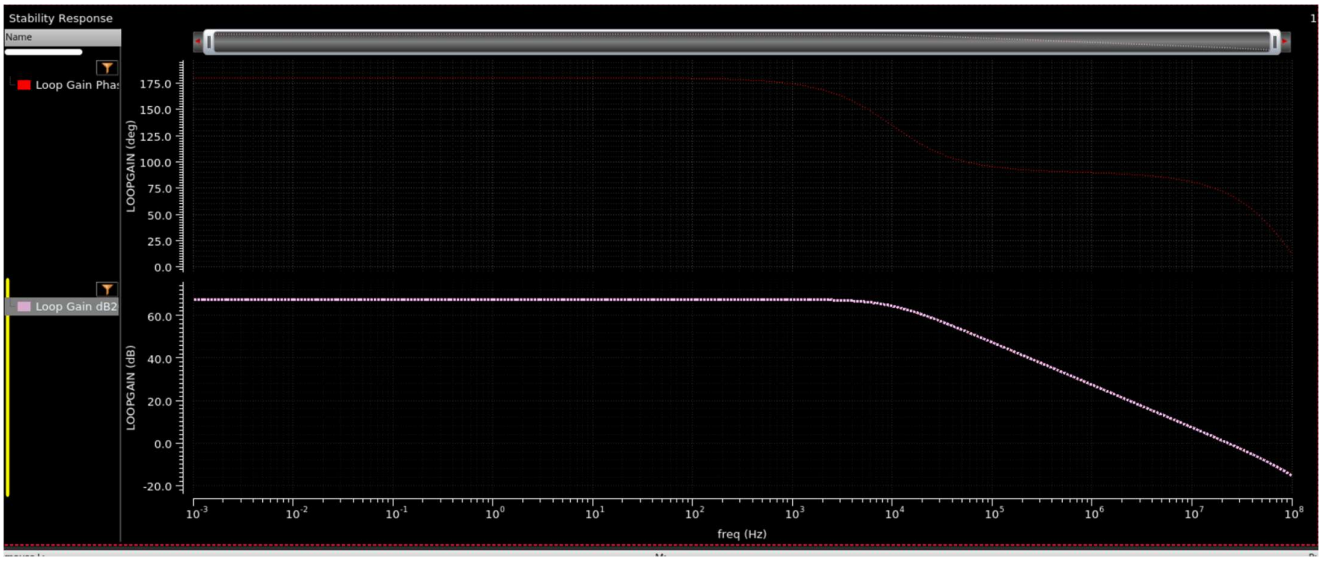
Outputs

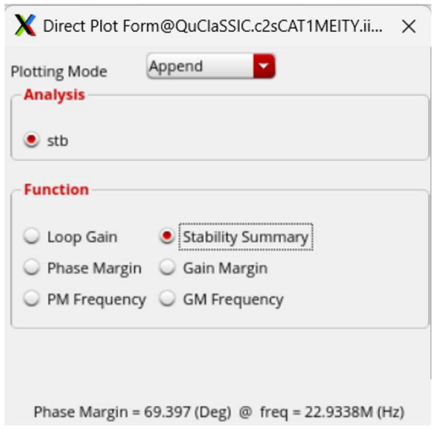
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	AC_gain_DB	wave	☑	☑	
2	Bandwidth	9.70215K	☑	☐	
3	Gain_Phase	wave	☑	☑	
4	UGF	22.944M	☑	☑	
5	PM	68.9624	☑	☑	
6	PowerConsumption	255.552u	☑	☑	

Plot after simulation: Auto Plotting mode: Replace

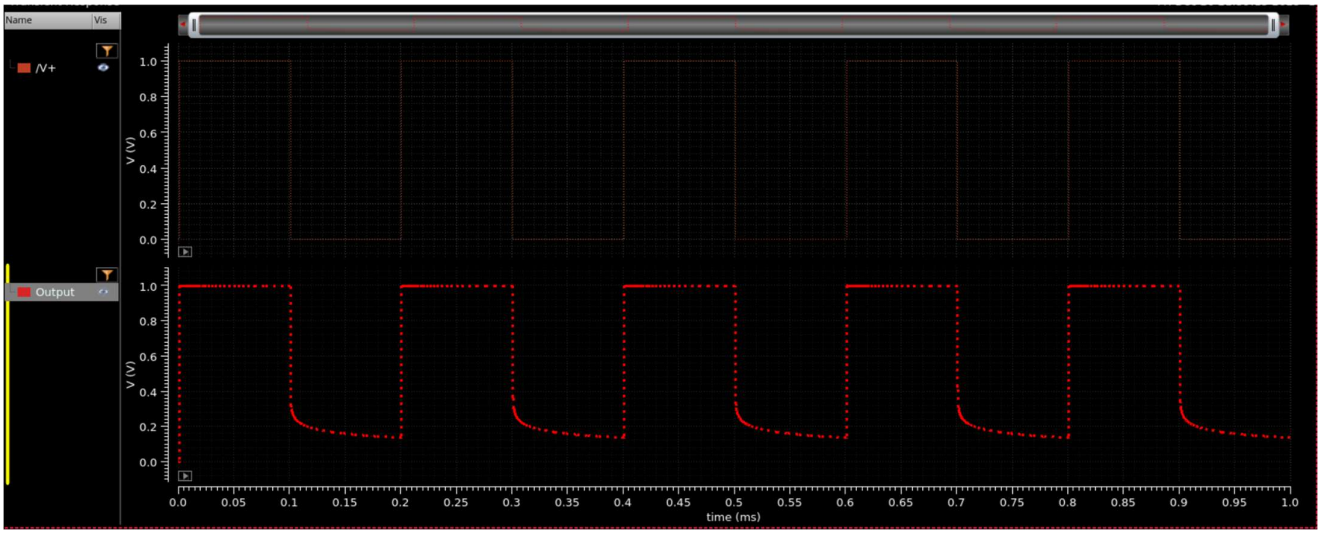


Stability analysis

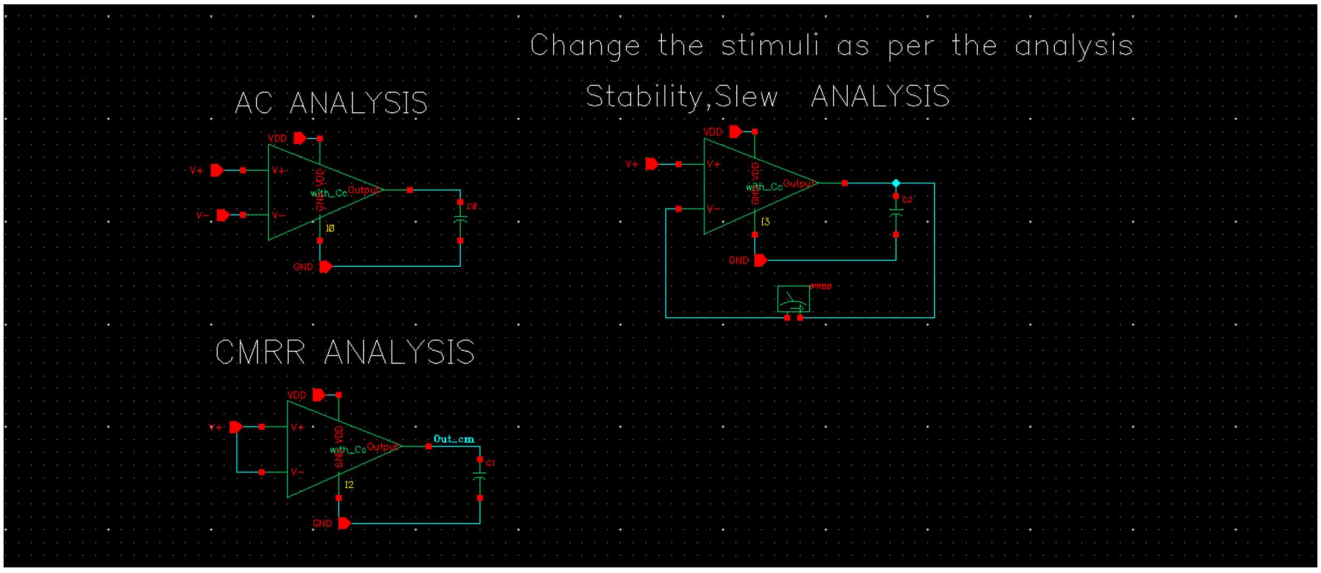




Transient analysis



Testbenches:



Finalized Design: