

# **Design and Stability Analysis of Two-Stage CMOS Opamp**



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GitHub project link : [https://github.com/pranizuky-ux/Two\\_stage\\_opamp](https://github.com/pranizuky-ux/Two_stage_opamp)

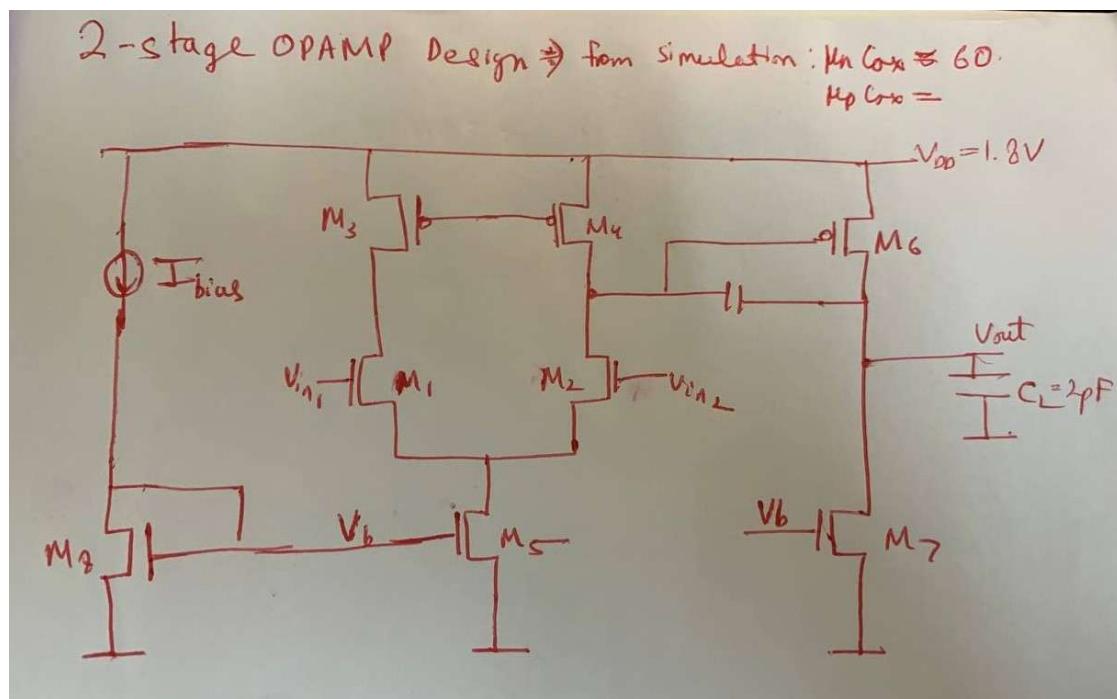
Parameter	Specification	Obtained
Open Loop, differential mode, DC Gain	$\geq 60$ dB	67.65 dB
CMRR	$\geq 50$ dB	80 dB
Unity Gain Band Width	$\geq 20$ MHz	22.94 MHz
Phase Margin	$\geq 60^\circ$	69.397°
Slew Rate	20V/ $\mu$ s	19.53V/ $\mu$ s
Power Dissipation	$\leq 500$ $\mu$ W	255.552 $\mu$ W

Node : 180 nm

VDD=1.8V

Load Capacitance= 2pF

### Design Procedure:



i) Phase Margin  $\geq 60^\circ \Rightarrow C_c \geq 0.22 C_L$   
 $\Rightarrow C_c \geq 440 \text{ pF}$   
 I started with  $C_c = 80 \text{ pF}$  (with simulation  $C_c = 1 \mu\text{F}$  for optimal PM)

ii) Slewrate =  $20/\mu\text{s} = \frac{I_{bias}}{C_c}$   
 $\Rightarrow I_{bias} = 20 \times 800 \times 10^{-9} = 16 \mu\text{A}$   
 To account for inaccuracy due to square law model,  $\boxed{I_{bias} = 20 \mu\text{A}}$

iii) Design of  $M_1, M_2$ :  
 $G_B = \frac{g_m L}{2\pi \times C_c} \Rightarrow g_m = 150.79 \mu\text{A} \rightarrow 160 \mu\text{V}$   
 $(\frac{W}{L})_{1,2} = \frac{g_m^2}{2 \mu_n C_c (I_{bias}/2)} \approx 4.22 \rightarrow \underline{\underline{6}}$

agreed by simulation:  
 $V_{TRAN} \in [0.47 - 0.58]$   
 $|V_{THP}| \in [0.501 - 510 \text{ V}]$

iv) Design of  $M_3, M_4$ :  
 Let's assume  $\rightarrow I_{CMR} \in [0.8 - 1.6 \text{ V}]$   
 $\Rightarrow I_{CMR+} < V_{DD} - V_{GS2} / \frac{I_{bias}}{2} + V_{THP} \text{ min}$   
 $\Rightarrow (\frac{W}{L})_{3,4} \gg 13.1 \dots \Rightarrow \boxed{(\frac{W}{L})_{3,4} = 14}$

v) Design of  $M_5, M_8$ :  
 $I_{CMR-} \geq V_{GS1,2} / \frac{I_{bias}}{2} + V_{DD} / I_{bias}$   
 $\rightarrow (\frac{W}{L})_5 \leq 12.09 \rightarrow (\frac{W}{L})_5 = 12 - (\frac{W}{L})_2$

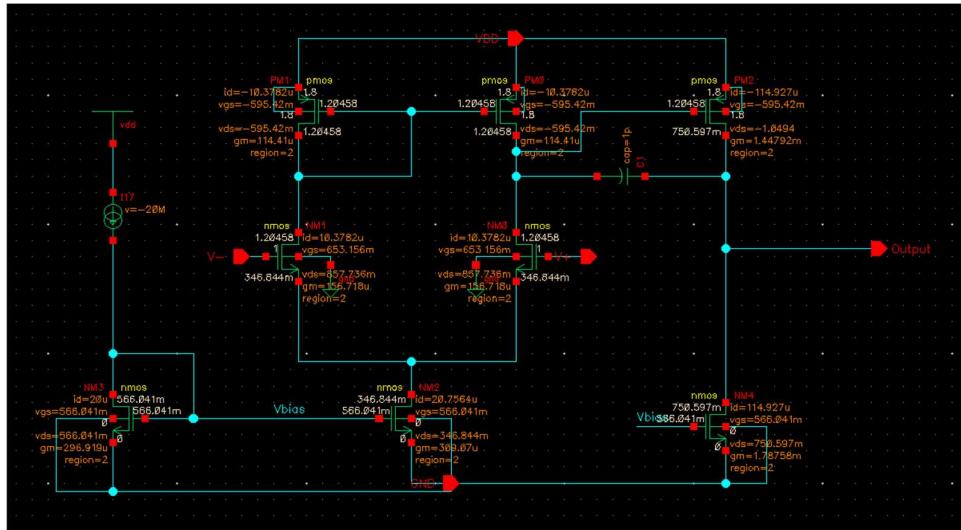
vi) Design of  $M_6$ :  
 for PM  $\geq 60^\circ \rightarrow g_m \geq 10 g_m \rightarrow \boxed{g_m = 1600}$   
 also by design, it's fixed that:  
 $\frac{(\frac{W}{L})_6}{(\frac{W}{L})_4} = \frac{I_6}{I_4} \Rightarrow \frac{(\frac{W}{L})_6}{(\frac{W}{L})_4} = \frac{g_m_6}{g_m_4} \quad \left| \begin{array}{l} g_m_4 = 130 \mu\text{V} \\ g_m_6 = 1600 \end{array} \right.$   
 $\rightarrow \frac{g_m_6}{g_m_4} \times (\frac{W}{L})_4 = (\frac{W}{L})_6 = 173 \rightarrow 174$

vii)  $\frac{I_6}{I_4} = \frac{174}{14} \Rightarrow I_6 \approx 125 \mu\text{A} \& (\frac{W}{L})_7 = \frac{I_7}{I_5} \times (\frac{W}{L})_5$   
 $\Rightarrow (\frac{W}{L})_7 = 75$

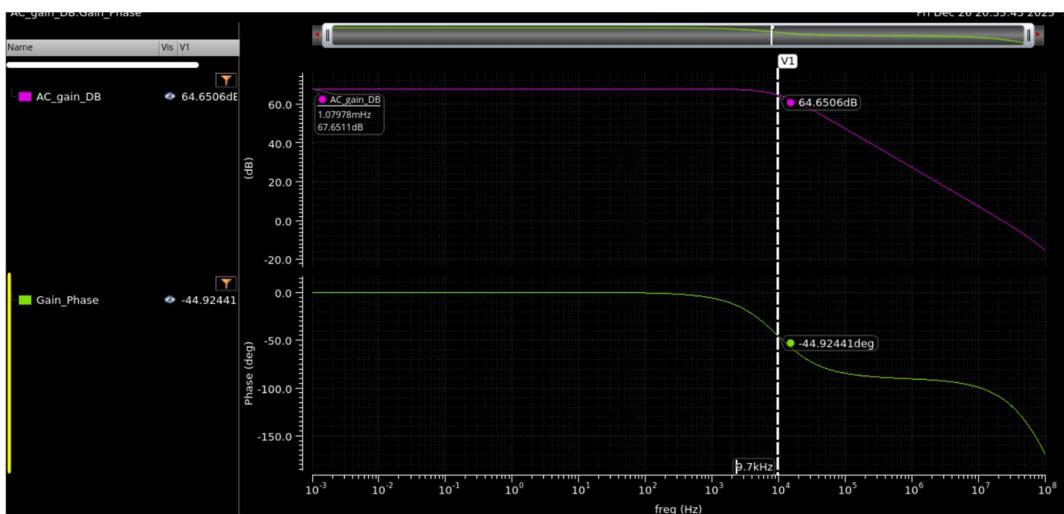
### Table listing Mosfet sizing:

M1, M2	W = 3um	L = 500nm
M3, M4	W = 7um	L = 500nm
M5, M8	W = 6um	L = 500nm
M6	W=43.5um	L = 250nm
M7	W=18.75um	L = 250nm

## DC Analysis and Schematic:

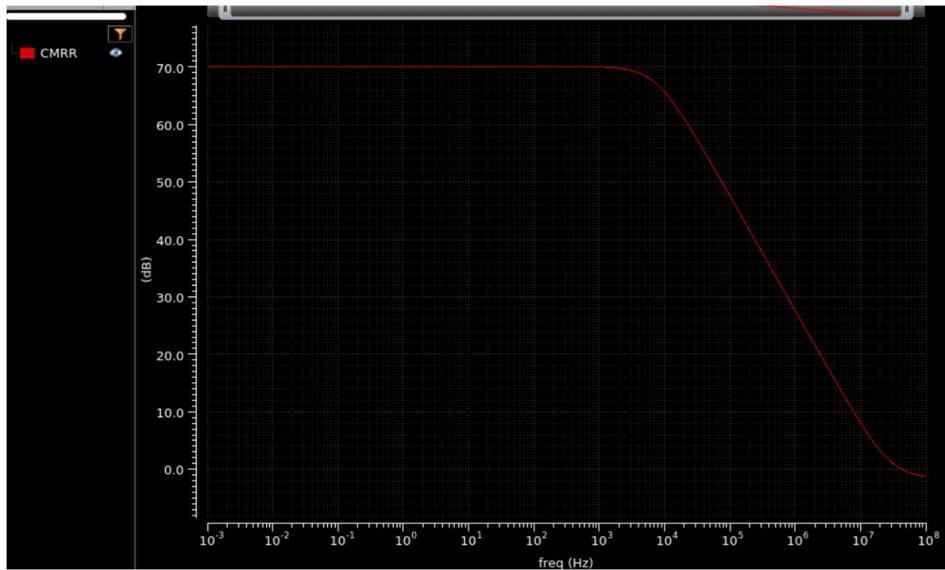


## AC analysis

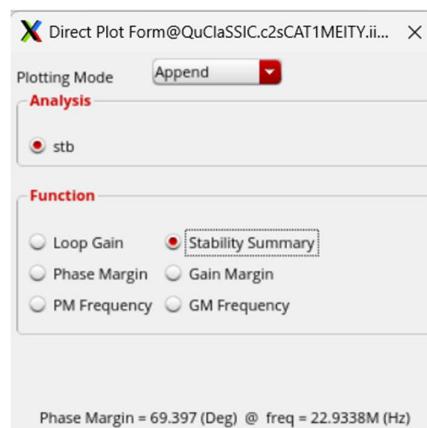
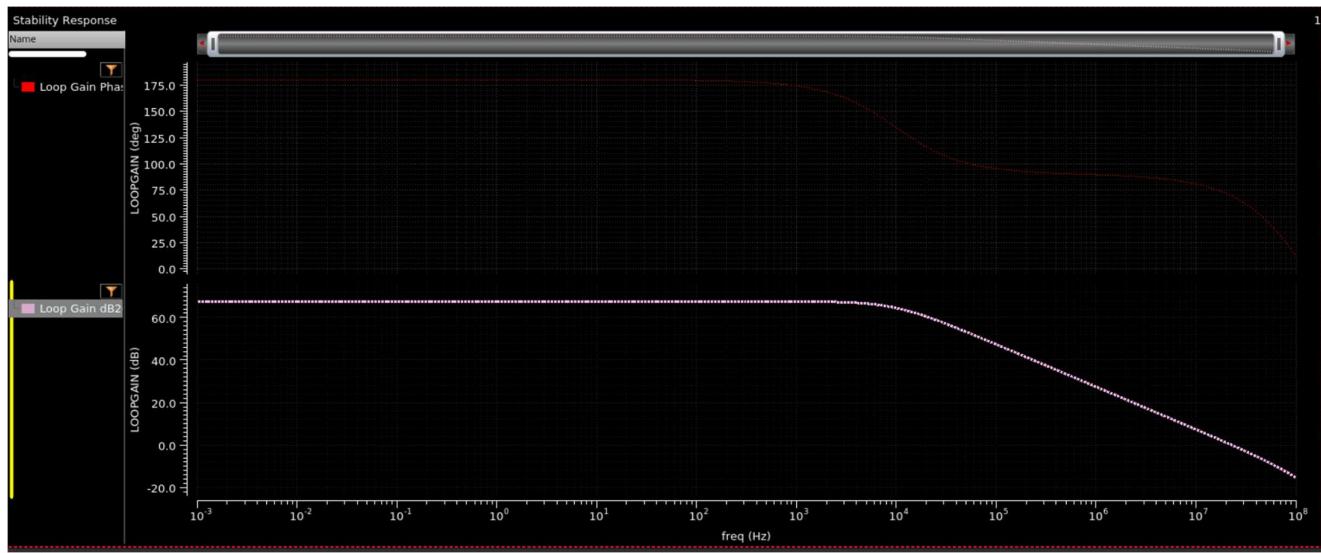


Outputs					
Name/Signal/Expr	Value	Plot	Save	Save Options	
1 AC_gain_DB	wave	✓	✓		
2 Bandwidth	9.70215K	✓	□		
3 Gain_Phase	wave	✓	✓		
4 UGF	22.944M	✓	✓		
5 PM	68.9624	✓	✓		
6 PowerConsumption	255.552u	✓	✓		

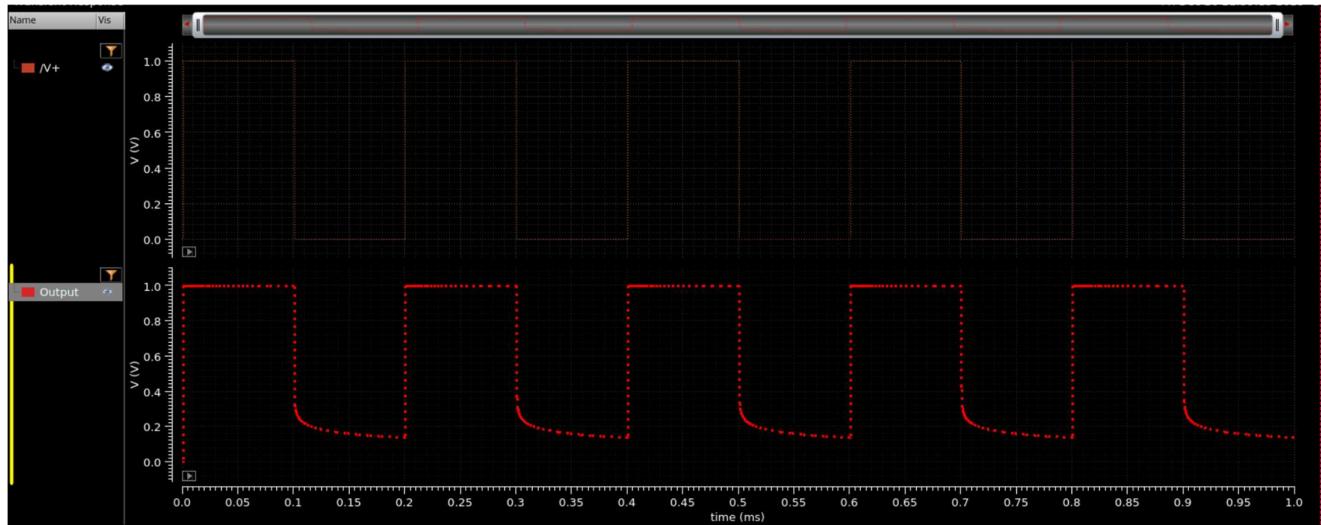
Plot after simulation: Auto      Plotting mode: Replace



## Stability analysis

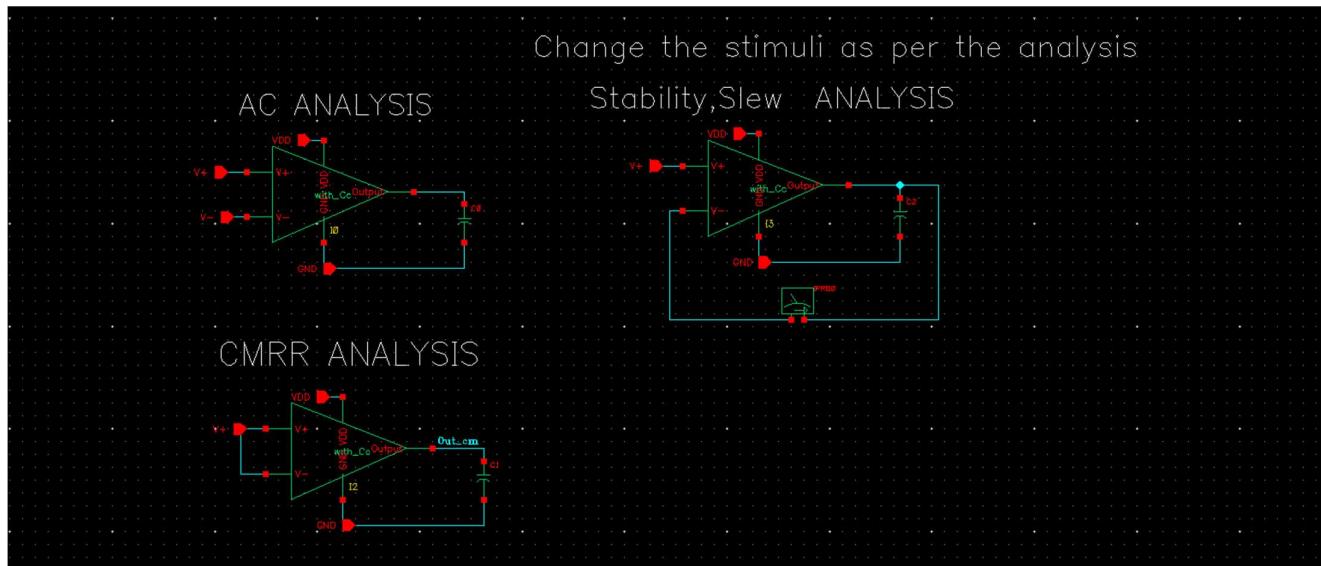


## Transient analysis



6 SlewRate 19.5368M

## Testbenches:



## Finalized Design:

