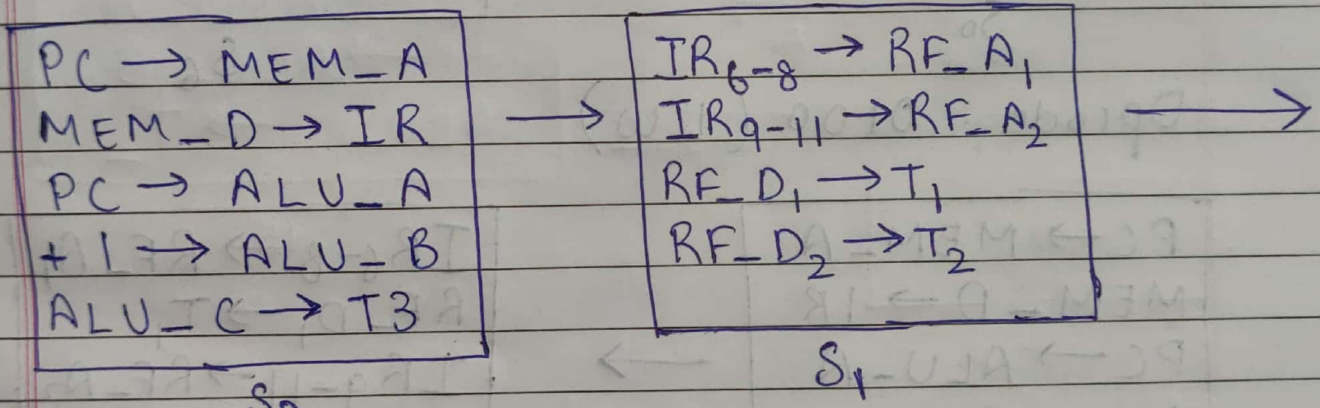
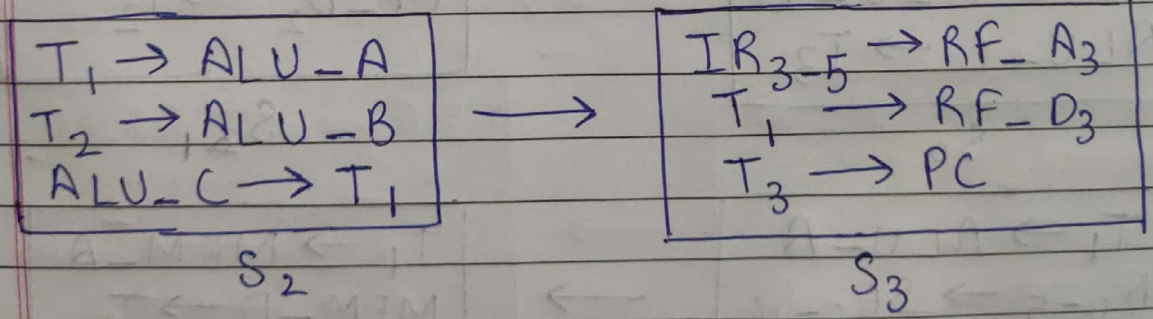
IITB - Proc
EE - 224

Anubhav Goel	170040043
Pranjal Jain	170070030
Vaibhav Malviya	170070057
Shreyas Goenka	170070037

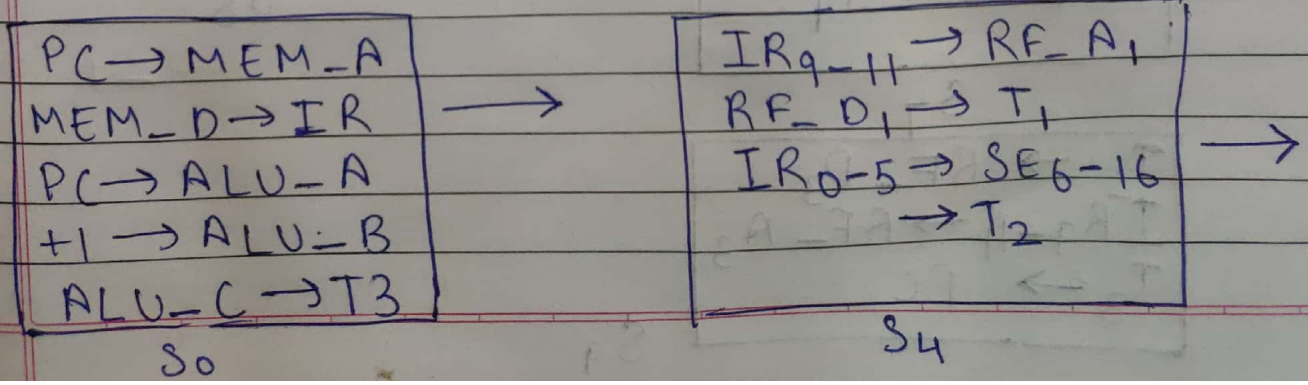
Defining States

Opcode : 0000 / 0010
ADD / ADC / ADZ / NDU / NDC / NDZ
(ALU Operations)





Opcode : 0001 (ADD1)



$T_1 \rightarrow ALU\_A$
$T_2 \rightarrow ALU\_B$
$ALU\_C \rightarrow T_1$

S_2

$\longrightarrow$

$IR_{6-8} \rightarrow RF\_A_3$
$T_1 \rightarrow RF\_D_3$
$T_3 \rightarrow PC$

S_5

Opcode : 0011 (LHI)

$PC \rightarrow MEM\_A$
$MEM\_D \rightarrow IR$
$PC \rightarrow ALU\_A$
$+1 \rightarrow ALU\_B$
$ALU\_C \rightarrow T_3$

S_0

$\longrightarrow$

$IR_{0-8} \rightarrow SE_{9-16}$
$\rightarrow LS_7$
$LS_7 \rightarrow RF\_D_3$
$IR_{9-11} \rightarrow RF\_A_3$
$T_3 \rightarrow PC$

S_6

Opcode : 0100 (LW)

$PC \rightarrow MEM\_A$
$MEM\_D \rightarrow IR$
$PC \rightarrow ALU\_A$
$+1 \rightarrow ALU\_B$
$ALU\_C \rightarrow T_3$

S_0

$\longrightarrow$

$IR_{6-8} \rightarrow RF\_A_1$
$RF\_D_1 \rightarrow T_1$
$IR_{9-11} \rightarrow RF\_A_2$
$RF\_D_2 \rightarrow T_2$

S_{21}

$\longrightarrow$

$T_1 \rightarrow ALU\_A$
$IR_{0-5} \rightarrow SE_{6-16}$
$\rightarrow ALU\_B$
$ALU\_C \rightarrow T_1$

S_7

$\longrightarrow$

$T_1 \rightarrow MEM\_A$
$MEM\_D \rightarrow T_2$

S_8

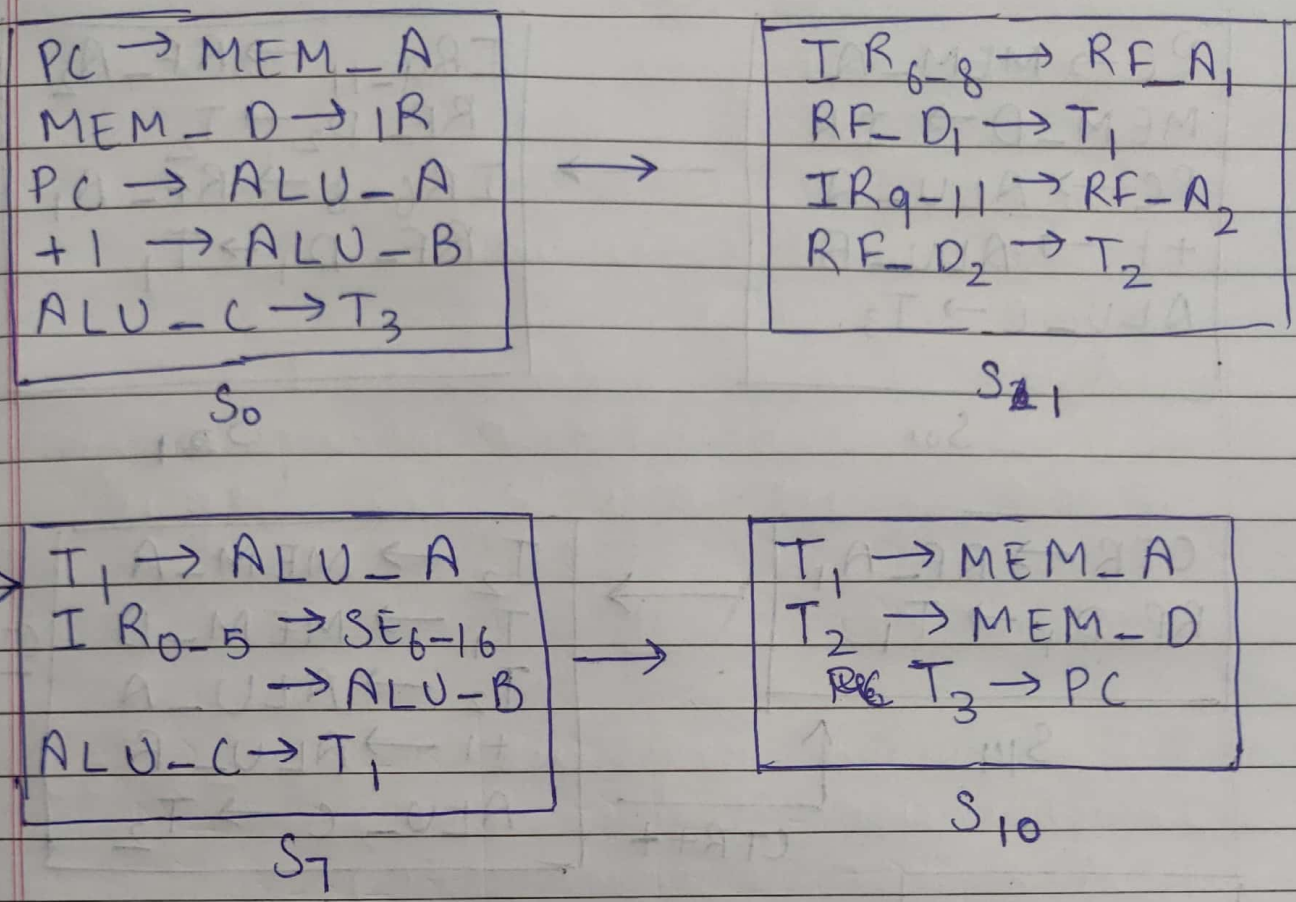
$\longrightarrow$

$T_2 \rightarrow RF\_D_3$
$IR_{9-11} \rightarrow RF\_A_3$
$T_3 \rightarrow PC$

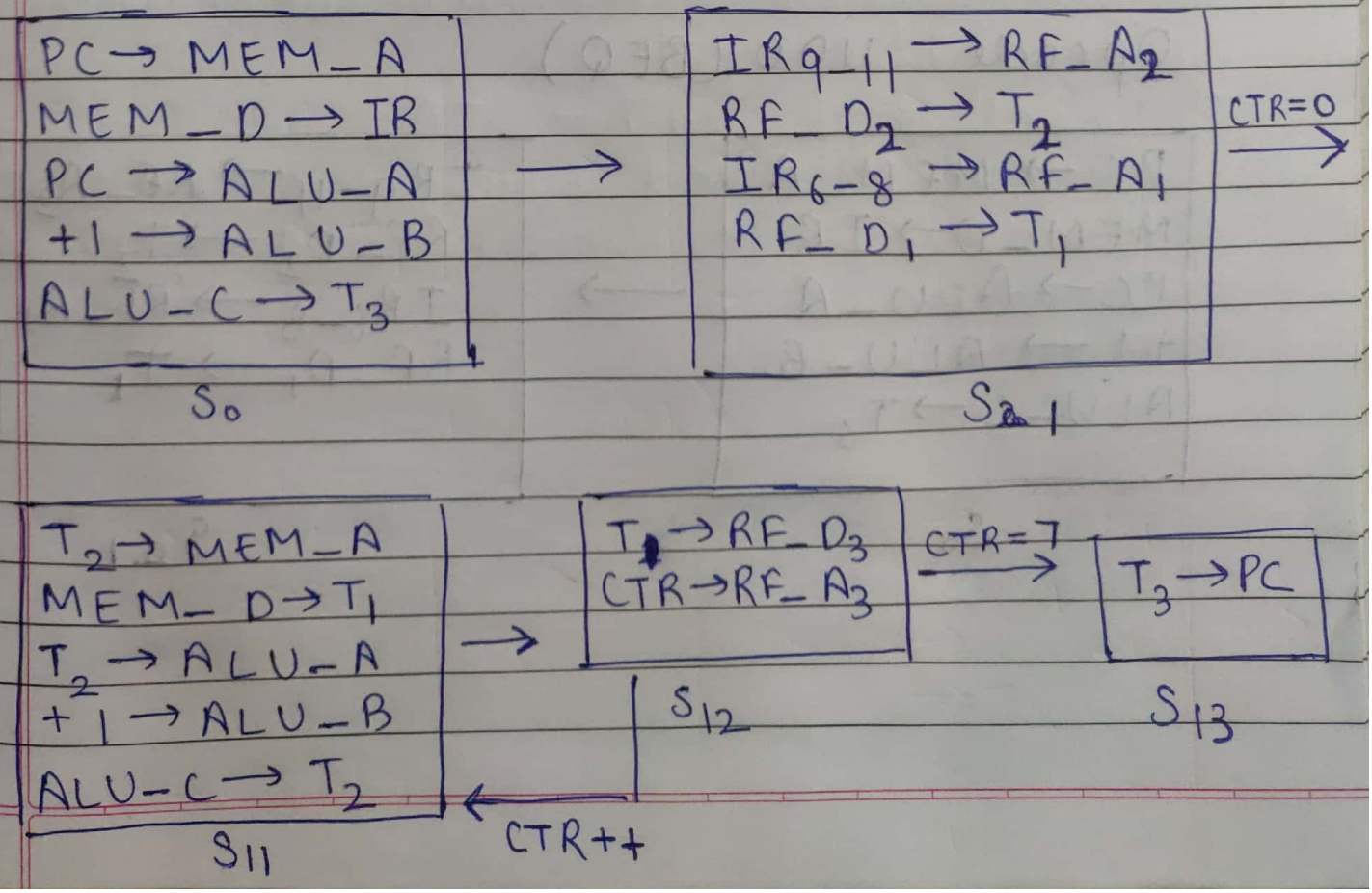
S_9

DATE / /

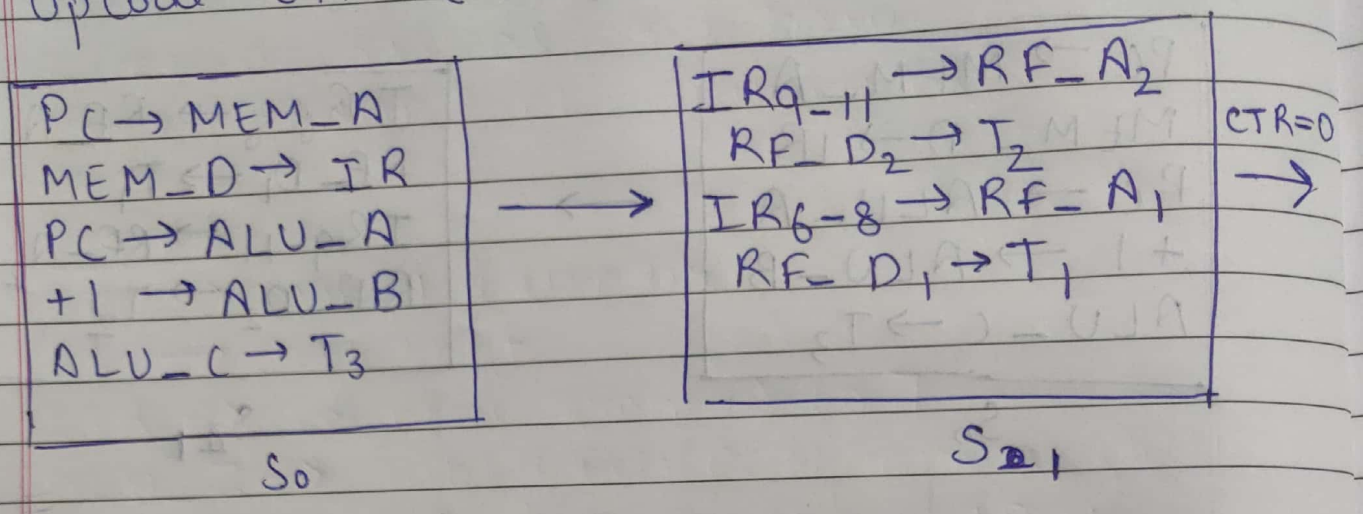
Opcode : 0101 (SW)

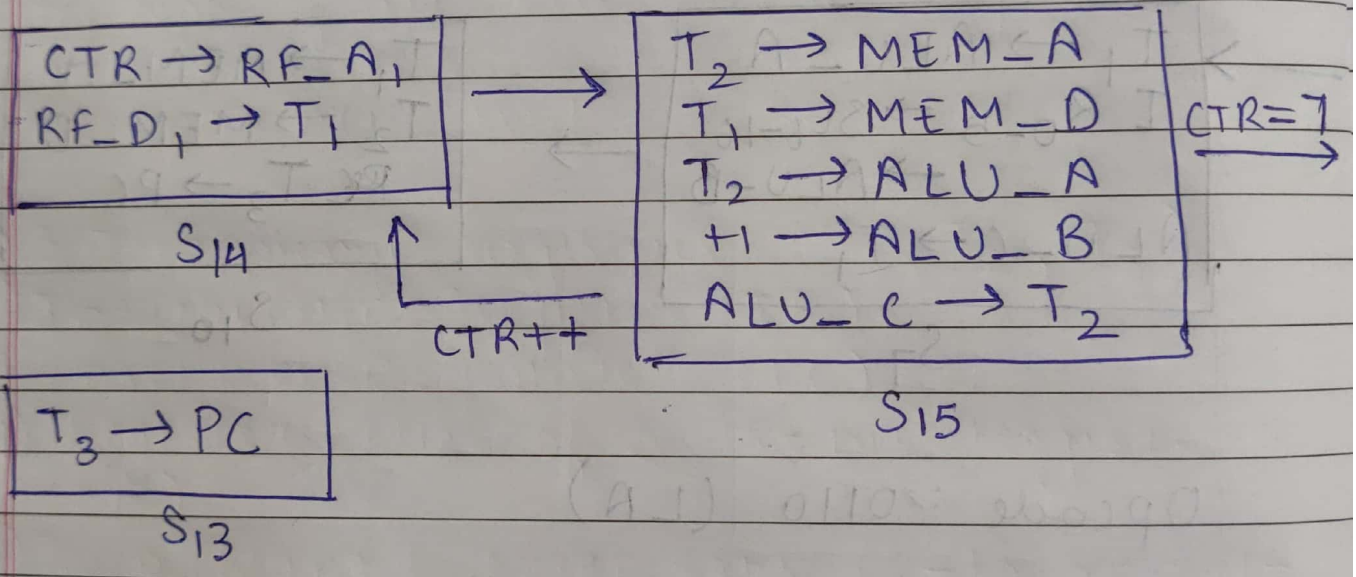


Opcode : 0110 (LA)

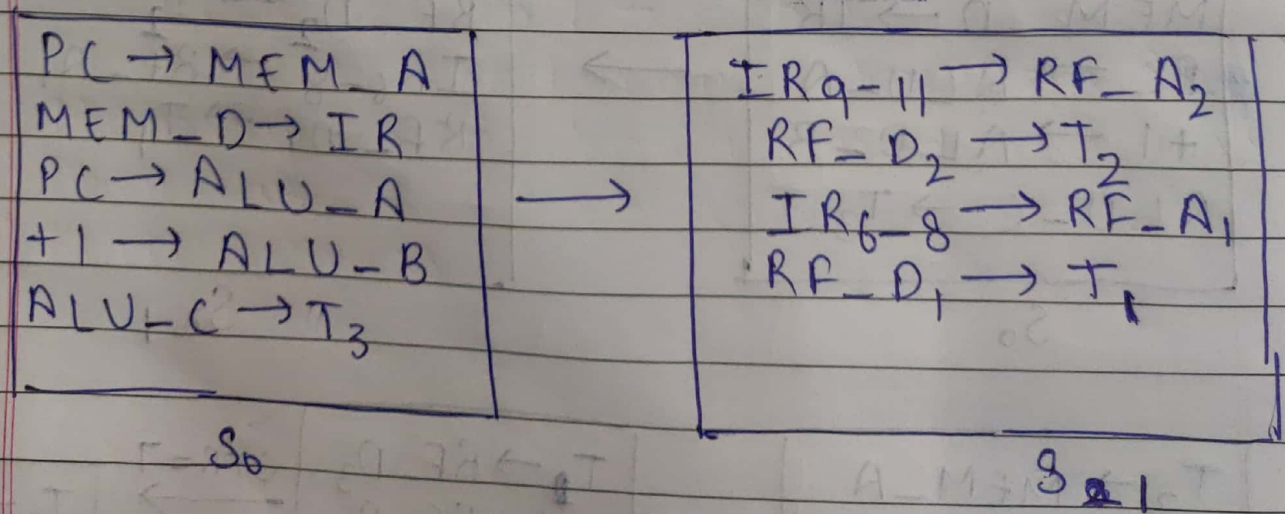


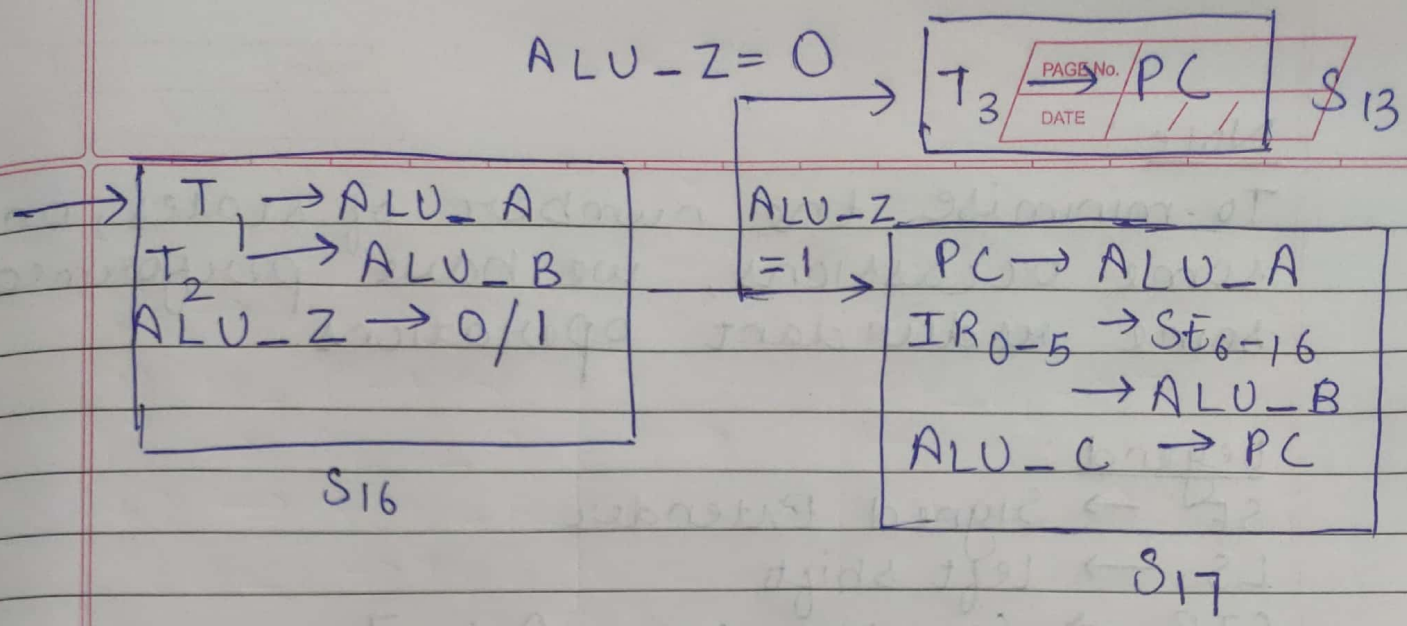
Opcode : 0111 (SA)



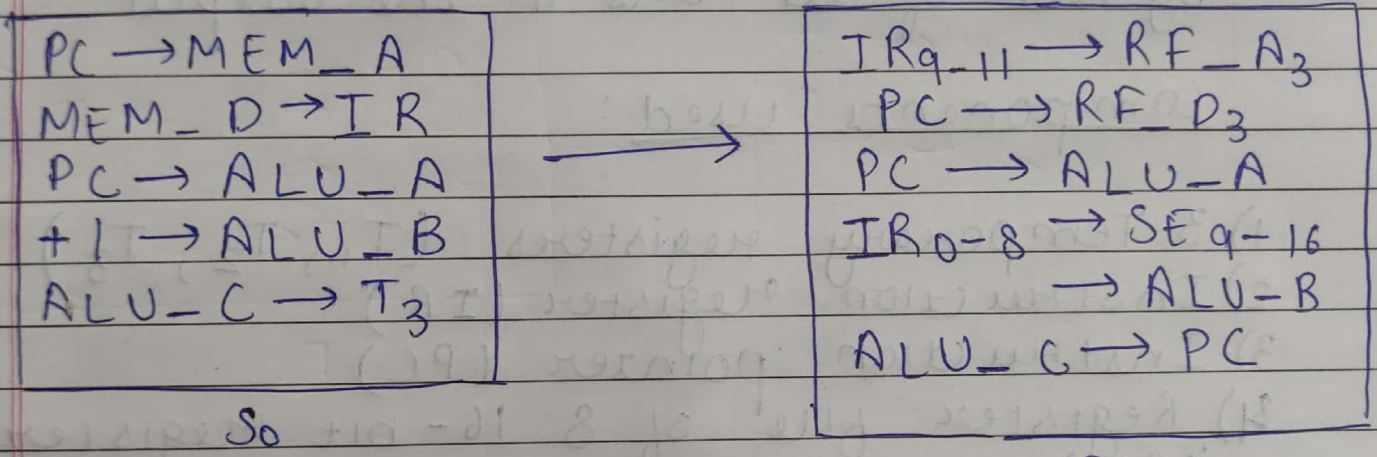


Opcode : 1100 (BEQ)

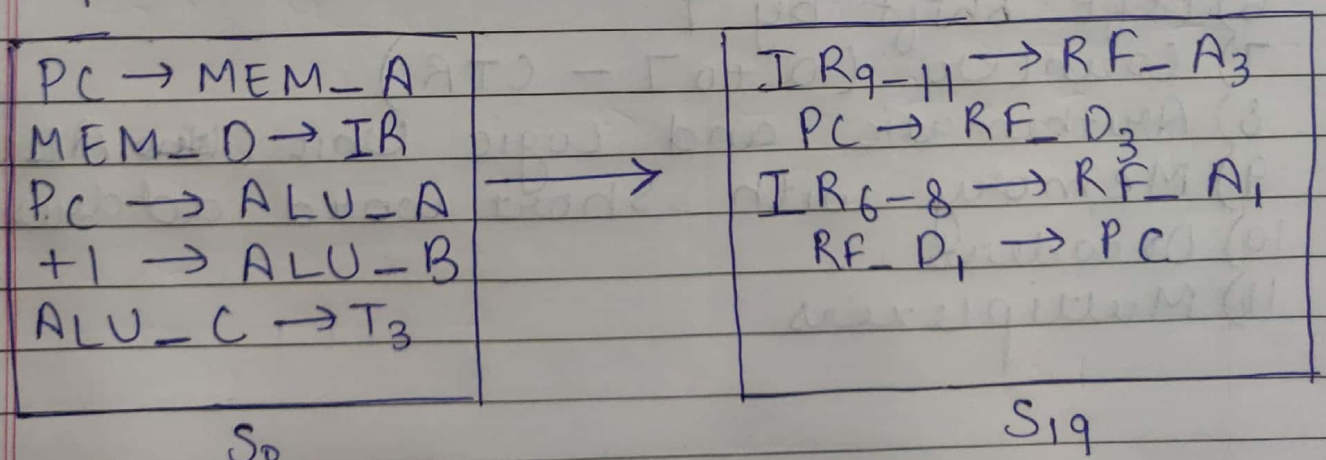




Opcode : 1000 (JAL)



Opcode : 1001 (JLR)



Therefore, we conclude the formation of states.

PAGE No.
DATE / /

Note:

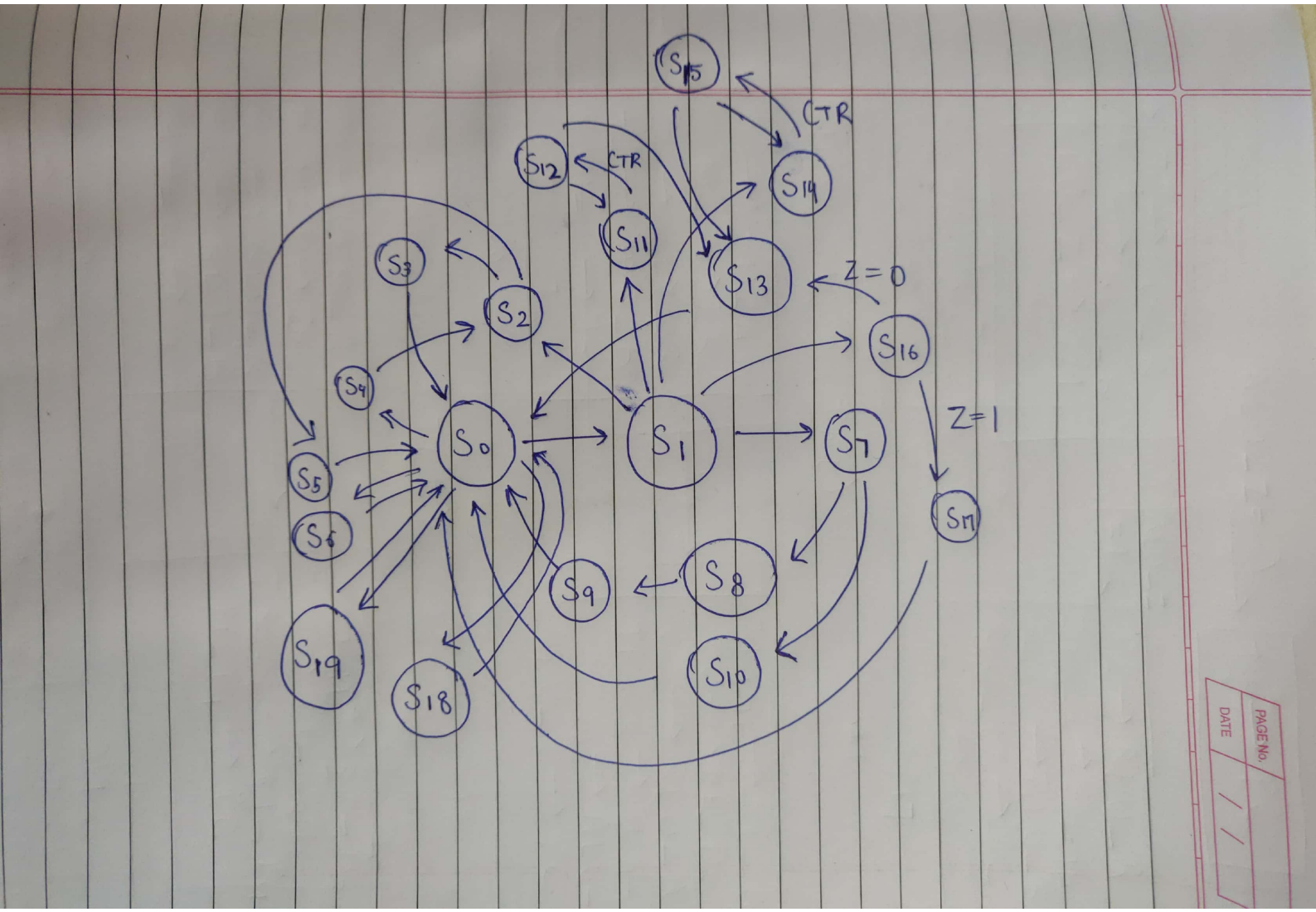
To minimise the number of states, on some occassions, we have performed some redundant operations.

Legend:

SE → Signed Extender
LS → left shift
CTR → Counter from 0 to 7
ALU_Z → Subtraction of inputs followed by NOR of all bits in the output.

Components used:

1) 3 Temporary registers (T_1, T_2, T_3)
2) Instruction register (IR)
3) Instruction pointer (PC)
4) Register file of 8 16-bit registers (RF)
5) Two signed extenders (6-16 and 9-16)
6) Left shift by 7
7) Counter (0 to 7 - CTR)
8) Arithmatic and Logic Unit (ALU)
9) Memory with short word address.
10) Decoders
11) Multiplexers



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control signals

PC: WR

MEM: WR

IR: WR

RF: WR

T1: WR

T2: WR

T3: WR

CTR: INIT

PC_IN: (3-1 MUX)

MEM_A: (3-1 MUX)

RFA1: (3-1 MUX)

RFA3: (4-1 MUX)

RFD3: (4-1 MUX)

T1_IN: (3-1 MUX)

T2_IN: (3-1 MUX)

ALUA: (3-1 MUX)

ALUB: (3-1 MUX)

MEM_D_IN: (2-1 MUX)

carry_flag_C:

zero_flag_Z:

PC: WR = S3, S5, S6, S9, S10, S13, S17, S18, S19 (OR off all)

MEM: WR = S10, S15 (OR off all)

IR: WR = S0

RF: WR = S3, S5, S6, S9, S12, S18, S19 (OR off all)

T1: WR = S1, S2, S4, S7, S11, S14

T2: WR = S1, S4, S8, S11, S15

T3: WR = S0

CTR: INIT = S1, 0110/0111