

IITB - Proc

EE - 224

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Defining States

Opcode : 0000 / 0010

ADD / ADC / ADZ / NDU / NDC / NDZ

(ALU Operations)

PC  $\rightarrow$  MEM\_A  
 MEM\_D  $\rightarrow$  IR  
 PC  $\rightarrow$  ALU\_A  
 +1  $\rightarrow$  ALU\_B  
 ALU\_C  $\rightarrow$  T3

S<sub>0</sub> $\rightarrow$ 

IR<sub>6-8</sub>  $\rightarrow$  RF\_A<sub>1</sub>  
 IR<sub>9-11</sub>  $\rightarrow$  RF\_A<sub>2</sub>  
 RF\_D<sub>1</sub>  $\rightarrow$  T<sub>1</sub>  
 RF\_D<sub>2</sub>  $\rightarrow$  T<sub>2</sub>

S<sub>1</sub> $\rightarrow$ 

T<sub>1</sub>  $\rightarrow$  ALU\_A  
 T<sub>2</sub>  $\rightarrow$  ALU\_B  
 ALU\_C  $\rightarrow$  T<sub>1</sub>

S<sub>2</sub> $\rightarrow$ 

IR<sub>3-5</sub>  $\rightarrow$  RF\_A<sub>3</sub>  
 T<sub>1</sub>  $\rightarrow$  RF\_D<sub>3</sub>  
 T<sub>3</sub>  $\rightarrow$  PC

S<sub>3</sub>

Opcode : 0001 (ADDI)

PC  $\rightarrow$  MEM\_A  
 MEM\_D  $\rightarrow$  IR  
 PC  $\rightarrow$  ALU\_A  
 +1  $\rightarrow$  ALU\_B  
 ALU\_C  $\rightarrow$  T3

S<sub>0</sub> $\rightarrow$ 

IR<sub>9-11</sub>  $\rightarrow$  RF\_A<sub>1</sub>  
 RF\_D<sub>1</sub>  $\rightarrow$  T<sub>1</sub>  
 IR<sub>0-5</sub>  $\rightarrow$  SE<sub>6-16</sub>  
 $\rightarrow$  T<sub>2</sub>

S<sub>4</sub> $\rightarrow$

$T_1 \rightarrow \text{ALU-A}$   
 $T_2 \rightarrow \text{ALU-B}$   
 $\text{ALU-C} \rightarrow T_1$

S<sub>2</sub>

$\text{IR}_{6-8} \rightarrow \text{RF-A}_3$   
 $T_1 \rightarrow \text{RF-D}_3$   
 $T_3 \rightarrow \text{PC}$

S<sub>5</sub>

Opcode : 0011 (LHI)

$\text{PC} \rightarrow \text{MEM-A}$   
 $\text{MEM-D} \rightarrow \text{IR}$   
 $\text{PC} \rightarrow \text{ALU-A}$   
 $+1 \rightarrow \text{ALU-B}$   
 $\text{ALU-C} \rightarrow T_3$

S<sub>0</sub>

$\text{IR}_{0-8} \rightarrow \text{SEQ-16}$   
 $\rightarrow \text{LS}_7$   
 $\text{LS}_7 \rightarrow \text{RF-D}_3$   
 $\text{IR}_{9-11} \rightarrow \text{RF-A}_3$   
 $T_3 \rightarrow \text{PC}$

S<sub>6</sub>

Opcode : 0100 (LW)

$\text{PC} \rightarrow \text{MEM-A}$   
 $\text{MEM-D} \rightarrow \text{IR}$   
 $\text{PC} \rightarrow \text{ALU-A}$   
 $+1 \rightarrow \text{ALU-B}$   
 $\text{ALU-C} \rightarrow T_3$

S<sub>0</sub>

$\text{IR}_{6-8} \rightarrow \text{RF-A}_1$   
 $\text{RF-D}_1 \rightarrow T_1$   
 $\text{IR}_{9-11} \rightarrow \text{RF-A}_2$   
 $\text{RF-D}_2 \rightarrow T_2$

S<sub>21</sub>

$T_1 \rightarrow \text{ALU-A}$   
 $\text{IR}_{0-5} \rightarrow \text{SEQ-16}$   
 $\rightarrow \text{ALU-B}$   
 $\text{ALU-C} \rightarrow T_1$

S<sub>7</sub>

$T_1 \rightarrow \text{MEM-A}$   
 $\text{MEM-D} \rightarrow T_2$

S<sub>8</sub>

$T_2 \rightarrow \text{RF-D}_3$   
 $\text{IR}_{9-11} \rightarrow \text{RF-A}_3$   
 $T_3 \rightarrow \text{PC}$

S<sub>9</sub>



Opcode : 0101 (SW)

PC  $\rightarrow$  MEM\_A  
MEM\_D  $\rightarrow$  IR  
PC  $\rightarrow$  ALU-A  
+1  $\rightarrow$  ALU-B  
ALU-C  $\rightarrow$  T<sub>3</sub>

S<sub>0</sub>

IR<sub>6-8</sub>  $\rightarrow$  RF-A<sub>1</sub>  
RF-D<sub>1</sub>  $\rightarrow$  T<sub>1</sub>  
IR<sub>9-11</sub>  $\rightarrow$  RF-A<sub>2</sub>  
RF-D<sub>2</sub>  $\rightarrow$  T<sub>2</sub>

S<sub>1</sub>

T<sub>1</sub>  $\rightarrow$  ALU-A  
IR<sub>0-5</sub>  $\rightarrow$  SE<sub>6-16</sub>  
 $\rightarrow$  ALU-B  
ALU-C  $\rightarrow$  T<sub>1</sub>

S<sub>7</sub>

T<sub>1</sub>  $\rightarrow$  MEM-A  
T<sub>2</sub>  $\rightarrow$  MEM-D  
T<sub>3</sub>  $\rightarrow$  PC

S<sub>10</sub>

Opcode : 0110 (LA)

PC  $\rightarrow$  MEM-A  
MEM\_D  $\rightarrow$  IR  
PC  $\rightarrow$  ALU-A  
+1  $\rightarrow$  ALU-B  
ALU-C  $\rightarrow$  T<sub>3</sub>

S<sub>0</sub>

IR<sub>9-11</sub>  $\rightarrow$  RF-A<sub>2</sub>  
RF-D<sub>2</sub>  $\rightarrow$  T<sub>2</sub>  
IR<sub>6-8</sub>  $\rightarrow$  RF-A<sub>1</sub>  
RF-D<sub>1</sub>  $\rightarrow$  T<sub>1</sub>

CTR=0  $\rightarrow$

S<sub>2</sub>

T<sub>2</sub>  $\rightarrow$  MEM-A  
MEM\_D  $\rightarrow$  T<sub>1</sub>  
T<sub>2</sub>  $\rightarrow$  ALU-A  
+1  $\rightarrow$  ALU-B  
ALU-C  $\rightarrow$  T<sub>2</sub>

S<sub>11</sub>

T<sub>1</sub>  $\rightarrow$  RF-D<sub>3</sub>  
CTR  $\rightarrow$  RF-A<sub>3</sub>

S<sub>12</sub>

CTR=7  $\rightarrow$

T<sub>3</sub>  $\rightarrow$  PC

S<sub>13</sub>

CTR++

Opcode: 0111 (SA)

PC  $\rightarrow$  MEM\_A  
MEM\_D  $\rightarrow$  IR  
PC  $\rightarrow$  ALU\_A  
+1  $\rightarrow$  ALU\_B  
ALU\_C  $\rightarrow$  T<sub>3</sub>

S<sub>0</sub>

IR<sub>9-11</sub>  $\rightarrow$  RF\_A<sub>2</sub>  
RF\_D<sub>2</sub>  $\rightarrow$  T<sub>2</sub>  
IR<sub>6-8</sub>  $\rightarrow$  RF\_A<sub>1</sub>  
RF\_D<sub>1</sub>  $\rightarrow$  T<sub>1</sub>

CTR=0

S<sub>21</sub>

CTR  $\rightarrow$  RF\_A<sub>1</sub>  
RF\_D<sub>1</sub>  $\rightarrow$  T<sub>1</sub>

S<sub>14</sub>

CTR++

T<sub>2</sub>  $\rightarrow$  MEM\_A  
T<sub>1</sub>  $\rightarrow$  MEM\_D  
T<sub>2</sub>  $\rightarrow$  ALU\_A  
+1  $\rightarrow$  ALU\_B  
ALU\_C  $\rightarrow$  T<sub>2</sub>

CTR=7

S<sub>15</sub>

T<sub>3</sub>  $\rightarrow$  PC

S<sub>13</sub>

Opcode: 1100 (BEQ)

PC  $\rightarrow$  MEM\_A  
MEM\_D  $\rightarrow$  IR  
PC  $\rightarrow$  ALU\_A  
+1  $\rightarrow$  ALU\_B  
ALU\_C  $\rightarrow$  T<sub>3</sub>

S<sub>0</sub>

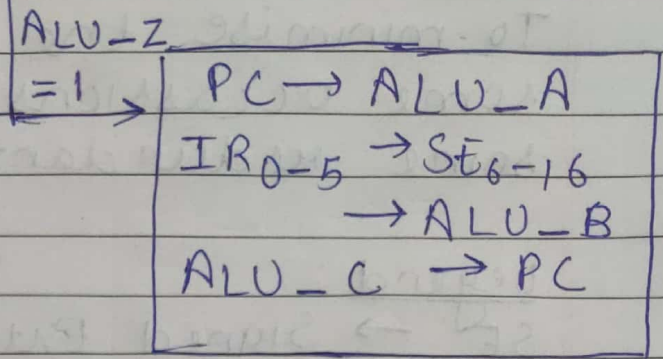
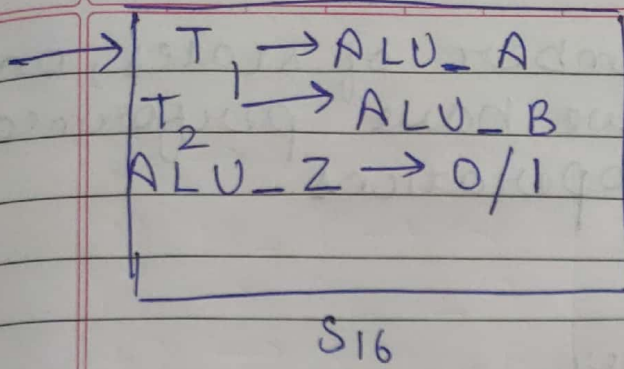
IR<sub>9-11</sub>  $\rightarrow$  RF\_A<sub>2</sub>  
RF\_D<sub>2</sub>  $\rightarrow$  T<sub>2</sub>  
IR<sub>6-8</sub>  $\rightarrow$  RF\_A<sub>1</sub>  
RF\_D<sub>1</sub>  $\rightarrow$  T<sub>1</sub>

S<sub>21</sub>

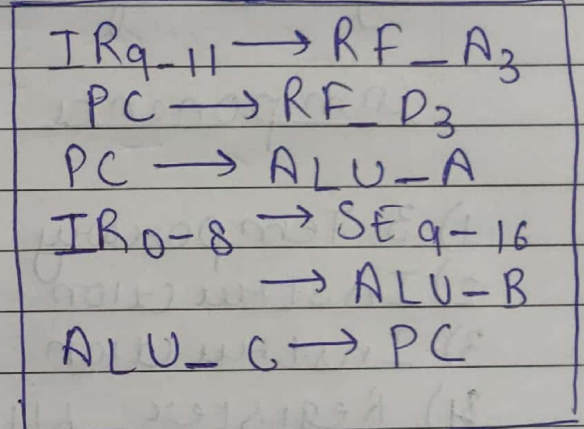
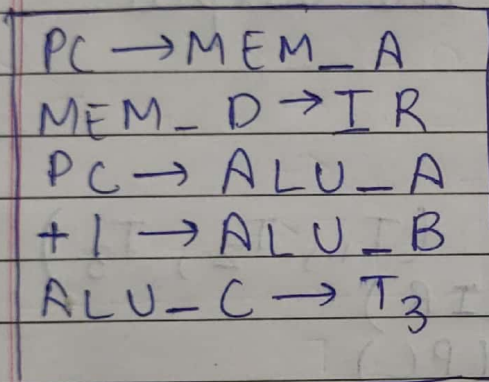


ALU-Z = 0

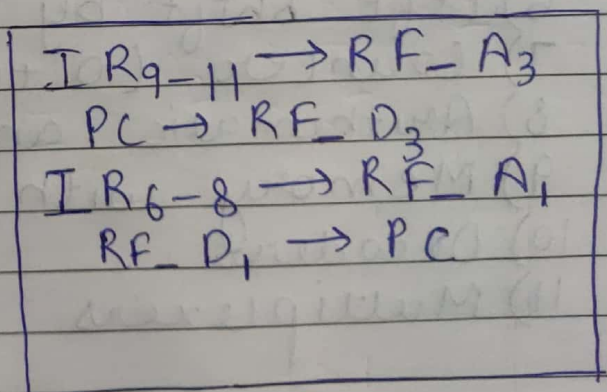
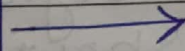
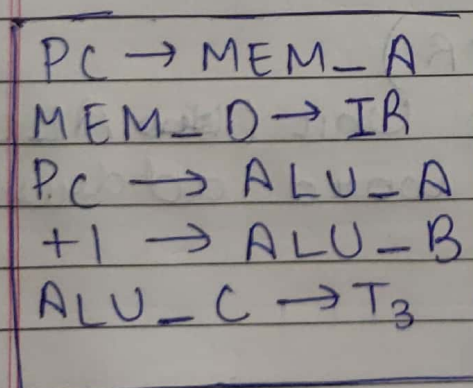
T <sub>3</sub>	PAGE No.	PC	S <sub>13</sub>
	DATE	/ /	



Opcode: 1000 (JAL)



Opcode: 1001 (JLR)



Therefore, we conclude the formation of states.

Note:

To minimise the number of states, on some occasions, we have performed some redundant operations.

Legend:

SE  $\rightarrow$  Signed Extender

LS  $\rightarrow$  Left Shift

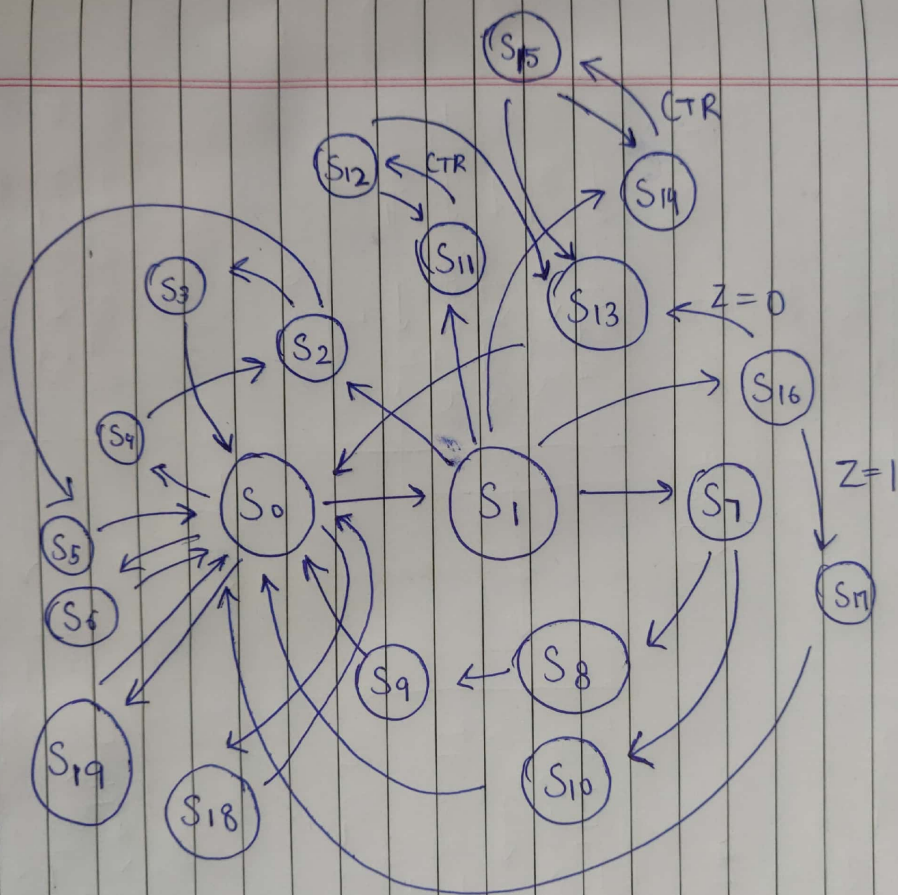
CTR  $\rightarrow$  Counter from 0 to 7

ALU\_Z  $\rightarrow$  Subtraction of inputs followed by NOR of all bits in the output.

Components used:

- 1) 3 Temporary registers ( $T_1, T_2, T_3$ )
- 2) Instruction register (IR)
- 3) Instruction pointer (PC)
- 4) Register file of 8 16-bit registers (RF)
- 5) Two signed extenders (6-16 and 9-16)
- 6) Left shift by 7
- 7) Counter (0 to 7 - CTR)
- 8) Arithmetic and Logic Unit (~~the~~ ALU)
- 9) Memory with short word address.
- 10) Decoders
- 11) Multiplexers







## Control signals

PC: ~~WR~~ MEM: WR IR: ~~WR~~ WR RF: WR T1: WR T2: WR T3: WR

CTR: INIT

PC-IN: (3-1 MUX) MEM-A: (3-1 MUX) RFA1: (3-1 MUX) RFA3: (4-1 MUX) RFD3: (4-1 MUX) T1-IN: (3-1 MUX)

T2-IN: (3-1 MUX) ALVA: (3-1 MUX) ALVB: (3-1 MUX) MEM-D-IN: (2-1 MUX) ~~MEM-D-IN~~

Carry-flag-C: zero-flag-Z:

PC: WR = S3, S5, S6, S9, S10, S13, S17, S18, S19  
~~WR = S3, S5, S6, S9, S10, S13, S17, S18, S19~~  
 (OR off all)

MEM: WR = S10, S15 (OR off all)

IR: WR = S0

RF: WR = S3, S5, S6, S9, S12, S18, S19 (OR off all)

T1: WR = S1, S2, S4, S7, S11, S14

T2: WR = S1, S4, S8, S11, S15

T3: WR = S0

CTR: INIT = S1, 0110/0111



PC-IN	PC OUT:	MEM A:	<del>MEM D</del>	ZR IN:	RFA1:	RFA2:	RFA3:	RFD1:	RFD2:	RFD3:
T3-OUT	MEM-A	PC-OUT	<del>TR-IN</del>	MEM-OUT	IR6-8	Seq-11	IR3-5	PC-IN	T2-IN	T1-OUT
ALU-C	RF-D3	T1-OUT	<del>T2-IN</del>		IR9-11		IR6-8	T1-IN		LS7-OUT
RF-D1	ALU-A	T2-OUT	<del>T2-OUT</del>		CTR		IR9-11			T2-OUT
		<del>PC-OUT</del>	<del>T1-IN</del>				CTR			PC-OUT
			<del>T1-OUT</del>							

T1 IN:	T2 IN:	T3 IN:	T1 OUT:	T2 OUT:	T3 OUT:	ALUA	ALUB	ALUC	SEG-16 IN	SEG-16 OUT:
MEM-D OUT	MEM-A OUT	ALU-C	MEM-A	MEM-A	PC-IN	T1-OUT	T2-OUT	PC-IN	IR0-5	T2-IN
RF-D1	RF-D2		MEM-D IN	MEM-D IN		T2-OUT	+1	T3-IN		ALU-B
ALU-C	ALU-C		RF-D3	RF-D3		PC-OUT	Seq-10 OUT	T1-IN		
			ALU-A	ALU-A				T2-IN		
			ALU-B	ALU-B						

Seq-16 IN:	Seq-16 OUT:	LS7-IN:	LS7 OUT:	<del>Seq-16 IN</del>	MEM-D-IN:	MEM-D-OUT:
IR0-8	LS7-IN	Seq-16 OUT	RF-D3		T2-OUT	TR-IN
	ALU-B				T1-OUT	T2-IN
						T1-IN

