Synthesis Report – Brent Kung Adder

Release 14.7 - xst P.20131013 (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.22 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.22 secs

--> Reading design: brentkung.prj

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===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "brentkung.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "brentkung"
Output Format   : NGC
Target Device   : xc7a100t-3-csg324

---- Source Options
Top Module Name   : brentkung
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Shift Register Extraction   : YES
ROM Style   : Auto

```
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 32
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

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=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file "D:\quartuslite\brentkung\brentkung.v" into library work
Parsing module <AND>.
Parsing module <XOR>.
Parsing module <aplusbc>.
Parsing module <brentkung>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <brentkung>.

Elaborating module <AND>.

Elaborating module <XOR>.
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Elaborating module <aplusbc>.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <brentkung>.
    Related source file is "D:\quartuslite\brentkung\brentkung.v".
    Summary:
Unit <brentkung> synthesized.

Synthesizing Unit <AND>.
    Related source file is "D:\quartuslite\brentkung\brentkung.v".
    Summary:
        no macro.
Unit <AND> synthesized.

Synthesizing Unit <XOR>.
    Related source file is "D:\quartuslite\brentkung\brentkung.v".
    Summary:
Unit <XOR> synthesized.

Synthesizing Unit <aplusbc>.
    Related source file is "D:\quartuslite\brentkung\brentkung.v".
    Summary:
        no macro.
Unit <aplusbc> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Xors                                                  : 17
 1-bit xor2                                            : 16
 16-bit xor2                                           : 1

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=========================================================================
*                      Advanced HDL Synthesis                           *
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=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Xors                                                  : 17
 1-bit xor2                                            : 16
 16-bit xor2                                           : 1

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=========================================================================
*                         Low Level Synthesis                           *
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Optimizing unit <brentkung> ...

Mapping all equations...
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Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block brentkung, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Found no macro
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=========================================================================
*                            Partition Report                           *
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Partition Implementation Status
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  No Partitions were found in this design.

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=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : brentkung.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 24
#      LUT3                        : 8
#      LUT5                        : 16
# IO Buffers                       : 50
#      IBUF                        : 33
#      OBUF                        : 17

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                  24  out of  63400     0%
    Number used as Logic:               24  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    24
   Number with an unused Flip Flop:     24  out of     24   100%
   Number with an unused LUT:            0  out of     24     0%
   Number of fully used LUT-FF pairs:    0  out of     24     0%
   Number of unique control sets:        0

IO Utilization:
 Number of IOs:                         50
 Number of bonded IOBs:                 50  out of    210    23%

Specific Feature Utilization:

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Partition Resource Summary:
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  No Partitions were found in this design.

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=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
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Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 4.215ns

Timing Details:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 321 / 17
-------------------------------------------------------------------------
Delay:               4.215ns (Levels of Logic = 10)
  Source:            a<1> (PAD)
  Destination:       sum<15> (PAD)

  Data Path: a<1> to sum<15>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   0.001   0.688  a_1_IBUF (a_1_IBUF)
     LUT5:I0->O            3   0.097   0.305  carry<2>1 (carry<2>)
     LUT5:I4->O            3   0.097   0.389  carry<4> (carry<4>)
     LUT5:I3->O            3   0.097   0.305  carry<6>1 (carry<6>)
     LUT5:I4->O            3   0.097   0.389  carry<8> (carry<8>)
     LUT5:I3->O            3   0.097   0.305  carry<10>1 (carry<10>)
     LUT5:I4->O            3   0.097   0.389  carry<12> (carry<12>)
     LUT5:I3->O            3   0.097   0.389  cout11 (cout1)
     LUT5:I3->O            1   0.097   0.279  cout2 (cout_OBUF)
     OBUF:I->O                 0.000          cout_OBUF (cout)
    ----------------------------------------
    Total                      4.215ns (0.777ns logic, 3.439ns route)
                                       (18.4% logic, 81.6% route)
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Cross Clock Domains Report:
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Total REAL time to Xst completion: 11.00 secs
Total CPU time to Xst completion: 11.00 secs

-->

Total memory usage is 4617988 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```