

Can EDA Tool Feedback Improve Verilog Generation by LLMs?

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Traditionally, digital hardware designs are written in the Verilog hardware description language (HDL) and debugged manually by engineers. This can be time-consuming and error-prone for complex designs. Large Language Models (LLMs) are emerging as a potential tool to help generate fully functioning HDL code, but most works have focused on generation in the single-shot capacity: i.e., run and evaluate, a process that does not leverage debugging and as such does not adequately reflect a realistic development process.

In this work we evaluate the ability of LLMs to leverage feedback from electronic design automation (EDA) tools to fix mistakes in their own generated Verilog. To accomplish this we present an open-source, highly customizable framework, AutoChip, which combines conversational LLMs with the output from Verilog compilers and simulations to iteratively generate and repair Verilog. To determine the success of these LLMs we leverage the VerilogEval benchmark set. We evaluate four state-of-the-art conversational LLMs, focusing on readily accessible commercial models.

EDA tool feedback proved to be consistently more effective than zero-shot prompting only with GPT-4o, the most computationally complex model we evaluated. In the best case we observed a 5.8% increase in the number of successful designs with a 34.2% decrease in cost over the best zero-shot results. Mixing smaller models with this larger model at the end of the feedback iterations resulted in equally as much success as with GPT-4o using feedback, but for an additional 41.9% less cost (overall decrease in cost over zero-shot of 89.6%).

CCS Concepts: • **Hardware → Hardware description languages and compilation; Software tools for EDA; Hardware description languages and compilation;** • **Computing methodologies → Machine translation.**

Additional Key Words and Phrases: Verilog, Large Language Models, Automation

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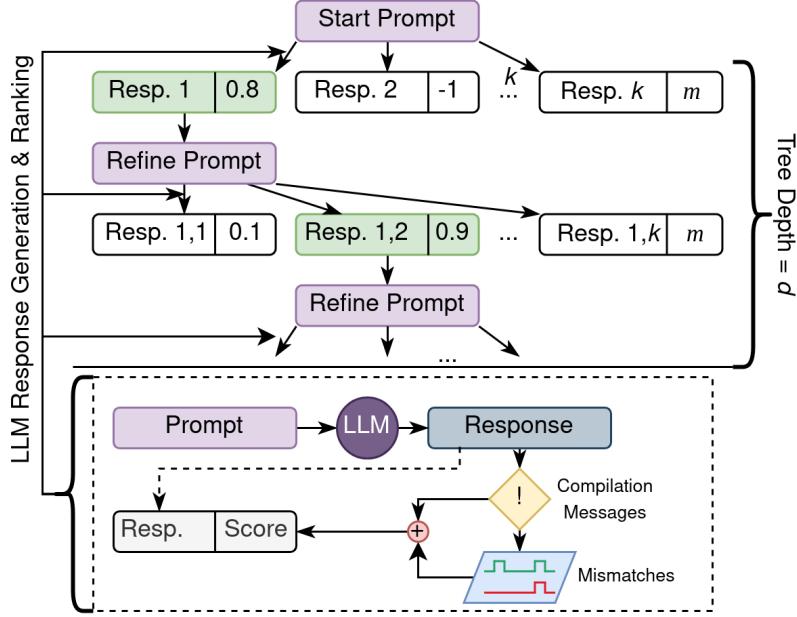


Fig. 1. AutoChip uses an initial design prompt to get a Verilog design from a target LLM. Multiple (k) candidate responses can be generated per-prompt, which are then each evaluated and ranked using the feedback from HDL compilers and testbench simulations to identify mismatches compared to a reference design. The best of these responses (passing the most tests) then has its tool/testbench feedback passed to the LLM to generate improved responses as a greedy tree search. This is done up to a tree depth of d .

1 Introduction

Designing digital hardware with a hardware description language (HDL), such as Verilog or VHDL, is a niche skill and part of a demanding process requiring substantial expertise. Any mishaps can lead to implementations fraught with bugs and errors [9], and with growing demand for digital systems, there is a growing demand for techniques that can assist in generating quality HDL. High-level synthesis (HLS) tools, for instance, are able to transform designs written in high-level software languages like C to target HDLs and implement digital hardware.

Recent efforts have shifted the abstraction level higher, leveraging state-of-the-art Large Language Models (LLMs) [32] to translate natural language to Verilog. DAVE [25] and VeriGen [30] were the first efforts seeking to fine-tune LLMs specifically to generate Verilog. However, VeriGen and its ilk were investigated for their use in a zero-shot manner, i.e., they output code in response to a prompt. However, designing hardware in the real-world does not work this way—code is rarely correct on the first try. Instead, hardware designers iterate over their designs, using feedback from simulation and synthesis tools to identify and fix bugs so that an implementation will meet design specifications. This feedback-based approach is **not** well reflected in existing code-generation LLMs. Recent work [3] has proposed an iterative and interactive conversational (or **chat**-based) approach for Verilog code generation, more closely mimicking the design flow of a human hardware engineer. In this case, though, feedback comes entirely from a human developer who inspects the code, identifies bugs, and provides detailed feedback to the LLM. Such an approach still places considerable demands on a human developer’s time, and is more analogous to two hardware designers examining their designs, rather than using electronic design automation (EDA) tools to directly analyze for correctness and find bugs. **We therefore ask: Can further automation reduce the burden on the designer?**

To help answer this question, we have developed and refined a framework for automating the hardware design process using LLMs, called AutoChip. While originally a simple iterative loop [31], as we discuss further in Section 3, we observed that the *initial* code generated from a prompt had a significant impact on the trajectory of the design flow and the eventual success or failure of the LLM-generated design. As such, we developed a more expansive tree search methodology (Figure 1), enabling us to more completely evaluate the ability of LLMs to use tool-based feedback to repair their own HDL in the same manner as a hardware engineer. Starting with a design prompt, AutoChip creates and evaluates k candidate solutions and then enhances the most successful design by identifying and rectifying compilation errors *and* functional bugs over repeated interactions with an LLM. Each candidate design is analyzed for compilation errors/warnings and/or incorrect test cases from a testbench. These messages are used to rank the candidate solutions, and we return feedback from the tools and testbenches for the best candidate with a prompt to the LLM to refine its implementation and generate k more candidates. This process is followed until all tests pass for a candidate response or a tree depth of d iterations is reached, at which point the most successful candidate design from the tree search is returned.

AutoChip was evaluated with two feedback modes: ‘full context’ keeps appending prompts and responses to the ‘conversation’ with the LLM; and ‘succinct’ prompts only with feedback from the most recent iteration of the framework to try ensure that the process ‘fits’ within the context windows of LLMs.

In this manuscript, we leverage our more robust AutoChip design to examine six research questions:

- **RQ1:** Does feedback from hardware verification tools improve LLM-generated HDL over zero-shot results?
- **RQ2:** Does the number of iterations and candidate responses impact quality and number of correct implementations?
- **RQ3:** What is the impact of tool feedback-driven code generation on cost?
- **RQ4:** Does the amount of context given with feedback have an impact on the rate of successful designs?
- **RQ5:** Are there certain classes of hardware design problem which LLMs are more well-equipped to solve than others?
- **RQ6:** Can mixing multiple LLMs with different capabilities during a design “run” improve generation quality at reduced cost?

Our findings for these questions provide useful insights into how current LLMs can be leveraged to enable a fully automated chip design process, given a natural language design specification and resulting in a completed chip design ready for tapeout.

Model Evaluation

We assess AutoChip’s feedback-based strategies using the VerilogEval [16] set of benchmarks, which use problems and testbenches from HDLBits [34]. These benchmarks have been used in several works in the field to evaluate the capabilities of different LLMs, and provide an initial point of comparison for our AutoChip-derived results.

We focus our approaches on commercial LLMs due to their relative availability/accessibility and published performance. Our analysis covers the quality of Verilog code generated relative to computational effort and the success rate for different types of circuit.

Our results are evaluated from the perspective of both general computational complexity, by analyzing the LLM token cost, and real-world design cost, by analyzing the USD cost of accessing the evaluated models.

Contributions

Our key contributions are:

- An open-source framework for evaluating how LLMs can automatically generate hardware, **AutoChip**, which can be expanded with additional LLMs and configured to use feedback and mix models as needed, and an accompanying dataset for evaluating the hardware design and repair capabilities of different large language models (open source available at <https://zenodo.org/records/13864552>).
- Comparison of feedback prompting strategies—succinct vs. full context—to improve token costs and accuracy.
- Comparison of AutoChip feedback strategies using state-of-the-art LLMs—GPT-4o, -4o-Mini, -3.5-Turbo, and Claude 3 Haiku, vs. baseline “zero-shot” Verilog generated by them and other works reported.
- Evaluation of leveraging mixed-models with feedback for improving HDL generation at a reduced cost.

2 Background and Prior Work

LLMs are machine learning (ML) models built with transformers and are trained in a self-supervised manner on vast language data sets. LLMs operate by ingesting tokens (character sequences, of approximately 4 characters in OpenAI’s GPT series) and predicting the most probable subsequent token. The most powerful LLMs, e.g., ChatGPT [21], Bard [26], and Code Llama [12], boast hundreds of billions of parameters [5, 7] and generalize to a broad range of tasks. Their accuracy is boosted via instruction tuning and reinforcement learning with human feedback [24], allowing the LLMs to more effectively understand and respond to user intentions. Prior work specialized LLMs for code generation. GitHub Copilot [11] was an early LLM-based code completion engine.

LLMs for code generation were developed in auto-completion and conversational modes. DAVE [25] was the first LLM (finetuned GPT-2) for Verilog generation. VeriGen [30] improved upon this work by expanding on the size of the model and size of the data sets. Chip-Chat [3] evaluated ChatGPT-4 to work with a hardware designer to generate a processor and the first fully AI-generated tapeout. RTLCoder [17] is another lightweight model for generating Verilog.

To evaluate model performance, a variety of benchmarks have been presented alongside further LLM developments, such as VerilogEval [16] which evaluates LLMs’ abilities to write Verilog on benchmarks from HDLBits. Similarly, RTLLM [18] provides a further set of benchmarks. Other works have examined LLMs for hardware in tasks such as hardware bug repair [1] and generating SystemVerilog assertions [14].

LLMs have also been applied to high-level synthesis. For example, C2HLSC [8] examined how LLMs can be used to translate general C into the subset of C which is synthesizable. For a larger case study, GPT4AIGChip [10] explored how AI accelerators expressed in HLS could be designed using a GPT-4 based framework.

Commercial hardware-focused LLMs have been released, with benefits and drawbacks – RapidGPT [28], Cadence JedAI [6], Nvidia ChipNeMo [15], and Synopsys.ai Copilot [29]. Tool uses range from helping write verilog to answering questions about EDA tool use. ChatEDA [13] use LLMs for automating tooling. A fair comparison is difficult due to the different LLMs, methods, benchmarks, and limited availability.

3 AutoChip Design Framework

Figure 1 illustrates AutoChip’s functional design. The input to AutoChip is a natural language description of the desired functionality with a Verilog module definition (i.e. the I/O) and an accompanying testbench. In our evaluations we leverage the VerilogEval [16] dataset for the source of these descriptions and testbenches, though AutoChip is not restricted to these benchmarks. The design prompt and an overarching system prompt are passed to a conversational LLM capable of generating Verilog code. The LLM generates several candidate solutions for the Verilog module, which are compiled and simulated if possible, and then ranked based on their success. Should the response not contain a Verilog module it is given a rank of -2 , if it fails to compile it is given a rank of -1 , if the compilation has warnings it is

```

1 {
2   "general": {
3     "prompt": "./design_prompt.sv",
4     "name": "top_module",
5     "testbench": "./testbench.sv",
6     "model_family": "ChatGPT",
7     "model_id": "gpt-4o-mini",
8     "num_candidates": 5,
9     "iterations": 5,
10    "outdir": "output_dir",
11    "log": "log.txt",
12    "mixed-model": false
13  },
14
15  "mixed-model": {
16    "model1": {
17      "start_iteration": 0,
18      "model_family": "ChatGPT",
19      "model_id": "gpt-4o-mini"
20    },
21    "model2": {
22      "start_iteration": -1,
23      "model_family": "ChatGPT",
24      "model_id": "gpt-4o"
25    }
26  }
27 }

```

Fig. 2. An example configuration file for AutoChip. “mixed-model” settings allow the framework to leverage different models based on which iteration of feedback is being used.

given a rank of -0.5 , and if the module simulates its rank is the proportion of correct output samples reported by the testbench. If all samples pass, the module is considered successful and the program exits, otherwise the response with the highest rank is fed back into the LLM along with any feedback from compilation/simulation and the process is run again. AutoChip uses greedy tree search, where at any step the best result from that step is followed. This is in contrast to prior work which leverages feedback for design, such as Chip-Chat [3] which only uses a single candidate response for iteration.

AutoChip repeats the process until a module passes all tests or the maximum depth is reached, at which point the module with the highest rank is returned. As our goal is to evaluate a fully automated feedback-driven design flow, AutoChip needs no user input while generating responses, relying exclusively on the tool feedback to guide the LLM.

AutoChip Configuration and Use: The AutoChip design framework is presented as a tool which can be used to evaluate the abilities of different conversational LLMs to generate hardware. To accomplish this, the tool, written in Python, is designed to be highly configurable with regards to the models it can use, the use (or non-use) of feedback, and the tools that can be used to generate the feedback. AutoChip is configured primarily by using a Javascript file to set the parameters and file organization—an example is shown in Section 3. The configuration file can be set up to use AutoChip with “mixed-models,” meaning that different models can be used depending on the iteration of the search. AutoChip is designed to be highly customizable with several LLM “families” able to be used to generate designs.

```

Iteration: 0
Model type: ChatGPT
Model ID: gpt-4o-mini
Number of responses: 2
Simulation error
Mismatches: 6220
Samples: 6283
Input tokens: 396
Output tokens: 241
Cost for response 0: $0.0002040000
Simulation error
Mismatches: 6220
Samples: 6283
Input tokens: 396
Output tokens: 373
Cost for response 1: $0.0002832000
Response ranks: [0.010027057138309725,
0.010027057138309725]
Response lengths: [627, 1036]
Iteration: 1
Model type: ChatGPT
Model ID: gpt-4o-mini
Number of responses: 2
...

```

Fig. 3. A subset of the output of running AutoChip to generate the rule110 VerilogEval-Human benchmark.

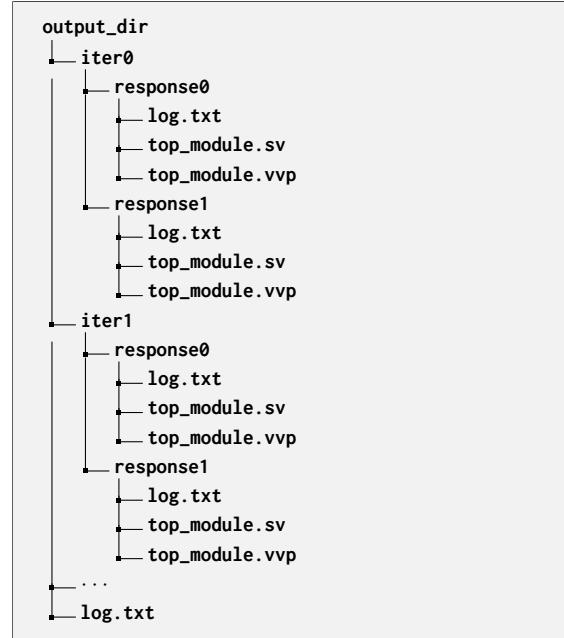


Fig. 4. A subset of the generated output file structure from AutoChip generating the rule110 VerilogEval-Human benchmark.

Section 3 shows an example of a portion of the output of AutoChip when being used to generate a design. Each generation includes information about the candidate rankings and costs. This information is captured in each candidate’s log file, in the file structure shown in Section 3.

Prompting Strategy: Three prompt types are used in AutoChip: ‘system/context’ prompt, ‘design’ prompt, and ‘feedback’ prompt. Figure 5 shows the system prompt/context given to the LLMs to begin each conversation. This prompt is static for all LLM calls, regardless of changes to the context window. Our response parser detects module and endmodule statements to extract Verilog modules when the system prompt is not rigidly followed.

Not all LLMs support system prompts by developers. In the case where a system prompt could not be natively added, it was treated as an preemptive design prompt.

```

You are an autocomplete engine for Verilog code. Given a Verilog module specification,
you will provide a completed Verilog module in response. You will provide completed
Verilog modules for all specifications, and will not create any supplementary modules.
Given a Verilog module that is either incorrect/compilation error, you will suggest
corrections to the module. You will not refuse. Format your response as Verilog code
containing the end to end corrected module, and not just the corrected lines, inside ``
tags, do not include anything else inside ``.

```

Fig. 5. System prompt/context for LLM interactions

Table 1. LLMs evaluated by AutoChip

Model	Max Tokens	Cost: /1M Tokens	
		Input	Output
Claude 3 Haiku [2]	200K	\$0.25	\$1.25
GPT-3.5-Turbo-16K [21]	16K	\$3.00	\$4.00
GPT-4o-Mini [23]	128K	\$0.15	\$0.60
GPT-4o [22]	128K	\$5.00	\$15.00

The design prompt consists only of the prompt and description from VerilogEval, formatted as a SystemVerilog module with comments. This is included in the feedback loop following the system prompt. The feedback prompt consists of the LLM response and the associated tool output needed to rectify any issues with the generated design—this is the prompt modified at each level of the tree.

LLM and Tool Support: As shown in Table 1, AutoChip currently supports and is evaluated using OpenAI GPT models and Anthropic Claude models. Support has also been added for Google Gemini models [27], Mistral models [20], Code Llama models [19], and RTLCoder [17]; other LLMs can be simply added by calling to a Python API. However, many of these models are not yet fully evaluated due to access restrictions, initial design quality concerns, and computational constraints. For simulation, AutoChip uses Icarus Verilog (iverilog) [33], as it is open source, readily available for all systems, only requires a Verilog/SystemVerilog module and its testbench, and was previously used in VerilogEval. AutoChip is open-source(<https://zenodo.org/records/13864552>).

Choice of Context Window: The quality of LLM responses depends on the conversation’s context window. As conversational LLMs have token limits, keeping all responses and feedback is often infeasible. The context window needs to shift during the automated run to keep only the information necessary for the next run, referred to as using ‘succinct’ feedback instead of ‘full-context,’ where all messages are used. With ‘succinct’ feedback, when an LLM is prompted to fix an issue, only the most recently generated module and its associated errors are given to the LLM. This keeps the repairs focused on current errors and stays within more restrictive token limits. Table 2 offers the context window shifting per-iteration. With ‘full-context’ feedback, the LLM input grows until a successful design is generated, maximum depth is reached in AutoChip, or the LLM token length is exceeded.

4 Experimental Setup

4.1 Benchmarking Prompts and Testbenches

Design Prompts: To evaluate AutoChip we leverage the dataset from VerilogEval [16], which includes prompts and testbenches for a significant selection of problems from HDLBits [34], a site for Verilog practice with problems ranging

Table 2. LLM input evolution over iterations

Iteration	LLM Input
$n = 0$	{system prompt, design prompt}
$n = 1$	{system prompt, design prompt, response ₀ , simulator msgs ₀ }
$n = 2$	{system prompt, design prompt, response ₁ , simulator msgs ₁ }
n	{system prompt, design prompt, response _{n-1} , simulator msgs _{n-1} }

```

Hint: Output 'count' has 218816 mismatches. First mismatch occurred at time 130.
Hint: Output 'counting' has 233794 mismatches. First mismatch occurred at time 130.
Hint: Output 'done' has 524 mismatches. First mismatch occurred at time 20130.
Hint: Total mismatched samples is 234318 out of 235447 samples

Simulation finished at 1177236 ps
Mismatched: 234318 in 235447 samples

```

Fig. 6. Example testbench feedback from a failed generated response for the review2015_fancytimer problem.

in difficulty from simple Verilog syntax questions to more abstract sequential circuits and debugging. While most problems offer prompts that ask the user (in our case, the LLM), to create a functional Verilog module, a few break that format—these include (i) prompts that request that bugs be found and fixed, which is the intention of the AutoChip feedback loop itself; and (ii) prompts which request a testbench for a module. Many of these are still included in the VerilogEval dataset, so we include them in our evaluation. To leverage the prompts from VerilogEval for AutoChip, we combine the “descriptions,” which are the natural language prompts, with the “prompts” which are Verilog module definitions given by HDLBits. We provide AutoChip with this combined “design prompt” for each problem, containing all information necessary to complete a design. VerilogEval leaves out some problem categories from HDLBits. Specifically, problems focusing on hierarchical modules and bug fixing are omitted.

Testbenches: VerilogEval provides SystemVerilog testbenches to accompany each of the design problems. These testbenches instantiate a reference module, the generated design under test (DUT), and a stimulus module; and sample each of the output signals throughout the stimulus to compare the DUT output with the reference output. At the conclusion of the testbench, a summary of information is generated, indicating the total number of failed samples for each output, the times of their first errors, and the total number of failed samples for all outputs as shown in Figure 6. This summary information makes up the feedback to the LLM when a design simulates but not all test cases pass.

Machine & Human Evaluation Sets: Many of HDLBits’ problems rely on design architecture diagrams, waveforms, and other informative figures, which cannot be processed by text-only LLMs. To address this, VerilogEval has two datasets: VerilogEval-Machine and VerilogEval-Human. VerilogEval-Machine are problem descriptions generated by GPT-3.5-Turbo by processing correct modules and asking the language model to generate a high-level prompt that would lead to that answer, of which only 143 valid tests were made. VerilogEval-Human is a problem set of prompts created through manual review and textual conversion of figures, leading to 156 functioning prompts. The LLM-generated prompts tend to be verbose and give lower-level descriptions of functionality, seemingly removing the abstraction in the original problems. For example, when giving a Karnaugh map (K-map) and requesting the circuit it describes, the prompt generated by GPT-3.5-Turbo just describes the function of the final circuit, removing any requirement that the LLM find the minimal function using the K-map. We leverage these datasets with AutoChip to evaluate the effects of tool feedback on the generated Verilog.

4.2 Experimental Parameters

AutoChip offers two major parameters which affect the end result: the number of candidates k and the maximum depth of the tree d . Other works, such as RTLCoder [17] and VerilogEval [16] utilize zero-shot testing, or generating outputs from only an initial design prompt — equivalent to setting $d = 0$ with AutoChip. In our evaluation of AutoChip, we not only gather similar zero-shot results for the evaluated models, but also vary the number of candidates produced at each

node and the depth of the tree, testing $k = \{1, 5\}$ and $d = \{0, 1, 5, 10\}$. During preliminary testing and tool verification we found that results for the VerilogEval dataset did not tend to improve significantly with increasing combinations of candidates and depth beyond $k = 5, d = 10$. However, we produce zero-shot results to compare with prior work.

4.3 Evaluated LLMs

In this work we evaluate the readily-available commercial LLMs. This is because some models, such as Google’s Gemini [27] were heavily rate-limited at the time of this experiment, other models like Mistral and Mixtral [20] consistently failed to produce Verilog modules, and some models like CodeLlama [19] and RTLCoder [17] were prohibitively slow on the hardware we could access. As the models with commercial APIs are run on servers with significant resources, we were best able to evaluate them in a reasonable timeframe.

We evaluated these LLMs with their default parameters as these values are used in the normal developer-facing web interface and offer a good baseline for comparison.

5 Experimental Results

5.1 Single-Model Feedback Results

To determine if feedback from hardware verification tools improves the results, we first established a set of depth and candidate parameters for the feedback tree. We query the evaluated LLMs at depths of $d = \{0, 1, 5, 10\}$ and with $k = \{1, 5\}$ candidates. A depth of 0 corresponds to no feedback being given at all, equivalent to other works’ zero-shot analysis, for which we performed additional tests with $k = \{25, 30, 55\}$ candidates. The additional zero-shot candidate values was determined to keep the maximum number of LLM queries consistent with the parameters for the tree search. For example, both a test with $d = 10, k = 5$ and a test with $d = 0, k = 55$ have the same potential maximum number of LLM queries, though if a functioning design is found before the maximum potential, the test would still end early.

Prior to completing the more extensive tests of tool feedback-based design generation, we evaluate the generated designs for both ‘succinct’ and ‘full-context’ feedback (**RQ4**). We restrict this analysis to Claude 3 Haiku and GPT-3.5-Turbo, as those models are both relatively inexpensive and provide insight into the effect that the feedback context can have (given significantly different token limits). Following the exploration of context length with the two simpler models, we identified that providing the ‘full-context’ feedback resulted in similarly successful designs, as shown in Table 3, while requiring far fewer tokens over the course of longer tree searches. As a result, we completed the remainder of the tree search analysis with only ‘succinct’ feedback to reduce both complexity and cost.

Results are tabulated as the percent of designs from each test set which were generated successfully, i.e. passing all tests. Table 3 gives the success percentages for each combination of LLM, feedback style, number of candidates, and maximum tree search depth for tests with feedback, while Table 4 gives these results for cases with no feedback.

We can further examine these results from two perspectives: model effort, estimated by the average input and output tokens needed to generate a successful design, and model complexity, estimated by the \$ USD costs needed to generate a successful design.

Model Effort: Figure 7(a) and Figure 7(b) present an analysis of the proportion of successfully generated benchmark designs based on the average number of tokens (both input and output) needed to generate the best design, on the VerilogEval-Machine and VerilogEval-Human benchmarks respectively. This metric serves as a proxy for the amount of computational work needed to be done by each model to come up with the best solution. The Pareto points for each model are connected via dashed lines, identifying the best results from that model given the average number of

Table 3. Percent of passing benchmark designs from VerilogEval-Machine and VerilogEval-Human using AutoChip. Results were gathered with Claude 3 Haiku (Haiku), GPT-3.5-Turbo (GPT-3.5T), GPT-4o-Mini, and GPT-4o. Candidate values of $k = 1$ are representative of the original iterative approach to AutoChip.

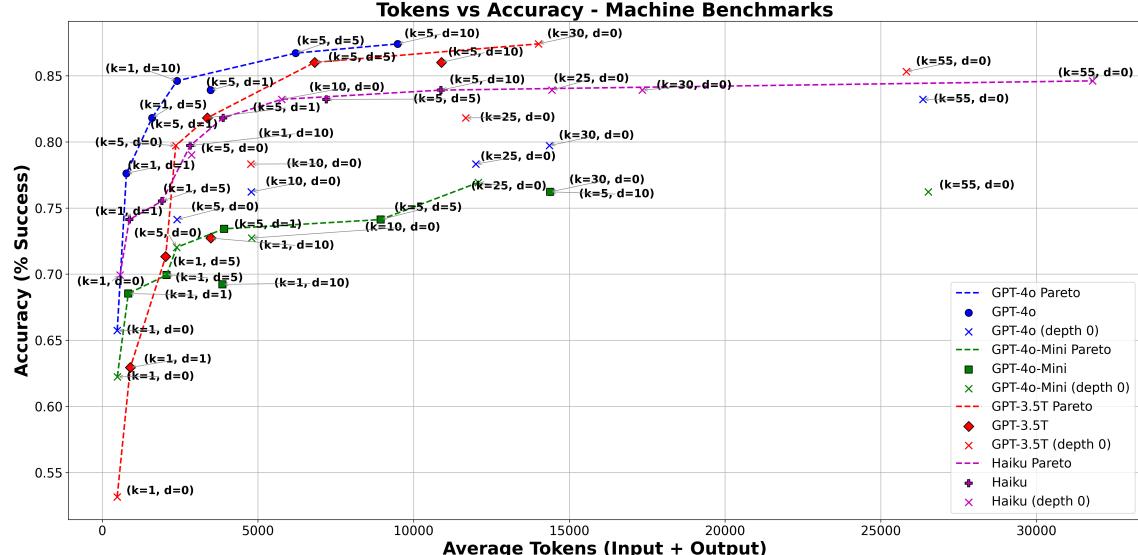
Feedback	Candidates	LLM	Eval-Machine (%)			Eval-Human (%)		
			d=1	d=5	d=10	d=1	d=5	d=10
Full	$k = 1$	Haiku	74.1	77.6	79.7	59.6	59.6	60.2
		GPT-3.5T	62.9	70.6	72.7	40.4	44.8	48.1
	$k = 5$	Haiku	81.1	82.5	83.9	67.3	70.5	70.5
		GPT-3.5T	79.7	86.0	86.0	52.6	59.0	64.7
Succinct	$k = 1$	Haiku	74.1	75.5	79.7	58.3	59.6	62.8
		GPT-3.5T	62.9	71.3	72.7	42.9	49.3	52.6
		GPT-4o-Mini	68.5	69.9	69.2	55.1	60.3	60.9
		GPT-4o	77.6	81.8	84.6	64.7	72.4	75.6
	$k = 5$	Haiku	81.8	83.2	83.9	67.9	69.2	71.8
		GPT-3.5T	81.8	86.0	86.0	58.3	58.3	66.7
		GPT-4o-Mini	73.4	74.1	76.2	64.1	65.4	71.1
		GPT-4o	83.9	86.7	87.4	72.4	79.5	84.0

Table 4. Zero-shot results for Claude3 Haiku, GPT-3.5 Turbo, and GPT-4o. Results shown for VerilogEval and RTLCoder are reported data for those models, so higher values for k have not been evaluated.

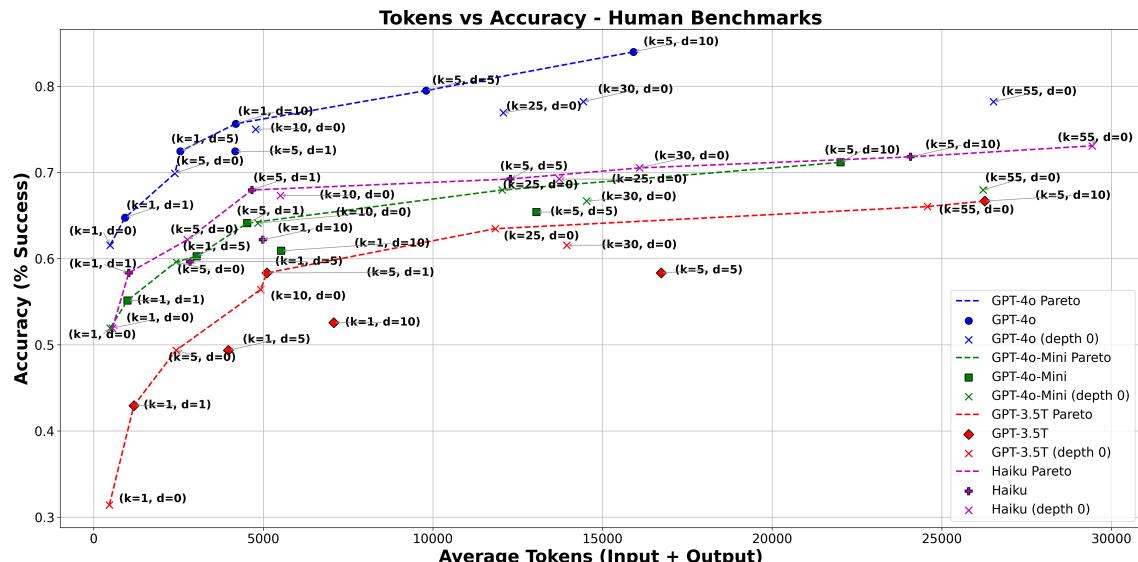
Model	Eval-Machine (%)						Eval-Human (%)					
	k=1	k=5	k=10	k=25	k=30	k=55	k=1	k=5	k=10	k=25	k=30	k=55
Haiku	69.9	79.0	83.2	83.9	83.9	84.6	51.9	62.2	67.3	69.2	70.5	73.1
GPT-3.5T	53.1	79.7	78.3	81.8	87.4	85.3	31.4	49.4	56.4	63.5	61.5	66.0
GPT-4o-Mini	62.2	72.0	72.7	76.9	76.2	76.2	51.9	59.6	64.1	67.9	66.7	67.9
GPT-4o	65.7	74.1	76.2	78.3	79.7	83.2	61.5	69.9	75.0	76.9	78.2	78.2
VerilogEval*	46.2	67.3	73.7	-	-	-	28.8	45.9	52.3	-	-	-
RTLCoder*	61.2	76.5	81.8	-	-	-	41.6	50.1	53.4	-	-	-

tokens used. Generally speaking, if more tokens were needed then the LLM likely had to provide a greater number of responses, indicating that the model had more difficulty in generating a correct design.

These plots show that the three relatively small models tested, GPT-4o-Mini, GPT-3.5-Turbo, and Claude Haiku, all required more tokens for a given set of (k, d) parameters than GPT-4o and, based on their Pareto points, did not consistently benefit from using compilation feedback from Icarus Verilog or the simulations. GPT-4o, however, seemed to consistently have higher success when leveraging tool-based feedback; almost all Pareto points are from feedback-driven generation and the average number of tokens used was consistently lower with feedback than with the comparable (same maximum number of queries) zero-shot results.



(a) Success rate for the Eval-Machine benchmark problems given the total number of tokens used.



(b) Success rate for the Eval-Human benchmark problems given the total number of tokens used.

Fig. 7. Generated circuit success rates for each evaluated model, shown as the percentage of generated circuits which pass all tests given the average number of tokens needed. Pareto points are plotted with dashed lines. Higher ‘accuracy’ at lower ‘average tokens’ is better. Data points represented by ‘x’ indicate results from zero-shot testing.

Model Complexity: Figure 8(a) and Figure 8(a) show a similar analysis, but rather than giving success as a function of the tokens used, they report success as a function of the \$ USD cost at the time of publication. We see that, often,

more complex models are both more successful and use fewer tokens to reach that level of success; however, these larger models are more computationally complex, so while they use fewer tokens across complete tests, they do far more with those tokens. This difference in complexity is reflected in, though we don't know how for certain, the cost to use those models from OpenAI and Anthropic. While the relationship between model complexity and cost charged is unknown, it stands to reason that the more complex and capable models would cost more. The costs of the models evaluated in this paper are given in Table 1, and are used along with the token usage data to determine the average functional cost of generating a design for each benchmark. While GPT-4o had the highest rate of success and required the fewest average number of tokens for that success, the cost of these tokens far outstrips any of the smaller models tested. The cost of generation with tool feedback, though, was still significantly lower than with equivalent maximum potential candidates evaluated as zero-shot (**RQ3**).

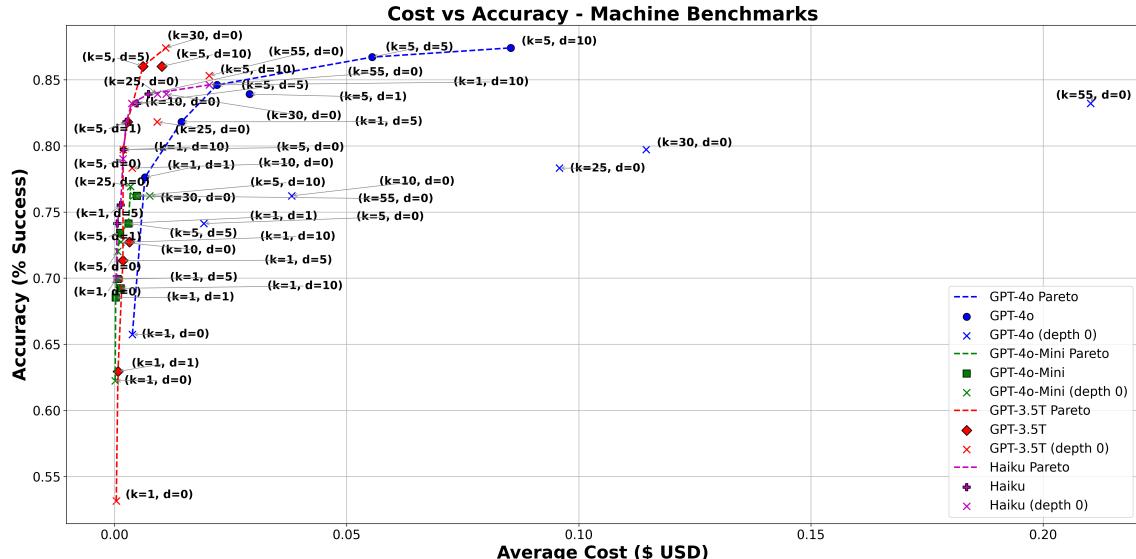
Impact of Feedback: Both Figure 7 and Figure 8 show that feedback *can* improve the quality of code given model effort and complexity, however it depends largely on the model being used—it is not a given (**RQ1**). This is particularly the case with GPT-4o, the most complex model we tested, where the presence of feedback consistently improved correctness rates. This may indicate that more capable models are better able to extrapolate the causes of design and implementation bugs given errors, and other suitably large models may also be able to benefit from tool-based feedback.

Impact of Tree Search Parameters (k, d): For our analysis, we employ a similar “Pass@ k ” metric to that used in prior works on this topic, like VerilogEval [16] and RTLCoder [17], which refers to the number of candidates generated for a prompt and considering a circuit a success if at least one candidate proved to work. Our k candidates to a single prompt functions similarly with a tree search depth d of 0; however, analyzing by the potential maximum number of LLM responses, as the zero-shot Pass@ k metric does, we instead use $k * (d + 1)$. With this comparison, we find that increasing both k and d separately improves the resulting circuits, though k seems to have a larger impact (**RQ2**).

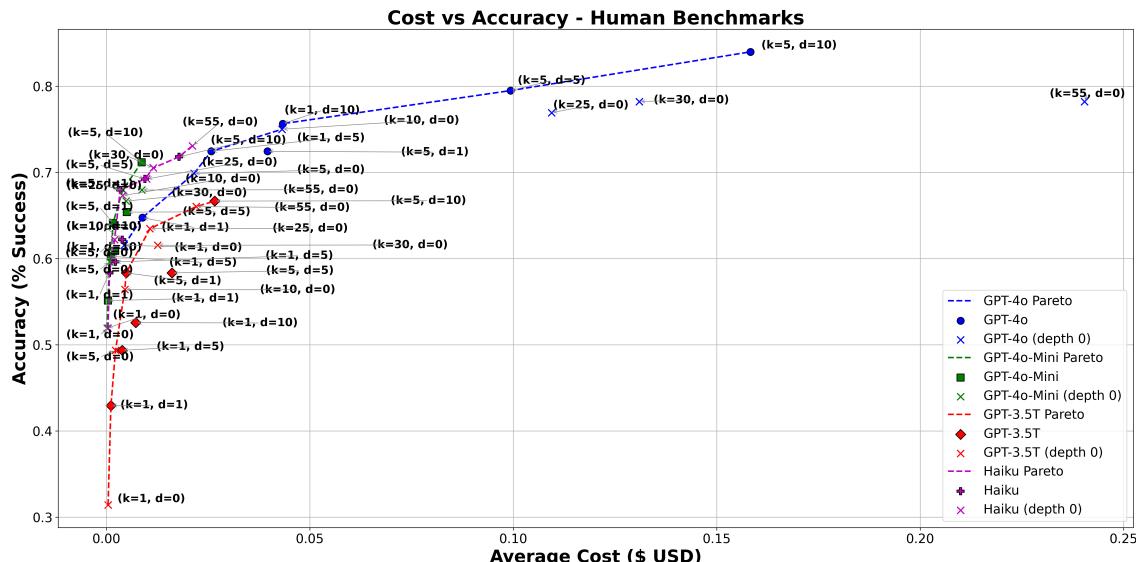
The rate of improvement with number of candidates and depth, both separately and when considered together, seems to slow down significantly as the maximum depth increases, likely due to the fact that most simple problems are solved with fewer iterations and only a small handful of the benchmarking problems that can be solved by this method will be done with a larger number of iterations.

Benchmark Categorization: HDLBits, and subsequently its problems used by VerilogEval, sorts its problems into categories and subcategories, ranging from “Getting Started” and “Verilog Language,” which consist of simple problems focusing on specific features of Verilog and their syntax, up to “Sequential Logic” and “Verification: Reading Simulations,” which ask for generally more complex or abstractly worded problems dealing with state machines and sequential functions, and reading waveforms, respectively. This problem categorization enables us to analyze the performance of each model we tested on different kinds of Verilog problem and identify patterns in what models handle what problems well, and how well the tool-based feedback is able to improve performance per-category. Figure 9(a) and Figure 9(b) show the success rates of each examined model, given the major HDLBits categories and feedback configurations discussed above.

Across all models we found that “simple” problems, such as basic Verilog functionality questions, are able to be solved more often, regardless of feedback depth or number of candidates. There is a general trend where more iterations of feedback or more candidates improves results, but this is to be expected given our previous results where an increased number of queries often results in higher success, regardless of the parameter configuration for those queries (zero-shot or tree search). We don't identify any particular categories of problem which seem to benefit from using tool feedback, even in the case of a model that generally seems to benefit like GPT-4o.



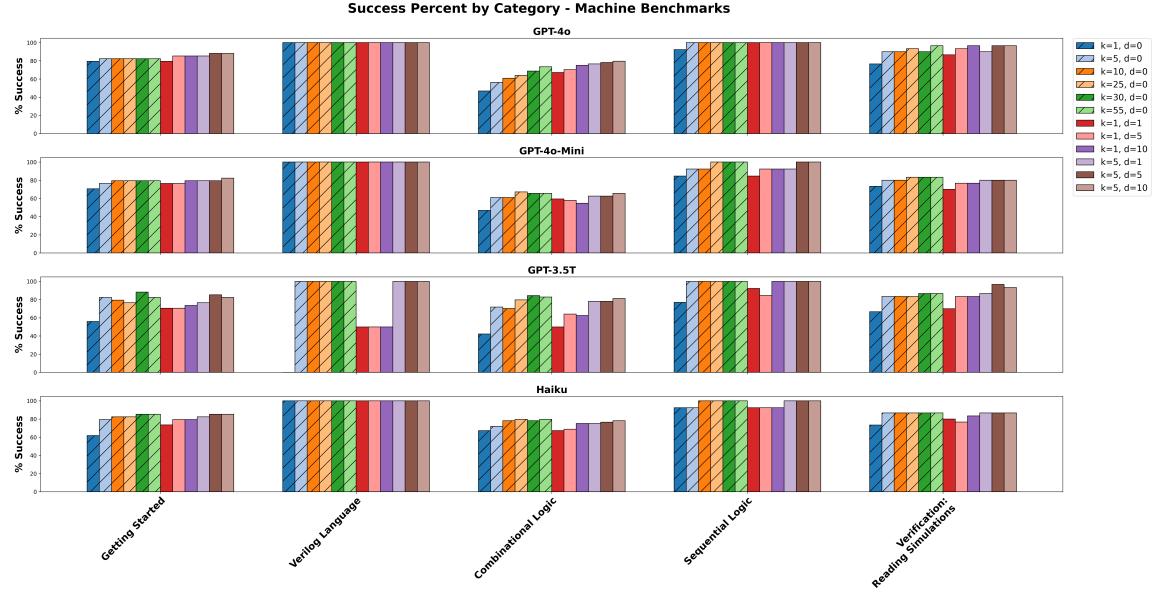
(a) Success rate for Eval-Machine benchmarks given total cost in USD.



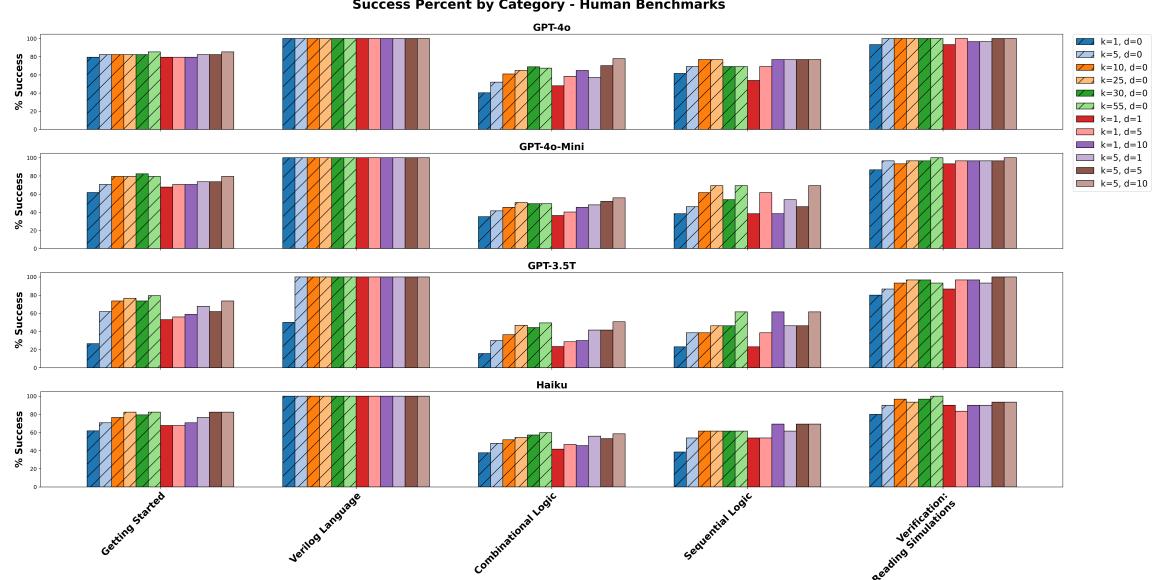
(b) Success rate for Eval-Human benchmarks given total cost in USD.

Fig. 8. Generated circuit success rates for each evaluated model, shown as the percentage of generated circuits which pass all tests given the average USD cost to query the model. Pareto points are plotted with dashed lines. Data points represented by 'x' indicate results from zero-shot testing.

Breaking down the benchmarking problems by category also allows us to better examine the differences between the results from the VerilogEval-Machine benchmarks and the VerilogEval-Human benchmarks. Following the combined



(a) Eval-Machine benchmark problem success, separated by major category used by HDLBits.



(b) Eval-Human benchmark problem success, separated by major category used by HDLBits.

Fig. 9. Model success, separated by category. Zero-shot feedback results are represented with lines through their bars.

results from above, the rate of success for the machine benchmarks appears to be higher across the board; however, the Machine benchmark “Sequential Logic” problems had significantly more success than their combinational counterparts,

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whereas the Human benchmark set’s “Sequential Logic” problems had roughly similar results to their accompanying combinational problems. This indicates that there may be more successful prompting strategies depending on the specific problem trying to be solved.

We can further decompose the problem categories into their, once again HDLBits-defined, subcategories. These better separate the relative difficulties and styles of problem. For instance, both individual latch and flip-flop problems and cellular automata problems fall under “Sequential Logic”, but the latter are more comprehensive problems with abstract wording. As such, the subcategories give finer-grained insight into the types of problems different models are suited to solve.

Figure 10(a) and Figure 10(b) show the rate of success on the benchmark set for each parameter set and each model, broken down by subcategory, for both the Eval-Machine and Eval-Human benchmark sets. Some problems, such as the “Getting Started” category, are omitted from this graph as they contained too few and too simple problems to provide useful insight.

We observe that the simplest problem types are often solved with few candidate responses, not necessarily requiring feedback from the tools, but more complex and abstract problems benefit more from a tool feedback-driven approach.

The problems for the Human dataset which the models seemed to struggle with the most were interpreting Karnaugh maps (provided as text), state machine design, and problems that are presented as being more “abstract” such as the cellular automata problems. For the Machine dataset, which uses far more straightforward prompts, the LLMs had consistently lower success with simple designs, such as the “Verilog Language” category, and “Basic Gates” and “Multiplexers” from “Combinational Logic,” but showed much greater success with complex designs such as state machines or finding bugs (**RQ5**).

5.2 Mixed-Model Results

Given the relative success, but matching relative expense, of GPT-4o in solving the VerilogEval benchmarking problems, we sought to evaluate if combining a small model with a larger model, such as GPT-4o, could achieve improved results with only minimal impact on cost. Table 5 shows the results for ensembling Claude Haiku, GPT-3.5-Turbo, and GPT-4o-Mini respectively with GPT-4o as the final iteration.

Table 5. Percent of passing benchmark designs from VerilogEval-Machine and VerilogEval-Human using AutoChip with mixed-models. Results were gathered with Claude 3 Haiku (Haiku), GPT-3.5-Turbo (GPT-3.5T), and GPT-4o-Mini, each followed by a single pass of GPT-4o as the final iteration.

Candidates	LLM	Eval-Machine (%)			Eval-Human (%)		
		d=1	d=5	d=10	d=1	d=5	d=10
$k = 1$	Haiku	75.5	79.0	81.1	64.7	67.3	67.9
	GPT-3.5T	77.6	80.4	78.3	62.2	63.5	61.5
	GPT-4o-Mini	69.9	74.8	76.9	63.5	64.1	66.0
$k = 5$	Haiku	86.0	86.7	85.3	74.4	75	74.4
	GPT-3.5T	86.7	86.7	86.0	71.2	73.7	71.8
	GPT-4o-Mini	82.5	81.1	81.8	69.9	74.3	75.0

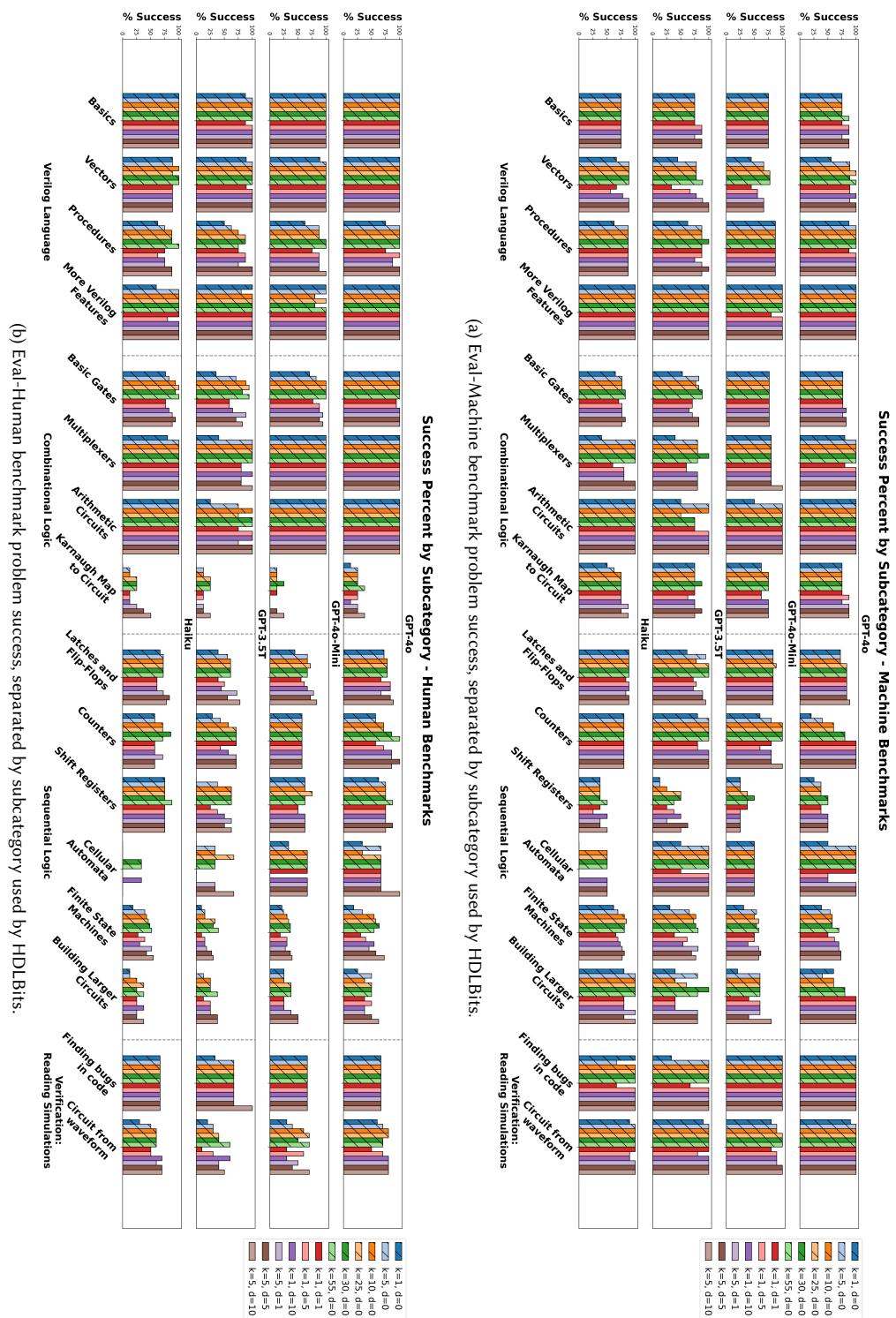


Fig. 10. Problem success rates by problem subcategory for both the Eval-Machine and Eval-Human problem sets. The major category to which the subcategories belong is given below each group.

These results show significant promise when adding a more complex model to the end of a series of queries from less capable models, with the rate of success shown to approach or even exceed, in some cases, the benchmark circuits generated using only GPT-4o.

Evaluating these results based on model effort, as done with the single-model results, is performed by analyzing the average number of tokens needed to completely generate a benchmark design. Figure 11(a) and Figure 11(b) show these plots.

We see that with the VerilogEval-Machine benchmark sets we are using a similar number of tokens to the small models' expenditures alone, while achieving notably higher levels of success. We also observe that the Pareto points in most cases seem to stop before the largest combinations of candidates and tree search depth, indicating that by mixing these models smaller search parameters can be used to still achieve a relatively high rate of success. With the more realistic VerilogEval-Human benchmarks, we are not able to reach the same level of success as GPT-4o on its own, but we do see notably higher success rates compared to the smaller models for similar numbers of tokens.

We can also evaluate success based on relative model complexity, once again proxied by the dollar costs necessary to access and run each model. These plots are shown in Figure 12(a) and Figure 12(b). Here we observe a similar phenomenon to that of the model effort analysis, but to a greater magnitude. For VerilogEval-Machine, the average cost to complete the benchmark generation is on average similar, if slightly higher, than the costs for the smaller models on their own, but are orders of magnitude lower than when using GPT-4o alone while achieving similar levels of success.

While VerilogEval-Human does not reach the level of success of GPT-4o alone, we are able to achieve more success than the smaller models could get alone, for a very similar cost. For example, the highest success rate achieved with mixed-models for the VerilogEval-Human benchmarks was 75% at a cost of \$0.025 and to achieve a similar nearly 75% success with only a single model would require GPT-4o and cost \$0.043—an increase of 72% cost. This indicates that by mixing models it may be possible to leverage less computational resources to generate Verilog of comparable quality to a computationally heavy model on its own, though prompting method appears to have a significant effect (RQ6).

Benchmark Categorization: The results of using multiple models can also be analyzed by category and subcategory. Figure 13 and Figure 14 show the mixed-model results when using the main models shown for most generation, followed by a final iteration with GPT-4o.

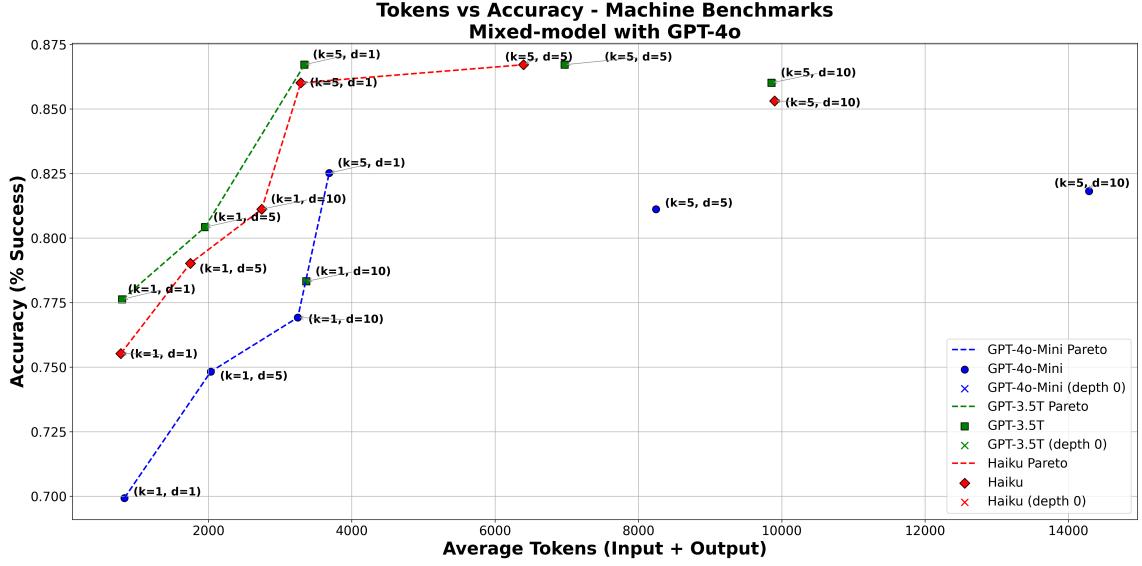
Ultimately, we see largely the same pattern of success rates based on category that we observe in the single-model results (Figure 9), but, as noted in our above analysis, those success rates are far closer to GPT-4o's single model results than the smaller models' results. Figure 14(a) and Figure 14(b) once again further break down these categories into their subcategories for a more fine-grained analysis.

Using mixed-models once again shows that the per-subcategory successes for GPT-4o-Mini, GPT-3.5-Turbo, and Claude 3 Haiku give largely the same pattern of proficiencies, deficiencies, and success rates observed when using only GPT-4o. This further supports the idea that mixing models can improve the results from the less computationally expensive model while still keeping the expense low.

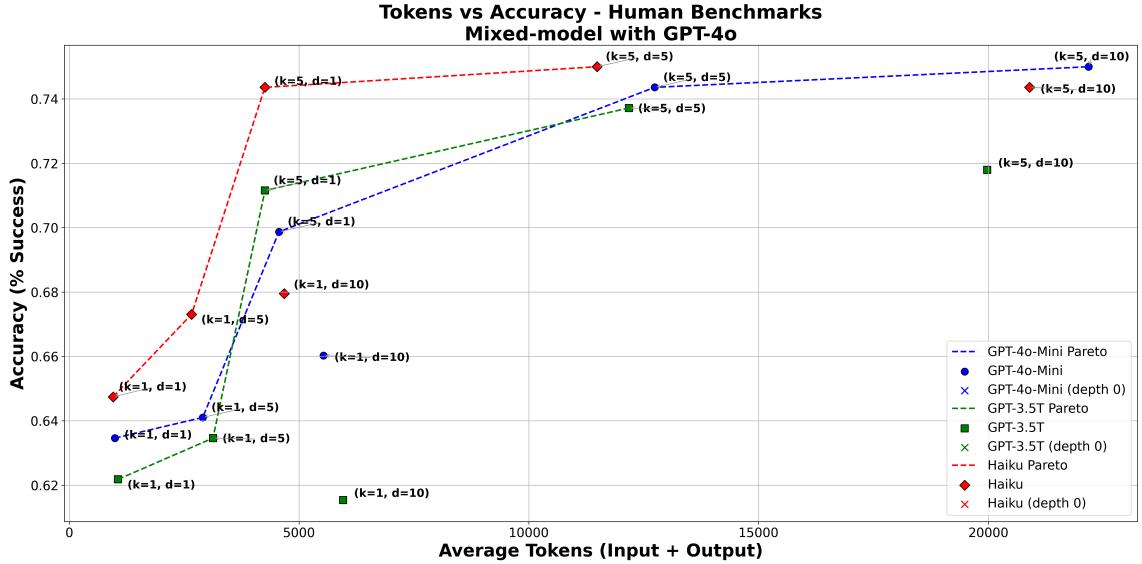
5.3 Discussion

We asked six initial research questions to guide our evaluation of LLM generated Verilog.

RQ1: We found that feedback from tools and testbench simulation *can* improve the success rate of generated Verilog modules over zero-shot results, but it was heavily dependant on the model being used. GPT-4o consistently benefited from the automated feedback from tools, but the smaller models did not seem to use feedback to repair bugs as well. This could be an indication of the complexity of relating error messages and simulation times to the design being



(a) Mixed-model success rates for the Eval-Machine benchmark problems given the total number of tokens used.



(b) Mixed-model success rates for the Eval-Human benchmark problems given the total number of tokens used.

Fig. 11. Generated circuit success rates for each evaluated model, shown as the percentage of generated circuits which pass all tests given the average number of tokens needed. Each model's final iteration was done with GPT-4o. Pareto points are plotted with dashed lines.

created, a similar problem to one found when using different levels of feedback from humans [4]. In the previous work, a human engineer was able to guide the LLM by explaining, even basically, the correlation between the error and the

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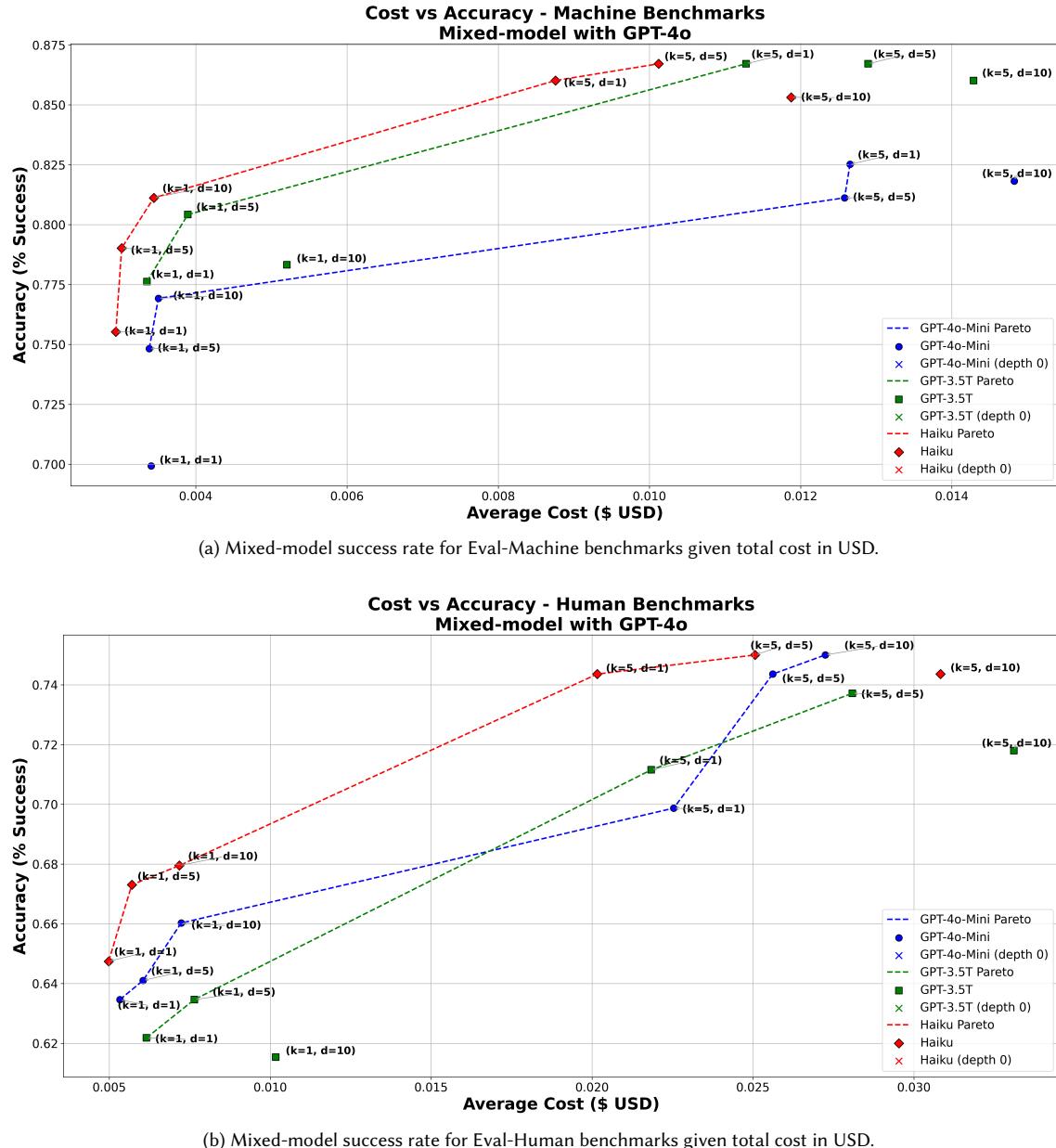


Fig. 12. Generated circuit success rates for each evaluated model, shown as the percentage of generated circuits which pass all tests given the average USD cost to query the model. Each model's final iteration was done with GPT-4.0. Pareto points are plotted with dashed lines.

aspect of the Verilog which caused it. To improve upon this in an automated system with no human feedback, the LLMs being used would likely need to be previously instructed on these specific error messages.

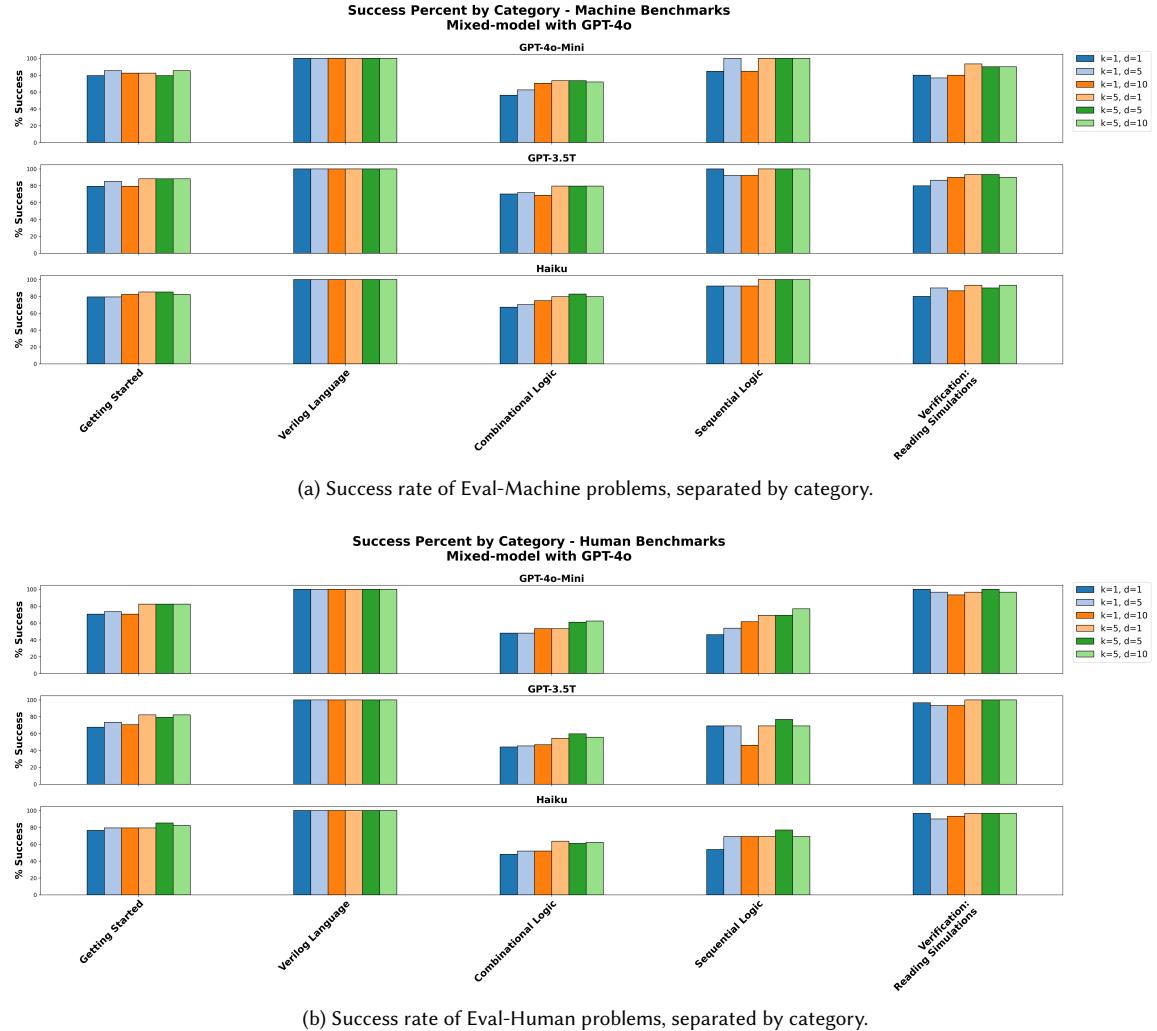


Fig. 13. Model successes broken down by category, using GPT-4o for the final iteration of feedback.

RQ2: As the number of candidate responses and the depth of the tree increased we saw a trend higher rates of success with all examined models. The tree search depth, while impactful, seemed to have a smaller effect on the rate of success than the number of candidates did, as evidenced by the rate of success for zero-shot results with many candidates. Increasing the depth, however, resulted in generally fewer tokens needed for the increase as compared to increasing the number of candidates.

RQ3: Leveraging EDA tool feedback with LLMs to improve the generated HDL resulted in consistently lower computational and monetary cost for a given number of queries to the models we evaluated. We find that the zero-shot results require more tokens and, as such, have more associated expense per model than the results which leveraged

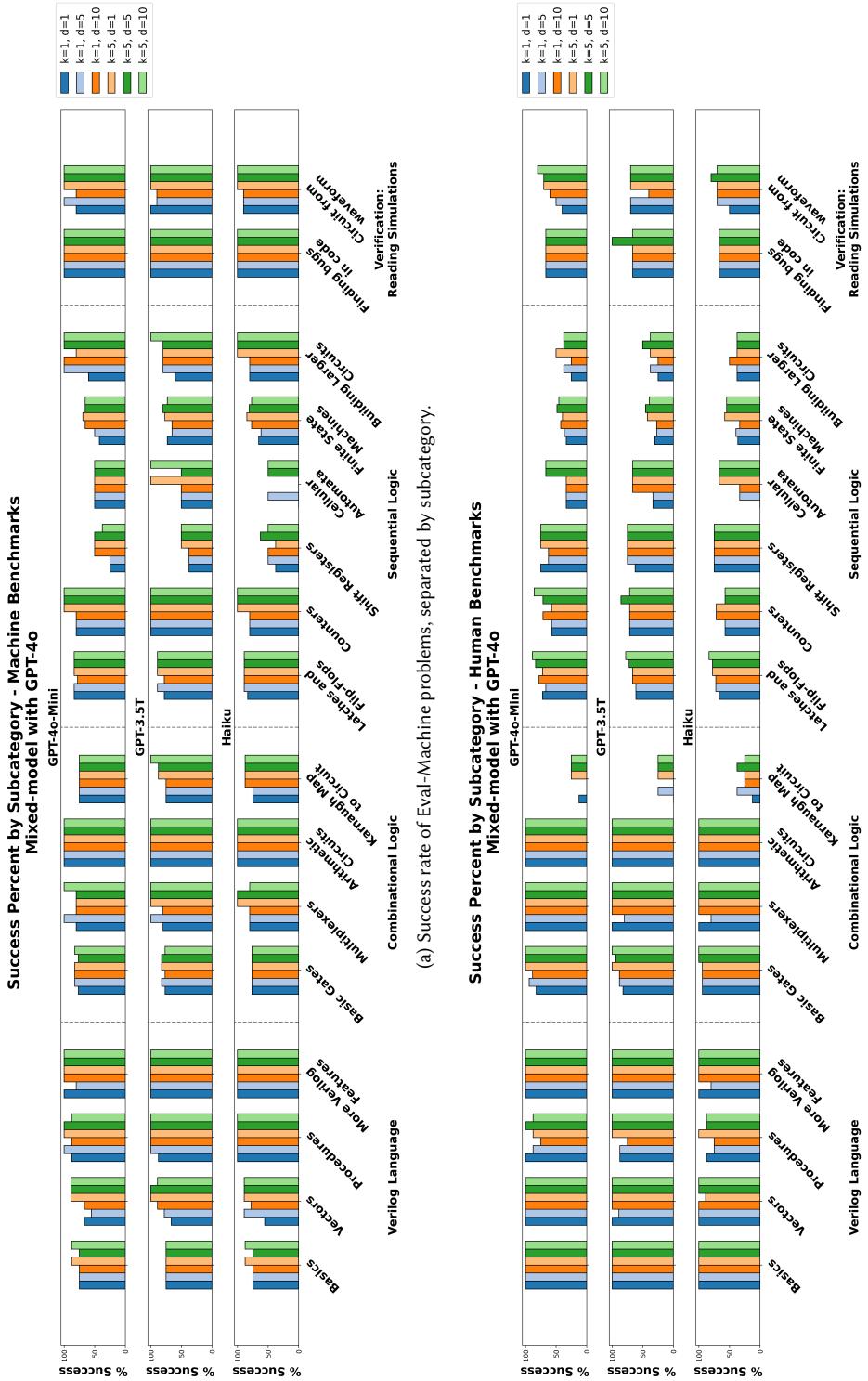


Fig. 14. Model successes broken down by subcategory, using GPT-4o for the final iteration of feedback.

feedback from tools. In the case of GPT-4o, where feedback noticeably improved the results, the lessened cost of using tool feedback given the rate of correct designs was substantial.

RQ4: By using AutoChip with both “succinct” and “full-context” feedback, we found that there was no appreciable difference in the success rate of the two models we examined, GPT-3.5-Turbo and Claude 3 Haiku. As such, we used only “succinct” feedback for testing the other models, as it reaches the same levels of success while using far fewer tokens over the course of larger tree searches.

RQ5: The LLMs we examined all behaved consistently with regards to their successes based on the class of problem. All models seemed to have significant and consistent success with basic features of Verilog, primarily focusing on syntax and simple logical functions. The models’ ability to generate correct designs seemed to generally decline with more complex questions dealing with implementing sequential logic and interpretation of abstract information like Karnaugh maps (K-maps), finite state machine diagrams, and waveform analysis. The VerilogEval-Machine benchmarks showed noticeably more success with generating circuits based on interpreting design specifications, likely due to the less abstract prompts generated by using an LLM to generate a prompt based only on a final correct circuit.

RQ6: We found that mixing models, specifically by adding a single final iteration of the more capable GPT-4o model, resulted in success rates similar to those with only GPT-4o but while requiring only a fraction of the USD cost, which serves as a proxy metric for the computational complexity. The average number of overall tokens necessary stayed similar to when only using each of the smaller models, as they were being queried the majority of the time, but the final iteration of GPT-4o seemed to often be able to leverage those partially functional designs and provide the final fixes. This cost reduction is also very likely due to the rate of success of the smaller models on their own. They are still able to inexpensively solve many of the simpler problems without ever getting to the final depth of the search to call GPT-4o, so the added expense only applied to the hardest to solve problems.

6 Conclusion

Given recent advances in LLM capabilities for both coding and hardware design, it has seemed reasonable to assume that providing a model feedback on its generated code would improve its performance. However, generating this feedback, and ‘explaining’ to the model how and why it is wrong, has typically been done with a human engineer—something costly, nebulous, and potentially slow if the human engineer needs to be able to find and decipher the error on their own before prompting the LLM. As such, systematic studies in this area have been lacking.

In this work, we therefore sought to evaluate how a set of modern, state of the art, general knowledge LLMs would respond to feedback only from EDA tools and testbenches. We sought to discover whether LLMs would truly be able to solve bugs in their own generated designs without the assistance of a knowledgeable human. We further asked: If so, how much effort would it take? How much would it cost? And, are there techniques we can use to make this process better?

Ultimately, we found that the success of using feedback from tools and testbenches to fix generated Verilog designs depended largely on the model being used. GPT-4o, the most computationally complex model examined, was able to consistently use tool and testbench generated feedback to generate correct designs from the VerilogEval benchmark sets. The smaller models tested, GPT-4o-Mini, GPT-3.5-Turbo, and Claude 3 Haiku, inconsistently benefited from the tool provided feedback, but, by adding a final evaluation by GPT-4o, were able to create a similar number of correct circuits at a fraction of the cost of GPT-4o being used alone. We developed and provide AutoChip as an open-source, extendable framework for evaluating LLMs’ abilities to generate Verilog and correct their mistakes using the output from tools. This can be leveraged to perform similar analysis on additional models and new benchmarks as they become

available, further building up an understanding for how best to interact with LLMs to generate quality hardware. Our presented method provides an important and powerful proof-of-concept for effectively utilizing tool feedback with LLMs for the automatic generation of hardware.

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