

# RTL CHALLENGE

**DAY -13:-** Verilog Code for Implementation of Decoder.

**Software used:-** Xilinx Vivado(2023.1)

**Theory:**

**Decoder:-**

In the realm of computing and communication, a 'decoder' assumes diverse roles

crucial for data interpretation and signal processing. In computing, it serves as the

counterpart to encoders, unwinding encoded data back into its original format,

ensuring seamless information retrieval and compatibility across systems. Within

the realm of artificial intelligence, particularly in sequence modeling tasks, such as

language translation or text generation, a decoder stands as an essential component

alongside the encoder, orchestrating the generation of output sequences based on

the encoded input representations. Moreover, in communication systems, decoders

play a pivotal role in extracting meaningful information from encoded signals,

enabling accurate interpretation and further processing of transmitted data.

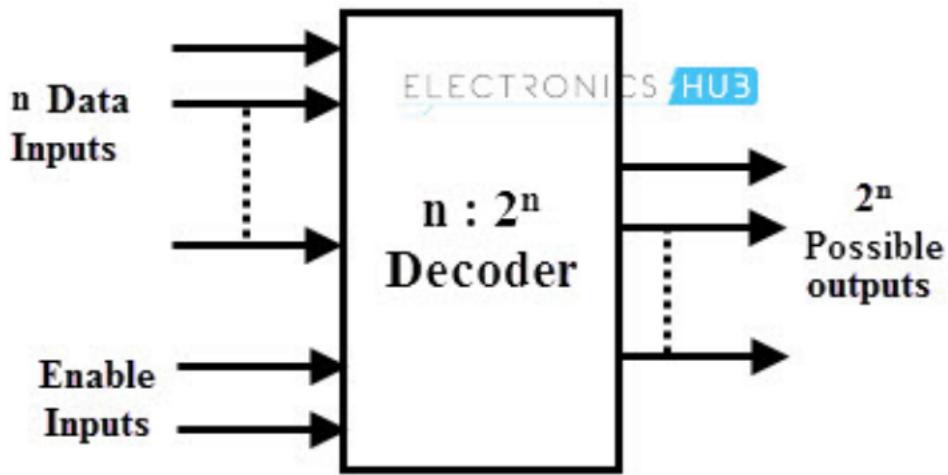
Whether unraveling encoded messages in computing, generating output sequences

in machine learning, or deciphering signals in communication systems, the decoder

embodies the essence of decoding, facilitating the flow of information across

diverse domains.

## Circuit Diagram:



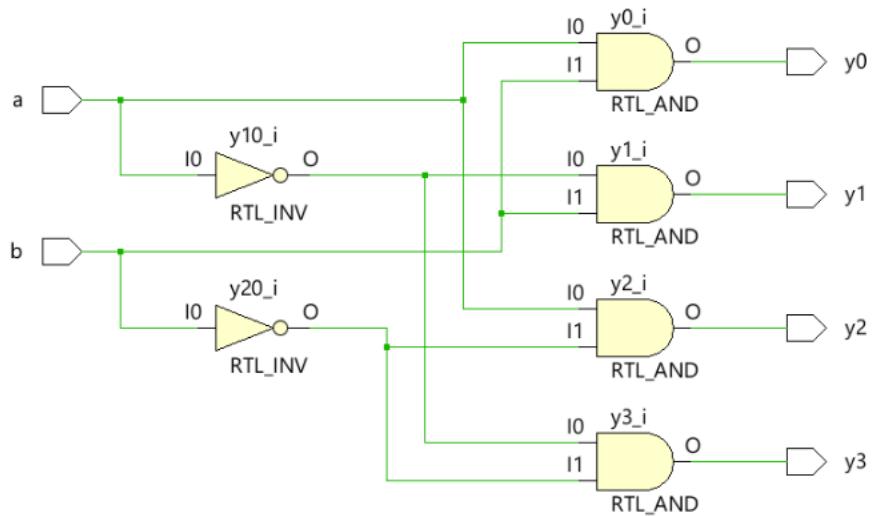
## Code for Decoder 2 to 4:-

```
| module Decoder2to4(
|   input a,b,
|   output y0,y1,y2,y3
| );
|   and(y0,a,b);
|   and(y1,!a,b);
|   and(y2,a,!b);
|   and(y3,!a,!b);
| endmodule
```

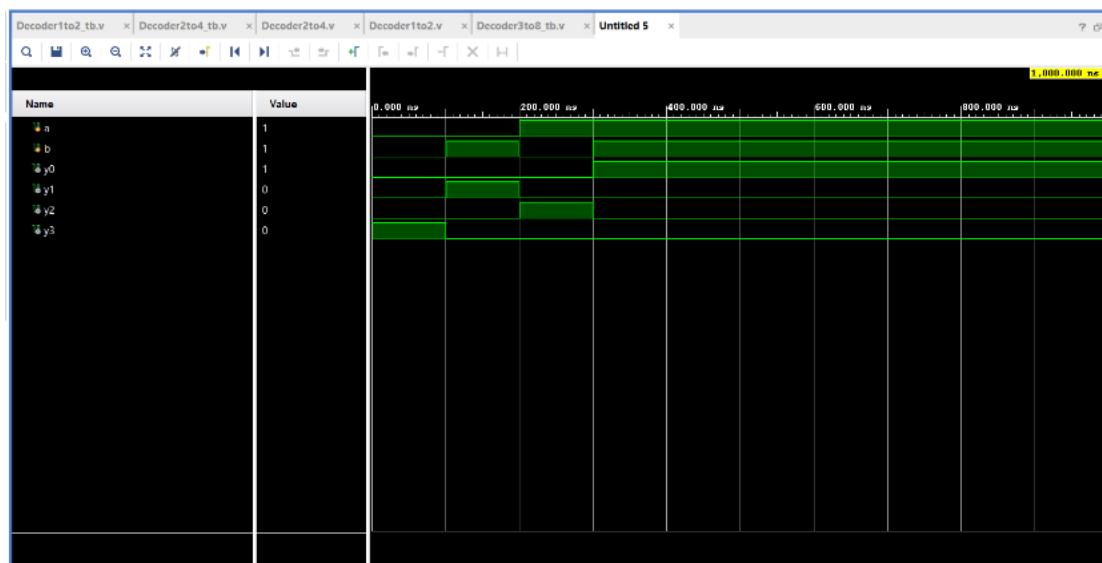
## Test Bench:-

```
module Decoder2to4_tb;
reg a,b;
wire y0,y1,y2,y3;
Decoder2to4 uut (.a(a), .b(b), .y0(y0), .y1(y1), .y2(y2), .y3(y3));
initial
begin
  a=0;b=0;#100;
  a=0;b=1;#100;
  a=1;b=0;#100;
  a=1;b=1;#100;
end
endmodule
```

## Schematic:-



## Waveforms:-



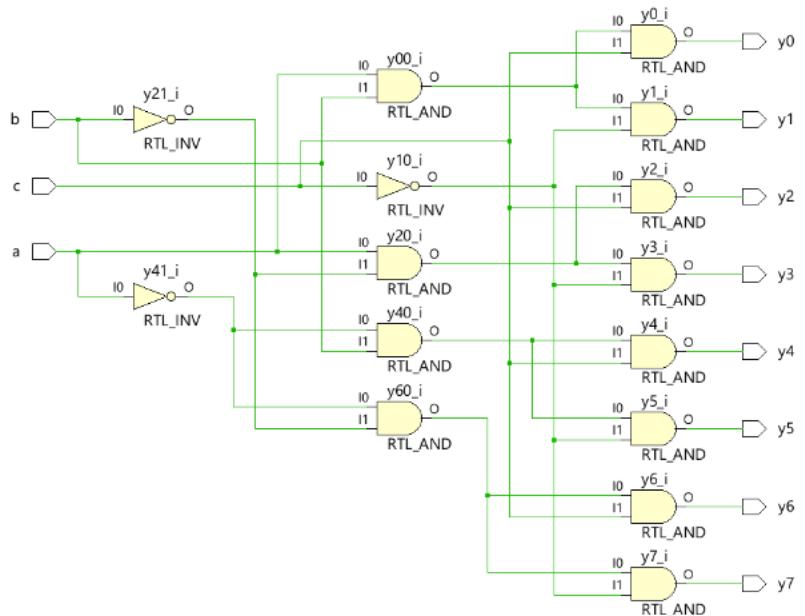
## Code for Decoder 3 to 8:-

```
) module Decoder3to8 (
    input a,b,c,
    input y0,y1,y2,y3,y4,y5,y6,
);
    and(y0,a,b,c);
    and(y1,a,b,!c);
    and(y2,a,!b,c);
    and(y3,a,!b,!c);
    and(y4,!a,b,c);
    and(y5,!a,b,!c);
    and(y6,!a,!b,c);
    and(y7,!a,!b,!c);
) endmodule
```

## Test Bench:-

```
module Decoder3to8_tb;
reg a,b,c;
wire y0,y1,y2,y3,y4,y5,y6,y7;
Decoder3to8 uut (.a(a), .b(b), .c(c), .y0(y0), .y1(y1), .y2(y2), .y3(y3), .y4(y4), .y5(y5), .y6(y6), .y7(y7));
initial
begin
    a=0;b=0;c=0;#100;
    a=0;b=0;c=1;#100;
    a=0;b=1;c=0;#100;
    a=0;b=1;c=1;#100;
    a=1;b=0;c=0;#100;
    a=1;b=0;c=1;#100;
    a=1;b=1;c=0;#100;
    a=1;b=1;c=1;#100;
end
endmodule
```

## Schematic:-



## Waveforms:-

