

RTL CHALLENGE

DAY -14:- Verilog Code for Implementation of 4*1 Multiplexer using 2*1 Multiplexer

Software used:- Xilinx Vivado(2023.1)

Theory:

4*1 Multiplexer using 2*1:

A 4-to-1 MUX has four data inputs, two select lines, and one output.

A 2-to-1 MUX has two data inputs, one select line, and one output.

By strategically cascading 2-to-1 MUXes, we can achieve the functionality of selecting one out of four data inputs for the final output based on the select lines.

Implementation:

Divide the four data inputs into two pairs (A0, A1) and (B0, B1).

Use two 2-to-1 MUXes: Each MUX takes one pair of inputs (A0, A1) and (B0, B1). The select line for each MUX determines which input of the pair gets passed to the next stage.

Select Lines for Stage 1: The select lines for these MUXes can be the first select line (S0) of the final 4-to-1 MUX.

Now you have two outputs from the first stage MUXes.

Final MUX: Use another 2-to-1 MUX with these two outputs as inputs.

Select Line for Final Stage: The select line for this final MUX becomes the second select line (S1) of the overall 4-to-1 MUX.

Code for 2*1 multiplexer:

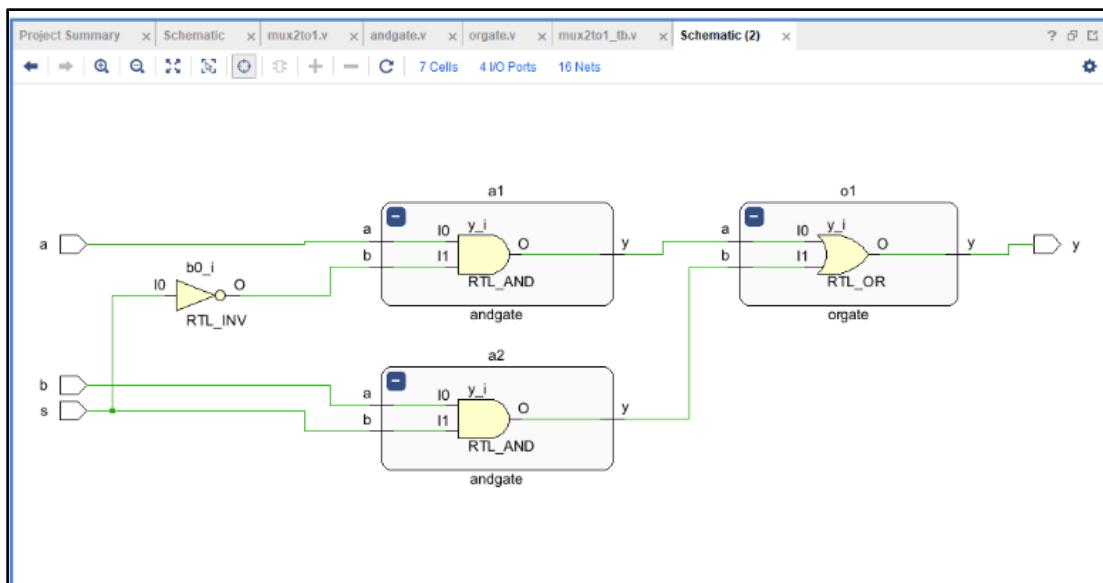
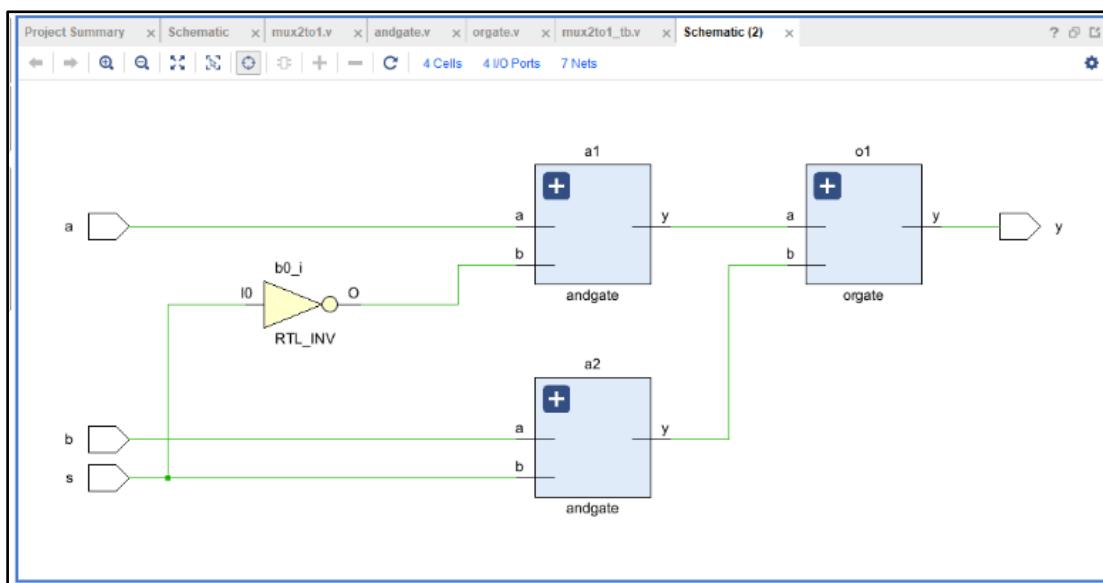
```
module mux2tol(
    input a,b,
    input s,
    output y
);
    andgate a1 (.a(a),.b(!s),.y(w1));
    andgate a2 (.a(b),.b(s),.y(w2));
    orgate o1 (.a(w1),.b(w2),.y(y));
endmodule
```

TESTBENCH:

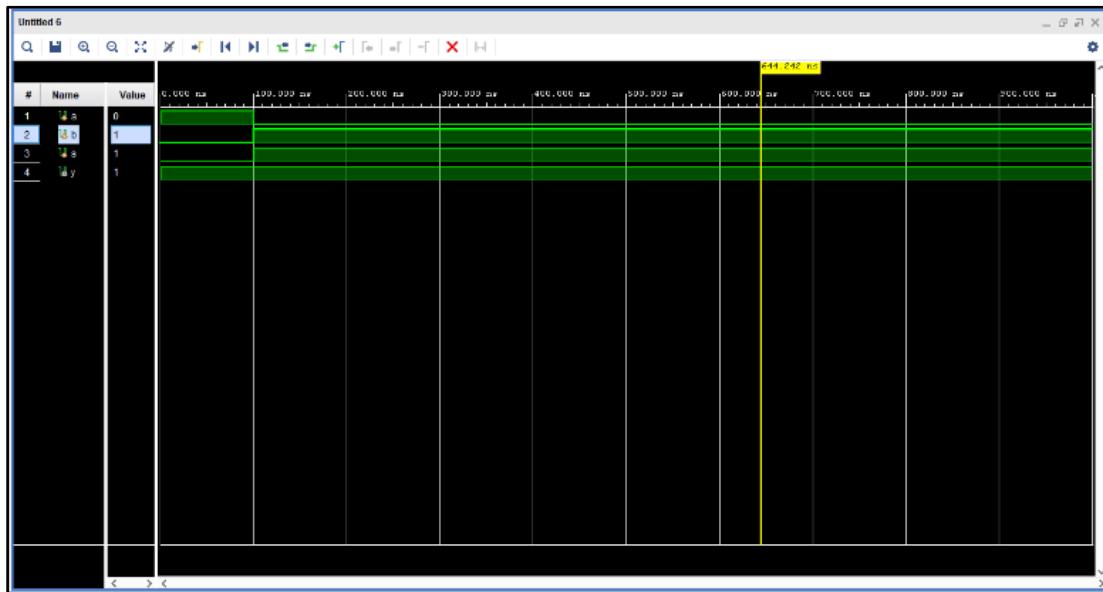
```
module mux2to1_tb();
reg a,b,s;
wire y;
mux2to1 uut (.a(a), .b(b), .s(s), .y(y));
initial
begin
    a=1;b=0;s=0;#100;
    a=0;b=1;s=1;#100;

end
endmodule
```

RTL SCHEMATIC:



OUTPUT WAVEFORM:



4*1 MULTIPLEXER Using 2*1 Multiplexer:

DESIGN CODE:

```
module mux4tolusing2tol(
    input a,b,c,d,
    input s0,s1,
    output y
);

mux2tol m1 (.a(a),.b(b),.s(s0),.y(w1));
mux2tol m2 (.a(c),.b(d),.s(s0),.y(w2));
mux2tol m3 (.a(w2),.b(w1),.s(s1),.y(y));

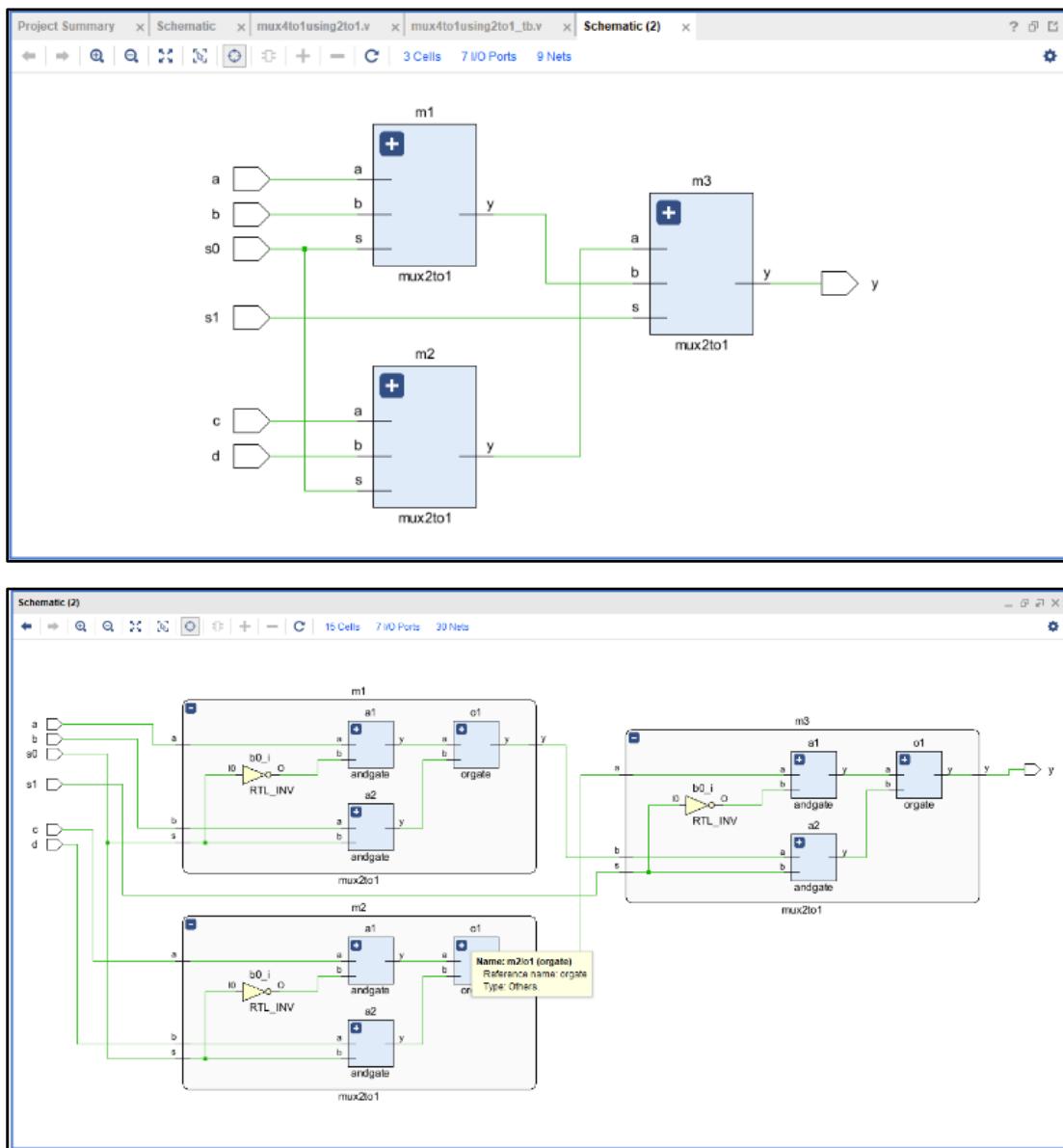
endmodule
```

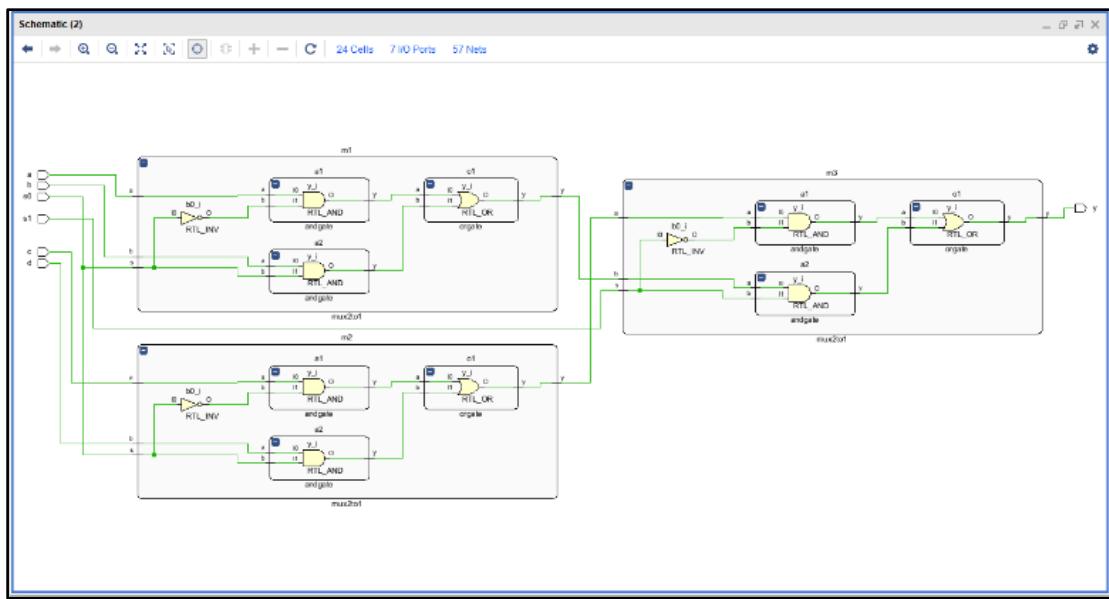
TEST BENCH:

```
module mux4tolusing2tol_tb();
reg a,b,c,d;
reg s0,s1;
wire y;
mux4tolusing2tol uut (.a(a),.b(b),.c(c),.d(d),.s0(s0),.s1(s1),.y(y));
initial
begin
    a=1;b=0;c=0;d=0;s0=0;s1=0;#100;
    a=0;b=1;c=0;d=0;s0=0;s1=1;#100;
    a=0;b=0;c=1;d=0;s0=1;s1=0;#100;
    a=0;b=0;c=0;d=1;s0=1;s1=1;#100;

end
endmodule
```

RTL SCHEMATIC:





OUTPUT WAVEFORM:

