

# RTL CHALLENGE

Day16 :- Verilog code for implementation of PRIORITY ENCODER:

Software used:- Xilinx vivado (2023.1)

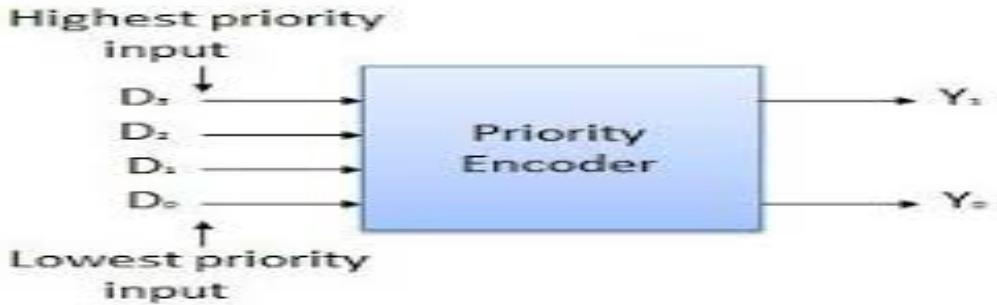
Theory:-

## PRIORITY ENCODER:

A priority encoder is a digital circuit that converts multiple binary inputs into a single output signal, indicating the highest-priority active input. It is commonly used in digital systems for tasks such as interrupt handling, address decoding, and data multiplexing.

The priority encoder assigns a priority to each input and generates a binary output code corresponding to the highest-priority active input. If multiple inputs are active simultaneously, the priority encoder outputs the code for the input with the highest priority. The output code typically corresponds to the position of the highest-priority active input, with lower-numbered inputs having higher priority.

Priority encoders are often used in conjunction with multiplexers or demultiplexers to efficiently handle multiple inputs or select one of several inputs for further processing. They are essential components in many digital systems, especially in applications where efficient handling of multiple inputs is required.



### DESIGN CODE:-

```
module priorityencoder(
    input a,b,c,d,
    output y0,y1
);
    and(w1,b,!c);
    or(y0,w1,d);
    or(y1,c,d);
endmodule
```

### TEST BENCH:-

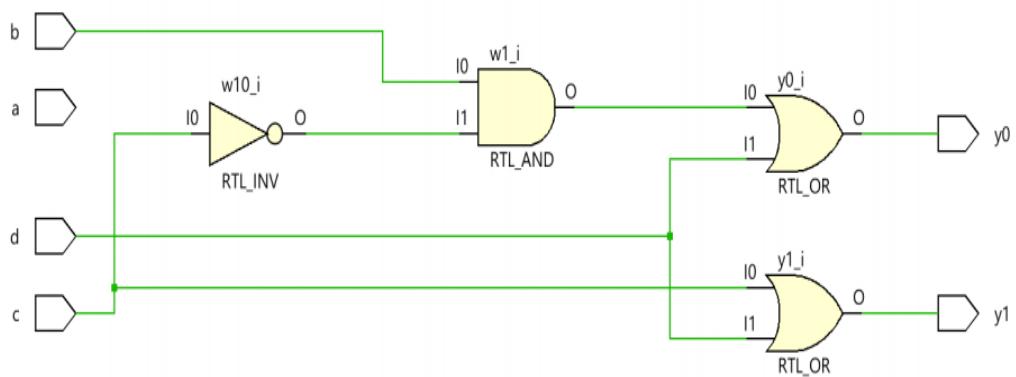
```
module priorityencoder_tb();
    reg a,b,c,d;
    wire y0,y1;
    priorityencoder uut(.a(a),.b(b),.c(c),.d(d),.y0(y0),.y1(y1));
    initial
        begin
            a=0;b=0;c=0;d=0;#100;
```

```

a=1;b=0;c=0;d=0;#100;
a=0;b=1;c=0;d=0;#100;
a=0;b=0;c=1;d=0;#100;
a=0;b=0;c=0;d=1;#100;
end

```

## RTL SCHEMATIC:-



## RTL SIMULATION:

