

# RTL CHALLENGE

**DAY-19:-** Verilog Code for Implementation of SUBTRACTORS Using Behavioral/Conditional Statements.

**Software used:-** Xilinx Vivado(2023.1)

**Half Subtractor using Conditional/Behavioral:**

**DESIGN CODE:-**

```
// Design Name: Cpnditional
// Module Name: HalfSubtractorUsingConditional_tb
// Project Name: RTL Challenge

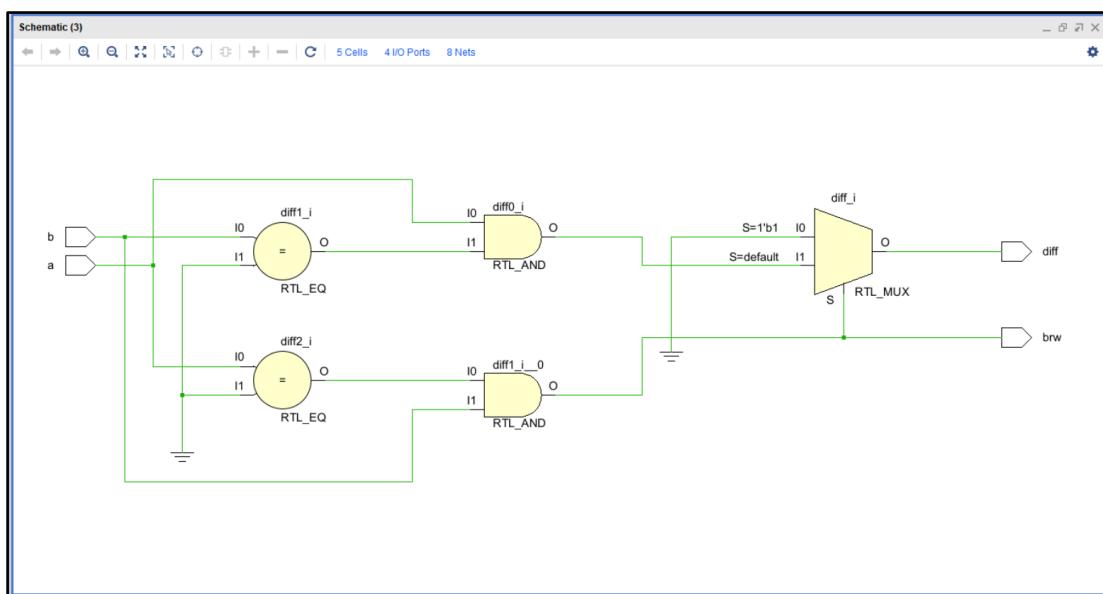
module HalfSubtractorUsingConditional(
    input a,b,
    output reg diff,brw
);
    always@(a,b)
    begin
        if(a==0&&b==1)
            begin
                diff=0;
                brw=1;
            end
        else if(a==1&&b==0)
            begin
                diff=1;
                brw=0;
            end
        else
            begin
                diff=0;
                brw=0;
            end
    end
endmodule
```

## TEST BENCH:-

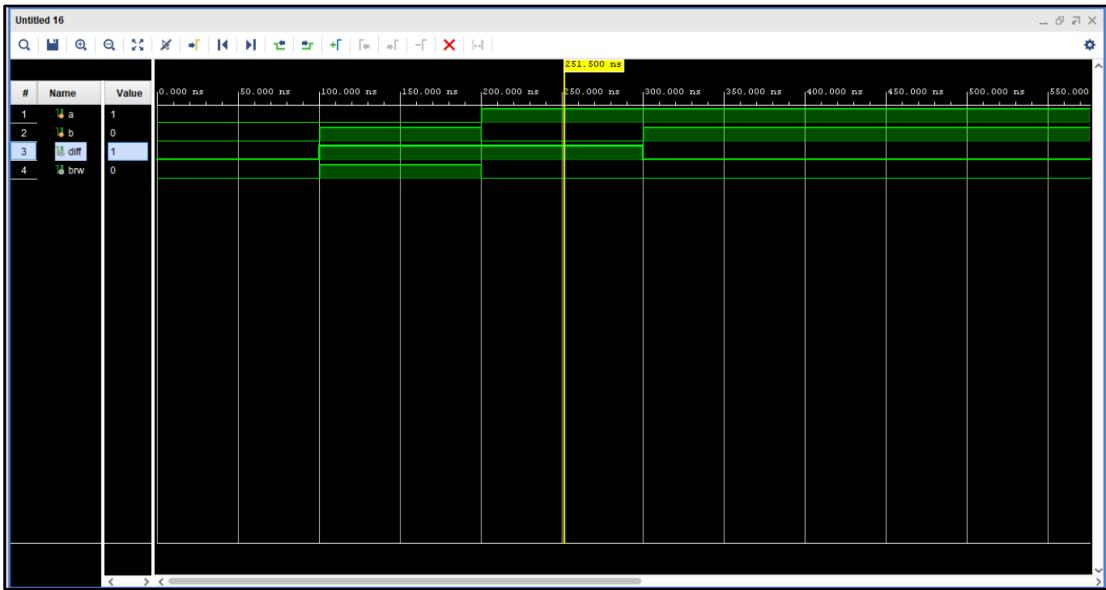
```
// Design Name: Cconditional
// Module Name: HalfSubtractorUsingConditional_tb
// Project Name: RTL Challenge

module HalfSubtractorUsingConditional(
    input a,b,
    output reg diff,brw
);
    always@ (a,b)
    begin
        if(a==0&&b==1)
            begin
                diff=1;
                brw=1;
            end
        else if(a==1&&b==0)
            begin
                diff=1;
                brw=0;
            end
        else
            begin
                diff=0;
                brw=0;
            end
    end
endmodule
```

## RTL SCHEMATIC:-



## OUTPUT WAVEFORM:-



## FULL SUBTRACTOR USING CONDITIONAL:-

```
// Design Name: Conditional  
// Module Name: FullAdderUsingConditional  
// Project Name: RTL DESIGN
```

```
module FullSubtractorUsingConditional(  
    input a,b,c,  
    output reg diff,brw  
,  
    always@(a,b,c)  
    begin  
        if(a==0&&b==0&&c==0)  
            begin  
                diff=0;  
                brw=0;  
            end  
        else if(a==0&&b==1&&c==1)
```

```
begin
    diff=0;
    brw=1;
end

else if(a==1&&b==0&&c==0)
begin
    diff=1;
    brw=0;
end

else if(a==1&&b==0&&c==1)
begin
    diff=0;
    brw=0;
end

else if(a==1&&b==1&&c==0)
begin
    diff=0;
    brw=0;
end

else
begin
    diff=1;
    brw=1;
end

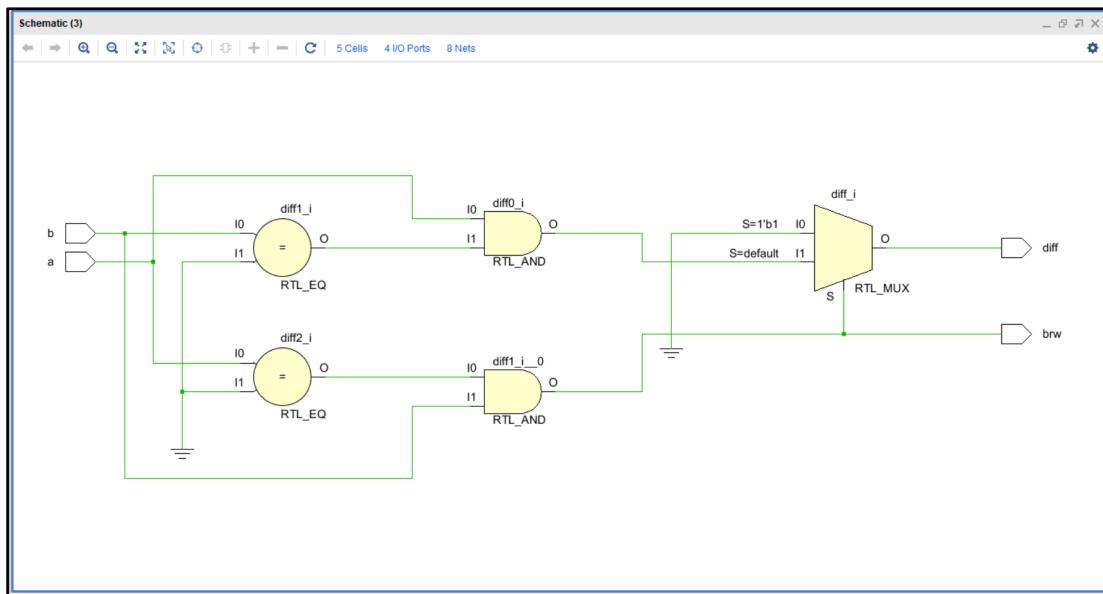
end
endmodule
```

## TEST BENCH:-

```
// Design Name: TEST BENCH
// Module Name: FullSubtractorUsingConditional_tb
// Project Name: RTL DESIGN

module FullSubtractorUsingConditional_tb();
reg a,b,c;
wire diff,brw;
FullSubtractorUsingConditional uut (
    .a(a),
    .b(b),
    .c(c),
    .diff(diff),
    .brw(brw)
);
initial
begin
    a=0;b=0;c=0;#100;
    a=0;b=0;c=1;#100;
    a=0;b=1;c=0;#100;
    a=0;b=1;c=1;#100;
    a=1;b=0;c=0;#100;
    a=1;b=0;c=1;#100;
    a=1;b=1;c=0;#100;
    a=1;b=1;c=1;#100;
end
endmodule
```

## RTL SCHEMATIC:-



## OUTPUT WAVEFORM:-

