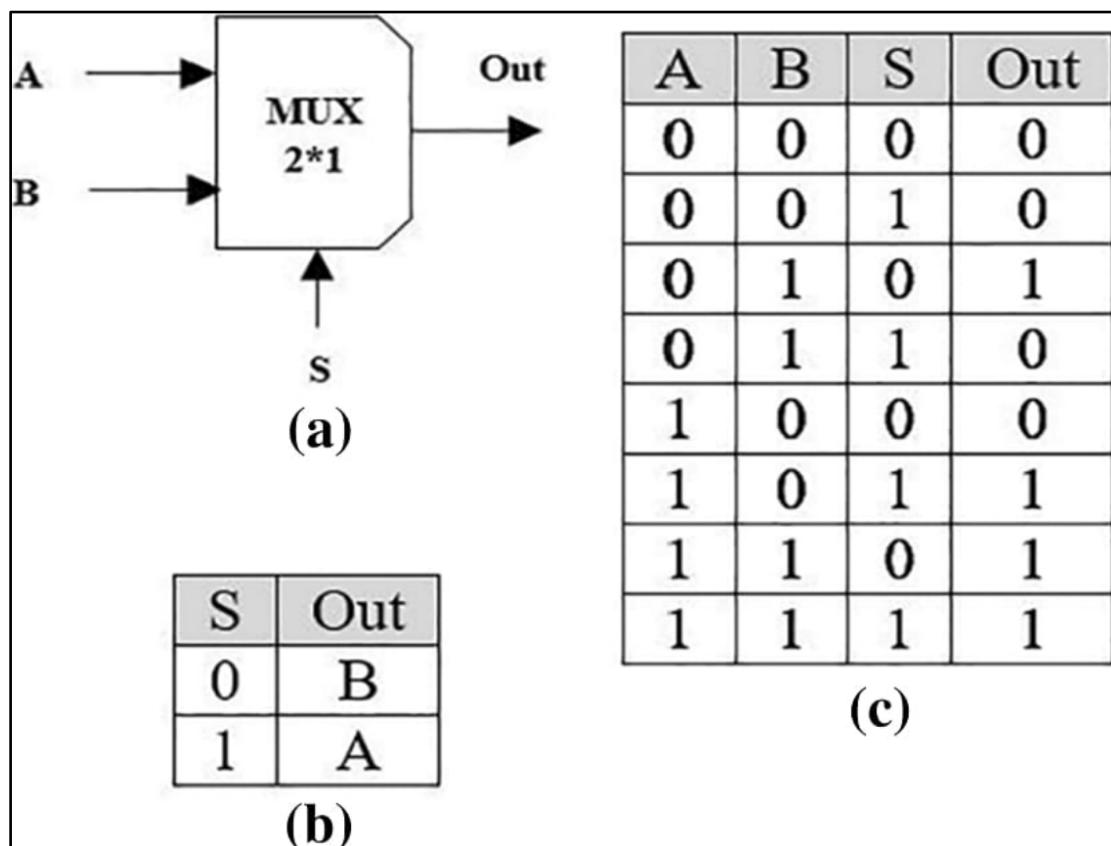


# RTL CHALLENGE

**DAY-20:-** Verilog Code for Implementation of Multiplexer and Demultiplexer Using Conditional/Behavioral Modeling Statements.

**Software used:-** Xilinx Vivado(2023.1)

**Multiplexer(MUX) using Behavioral Modeling:**



## DESIGN CODE:-

```
// Design Name: MULTIPLEXER IN Conditional
// Module Name: mux2tolusingConditional
// Project Name: RTL DESIGN

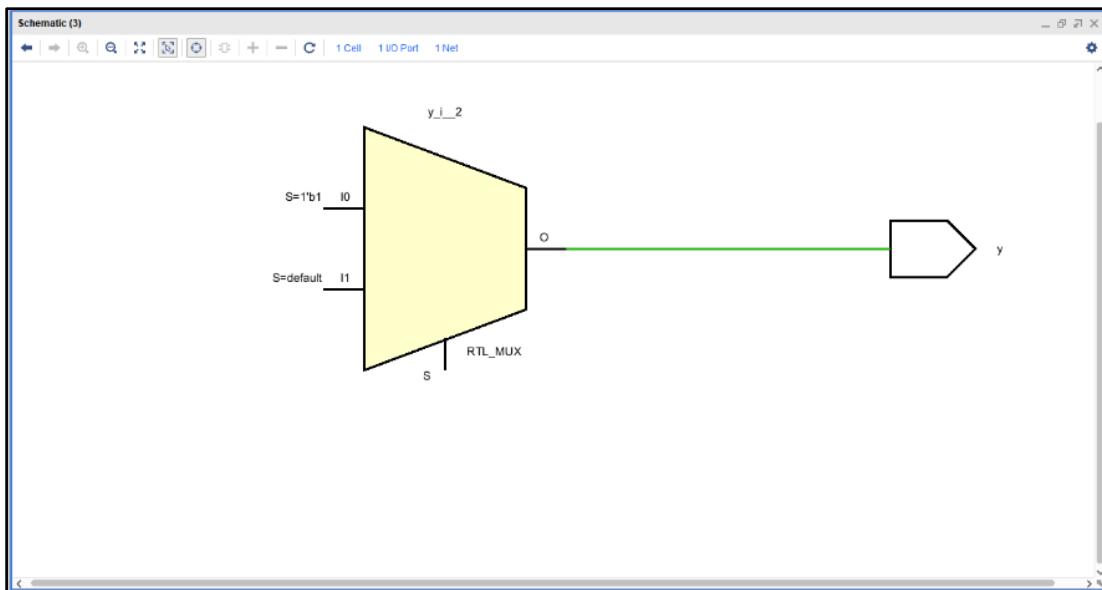
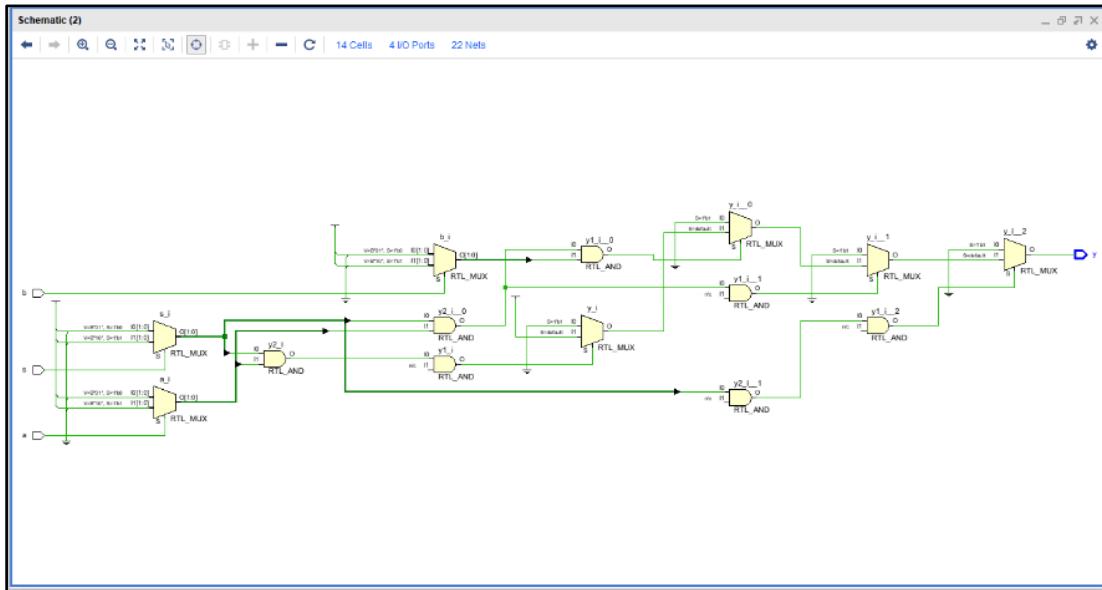
module mux2tolusingConditional(
    input a,b,s,      //asb are inputs and S is Select Line
    output reg y
);
    always@(a,b,s)
    begin
        if(s==0&&a==0&&b==0)
            begin
                y=0;
            end
        else if(s==0&&a==0&&b==1)
            begin
                y=0;
            end
        else if(s==1&&a==0&&b==0)
            begin
                y=0;
            end
        else if(s==1&&a==1&&b==0)
            begin
                y=0;
            end
        else
            begin
                y=1;
            end
    end
endmodule
```

## TEST BENCH:-

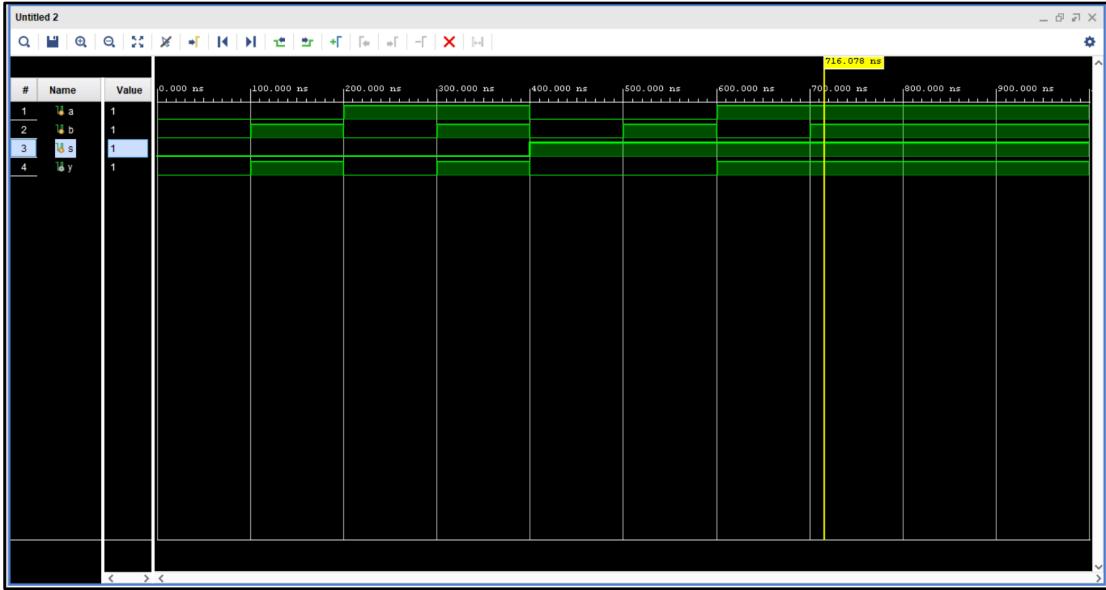
```
// Design Name: TEST BENCH
// Module Name: mux2tolusingConditional_tb
// Project Name: RTL DESIGN

module mux2tolusingConditional_tb();
reg a,b,s;
wire y;
mux2tolusingConditional uut ( .a(a),.b(b),
                               .s(s),.y(y)
                             );
initial
begin
    s=0;a=0;b=0;#100;
    s=0;a=0;b=1;#100;
    s=0;a=1;b=0;#100;
    s=0;a=1;b=1;#100;
    s=1;a=0;b=0;#100;
    s=1;a=0;b=1;#100;
    s=1;a=1;b=0;#100;
    s=1;a=1;b=1;#100;
end
endmodule
```

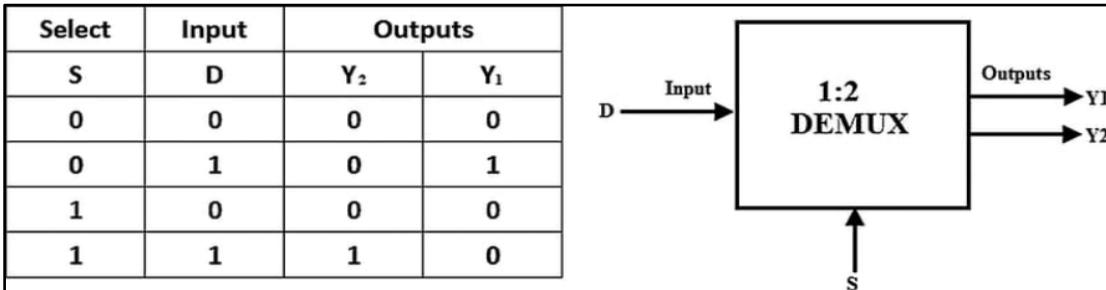
## RTL SCHEMATIC:-



## OUTPUT WAVEFORM:-



## DeMultiplexer(MUX) using Behavioral Modeling:



## DESIGN CODE:

```
// Design Name: DEMUX IN CONDITIONAL
// Module Name: demux1to2usingConditional
// Project Name: RTL DESIGN

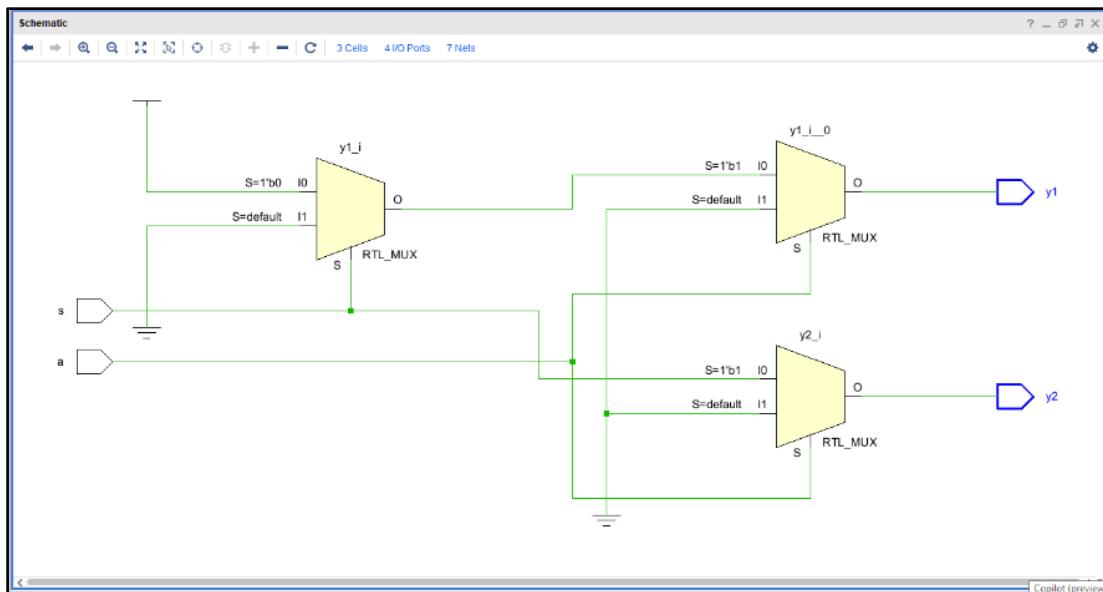
module demux1to2usingConditional(
    input s,a,
    output reg y2,y1
);
    always@(s,a) // 's' is select line & 'a' is input
    begin
        if(a==1)
            begin
                if(s==0)
                    begin
                        y2=0;
                        y1=1;
                    end
                else
                    begin
                        y2=1;
                        y1=0;
                    end
            end
        else
            begin
                y2=0;
                y1=0;
            end
    end
endmodule
```

## TESTBENCH:-

```
// Design Name: TEST BENCH
// Module Name: demuxlto2usingConditional_tb
// Project Name: RTLDESIGN

module demuxlto2usingConditional_tb();
reg s,a;
wire y2,y1;
demuxlto2usingConditional uut (.s(s),.a(a),.y2(y2),.y1(y1));
initial
begin
    s=0;a=0;#100;
    s=0;a=1;#100;
    s=1;a=0;#100;
    s=1;a=1;#100;
end
endmodule
```

## RTL SCHEMATIC:-



## OUTPUT WAVEFORM:-

