

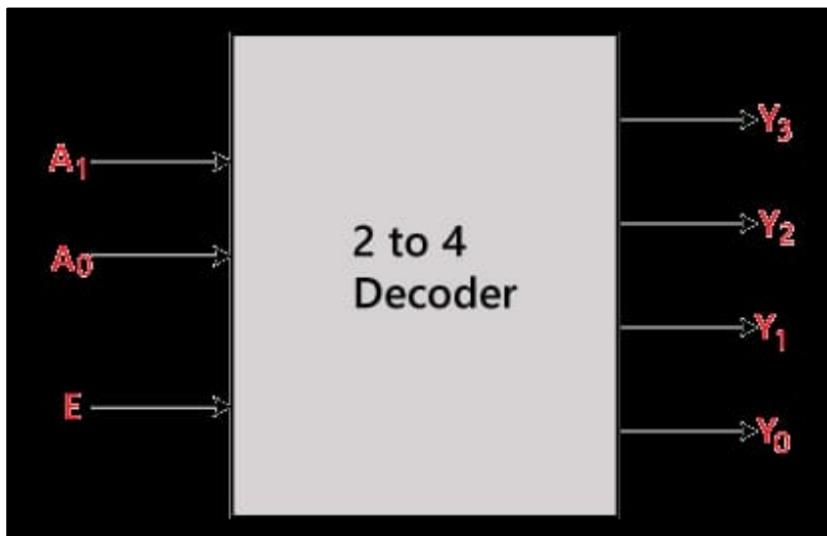
# RTL CHALLENGE

DAY-20:- Verilog Code for Implementation of Decoder and Encoder Using Conditional/Behavioral Modeling Statements.

Software used:- Xilinx Vivado(2023.1)

Decoder using Behavioral Modeling:

2:4 DECODER:



TRUTH TABLE:-

Enable	INPUTS		OUTPUTS				
	$E$	$A_1$	$A_0$	$Y_3$	$Y_2$	$Y_1$	$Y_0$
0	X	X	0	0	0	0	0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	1	0	0	0
1	1	1	1	0	0	0	0

## DESIGN CODE:-

```
// Design Name: BEHAVIORAL MODELING
// Module Name: Decoder2to4usingconditional
// Project Name: RTL DESIGN

module Decoder2to4usingbehaviour(
    input en,a,b,
    output reg [3:0] y
);
    always @(en,a,b)
        begin
            if(en==0)
                begin
                    if(a==1'b0&&b==1'b0)
                        y=4'b1110;
                    else if(a==1'b0&&b==1'b1)
                        y=4'b1101;
                    else if(a==1'b1&&b==1'b0)
                        y=4'b1011;
                    else if(a==1'b1&&b==1'b1)
                        y=4'b0111;
                    else
                        y=4'bXXXX;
                end
            else
                y=4'b1111;
        end
    endmodule
```

## TEST BENCH":-

```
// Design Name: Behavioral Testbench
// Module Name: Decoder2to4usingconditional_tb
// Project Name: RTL DESIGN

module Decoder2to4usingbehaviour_tb();
reg a,b,en;
wire [3:0] y;
Decoder2to4usingbehaviour uut (.en(en),.a(a),.b(b),.y(y));
initial
begin

$monitor("en=%b a=%b b=%b y=%b" ,en,a,b,y);
// with reference to truth table provide input values
en=1;a=1'bX;b=1'bX;#100;
en=0;a=0;b=0;#100;
en=0;a=0;b=1;#100;
en=0;a=1;b=0;#100;
en=0;a=1;b=1;#100;

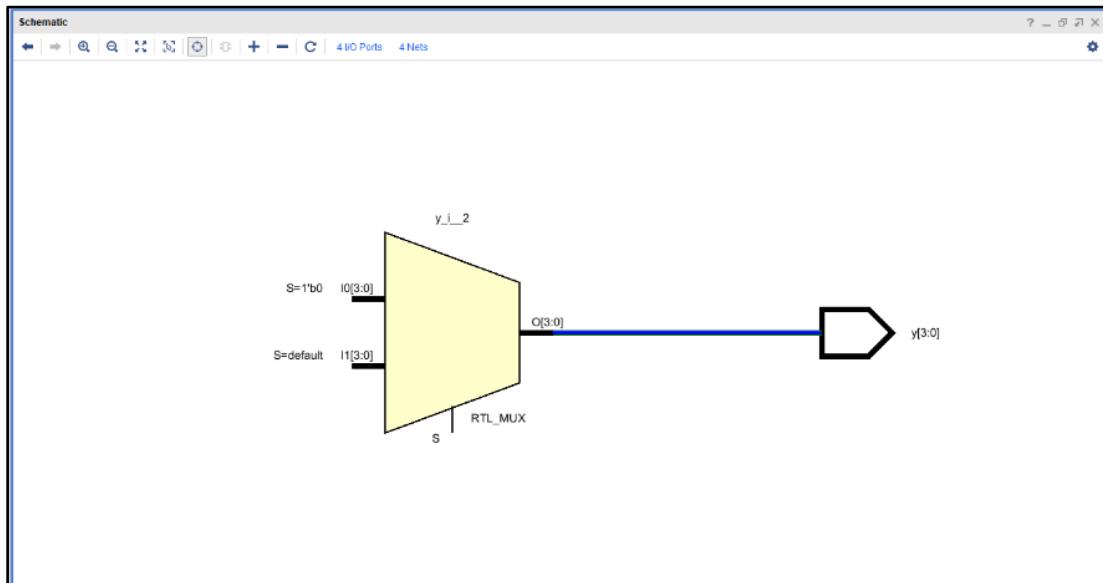
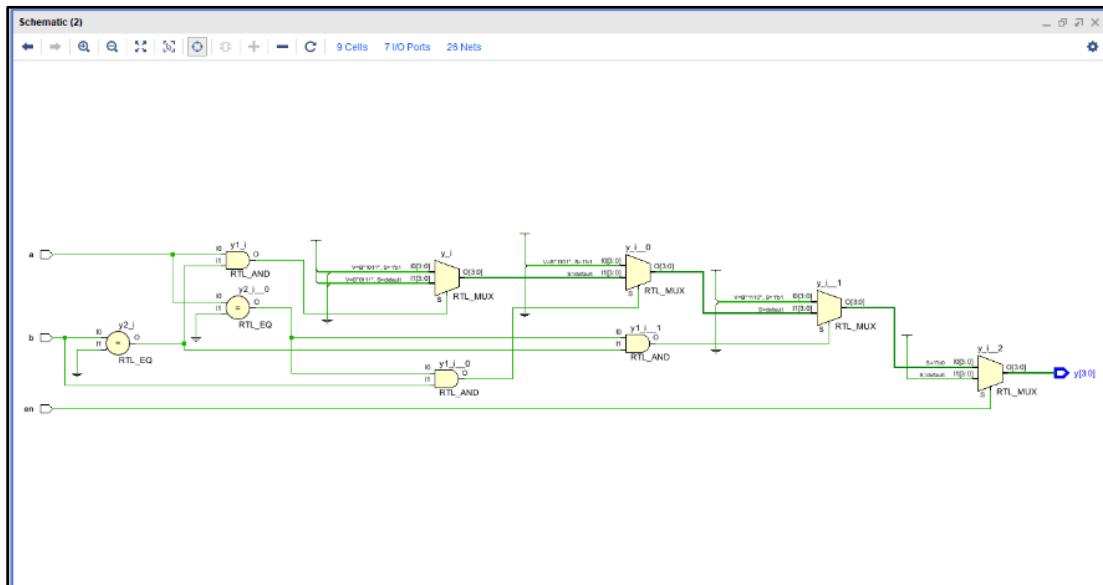
$finish; //terminate simulation using $finish system task

end
endmodule
```

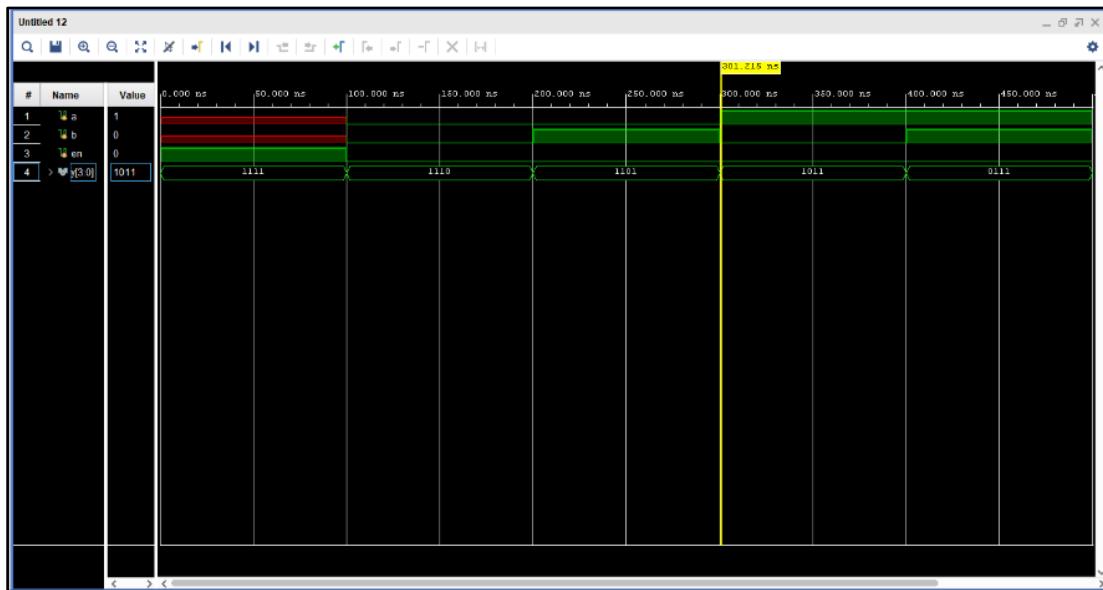
## OUTPUT FOR TEST BENCH:-

```
# run 1000ns
en=1 a=x b=x y=1111
en=0 a=0 b=0 y=1110
en=0 a=0 b=1 y=1101
en=0 a=1 b=0 y=1011
en=0 a=1 b=1 y=0111
$finish called at time : 500 ns : File "C:/Users/venky/conditional/conditional.srccs/sim_1/new/Decoder2to4usingconditional_tb.v" Line 21
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Decoder2to4usingbehaviour_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:13 . Memory (MB): peak = 3297.117 ; gain = 0.000
```

## RTL SCHEMATIC:-

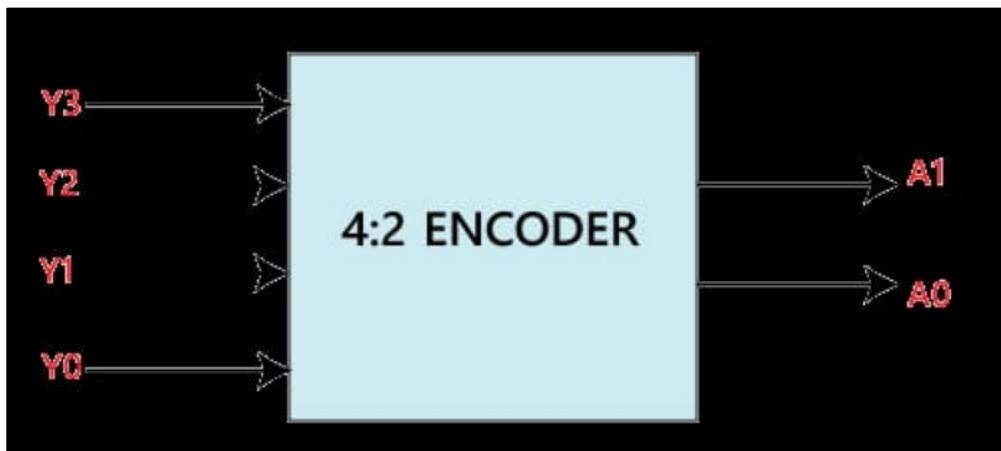


## OUTPUTWAVEFORM:-



Encoder using Behavioral Modeling:

4:2 ENCODER:



TRUTH TABLE:-

INPUTS				OUTPUTS	
Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>	A <sub>1</sub>	A <sub>0</sub>
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

## DESIGN CODE:-

```
// Design Name: BEHAVIORAL MODELING
// Module Name: Encoder4to2usingbehaviour
// Project Name: RTL DESIGN

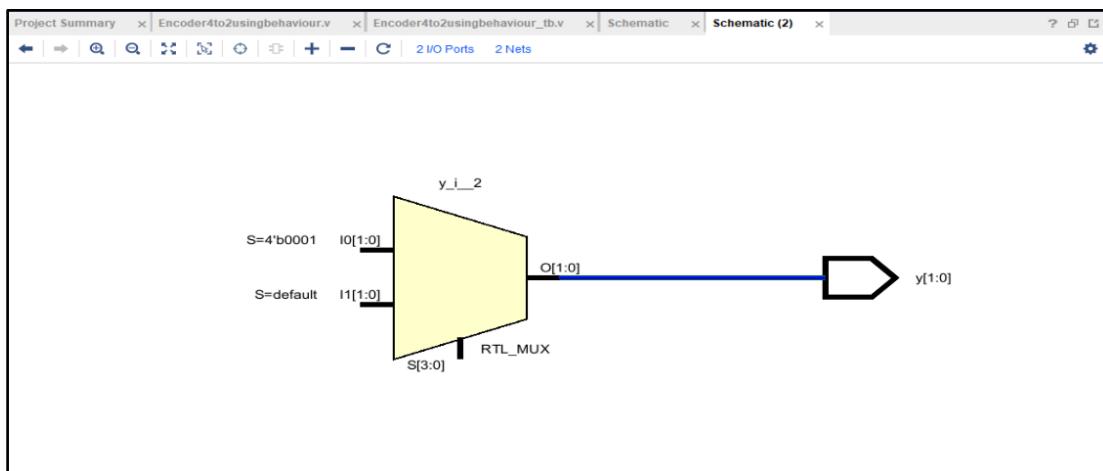
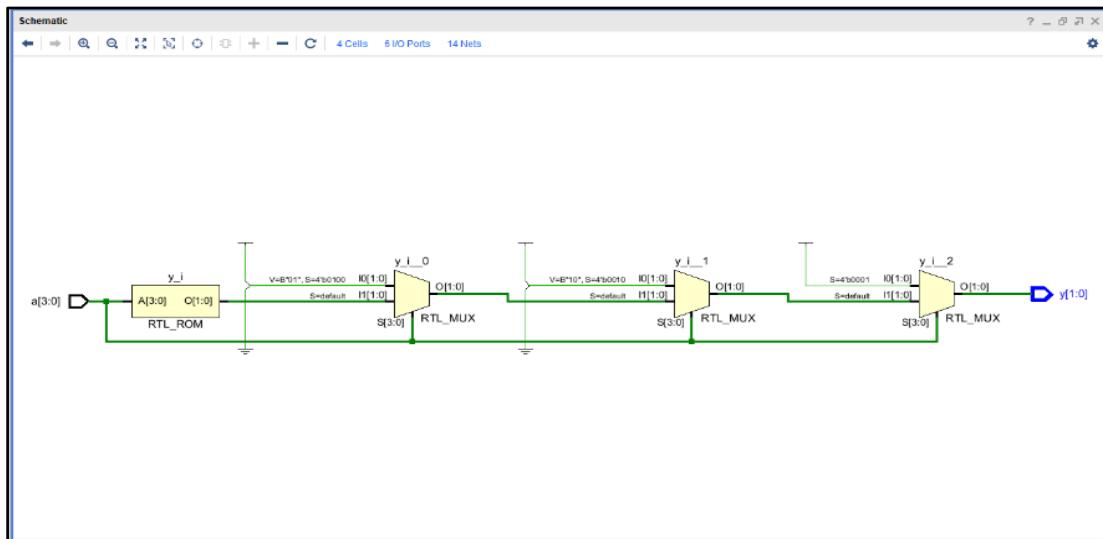
module Encoder4to2usingbehaviour(
    input [3:0] a,
    output reg [1:0] y
);
    always @ (a)
        begin
            if (a==4'b0001)
                begin
                    y=2'b11;
                end
            else if (a==4'b0010)
                begin
                    y=2'b10;
                end
            else if (a==4'b0100)
                begin
                    y=2'b01;
                end
            else if (a==4'b1000)
                begin
                    y=2'b00;
                end
            else
                begin
                    y=2'b11;
                end
        end
endmodule
```

## TEST BENCH:-

```
// Design Name: Behavioral Testbench
// Module Name: Encoder4to2usingbehaviour_tb
// Project Name: RTL DESIGN

module Encoder4to2usingbehaviour_tb();
reg [3:0] a;
wire [1:0] y;
Encoder4to2usingbehaviour uut (.a(a), .y(y));
initial
begin
    a=4'b0001;#100;
    a=4'b0010;#100;
    a=4'b0100;#100;
    a=4'b1000;#100;
    a=4'b0011;#100;
    a=4'b0100;#100;
    a=4'b0101;#100;
    a=4'b0110;#100;
    a=4'b0001;#100;
    a=4'b0010;#100;
    a=4'b0100;#100;
    a=4'b1000;#100;
    a=4'b0111;#100;
    a=4'b1111;#100;
end
endmodule
```

## RTL SCHEMATIC:-



## OUTPUT WAVEFORM:-

