

RTL CHALLENGE

DAY-21:- Verilog Code for Implementation of Using Priority Encoder

Conditional or Behavioral Modeling Statements.

Software used:- Xilinx Vivado(2023.1)

Priority Encoder using Behavioral Modeling:

In Digital System Circuit, an Encoder is a combinational circuit that takes 2^n input signal lines and encodes them into n output signal lines. When the enable is true i.e., the corresponding input signal lines display the equivalent binary bit output.

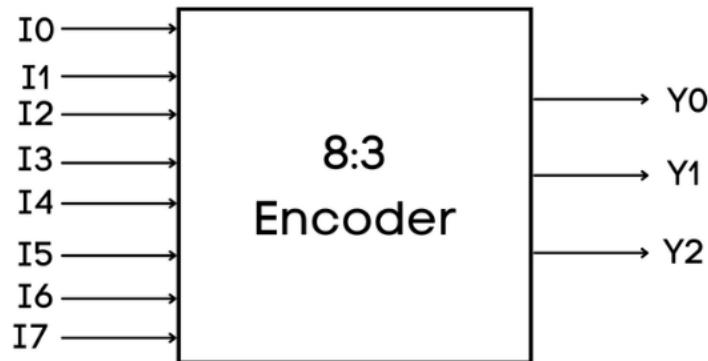
For example, 8:3 Encoder has 8 input lines and 3 output lines, 4:2 Encoder has 4 input lines and 2 output lines, and so on.

An 8:3 Priority Encoder has seven input lines i.e., i_0 to i_7 , and three output lines y_2 , y_1 , and y_0 . In 8:3 Priority Encoder i_7 have the highest priority and i_0 the lowest.

Truth Table:

		Input										Output		
en	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0	y_2	y_1	y_0			
0	x	x	x	x	x	x	x	x	z	z	z			
1	0	0	0	0	0	0	0	1	0	0	0			
1	0	0	0	0	0	0	1	x	0	0	1			
1	0	0	0	0	0	1	x	x	0	1	0			
1	0	0	0	0	1	x	x	x	0	1	1			
1	0	0	0	1	x	x	x	x	1	0	0			
1	0	0	1	x	x	x	x	x	1	0	1			
1	0	1	x	x	x	x	x	x	1	1	0			
1	1	x	x	x	x	x	x	x	1	1	1			

Logic Symbol:



Design Block: Behavior Modeling

```
// Design Name: Behavioral
// Module Name: priorityencoder_83
// Project Name: RTLDESIGN

module priorityencoder_83(
    input en,
    input [7:0] i,
    output reg [2:0] y
);
    always @(en,i)
    begin
        if(en==1)
            begin
                if(i[7]==1)
                    y=3'b111;
                else if(i[6]==1)
                    y=3'b110;
                else if(i[5]==1)
                    y=3'b101;
                else if(i[4]==1)
                    y=3'b100;
                else if(i[3]==1)
                    y=3'b011;
                else if(i[2]==1)
                    y=3'b010;
                else if(i[1]==1)
                    y=3'b001;
                else
                    y=3'b000;
            end
        else
            y=3'bzzz;
    end
endmodule
```

TESTBENCH:-

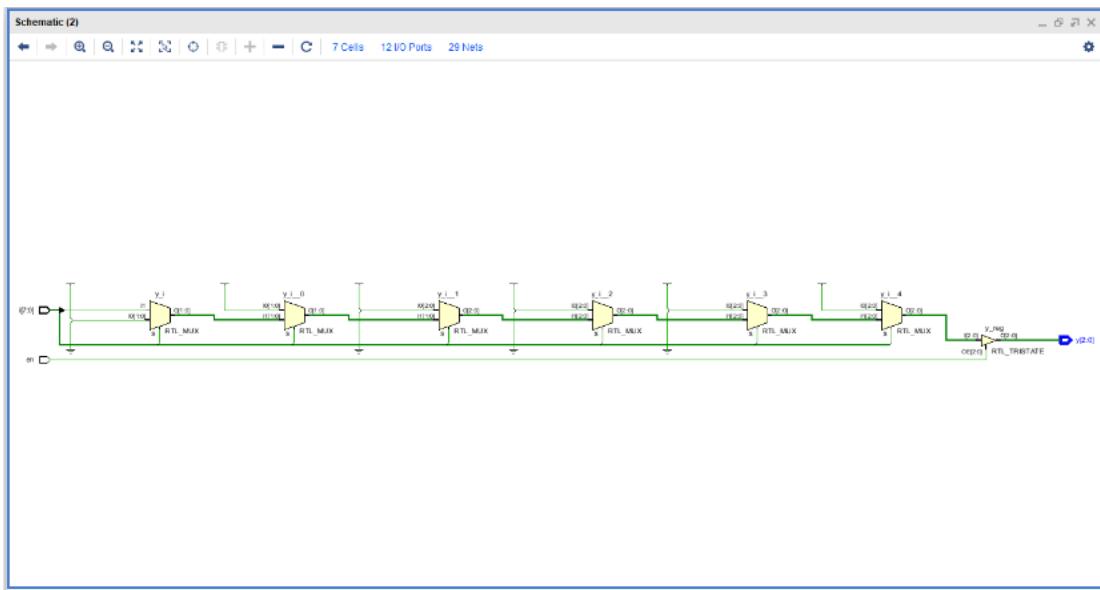
```
// Design Name: TEST BENCH
// Module Name: priorityencoder_83_tb
// Project Name: RTLDESIGN

module priorityencoder_83_tb();
reg [7:0] i;
reg en;
wire [2:0]y;
priorityencoder_83 dut(en,i,y);
initial
begin
//monitor is used to displayb the information
$monitor("en=%d i=%d y=%d realtime",en,i,y, $realtime);
en=1; i=128:#100;
en=1; i=64:#100;
en=1; i=32:#100;
en=1; i=16:#100;
en=1; i=8:#100;
en=1; i=4:#100;
en=1; i=2:#100;
en=1; i=0:#100;
en=0; i=8'bxx:#100;
en=0; i=32'bxx:#100;
$finish;
end
endmodule
```

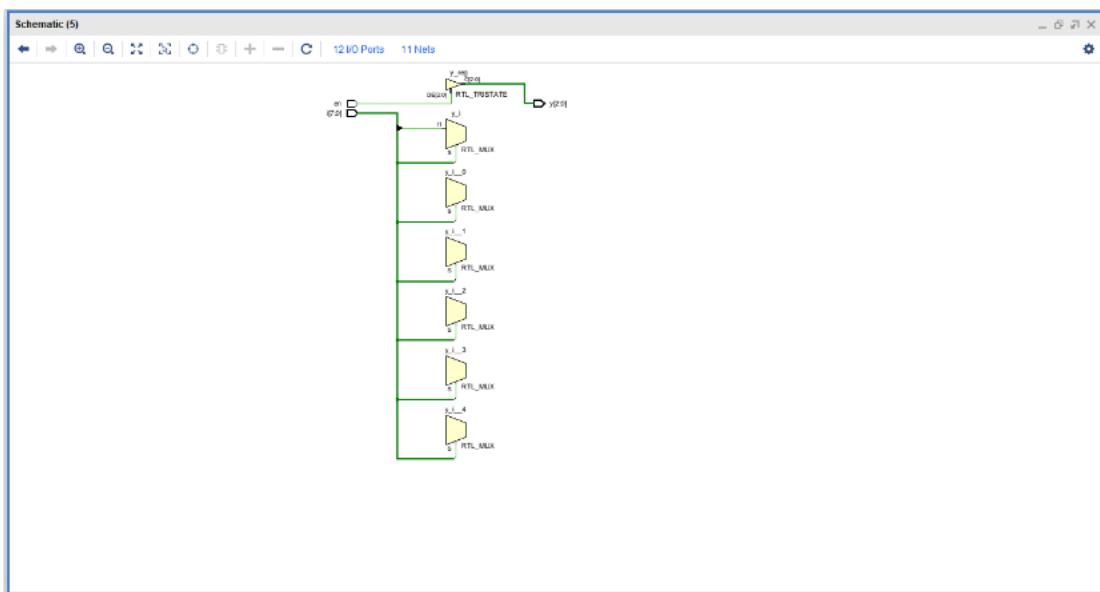
OUTPUT:-

```
en=1 i=128 y=7 realtime0
en=1 i= 64 y=6 realtime100
en=1 i= 32 y=5 realtime200
en=1 i= 16 y=4 realtime300
en=1 i= 8 y=3 realtime400
en=1 i= 4 y=2 realtime500
en=1 i= 2 y=1 realtime600
en=1 i= 0 y=0 realtime700
en=0 i= x y=z realtime800
$finish called at time : 1 us : File "C:/Users/venky/conditional/conditional.srccs/sim_1/new/priorityencoder_83_tb.v" Line 25
INFO: [USF-XSim-96] XSim completed. Design snapshot 'priorityencoder_83_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
| launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:11 . Memory (MB): peak = 3362.426 ; gain = 0.000
```

RTL SCHEMATIC:-



or



OUTPUT WAVEFORM:-

