RTL CHALLENGE

DAY-3 : Verilog Code for Implementation of 3 Inputs of Basic Logic Gates in GateLevel and DataFlow.

Software used : Xilinx Vivado(2023.1)

BASIC GATES :

AND GATE, OR GATE, NOT GATE, NAND GATE, NOR GATE, XOR GATE, XNOR GATE

By using these gates to implement the RTL schematic and waveform in Xilink Vivado (2023.1) software

DATA FLOW :

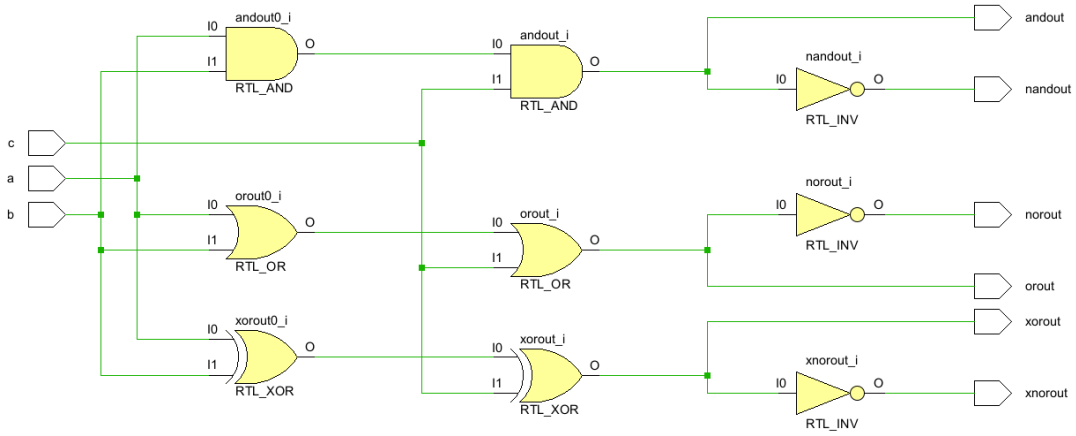
DESIGN CODE:

```
// Design Name:
// Module Name: basicthreeinputgates

module basicthreeinputgates(
    input a,b,c,
    output andout,orout,norout,nandout,xorout,xnorout
    );

    assign andout = (a&b&c);
    assign orout =  (a|b|c);
    assign norout = !(a|b|c);
    assign nandout = !(a&b&c);
    assign xorout =  (a^b^c);
    assign xnorout = !(a^b^c);

endmodule
```

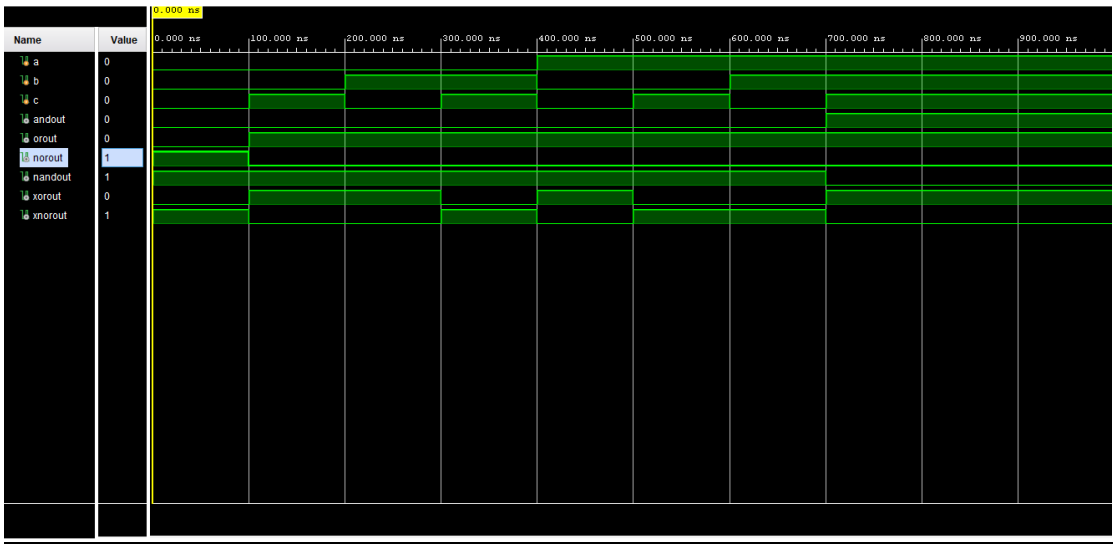
TEST BENCH :

```
// Design Name: Gate Level
// Module Name: basicgatesusinggatelevel_tb

module basicgatesusinggatelevel_tb();
  reg a;
  reg b;
  wire andout,orout,notout,xorout,nandout,norout,xnorout;
  basicgatesusinggatelevel uut(.a(a),.b(b),.andout(andout),.orout(orout),.
  notout(notout),.xorout(xorout),.nandout(nandout),.norout(norout),.xnorout(xnorout));

  initial
      begin

          a=0;b=0;#100;
          a=0;b=1;#100;
          a=1;b=0;#100;
          a=1;b=1;#100;

      end

endmodule
```

RTL SCHEMATIC :



WAVE FORM:-


0.000 ns
Name
Value
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
a
0
b
0
c
0
andout
0
orout
0
norout
1
nandout
1
xorout
0
xnorout
1

GATE LEVEL :

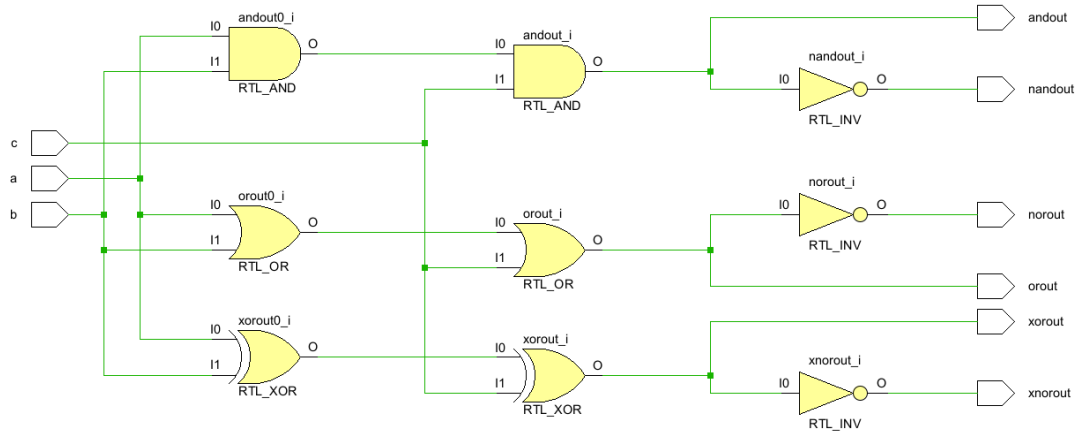
DESIGN CODE:-

```
//Gate Level
module basicthreeinputgatel(
    input a,b,c,
    output andout,orout,norout,nandout,xorout,xnorout
    );

    and(andout,a,b,c);
    or(orout,a,b,c);
    nor(norout,a,b,c);
    nand(nandout,a,b,c);
    xor(xorout,a,b,c);
    xnor(xnorout,a,b,c);

endmodule
```

TEST BENCH :-

```
module basicthreeinputgatel_tb();
reg a,b,c;
wire andout,orout,norout,nandout,xorout,xnorout;
basicthreeinputgatel uut(andout,orout,norout,nandout,xorout,xnorout,a,b,c);

initial
    begin
        a=0;b=0;c=0;#100;
        a=0;b=0;c=1;#100;
        a=0;b=1;c=0;#100;
        a=0;b=1;c=1;#100;
        a=1;b=0;c=0;#100;
        a=1;b=0;c=1;#100;
        a=1;b=1;c=0;#100;
        a=1;b=1;c=1;#100;
    end
endmodule
```

RTL SCHEMATIC :-



WAVE FORM :