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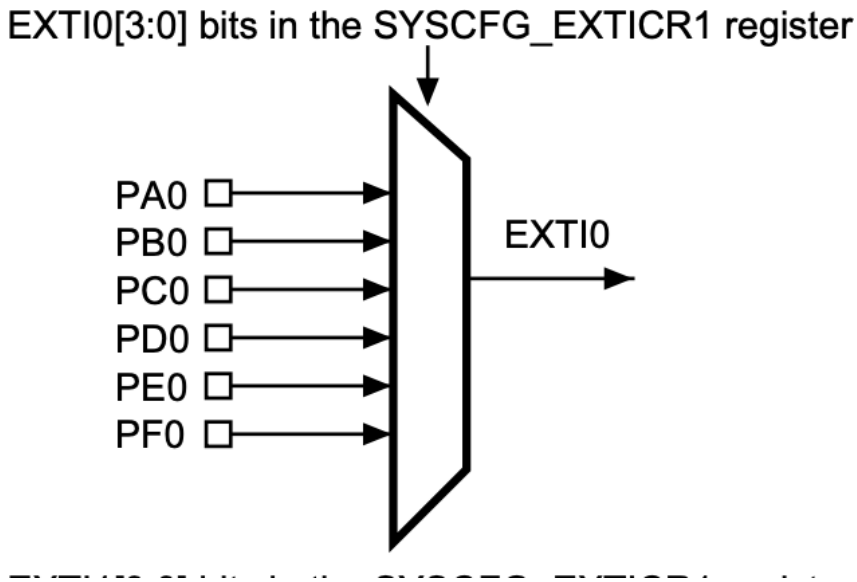
POSTLAB-2

Q1- Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?



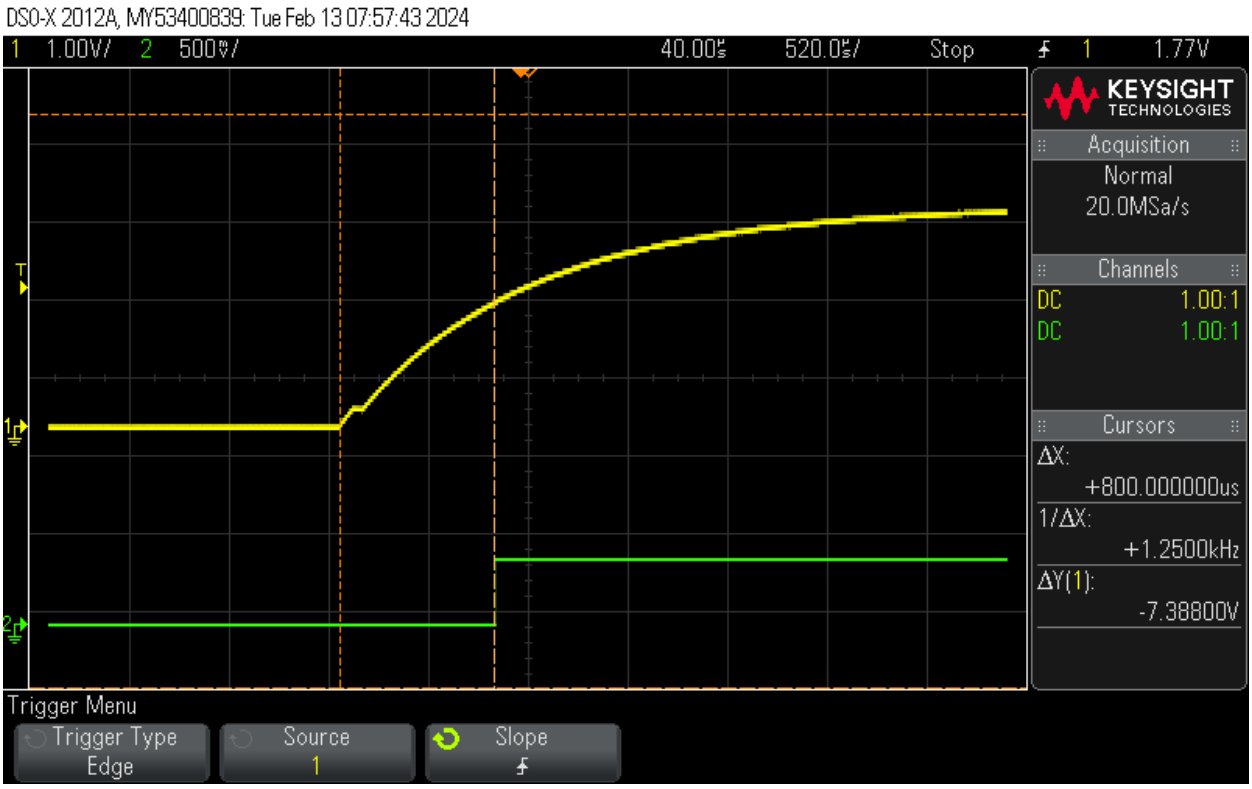
As the PA0 and PC0 are mapped to the same EXTI0 line, hence they cannot be triggered at the same time.

Q2-
Priority 1 means the highest priority and priority 3 means the lowest priority. For example, NVIC_SetPriority (EXTI0_1_IRQn, 1) Basically lower the numerical value higher the priority.

Q3-
Each IPR register contains four 8-bit regions to set the priority of an interrupt; the NVIC within the STM32F0 only has the uppermost two bits from these regions implemented, giving four possible configurable priority levels (0-3). More bits are available on other chipsets.

Q4-

800us



Q5-

Most peripherals have a status register containing flag bits for pending interrupt requests. We need ti clear status flag bits in peripherals when servicing their interrupts because if we don't clear, the interrupt will repeat continuously because the request never acknowledges as complete.