Techniques for Leakage Power Reduction Using Not and Nand Logic Gates in Tanner Tool

M Siva Kumar [a)], Syed Inthiyaz [b)], T Srinivasa Rao[c)], G R K Prasad[d)], ParasuSai Prasanthi[e)], Karamsetty Venkata Mourya[f)], CH. Sai Krishna [g)]

Department of Electronics and Communication Engineering
Koneru Lakshmaiah Education Foundation, Green Fields, Vaddeswaram,Guntur, A.P-522 502, India.

[a)] *Corresponding author: msivakumar@kluniversity.in*
[b)] *syedinthiyaz@kluniversity.in*
[c)] *tsr_2505@kluniversity.in*
[d)] *ramguda1978@kluniversity.in*
[e)] *170041040@kluniversity.in*
[f)] *170040370@kluniversity.in*
[g)] *170040149@kluniversity.in*

Abstract. The modern skill accessible in today's world is CMOS. And also the large advantage of this technology is it doesn't utilize any power. That the total power utilization relies on its discharge power. Since discharge exists within the circuit although it's in stand by state i.e the state within which gate of the transistor circuit is not obtaining power- supply. Therefore the power-loss within the circuit is added more. The major apprehension is toward to measure leakage current within the circuit. Types of completely various techniques area unit obtainable to scale back the discharge current and still obtain other, higher methods. During this paper 5 completely different techniques that areaunit supported a concept are comparatively examined.

Keywords: forced stack, sleepy transistor, sleepy keeper, Lector, LCPMOS

1. INTRODUCTION

Advancement of semiconductor technology leads to ultimatum to style less power consumed electronic devices and subsystems. Whereas in attaining the less power style, the size of the design rises up above. The energy devoured by subthreshold currents and diodes during a CMOS semiconductor device is taken-into account as a Discharge Power. To amplify the accumulator viability, the enormous procedure capability of transportable systems like folding computers, communication systems (tablets, Personal computers, mobile phones), hearing devices and implantable pacemakers has got to be complete with terribly low power needs. The power loss emerges as a vital style metric because of capability to manufacture smaller mechanical, optical, and electronic systems and rise with regard to wireless communication Maximum time battery persists, the greater is the system. The power loss has not reduced regardless of minimizing the provisional voltage. The trouble of removal of heat and power loss is degenerating because the dimension of power per space is increasing. Based on the product and alertness requirement, the person needs toward choice prepared the extreme suitable method. In case of high-performance transportable gadgets electricity dissipation is the foremost problem Three components perform an essential role for energy consumption which can be all leakage present day, brief circuit and dissipation of energyfrom dynamic switching.

2. POWER DISSIPATION

Low power usage and high-density ICs require the accelerated production of potential devices such as Personal computers, Voice assistants, digital watches, embeddable pacemakers and cell phones. As a result, the innovative development of low-power devices and design strategies is on the increase. In certain cases, less energy utilization requirements should satisfy the similarly commanding achievements of maximum chip area and maximum density circuit. Digital less-energy architecture and digital semiconductors exist together the maximum significant area in study. Decreasing power dissipation is a crucial challenge in this state-of-the-art technology particularly while the scope of the electronic transistor is scaled down over the silicon chip to improve transistor density. The energy decrease in power usage also plays a crucial priority for architecture of logical devices. Methods for designing CMOS circuits.

Global control dissipation in a CMOS Device can be summed as the sum of 3 main factors:

1. Static power-dissipation
2. Dynamic power-dissipation
3. Short-circuit power-dissipation during switching of transistors

2.1 Dissipation of Static Power

There is also some constant dissipation of energy when the CMOS circuit is idle due to leakage of current by nominally off transistors. Finite inverse leakage and sub-threshold voltage are found in both p-MOS and NMOS semiconductor devices used in CMOS logic gates. More amount of semiconductor device are in the chip made by sillcon and the total dissipation of power due to current leakage is similar as dissipation in dynamic nature. Leakage and substrate voltage numerical are dependent on parameters for processing the reverse-biased diode structure in which the n+ bar forms the p-substrate and n-substrates that form the p-substrate of diode is one of the key current leakage components in n-MOS. equation-1 gives magnitude of this leakage current:

$$Ireverse=A.Js(e^{q.Vbias/K.T}-1)$$

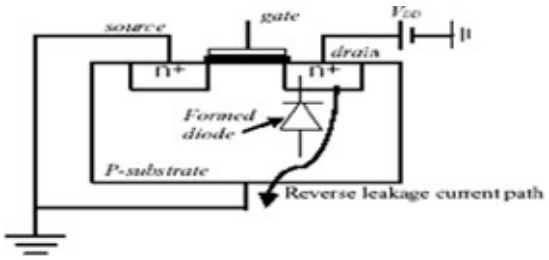

FIGURE 1. Present direction of reverse leakage due to formation of diode

2.2 Dissipation in Dynamic Power

As the MOS integrated circuit transitions to on and off the result capacitance load at a specific part at the conduction frequency, variable energy usage occurs. A CMOS not circuit with result load of capacitance CL is presented in below image

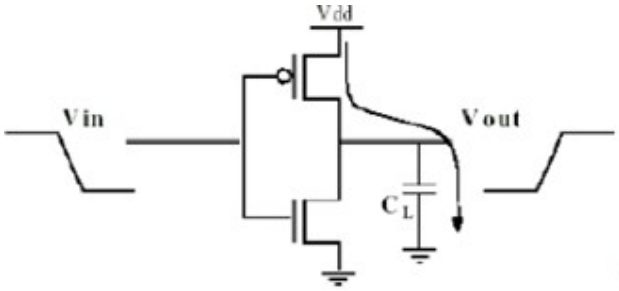

FIGURE 2. Charging of output load capacitance CL

The result node supply voltage usually makes up a complete transformation from GND to VDD during the charge- up process and a quantity of energy from the supply is released as heat in the p-MOS transistor conducting it. None of power is taken from the supply voltage in the load capacitance discharge process, only the power is retained (during the on-up time) in the result resistance is evolved as heat form in the n-MOS semiconductor conduction. At less static capacity, much of the power in CMOS circuits is absorbed by charging and discharging output node capacitance. Then the dynamic dissipation of power in specific output node is given by $P= Cl.V^2DD.Fclk.$

2.3 Short Circuit Power Dissipation

Taking from above observation, dissipation of the on/off power is due solely to the power needed to on and discharge the capacity and also is not dependent on the up and down time of the driving graph. Any way in the CMOS device, if the up and the down time have a not limited growth and decrease period value, both n-MOS and p-MOS transistors can work concurrently for a exact period and stretch a indirect route among the VDD and the GND path resulting in short- device control energy usage. The present portion which permits over the dual of the PMOS and NMOS electronic transistor in switching will not contribute to the of the capacitance in the device andthe therefore named as the short-device current.

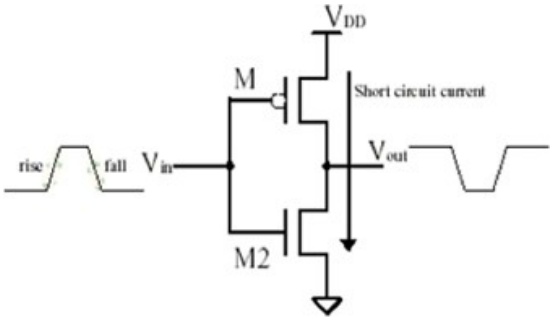

FIGURE 3. Quick system direction while couple of ic's are charge

3. LEAKAGE POWER

The power spent by the sub threshold currents and diodes in the CMOS semiconductor is taken into account as the discharge power. The discharge power of the CMOS gate does not depend on input transmutation or load capacitance, later it leftovers continual for the logic accumulator. Power dissipation has become a very significant architectural parameter due to device miniaturization and rapid wireless growth. The more the battery is consecutively, the sooner the device is. And as the power dissipation happened, the dissipation did not decrease with the scaling down of the supply voltage. The problem of heat removal and dissipation is getting worse as the amount of power per unit area continues to increase. There is a little encouragement from advanced refrigeration and fast packaging methods, an improvement in the use of new chips. The prices related with the storage and cooling of such equipment are continuously high-priced. In addition to costs, the issue of reliability is a major concern. There are different components which contribute to leakage power: They are:

1. Sub-threshold current

2. Drain induced barrier lowering (DIBL)

3. 3.PN-junction current

4. Thin oxide gate tunneling.

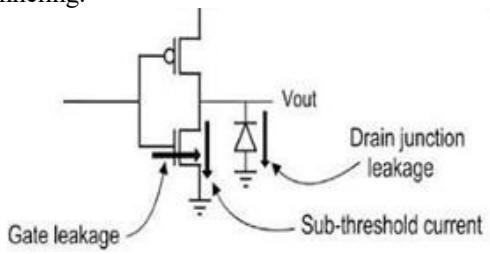

FIGURE 4. Leakage power mechanisms in a cmos inverter

4. METHODOLOGY & IMPLEMENTATION

4.1 Forced Stack Technique

The semiconductor device stack could be an outflow minimizing technique which works in non-inert mode and also in idle mode. This technique is based upon the examination that two logic-0 state transistors connected in non-parallel, considerably cause less outflow than a one device. Any way in trendy deep sub-micron systems, the brink voltage might.

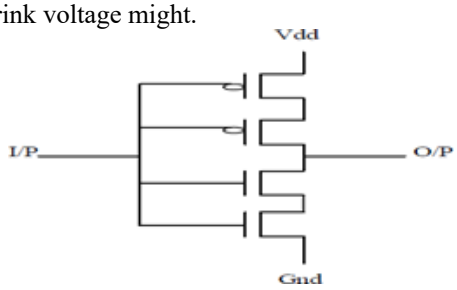

FIGURE 5. Forced stack using not and nand gates.

4.2 Sleepy Transistor Technique

The sleep technique is unity of the most generally known conventional method for subthreshold leakage drop. In this sleep approach, extra transistors (so called sleep transistors) are positioned in among the power source and ground. Another additional "sleep" PMOS transistor is implanted in among VDD and the pull-up network of a route and an extra "sleep" NMOS electronic transistor is located among the pulldown network of the routes and GND. In course of the standby mode these transistors are switched in "off" condition and bring in larger resistance in the transmission track such that leakage power is deducted in the route. On cutting off the power source, this method can decrease the leakage power effectively.

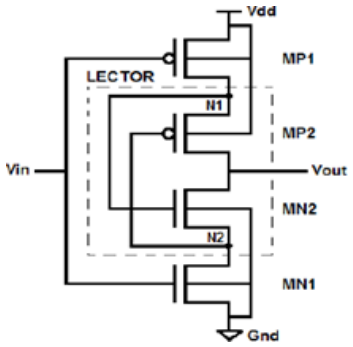

FIGURE 6. Sleep transistor for logic circuit

4.3 Sleepy Keeper Technique

The "sleepy keeper" method is another leakage power reduction strategy. The structure of the sleepy keeper technique is defined here as well as its function. In snooze manner, an additional only NMOS transistor positioned similar to the pull-up sleep transistor binds the VDD to the pull- up network. This NMOS device is the only VDD source on the pull-on network as the sleep transistor is idle state. Next an extra solo PMOS electronic transistor positioned parallel to the pull- down sleep transistor is the only GND link on the pull-down network. All that is required for this solution to work is for the NMOS linked to the VDD and the PMOS connected to the GND to be capable to establish the right logical state.

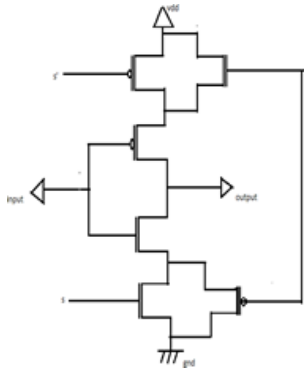

FIGURE 7. Sleepy keeper approach for a circuit

4.4 Lector Technique

The efficient assembling of electronic transistor in the track since source power to ground is the basic concept behind the LECTOR technique for the reduction of drip power. This is claimed on the basis of the observation.

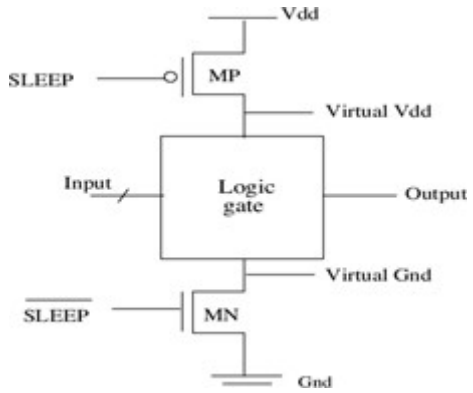

FIGURE 8. Lector approach of a inverter

that the state is much less than that. A leak of extra than single OFF electronic transistor in the direction from the supply voltage to the ground relative to a situation of only one OFF transistor in the path." In this procedure, dual outflow switch electronic transistor are introduced between the pull-up and the pull-down network inside the logic gate (one NMOS for pull-down and one PMOS for pull-up) for which the entrance fatal of leakage control transistor (LCT) is operated by the source of the another. This structure guarantees that single of the LCTs still works in its near-disconnected zone.

4.5 LCPMOS Technique

In this suggested procedure, a single leak control transistor is introduced inside the logic gate intended for which the outflow control transistor gate terminal (LCT) is operated by the act of the circuit itself. This raises the resistance of the direction from pull down the network to the ground, thereby growing the confrontation of the Vdd to ground, contributing to a large decrease in outflow flows. The key benefit compared to other techniques is that the LCPMOS technique prepares not requirement some peripheral control and tracking circuitry, thus restricting the region and likewise the indulgence of power in the dynamic state.

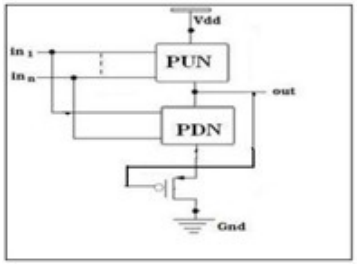

FIGURE 9. Lcpmos approach

4.6 MTCMOS Technique

Although sleep transistor size is heavily reliant also on radiative balance within the digital circuit, MTCMOS circuitry is an important idle leak management strategy, and it is challenging to introduce They demonstrated that dual Vt domino logic prevents the scaling issues and underperformance of MTCMOS. When flow must be avoided, high Vt cells are being used, while short Vt compartments have been used

while rate is a tricky. In the MTCMOS procedure, all cells work well .High Vt semiconductors are switched apart in efficient way of operating, allowing logic gates made up of low Vt transistors to work with less switching energy dissipation and a shorter simulation time. The central low Vt circuitry is shut off when the high Vt semiconductors are switchedoff in steady state.

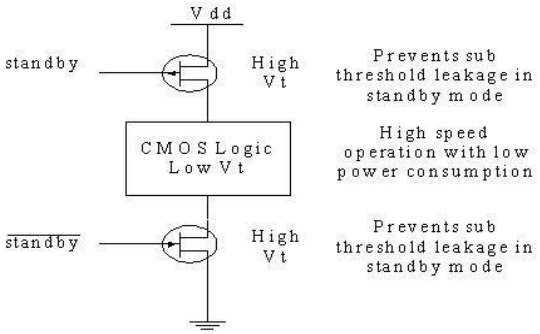

FIGURE 10. MTCMOS technique

4.7 VTCMOS Technique

Designers understand that while in CMOS digital logic, and use a low voltage level (VDD) and a low tolerance voltage (VT) is an effective way to reduce overall switching losses while retaining superfast output. However, using only low-VT capacitors in a CMOS logic gate would eventually result in increased sub - threshold leakage and, as a result, higher hang energy dissipation while the performance is not changing. By adjusting the interface bias, one potential solution to this issue is to modification the electronic transistor threshold voltage stages to prevent leakage throughout the hold mode.

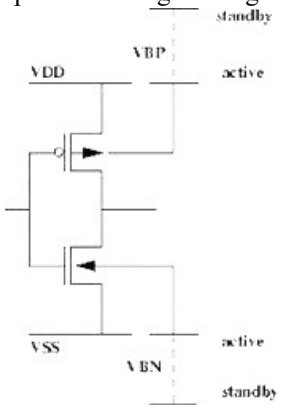

FIGURE 11. VTCMOS schematic

5. SIMULATION AND RESULTS

The VTCMOS technique is an operative method comparative to other wastage deduction methods, so this method is applied trendy the Tanner program and its power dissipation, delay and power quality are measured in the Tanner tool.

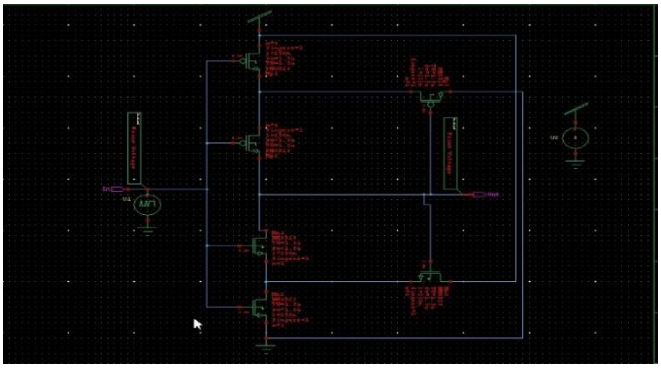

FIGURE 12. Lector method using not gate

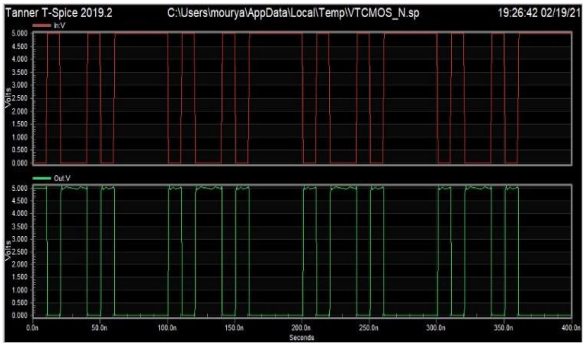

FIGURE 13. Lector method using not Graph

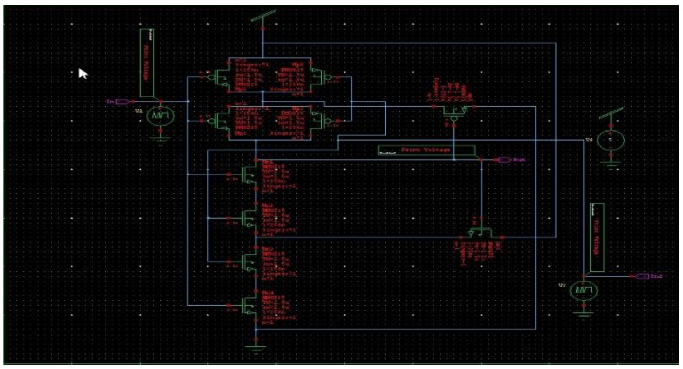

FIGURE 14. Lector method using nand gate

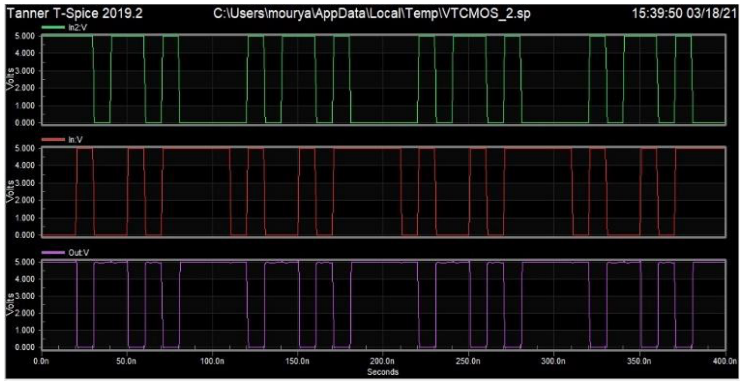

FIGURE 15. Lector method using nand graph

TABLE 1. ANALYZING THE DIFFERENT TECHNIQUES POWER VALUES FOR NOT AND NAND

METHODS	NAND(mW)	NOT(mW)
FORCED STACK	7.727404e06	7.63655e-06
SLEEP TRANSISTORS	8.26879e-06	7.48398e-06
SLEEPY KEEPER	8.5444e-07	6.30460e-06
LECTOR TECHNIQUE	7.01498e-06	6.28481e-06
LCPMOS TECHNIQUE	6.492673e-06	5.45987e-06
MTCMOS TECHNIQUE	5.567558e-03	4.44391e-04
VTCMOS TECHNIQUE	6.340749e-04	34.9602e-06

TABLE 2. NOT GATE TIME DELAY, EFFICIENCY AND AREA

METHODS	DELAY(ns)	EFFICIENCY (%)	AREA(um2)
FORCED STACK	0.631	63.1	35.4
SLEEP TRANSISTOR	0.350	23.0	34.9
SLEEPY KEEPER	0.256	34.8	38.6
LECTOR TECHNIQUE	0.309	22.4	28.4
LCPMOS TECHNIQUE	0.444	36.2	22.7
MTCMOS TECHNIQUE	0.213	13.5	14.9
VTCMOS TECHNIQUE	0.132	15.3	12.3

TABLE 3. NAND GATE TIME DELAY, EFFICIENCY, AND AREA

METHODS	DELAY(ns)	EFFICIENCY (%)	AREA(um2)
FORCED STACK	0.343	32.5	18.3
SLEEP TRANSISTOR	0.212	12.2	22.7
SLEEPY KEEPER	0.102	12.7	37.3
LECTOR TECHNIQUE	0.161	12.3	27.3
LCPMOS TECHNIQUE	0.137	22.5	13.9
MTCMOS TECHNIQUE	0.138	23.5	29.3
VTCMOS TECHNIQUE	0.265	31.2	26.5

6. CONCLUSION

The enhancement of leakage capacity due to the system Aspects, input and voltages of the threshold to reach High output and dissipation of low dynamic strength, it It's a high priority to resolve the topic of Control from leaks. One LCT that is used by LCPMOS is Driven by the circuit output itself. With LCPMOS Compared to the reduction in leakage capacity, Other methods for leakage prevention, such as Forced Reduction Stacking, Sleepy Stack, Sleepy Keeper, Reader, MTCMOS And so on, along with benefit of not Effecting on the Dynamic power and its use of criteria for restricted areas level however this technique will not entail several extra steps, Circuitrymonitoring and track including in this methodology.

As extended with standard concepts, their LCPMOS methodology Leakage control over the appropriate circuits is done the same While influencing the complex, typical circuits m ay. Strength. A trade off between the gap in transmission and the field Under, utilization occurs With numerous leakage power reduction strategies LECTOR and suggested methods, this paper multiplier is built. The suggested technique would be an optimized circuit technique used to enhance efficiency and uses either extreme and lowest threshold current semiconductors to have reduced computational strategies. From the findings of the analysis, those are inferred also that suggested technique essentially eliminates leakage capacity by 99 percent.

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