

4th Feb.

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Assignment-2.

Q No.1.

Explain the term : Timing diagram, instruction cycle, machine cycle and T-states. What are the control signals used in the timing diagram of 8085 microprocessors? Explain.

Ans. Timing diagram.

The graphical representation of status of various signals involved during a machine cycle with respect to time is called timing diagram. This gives basic idea of what is happening in the system when the instruction is getting fetched and executed, at what instant which signal is getting activated.

Instruction cycle.

Instruction cycle is the total number of machine cycles required to execute a complete instruction.

Machine cycle.

Machine is the time required by the microprocessor to complete the operation of accessing the memory devices or I/O devices. In machine cycle various operations like opcode fetch, memory read, memory write, I/O read, I/O write are performed.

T-state.

It is the time period of a single cycle of the clock frequency.

The control signals used in the timing diagram of 8086 processor are as follows:

(i) IO/M

This signal specifies whether the operation (read or write) is being performed on memory or on I/O device.

(ii) RD

This signal is used to read the data. It goes low for read operation and becomes high otherwise.

(iii) WR

This signal is used to write the data. It goes low for a write operation and becomes high otherwise.

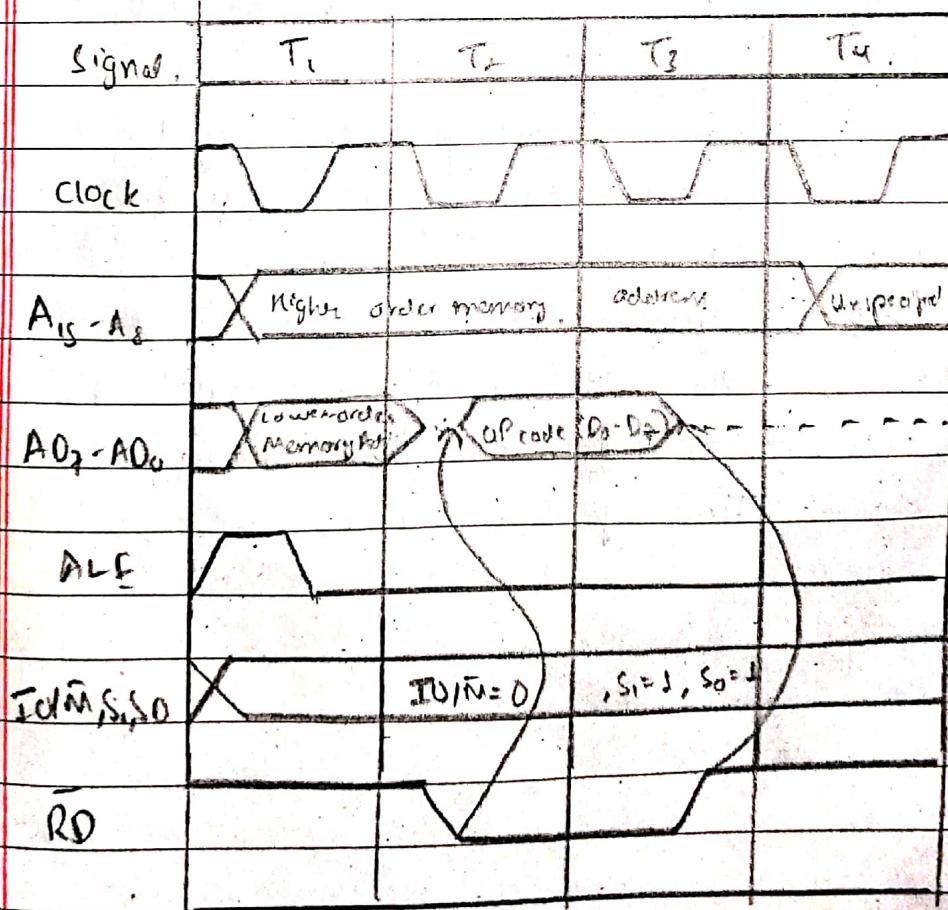
Q No. 2.

What are different machine cycles of in 8085 microprocessor. Draw timing diagram of each of them and explain.

A. The different machine cycles in 8085 microprocessors are:

- (i) Op-code fetch cycle.
- (ii) Memory read cycle.
- (iii) Memory write cycle
- (iv) I/O read cycle.
- (v) I/O write cycle.
- (vi) Interrupt acknowledge cycle.

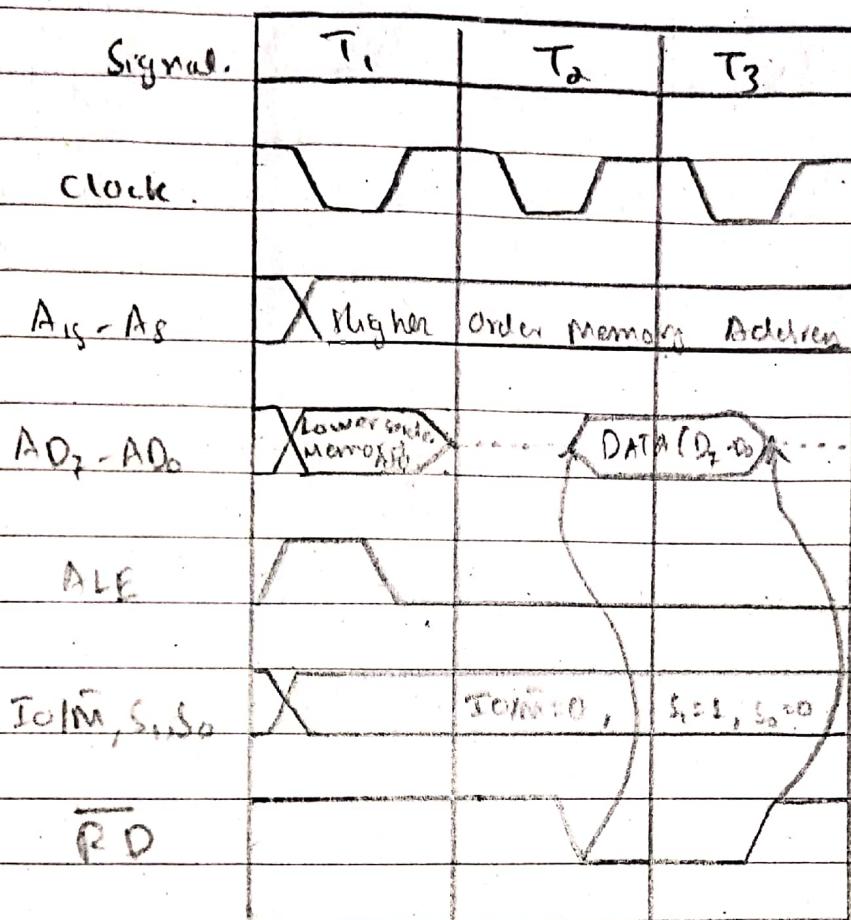
(i) Op-code fetch cycle.



The op-code fetch timing diagram can be explained as below.

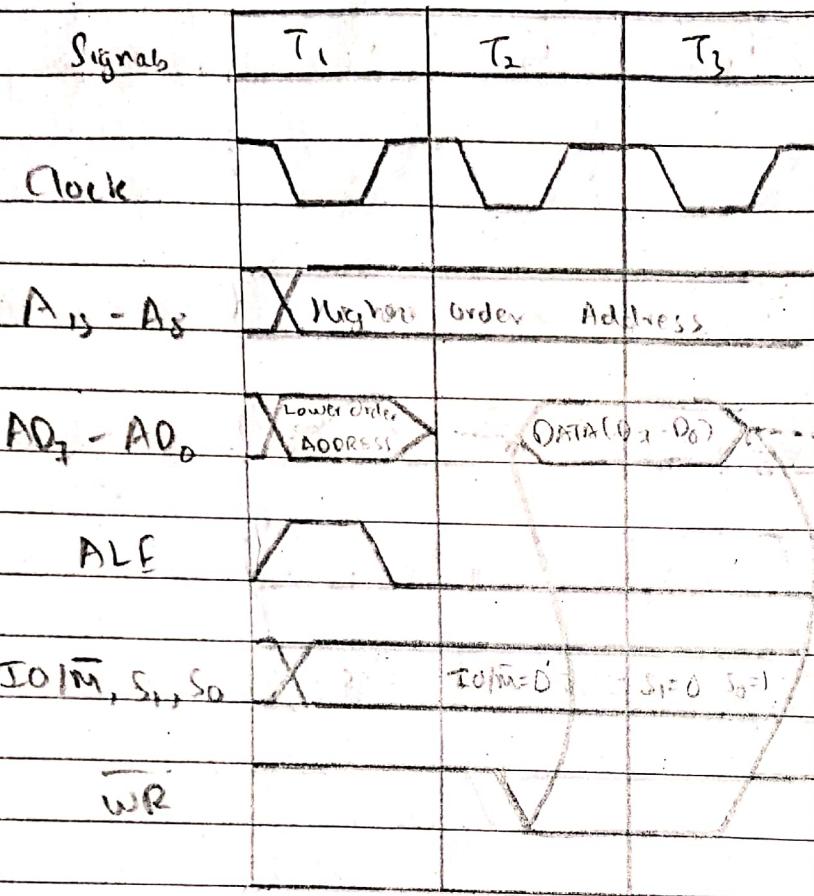
- (i) The MP places the 16-bit memory address from the program counter on address bus. At time period T_1 , the higher order memory address is placed on the address line $A_{15} - A_8$. When ALE is high, no lower order address is placed on the bus $A_7 - A_0$. The status signal $I/O/M$ goes low indicating no memory operation and two status signals $S_1 = 1, S_0 = 1$ to indicate op-code fetch operation.
- (ii) At time period T_2 , the MP sends \overline{RD} control line to enable the memory read. When memory is enabled with \overline{RD} signal, the op-code value from the addressed memory location is placed on the data bus with ALE low.
- (iii) The op-code value is reached at processor register during T_3 time period. When data (op-code value) is arrived, the \overline{RD} signal goes high. It causes the bus to go into high impedance state.
- (iv) The op-code byte is placed in instruction decoder of MP and the op-code is decoded and executed. This happens during time period T_4 .

ii) Memory read cycle.



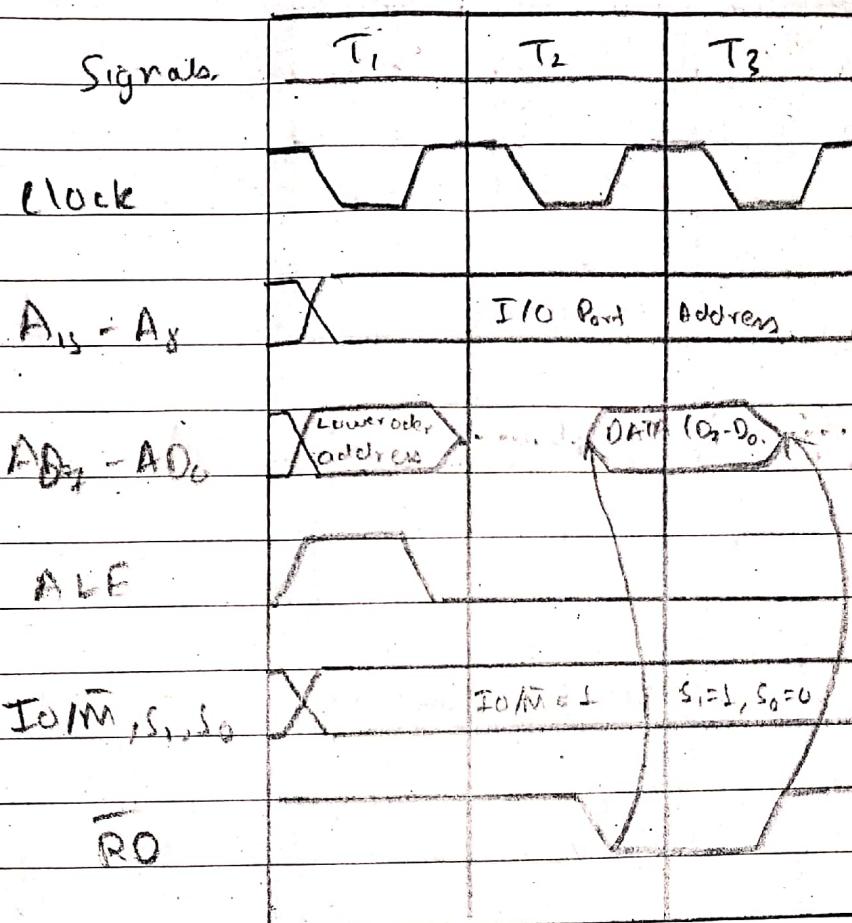
The $I_{O/M}$ signal goes low for memory operation, and the status signals $S_1=1$, $S_0=0$ to indicate memory operation in T_1 . In T_2 , the $\bar{R}D$ line goes low to enable memory read where the data is read. At T_3 data reaches register and $\bar{R}D$ signal goes high.

(iii) Memory write cycle.



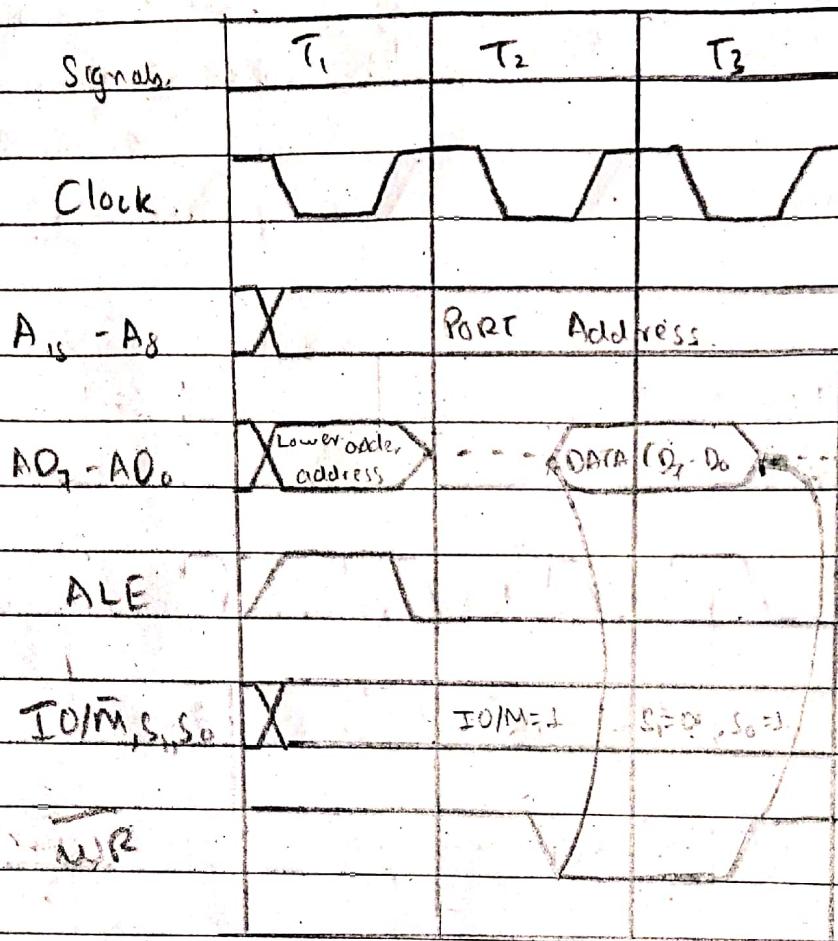
The IOM goes low for memory operation and status signals $S_1=0$ and $S_0=1$ for memory write operation in T_1 . In T_2 , the \bar{WR} goes low to enable memory write. In T_3 , data is placed on the addressed location with ALE low. In T_3 , data reaches memory location and the \bar{WR} line goes high.

(iv) I/O Read cycle.



The $I_{O/M}$ goes high for I/O operation and status signals $S_1=1$ and $S_0=0$ for ~~memory write~~ ^{read} operation in T₁. In T₂, the $\bar{R}D$ line goes low to enable memory read and the data is read. In T₃, the data reaches register and $\bar{R}D$ line goes high.

(v) I/O write cycle.



The $I/O\bar{M}$ goes high for I/O operation, and status signals $S_1=0$ and $S_0=1$ for write operation in T_3 . In T_2 the WR line goes low for I/O write operation and data is written in I/O. In T_3 , the data is written and the WR line goes high.

Q No. 3

Draw the timing diagram of instruction MVI A, 01 H stored in memory location 2030 X and explain it.

Ans.

MVI A @, 01 H.

Operation: OP fetch, Memory read.

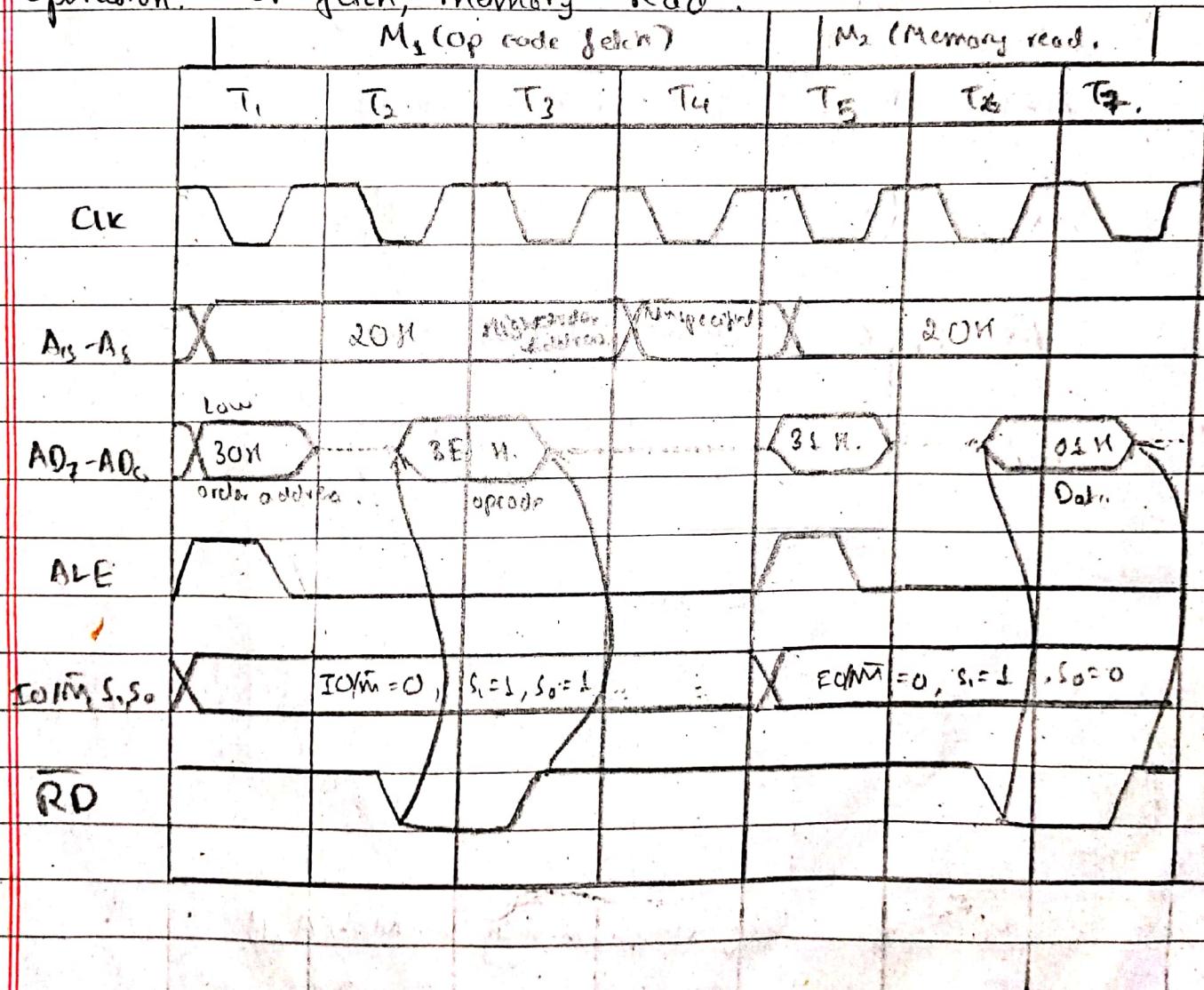


Fig: Timing diagram for MVI A, 01 H.

(4) Draw the timing diagram of instruction MOV A, B and explain it.

Ans MOV A, B. (Address : 0002 H.)

Operation: OP fetch.

OP fetch.

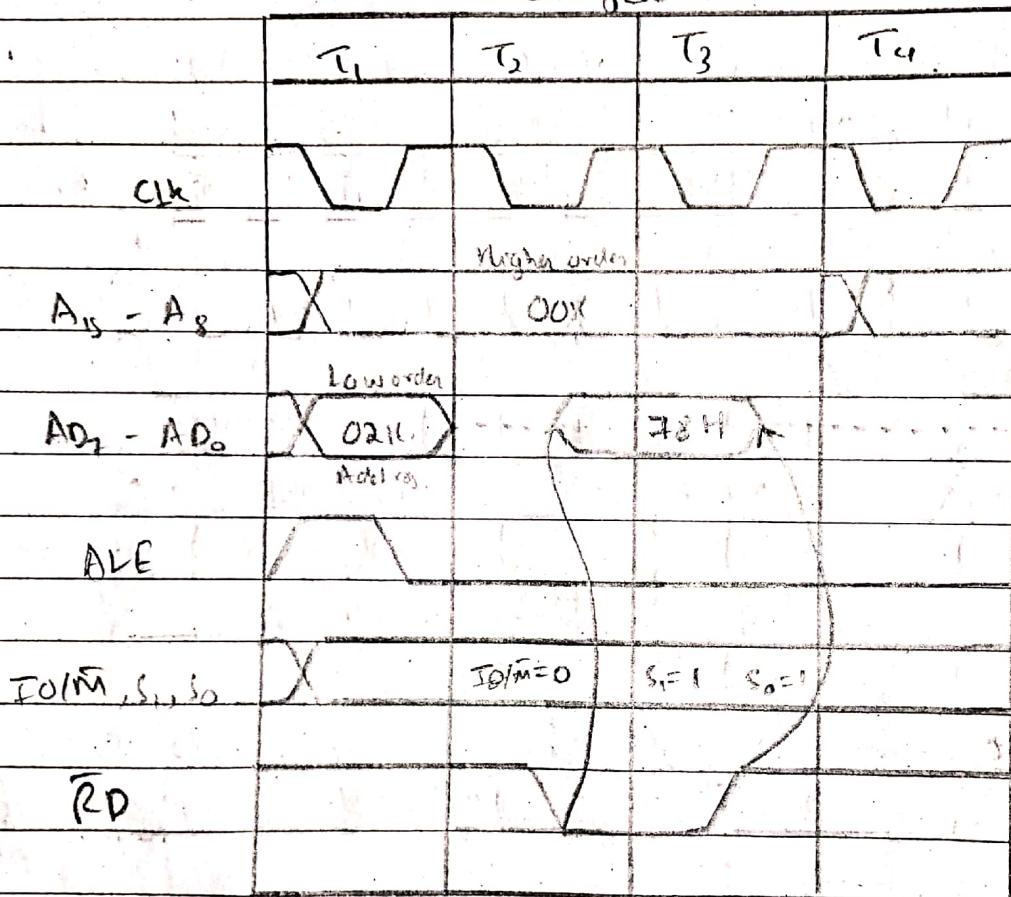


Fig: Timing diagram for MOV A, B.

(5) Draw the timing diagram of STA 1001 H and explain it.

Ans STA 1001 H.

Op code = 32 H.

Operation: Op fetch, Memory read, Memory read, Memory write.

Let address be 0003H.

Data in accumulator be ~~AAH~~ 21H.

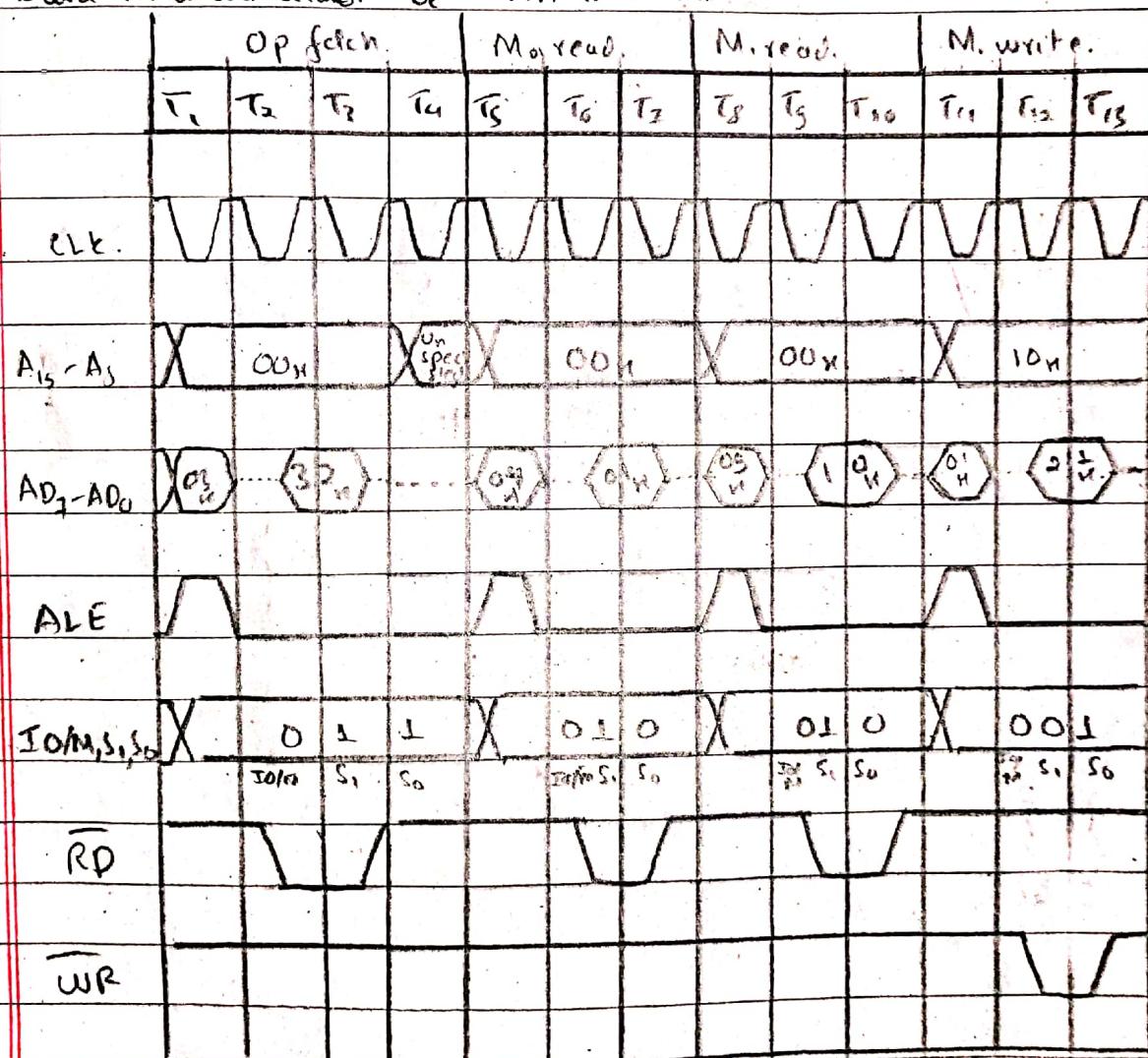


Fig. Timing diagram for STA 1001H.

[6] Draw the timing diagram of instruction LDA 0101 H and explain it.

As LDA 0101 H,

Op code : 8A H.

Operations: Op fetch, Read, Memory read, memory read, memory read.

Data in 0101 H = A1 H.

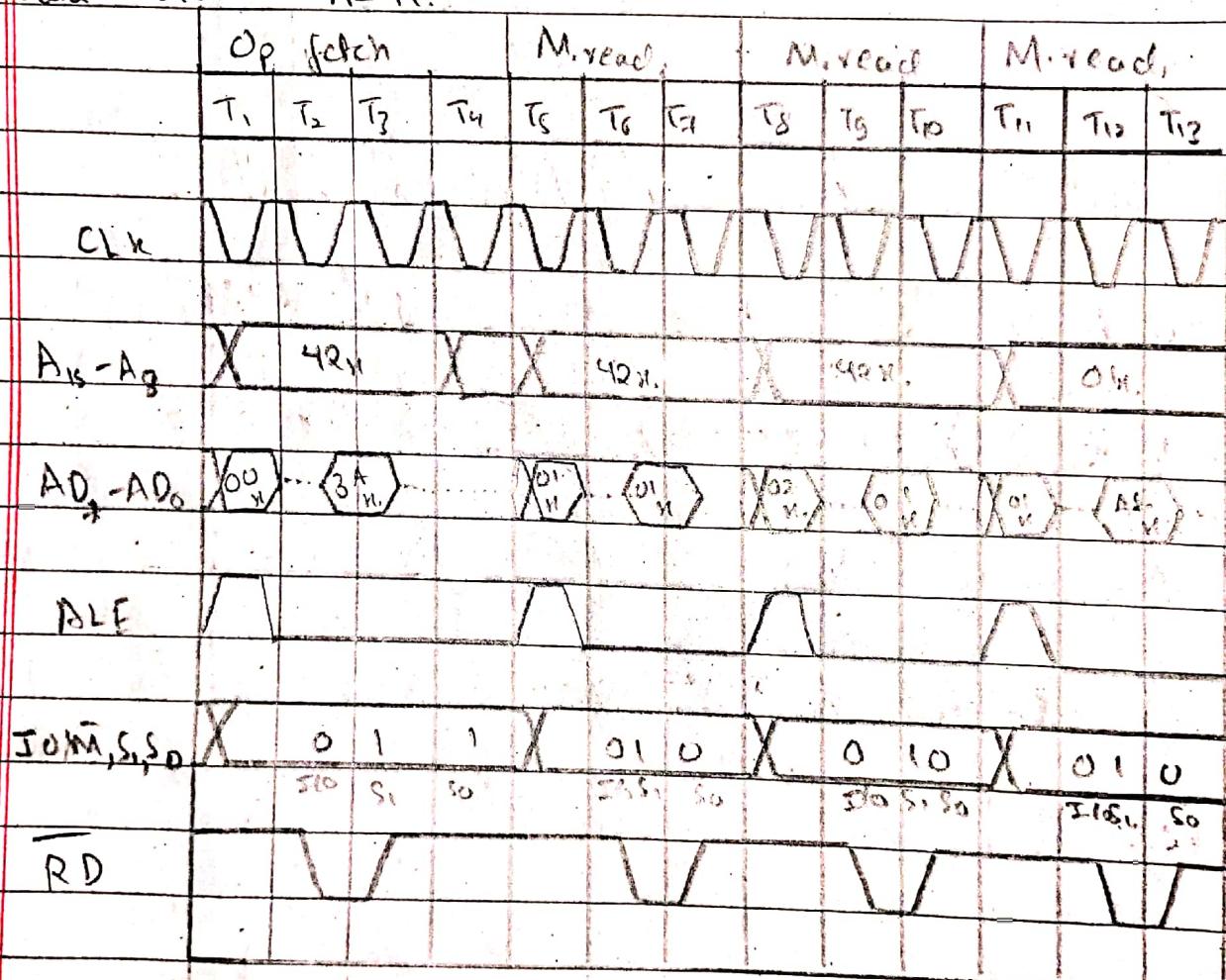


Fig: Timing diagram of LDA 0101 H.

(7) Draw the timing diagram of ADD R and explain it.
on ADD B.

Op code = 81H, 80H.

Operations = Op fetch, ~~Op and memory read,~~

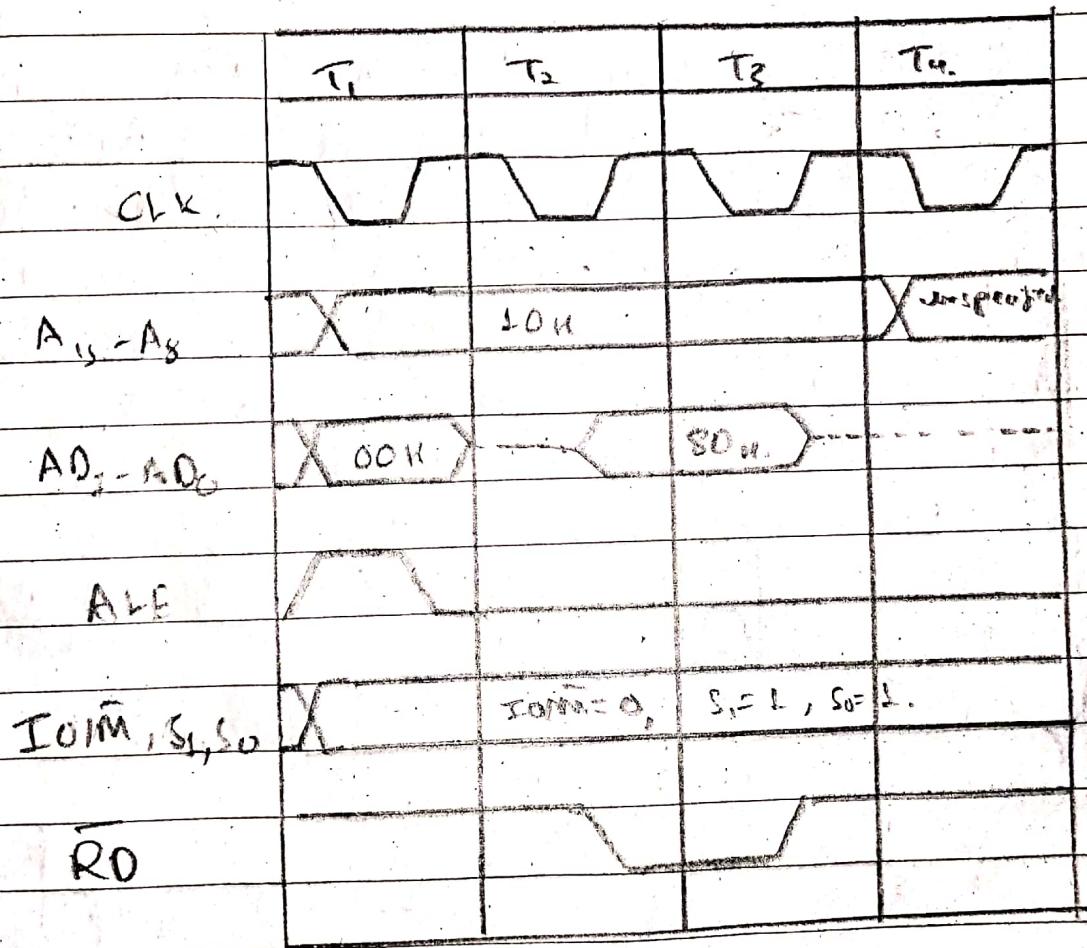


Fig: Timing diagram of ADD R

(8) Draw the timing diagram of instruction INR C and explain it.

Ans. INR : C.

Op code = 0C H.

Operations = Op fetch, Memory read, memory write.

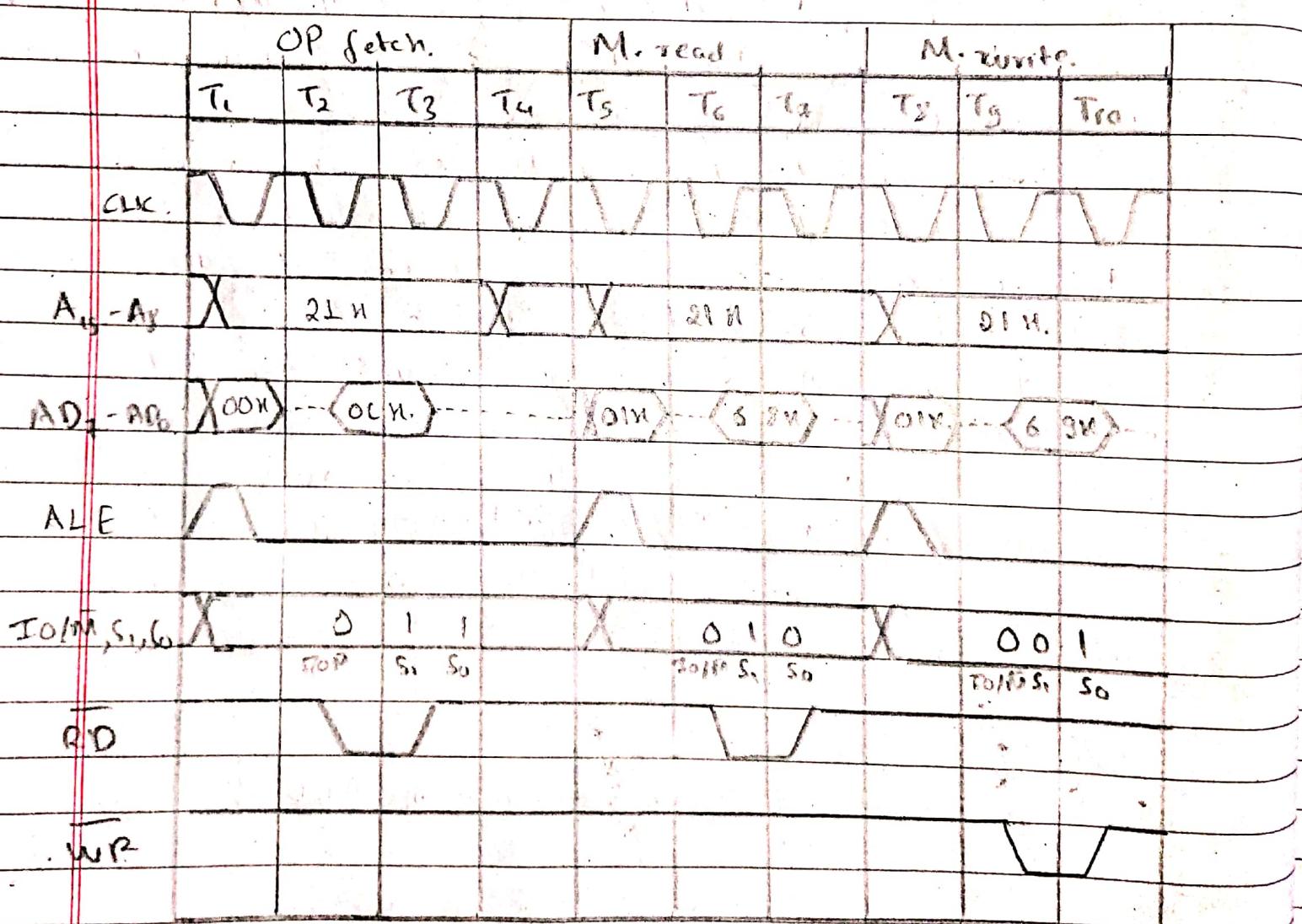


Fig: Timing diagram of INR C.

(9) Draw the timing diagram of instruction MVI A, 01 H and explain it.

Ans MVI A, 01 H.

Opcode = 3E H.

Operations = Op fetch, memory read.

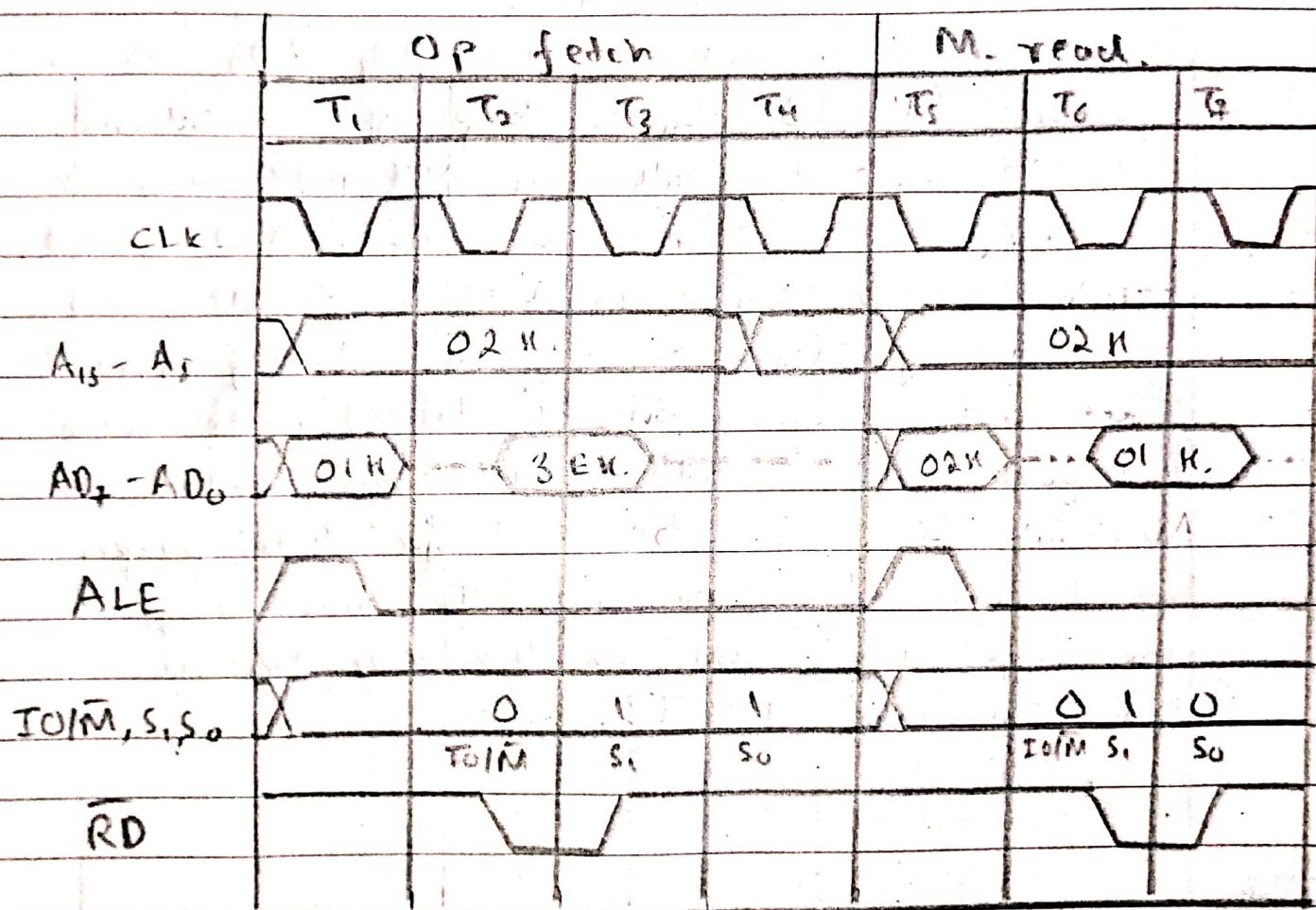


Fig: Timing diagram of MVI, 01 H.

(10) As we know that the address bit on line $AD_7 - AD_0$ remains only for machine cycle T_1 but we need it till machine cycle T_3 . During machine cycle T_2 and T_3 , line $AD_7 - AD_0$ acts as data bus. How does the low address bit on line $AD_7 - AD_0$ made available till T_3 ? What is the mechanism behind it? Explain it.

Ans The low address bit on line $AD_7 - AD_0$ is made available till T_3 by the help of an external latch to save the value of $AD_7 - AD_0$ when it is carrying the address bit. ALE (Address Latch ~~Enable~~ Latch) signal is used to enable this latch. ALE operates as a pulse during T_1 , so the ~~the~~ address can be latched. Then when ALE goes low, the address is saved and the $AD_7 - AD_0$ lines can be used for their purpose as the bi-directional data lines. In this way, the low address bit on line $AD_7 - AD_0$ is made available till T_3 .