

8085 Microprocessor: Timing Diagram

1. Explain the term: Timing diagram, instruction cycle, machine cycle and T-states. What are the control signals used in the timing diagram of 8085 microprocessors? Explain

Ans Timing diagram is defined as the graphical representation of the status of various signals involved during a machine cycle with respect to time. Timing diagram helps us to get the idea of what is happening in the system, like when the data instruction is getting fetched and executed, when the signal is getting activated.

The total number of machine cycles required to execute a complete instruction is known as Instruction Cycle.

The time required by microprocessors to complete the operation of accessing the memory devices or I/O devices is known as machine cycle. Various operations like opcode fetch, I/O read/write, memory read, etc. are performed in the machine cycle.

The time period of a single cycle of the clock frequency is known as T-state.

The control signals used in the timing diagram of 8085 processor are as follows:

1) ~~I/E IO/ms~~

This signal specifies whether the operation (read or write) is being performed on memory or I/O devices.

2) RO:

This signal is used to read the data. It goes low for read operation and becomes high otherwise.

3) wR ;

WR signal is used to write the data. It goes low for write operation and becomes high otherwise.

Q.2. What are different machine cycle in 8085 microprocessor.

Draw timing diagram of each of them and explain.

\Rightarrow The different machine cycle in 8085 microprocessor are as follows:

1) Opcode fetch cycle

2) Memory read cycle

3) Memory write cycle

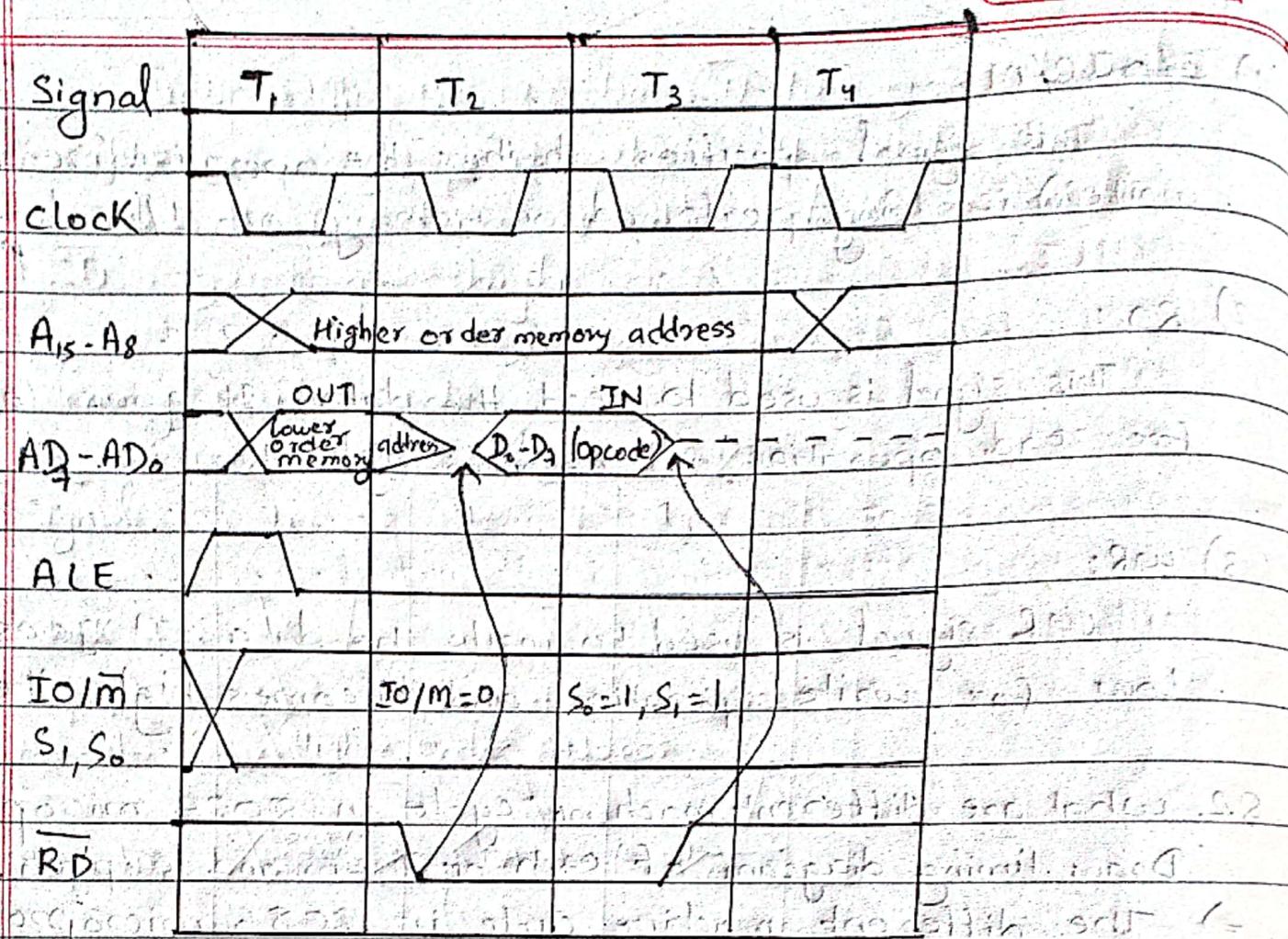
4) I/O Reading from memory takes much less time than writing.

5) I/O ~~new~~ write

respektive zu geschickter technischer Ausbildung und Praxis ist es erforderlich.

1) |Op code| Fetch (

⇒ The diagram of the op code fetch cycle is as follows:



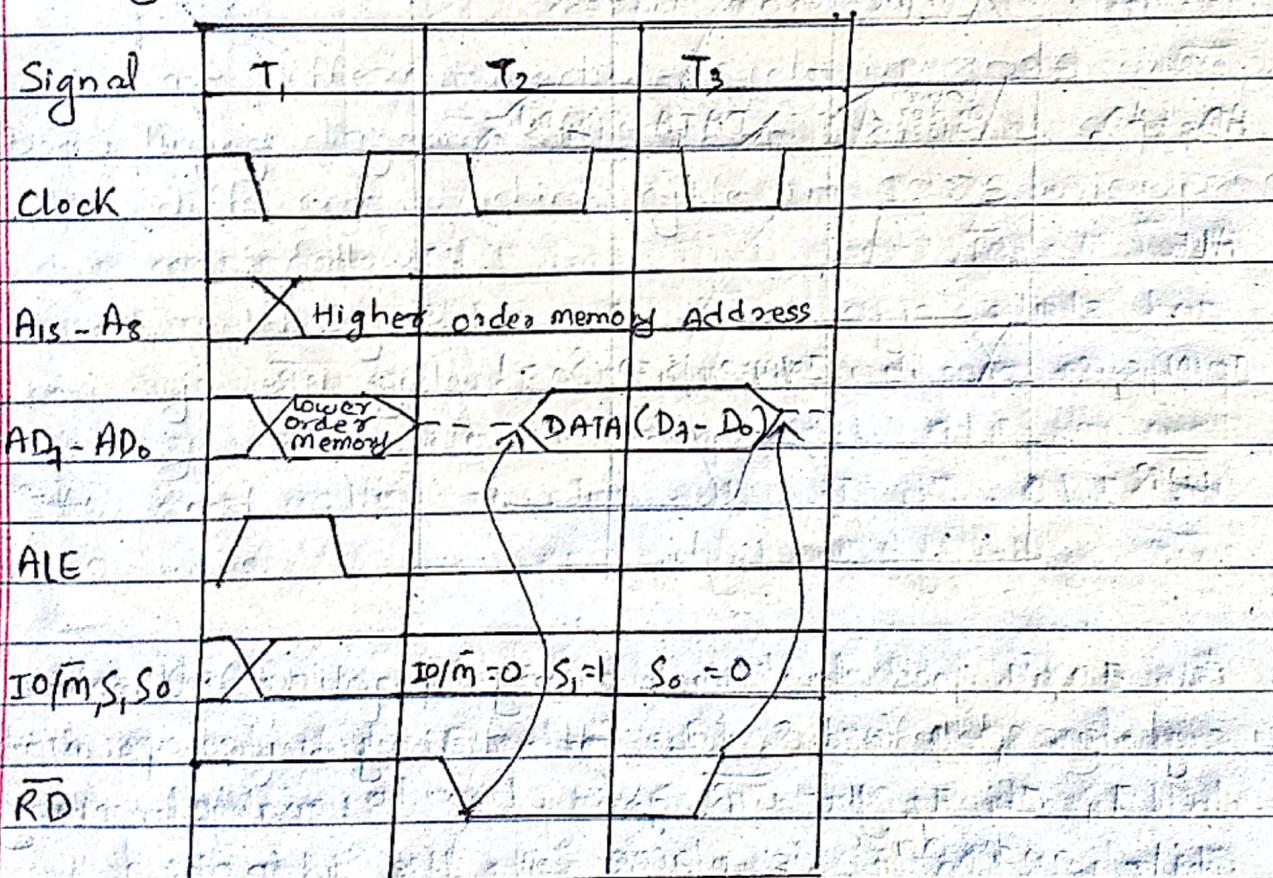
The above diagram can be explained as follows:

- 1) The MP places the 16-bit memory address from the program counter on address bus. At time period T₁, the higher order memory address is placed on the address line A₁₅-A₈; when ALE is high, the lower order address is placed on the bus AD₉-AD₀. The status signal IO/m goes low indicating the memory operation & two status signals S₁ = 1, S₀ = 1, indicating opcode fetch operation.
- 2) During the time period T₂, the MP sends RD control line to enable the memory read. When memory is enabled with RD signal, the op-code

value from the address memory location is placed on the data bus with ALE low.

- 3) During time period T_3 , the op code value reaches at processor register. When data (op-code value) is arrived, the \bar{RD} signal goes high. It causes the bus to go into high impedance state.
- 4) The opcode byte is decoded and executed in the instruction decoder of MP. This happens during time period T_4 .

ii) Memory read cycle



The $I_{O/M}$ signal goes low for memory operation and the status signals $S_1 = 1, S_0 = 0$ to indicate memory

operation in T_1 . In T_2 , the \overline{RD} line goes low to enable memory read where the data in read. At T_3 , data reaches register and \overline{RD} signal goes high.

iii) Memory write cycle

Signal	T_1	T_2	T_3	T_4
Clock	High	Low	High	Low
$A_{15} - A_0$	X	Higher Order Address		
$AD_1 - AD_0$	X	Lower Order Address	DATA ($D_7 - D_0$)	
ALE	High	Low	High	Low
$JO/M, S_1, S_0$	X	$JO/M = 0, S_1 = 0, S_0 = 1$		
\overline{WR}	High	Low	High	Low

The JO/M goes low for memory operation and status signals $S_1 = 0$ and $S_0 = 1$ for memory write operation in T_1 . In T_2 the \overline{WR} goes low to enable memory write and data is placed on the addressed location with ALE low. In T_3 , data reaches memory location and the \overline{WR} line goes high.

iv) I/O Read Cycle

Signal	T ₁	T ₂	T ₃
clock			
A ₁₅ - A ₈	X	I/O Port Address	Address
A D ₇ - A D ₀	X Lower Order Address	DATA	D ₇ - D ₀
ALE			
I ₀ / M ₁ , S ₁ , S ₀	X	I ₀ / M ₁ = 1	S ₁ = 1, S ₀ = 0
RD		V	

The I_0/m goes high for I/O operation and status signals $S_1=1$ and $S_0=0$ for read operation in T_1 . In T_2 , the \overline{RD} line goes low to enable memory read and the data is read. In T_3 , the data reaches register and \overline{RD} line goes high.

v) I/O write cycle

Signals	T ₁	T ₂	T ₃	
Clock				
A ₁₅ -A ₈	X			PORT ADDRESS
AD ₇ -AD ₀	X Lower Order Address		DATA(DA-D ₀)	
ALE				
I ₀ /I _m , S ₁ , S ₀	X	I ₀ (M=1)	S ₁ =0, S ₀ =1	
WR				

The I₀/I_m goes high for I/O operation and status signals S₁=0 and S₀=1 for write operation in T₁. In T₂ the WR line goes low for I/O write operation and data is written in I/O. In T₃, the data is written and the WR gate goes high.

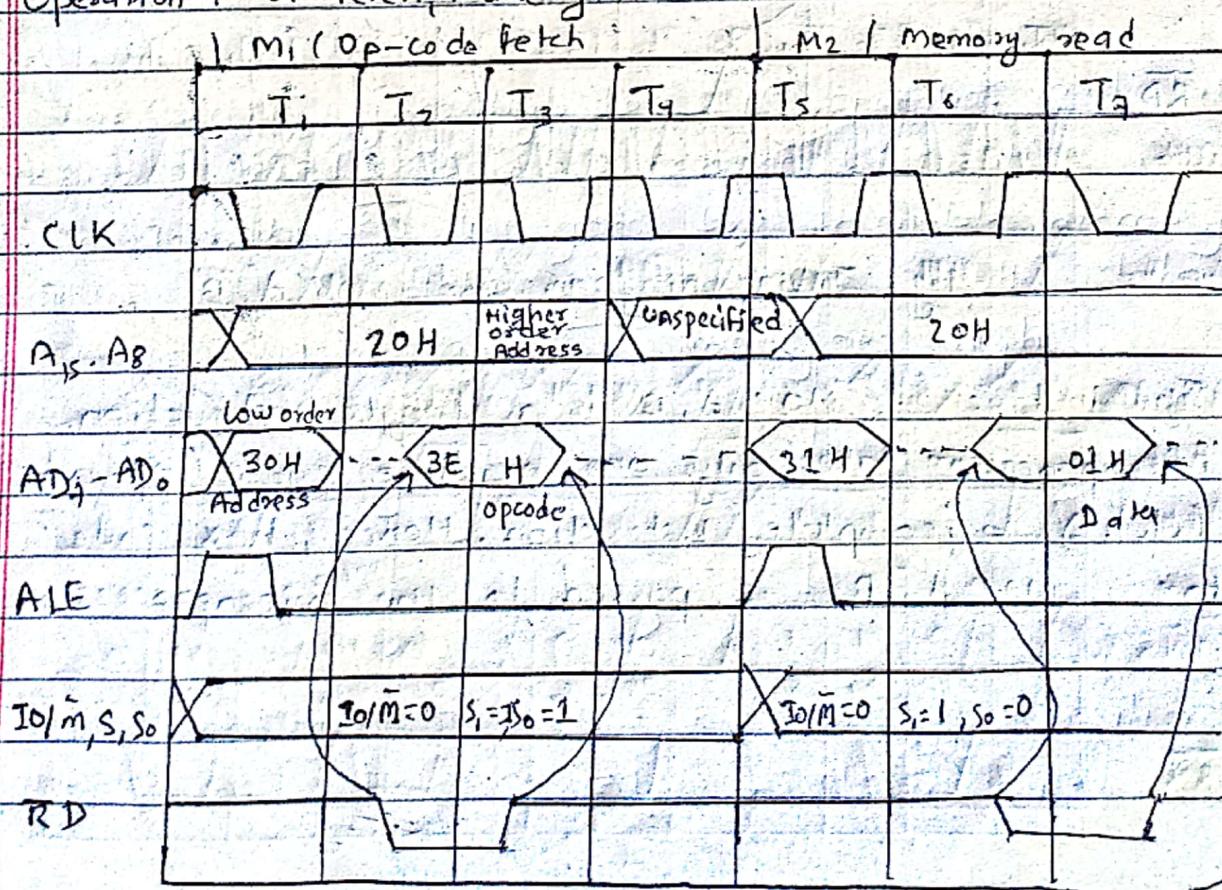
Q. As we know that the address bit on line AD₇-AD₀ remains only for machine cycle T₁ but we need it till machine cycle T₃. During machine cycle T₂ and T₃, line AD₇-AD₀ acts as data bus. How does the lower address bit on the line AD₇-AD₀ made available till T₃? What is the mechanism behind it? Explain it.

⇒ On the line $AD_7 - AD_0$, the low address bit is made available $H11 T_3$ with the help of an external latch to save the value of $AD_7 - AD_0$, when it carries the address bit. ALE (Address Latch Latch) signal is used to enable this latch. During T_1 , ALE acts as a pulse so that the address can be latched. When ALE goes low, then the address is saved. $AD_7 - AD_0$ lines can be used for the purpose as the bi-directional data lines. In this way, the low address bit on line $AD_7 - AD_0$ is made available $H11 T_3$.

3. Draw the timing diagram of instruction MVI A, 01H stored in memory location 2030H and explain it.

⇒ MVI A, 01H

Operation : OP fetch, memory read



4) Draw the timing diagram of instruction MOV A, B and explain it.

$\Rightarrow \text{MOV A, B}$ (Address : 0002 H)

Operation : OP Fetch

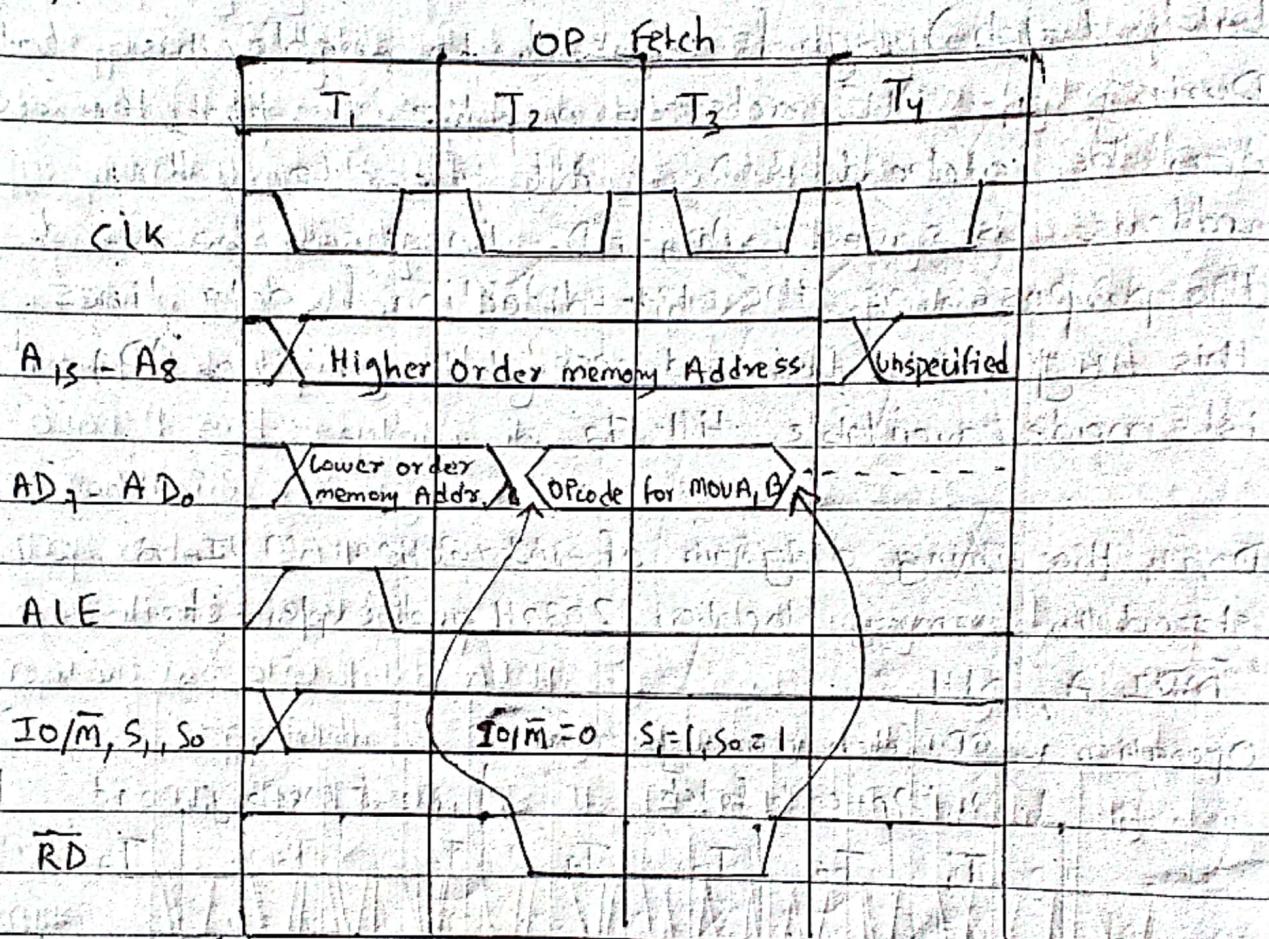


Fig : Timing diagram for MOV A, B

The instruction MOV A, B is a 1-byte instruction. microprocessor takes only one machine cycle (op-code fetch) to complete instruction. Hence, hex code for MOV A, B is passed to the microprocessor.

5. Draw the timing diagram of instruction STA 1001H and explain it.

=) STA 1001H

Op code = 32H

Operation: Op fetch, Memory read, Memory read, Memory write
let address be 00031H and

Data in accumulator be 21H

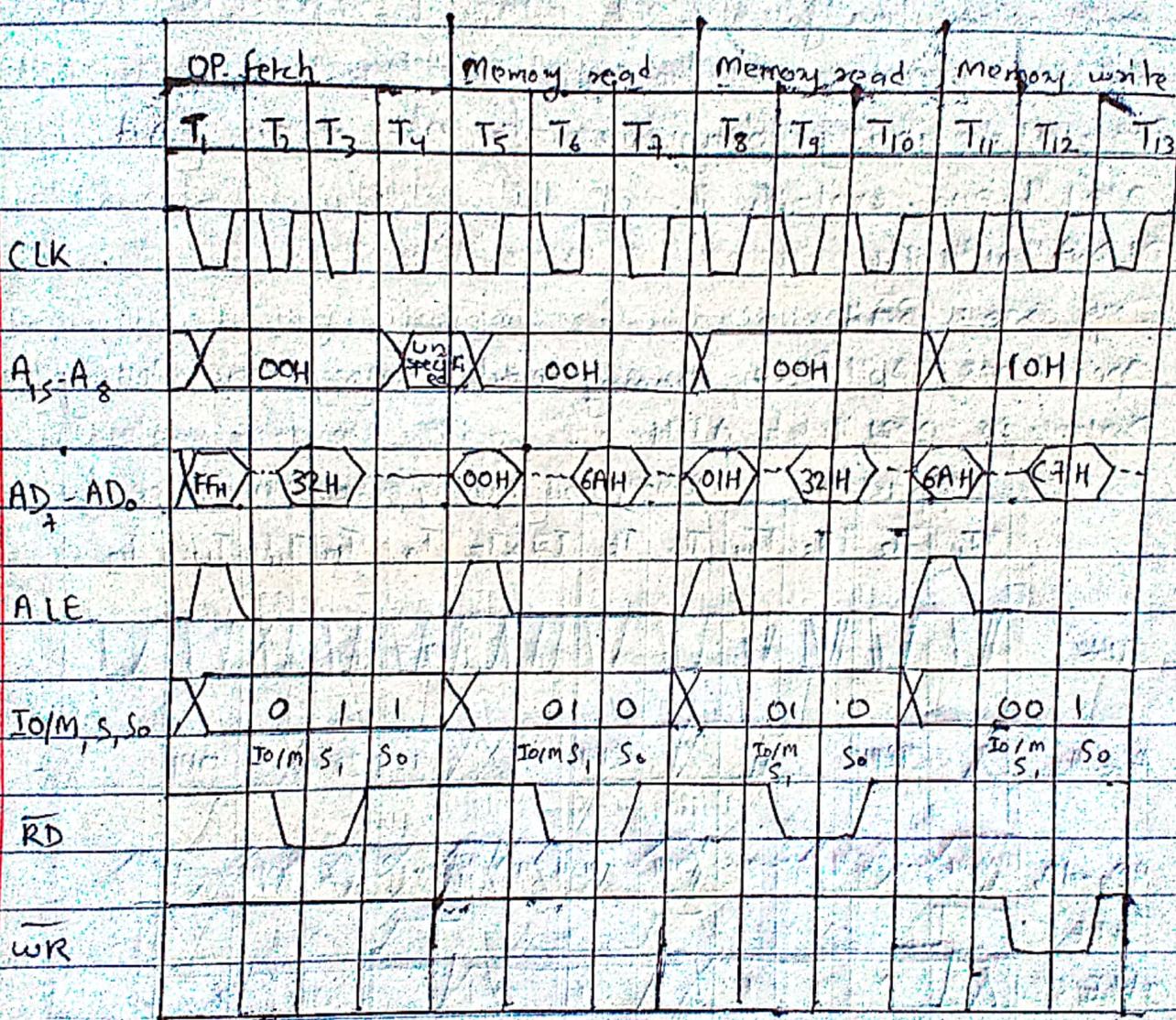


Fig: Timing diagram for STA 1001 H

STA is a mnemonic that stands for Store Accumulator contents in memory. In this instruction, Accumulator 8-bit

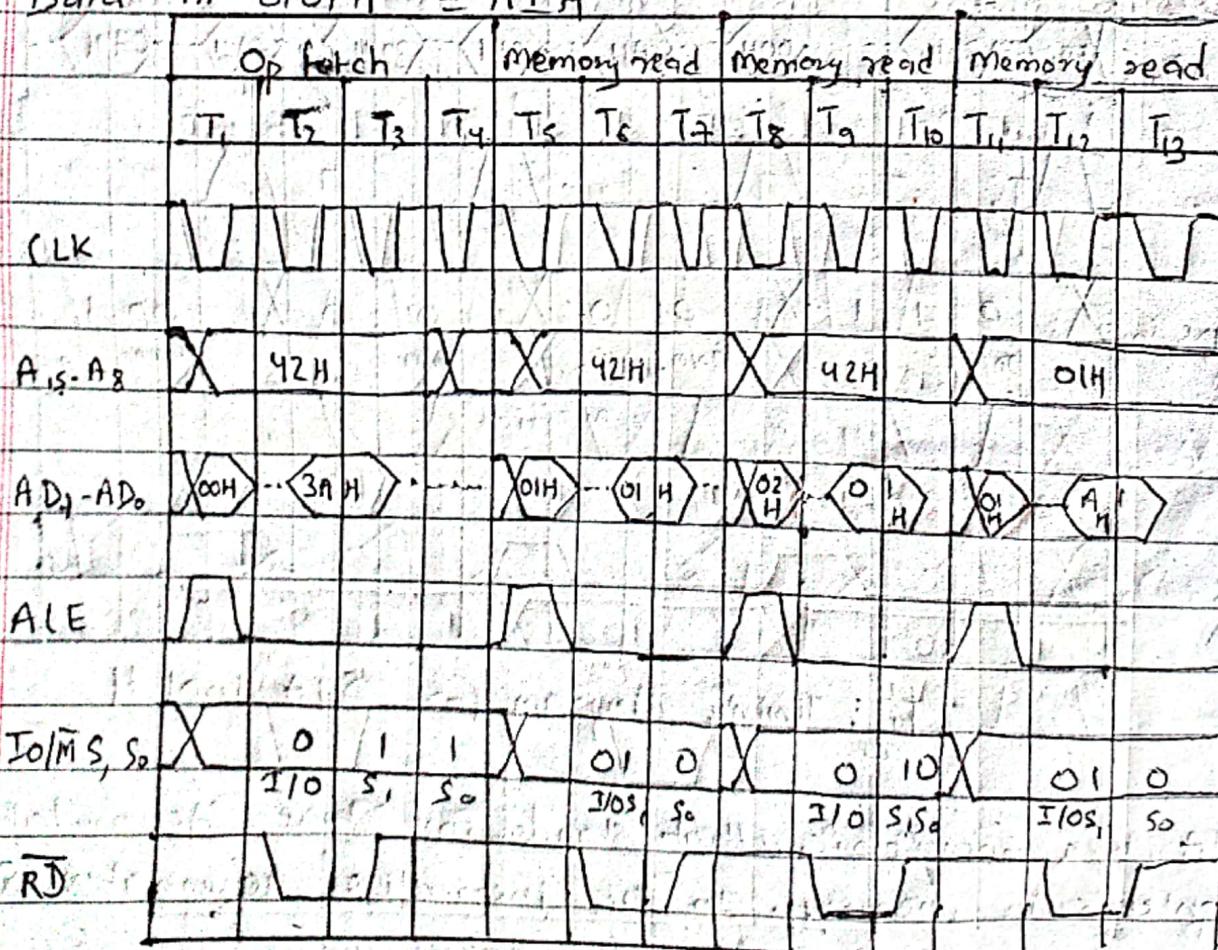
content will be stored to a memory location whose 16 bit address is indicated in the instruction as a_{16} . This instruction uses absolute addressing for specifying the destination. This instruction occupies 3-bytes of memory. First byte is required for the Op code, and next successive 2-bytes provide the 16-bit address divided into 8-bits each consecutively.

6) Draw the timing diagram of instruction LDA 0101 H and explain it.

=) LDA 0101 H

Op code: 3AH

Operations: Op fetch, Memory read, Memory read, Memory read
Data in 0101 H = A1H



In 8085 instruction set, LDA is a mnemonic that stands for load Accumulator with the contents from memory. In this instruction, Accumulator will get initialized with 8-bit content from the 16-bit memory address as indicated by as a 16. This instruction uses absolute addressing for specifying the data. It occupies 3-bytes in the memory, first byte specifies the Opcode, and the successive 2-bytes provide 16-bit address i.e. each 1-byte for each memory location.

7) Draw the Timing diagram of ADD B and explain it.

\Rightarrow ADD B

Op code = 80H

Operations = op fetch

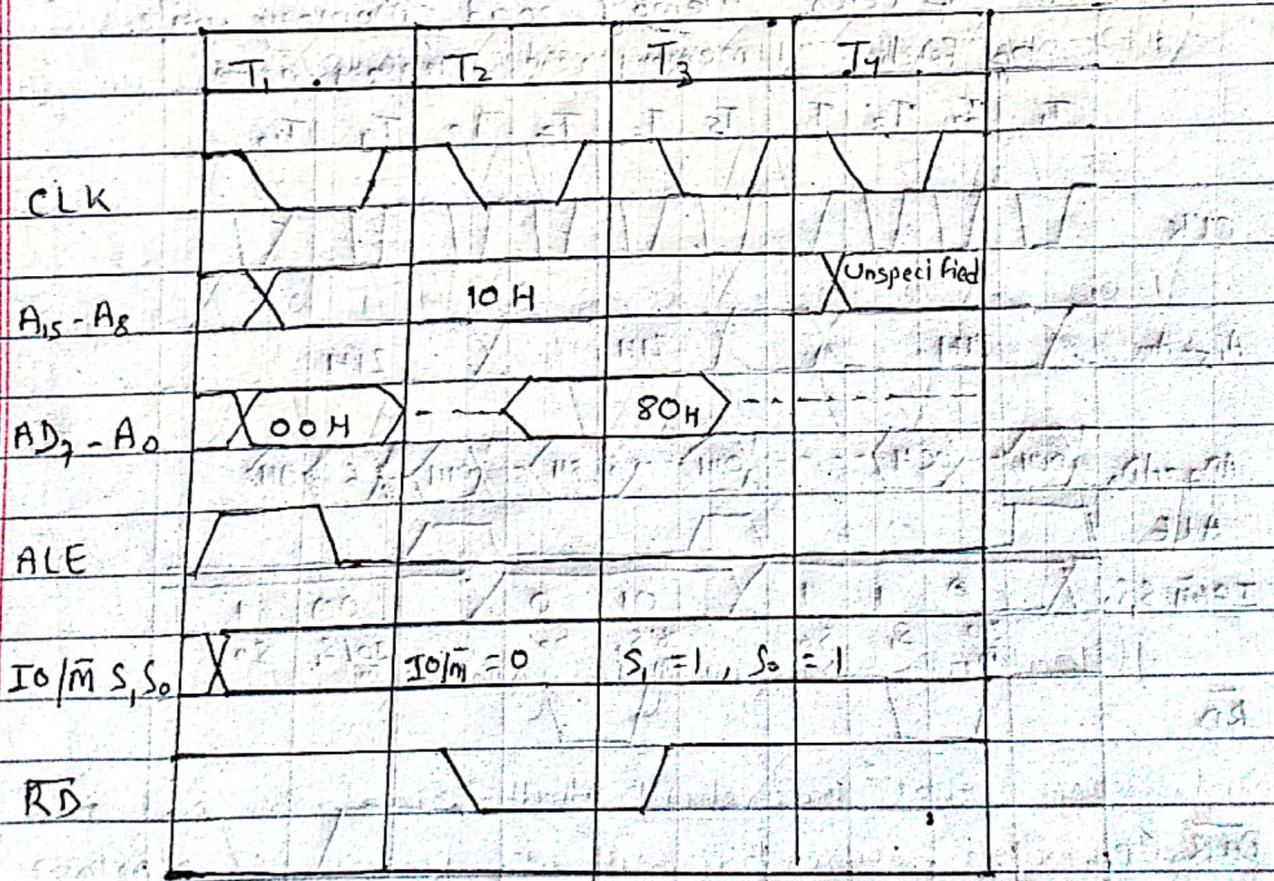


Fig: Timing Diagram of ADD B

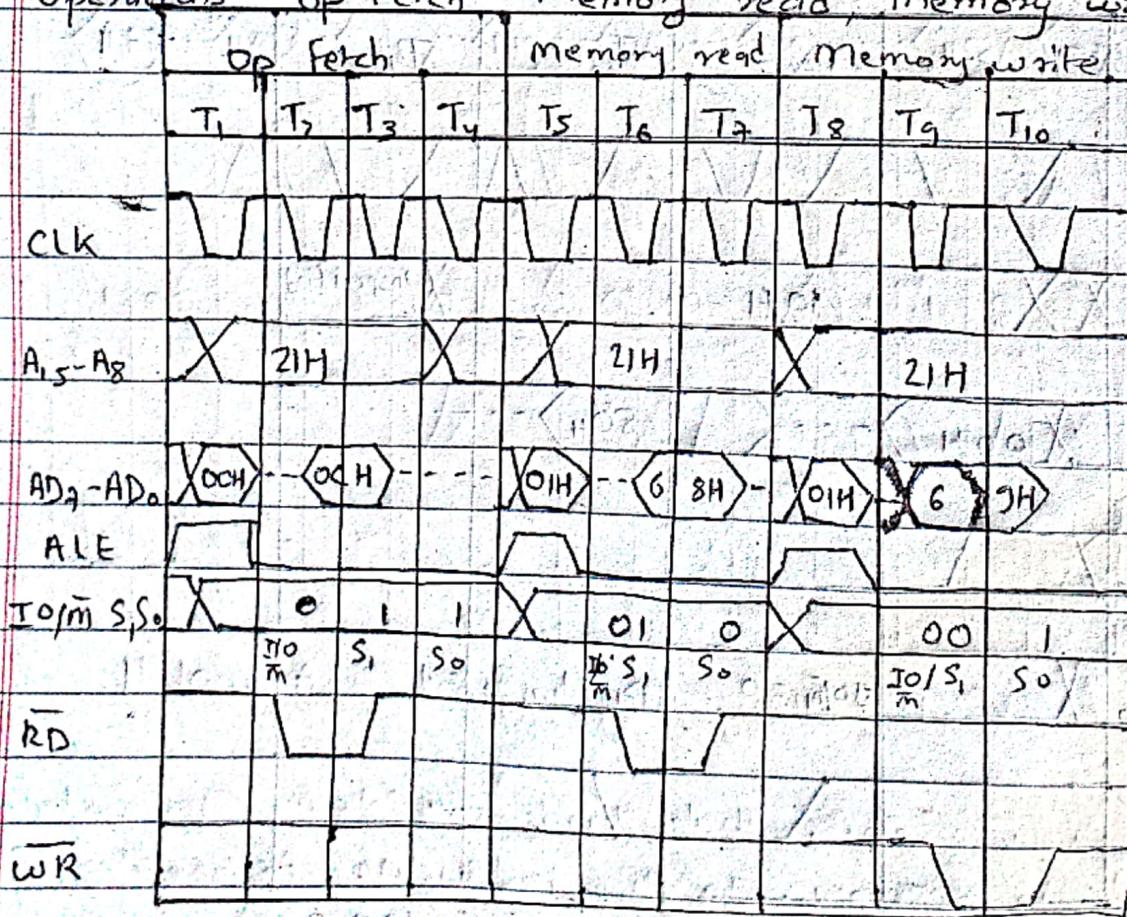
ADD B instruction adds contents of accumulator with contents of register B and result will be stored in accumulator. In executing any instruction, micro-processor first needs to fetch its Opcode which requires four T-states. In case of ADD B also, as soon as it fetches the opcode, it understands the function to be performed ^{as it} and does not need extra machine cycle as both A and B are internal registers. Hence, addition operation will be completed by the end of the 4th T-state & result will be stored.

8. Draw the timing diagram of instruction INR C and explain it.

⇒ INR C

Op code = DC H

Operations = Op Fetch, Memory read, Memory write.



Fg: Timing Diagram of INR C

In 8085 instruction set, INR is a mnemonic that stands for 'INCrement' and 'R' stands for any of the registers or memory location M pointed by HL pair. This instruction is used to add 1 with contents of R.

g. Draw the timing diagram of instruction MVI A, 01H and explain it.

i) MVI A, 01H

Op code = 3EH

Operations = Op fetch, memory read

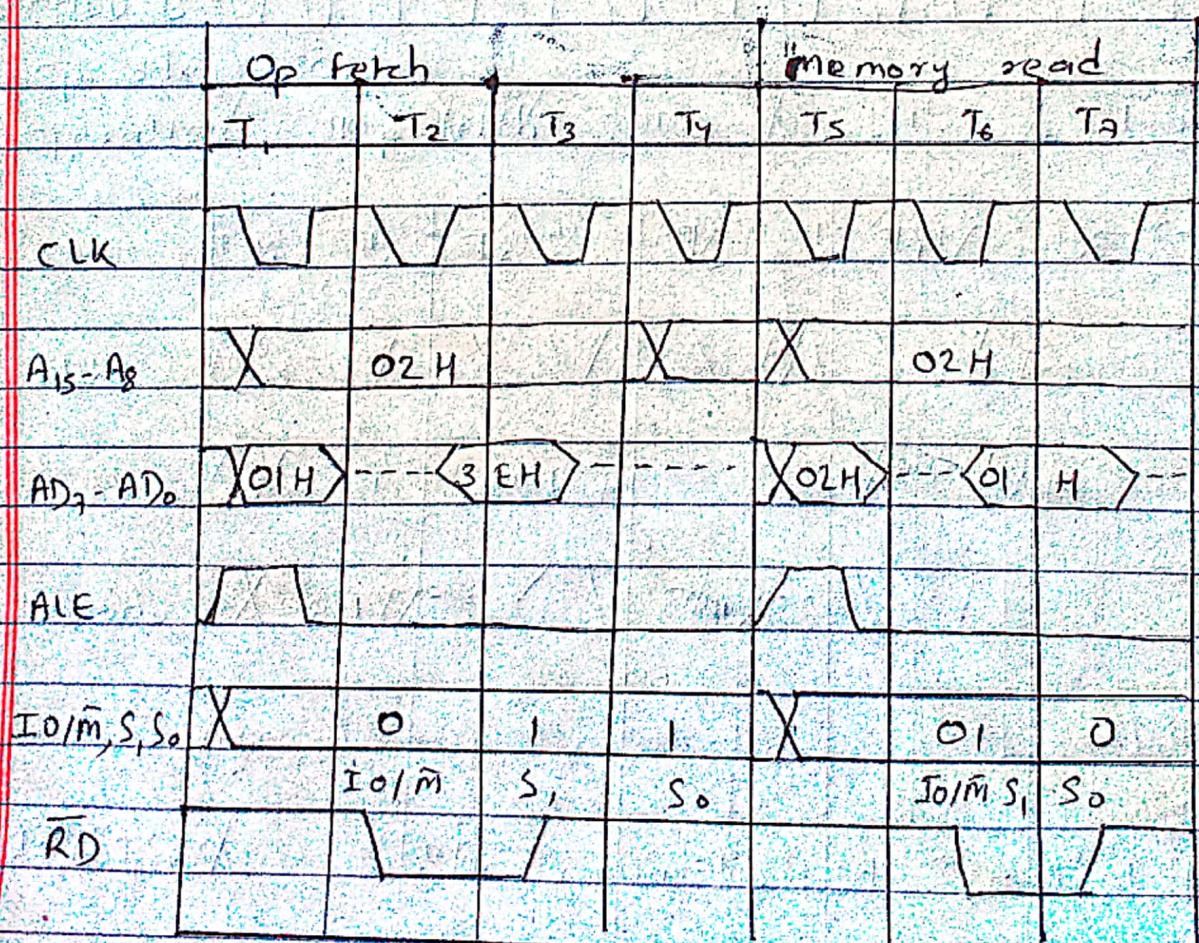


Fig: Timing Diagram of MVI, 01 H

MVI is a mnemonic which actually means "Move immediate". With this instruction, we can load a register with an 8-bit or 1 byte value. This instruction supports immediate addressing mode for specifying the data in the instruction. In the instruction "d8" stands for any 8-bit data, and "r" stands for any one of the registers e.g. A, B, C, D, E, H or L. So this r can replace any one of the seven registers.