Sidhant Priyadarshi

sidhant1922@gmail.com | 9560121498

Last Updated on 25th August 2022

EDUCATION

KLE TECHNOLOGICAL UNIVERSITY

Bachelor in Engineering
Expected in july 2023 | Karnatak, IN
CGPA: 8.73

MOTHER KHAZANI CONVENT SCHOOL

Senior Secondary
Passed in July 2019 | Delhi, IN
CGPA 8.25

LINKS

Github: **sidhantp1906**
LinkedIn: **Sidhant Priyadarshi**

EXPERIENCE

KLE TECHNOLOGICAL UNIVERSITY

EA Office Bearer
June 2021 – june 2022 | Hubli, Karnatak

- Organizing academic events for ECE branch.
- We have organized workshops on Python, MATLAB and quizes on pre-placement activities, etc.
- I was the speaker of RTL Workshop at KLE Technological University and VLSI Overview at MJCET, Hyderabad.

SKILLS

PROGRAMMING

Verilog, SystemVerilog, OOPS
Python, C, MATLAB, UNIX.

TOPICS

Computer Architecture, STA,
Digital/Analog Electronics, VMM,
AMBA Protocols, UART/I2C/SPI,
Arduino, 8051/8086.

TOOLS

Digital
Xilinx ISE, Cadence Genus, IcarusVerilog and GTKWAVE.
Analog
Cadence Virtuoso, Synopsys Custom Compiler.
Mixed Signal
LTSpice, eSIM.

LANGUAGE

English
Hindi

PERSONAL PROJECTS

RISC-V RV32I DESIGN AND VERIFICATION

Designed 5-stage pipelined RV32I core for few of the arithmetic and memory instruction sets like add,load and store, etc using Verilog HDL which is verified using python based(CoCoTB) verification module and currently verifying using UVM architecture.
Link to Project.

AMBA - APB4 AND AHB-LITE

Designed a AMBA protocols like APB and AHB-LITE which performs simple read and write using Verilog HDL.
Link to Project.

FCFS ARBITER RTL2GDS

Designed a FCFS Arbiter to grant request to 4 processes based on first come first serve algorithm using Verilog HDL, verfied using VMM based verification and synthesized using Genus and Backend is done in Innovus.
Link to Project.

32-BIT CSD MULTIPLIER

Designed a CSD multiplier to multiply signed number by reducing stream of ones in digit with booth algorithm using Verilog HDL.
Link to Project.

RESEARCH

PARALLEL DIGITAL VLSI ARCHITECTURE FOR COMBINED SVM TRAINING AND CLASSIFICATION

Research Experience Undergrad
Feb 2022 – Present | Hubli, Karnatak
Working with **Prof. Dr Saroja V Siddamal** on research and design of SVM training and classification digital architecture which classifies between diabetic and non diabetic person based on glucose level. This work will be published by the end of this year.

COURSES/CERTIFICATES

VLSI CAD Logic to Layout:	Coursera
Learn to build UVM/OVM testbench from scratch:	Udemy
VLSI SOC Design using Verilog HDL:	MAVEN SILICON
eSIM Marathon finalist:	IIT-Bombay and VSD
Cloud based Analog Design Hackathon finalist:	Synopsys and VSD
VLSID 2022 Participation:	VLSI Society of India

AREAS OF INTEREST

RTL Design, Computer Architecture
SOC Design and Verification
Programming

SUMMARY

Computer Architecture, Design and Verification enthusiast. My goal is to leverage my expertise to help succeed the semiconductor industry.