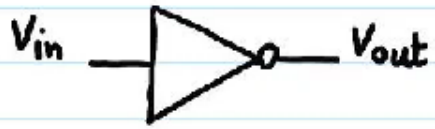
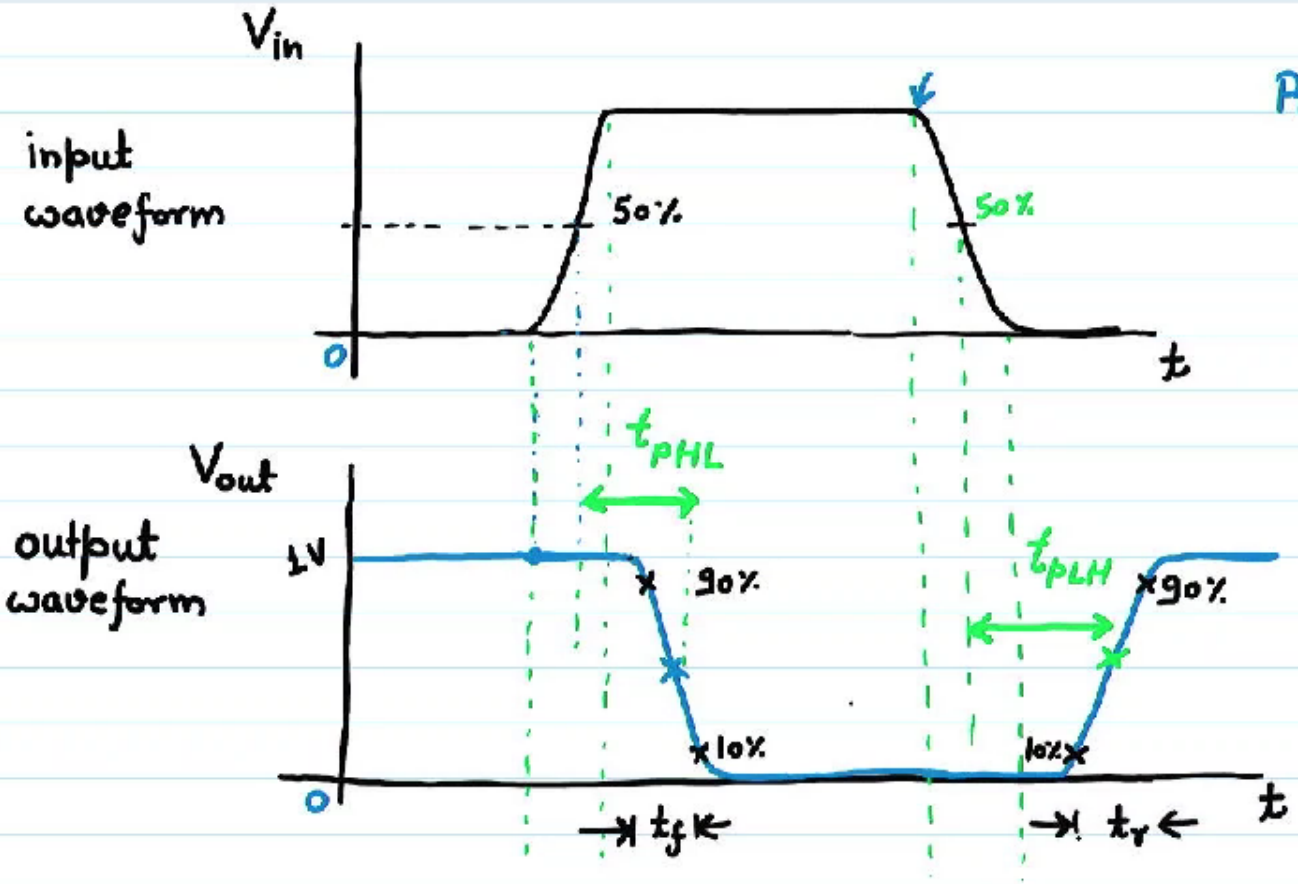
Circuit Delay Definitions :





Propagation Delay

$$t_p = \left(\frac{t_{PHL} + t_{PLH}}{2} \right)$$

Definitions :

Rise - Time (t_r) : time to rise from 10 % of V_{DD} to crossing 90 % of V_{DD}.

Fall - Time (t_f) : time to fall from 90 % of V_{DD} to crossing 10 % of V_{DD}.

$$\text{Edge - rate } (t_{rf}) = \left(\frac{t_r + t_f}{2}\right)$$

T_{pHL} : Delay when output goes from High to Low when input is rising.

T_{pLH} : Delay when output goes from Low to High when input is falling.

$$\text{Delay } (t_p) = \left(\frac{T_{pLH} + T_{pHL}}{2}\right)$$

Where does the power go in CMOS Circuits :

1) Dynamic Power Dissipation

Charging and discharging of capacitors.

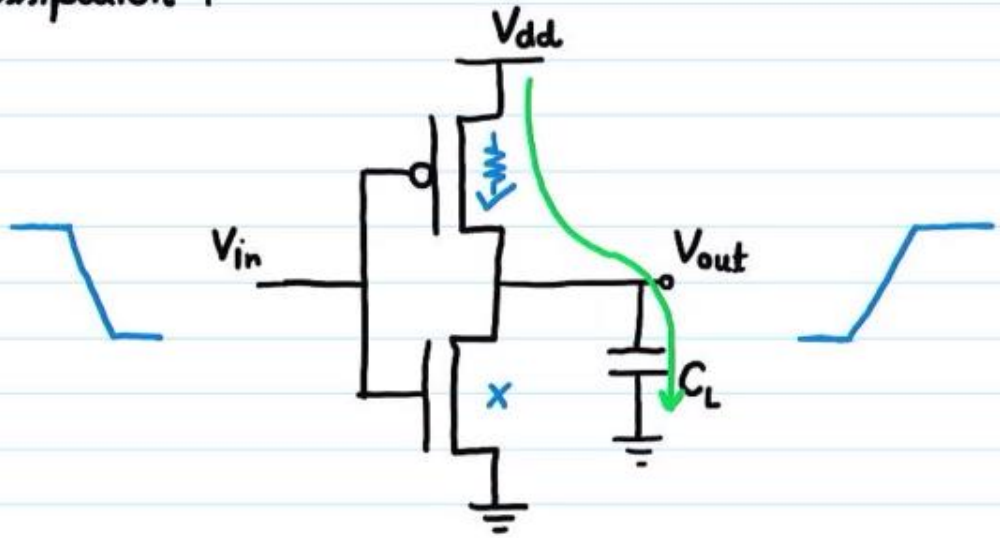
2) Short - Circuit Current

Short circuit path between supply-rails during switching

3) Leakage

Leaking diodes and transistors.

Dynamic Power Dissipation :



$$\text{Energy / Transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/Transition} * f = C_L \cdot V_{dd}^2 \cdot f$$

- Not a function of transistor sizes.
- Need to reduce C_L, V_{dd} and f to reduce power.

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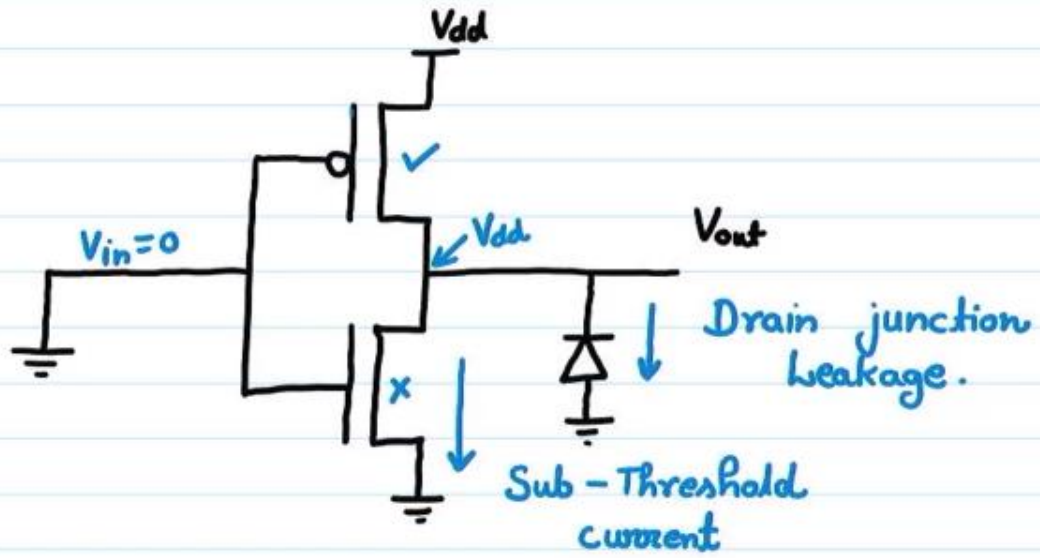
Leakage :



Sub-threshold current is one of the most compelling issue in low-power circuit design.

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