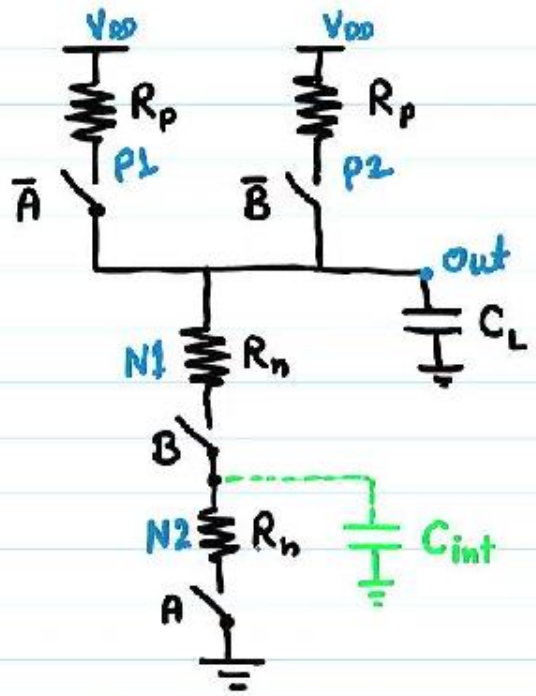
Input Pattern dependent delay :



- Delay is dependent on the patterns of input.

→ Low to High Transition

- both inputs go low

delay is $0.69 \cdot \frac{R_p}{2} \cdot C_L$

- one input goes low

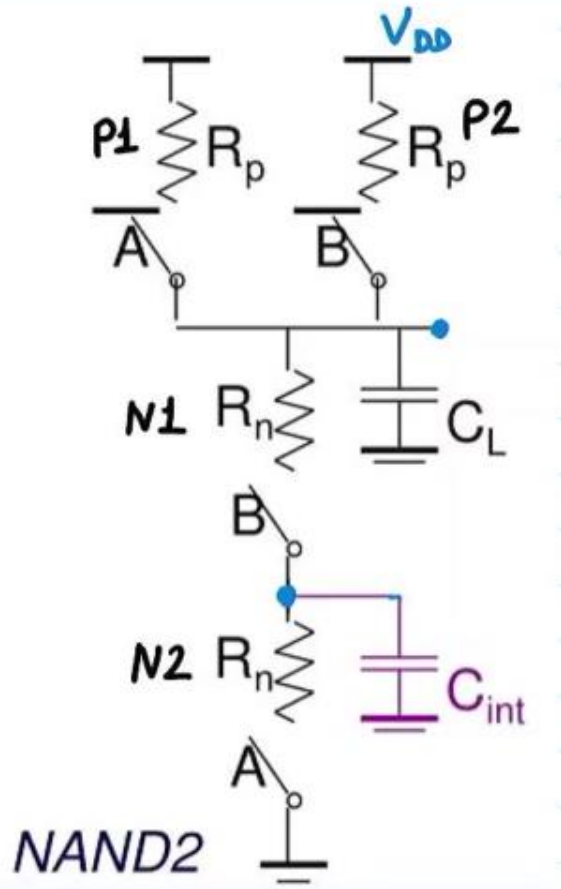
delay is $0.69 \cdot R_p \cdot C_L$

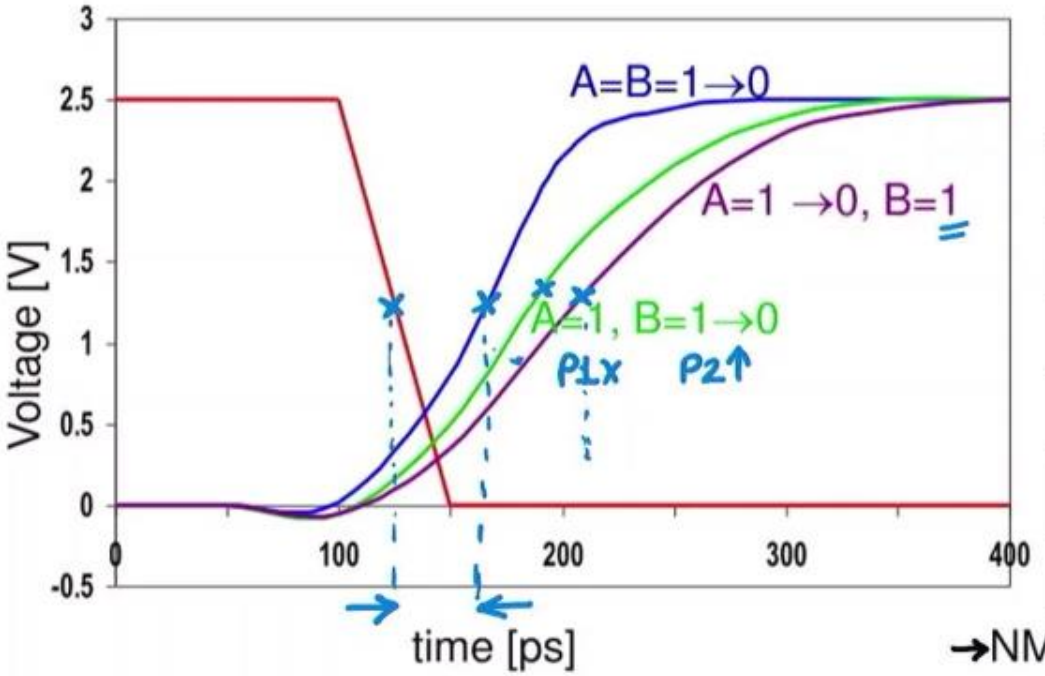
→ High to Low Transition

- both input go high

delay is $0.69 \cdot 2R_n \cdot C_L$

Delay dependence on input pattern :



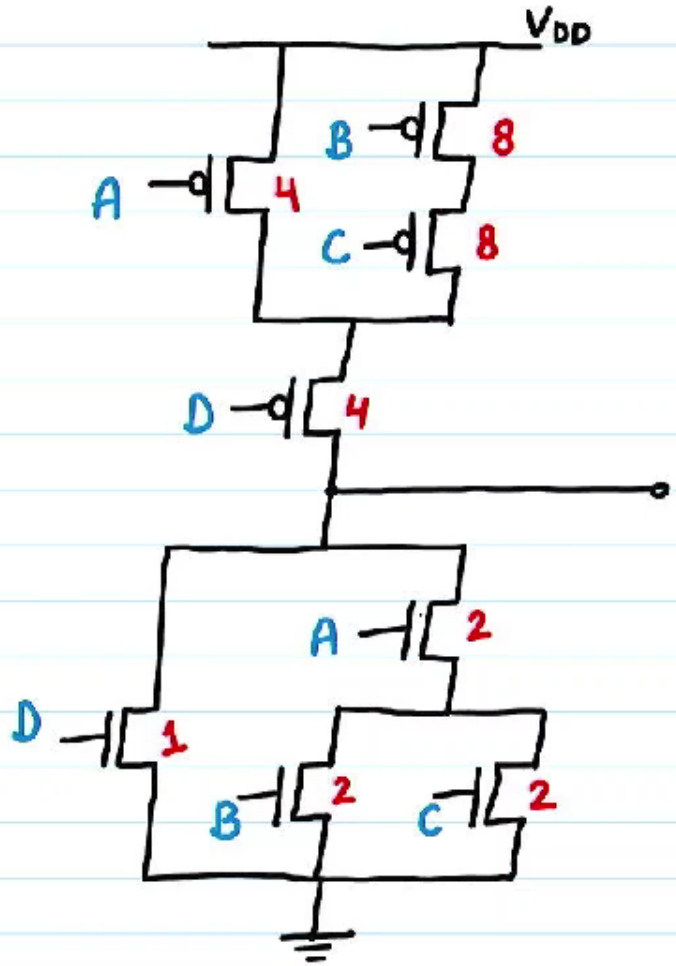


Input Data Pattern	Delay (psec)
A=B=0→1	67
A=1, B=0→1	64
A= 0→1, B=1	61
A=B=1→0	45 best Case
A=1, B=1→0	80
A= 1→0, B=1	81 worst Case..

→NMOS = 0.5μm/0.25 μm
→PMOS = 0.75μm/0.25 μm

NPTEL

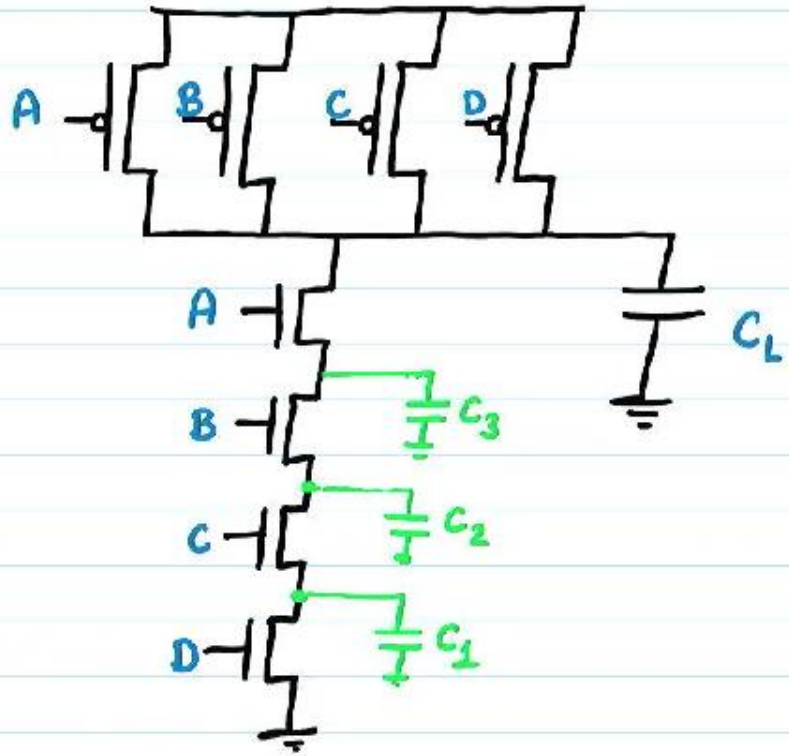
Transistor sizing of complex CMOS gates :



$$OUT = \overline{D + A \cdot (B + C)}$$

Fan - In of Gate :

4 - INPUT NAND



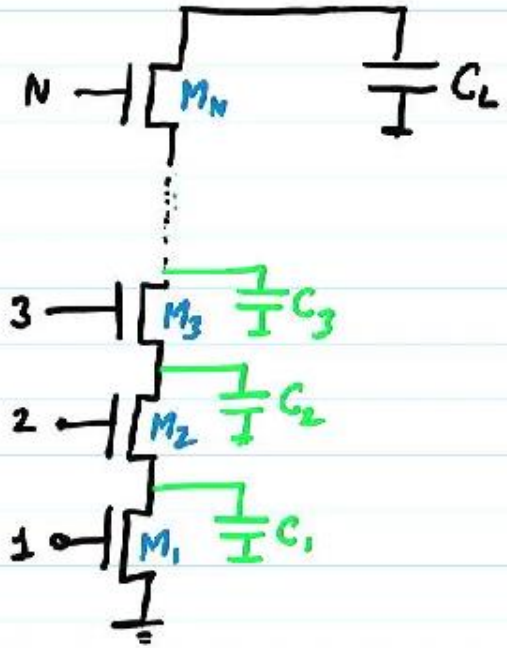
Distributed RC model
(Elmore delay)

$$t_{pHL} = 0.69 \cdot R_{eqn} (C_1 + 2C_2 + 3C_3 + 4C_L)$$

Propagation delay degrades rapidly as a function of fan - in. - Quadratically in the worst case.

Design Techniques for fast logic gates.

- Progressive Sizing :



Distributed RC line

M1 > M2 > M3 > --- > MN

(the transistor closest to the output is smallest)

Can reduce delay by more than 20%.