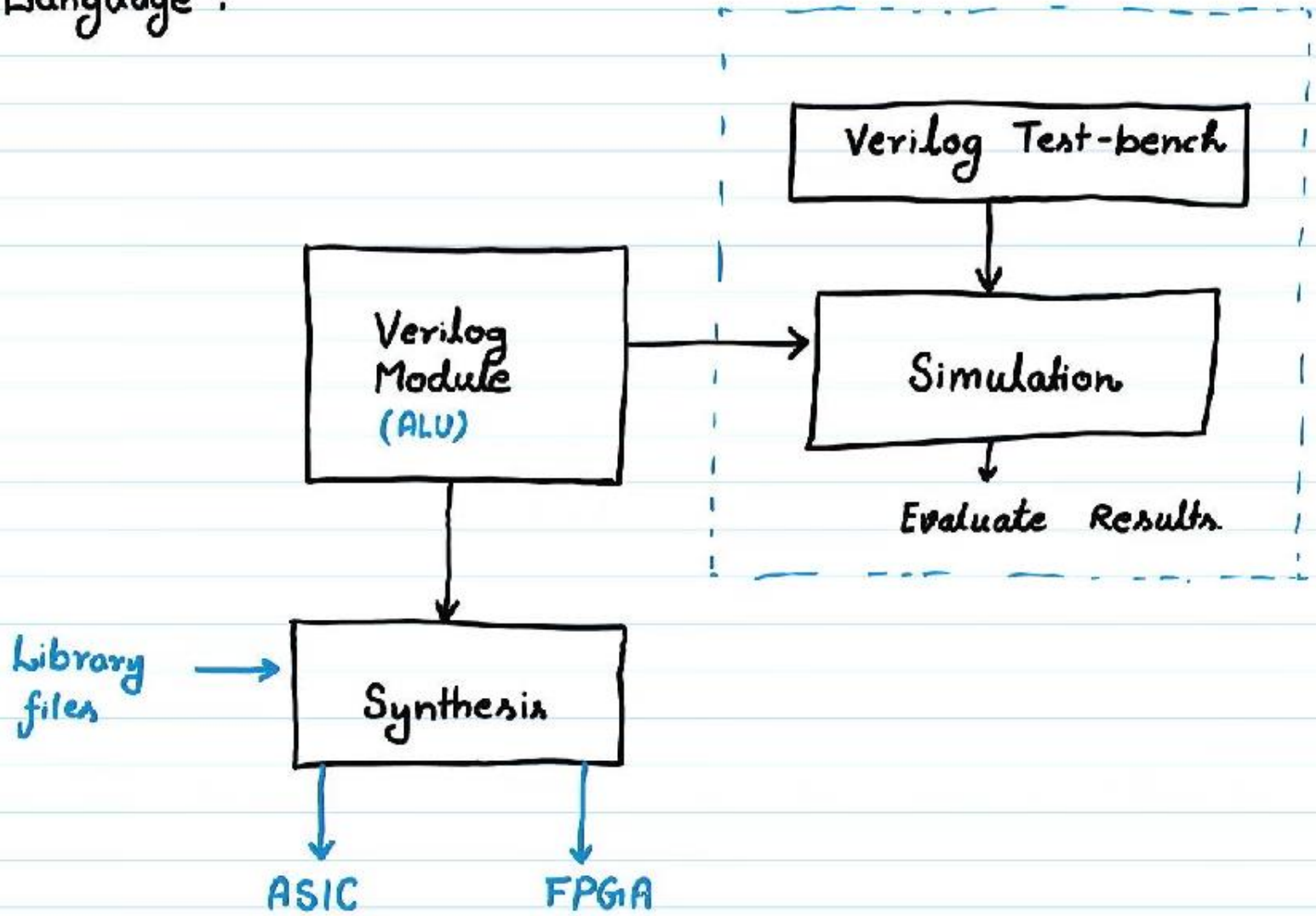
Verilog Language :



NPTEL

Simulation :

- It is used to verify the functionality of the digital design that is modeled using Verilog language.

- We apply different input stimulus to the design at different time, to check whether the RTL code behaves like the intended way or not.

Synthesis : This is a process in which the digital design that is modeled is translated into an implementation consisting of different logic gates.

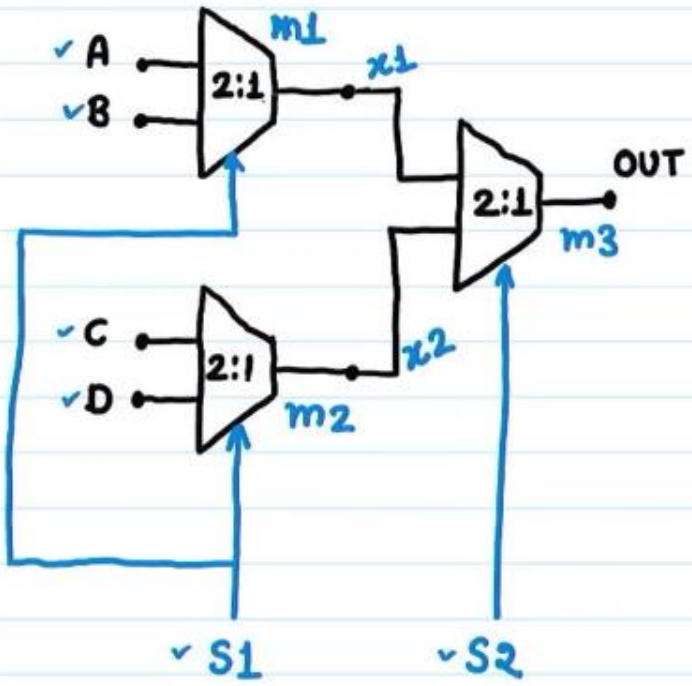
Module Instantiation.

- This is the process of creating object from the module template. These objects are called instances.

- One module definition can not contain another module definition.

- However, we can include copies of other modules by instantiation.

Example : Design a 4:1 MUX using 2:1 MUX.




```
module  mux_4to1 ( A , B , C , D , S1 , S2 , out ) ;
    input  A,B,C,D,S1,S2 ;
    output  out ;
    wire  x1 , x2 ;

    mux_2to1  m1 ( A,B , S1 , x1) ;
    mux_2to1  m2 ( C , D , S1 , x2) ;
    mux_2to1  m3 ( x1,x2 , S2 , out ) ;
endmodule

module  mux_2to1 ( x , y , sel , out ) ;
   input  x , y , sel ;
   output  out ;
    :
    :
    :
    :
endmodule
```

Delay :

```
module   D ( a ,b,c , out )

    input  a , b, c ;
    output  out ;

  and  #(3)  a1(c1, a ,b)
   or  #(4)  o1(out,c,c1)

endmodule
```