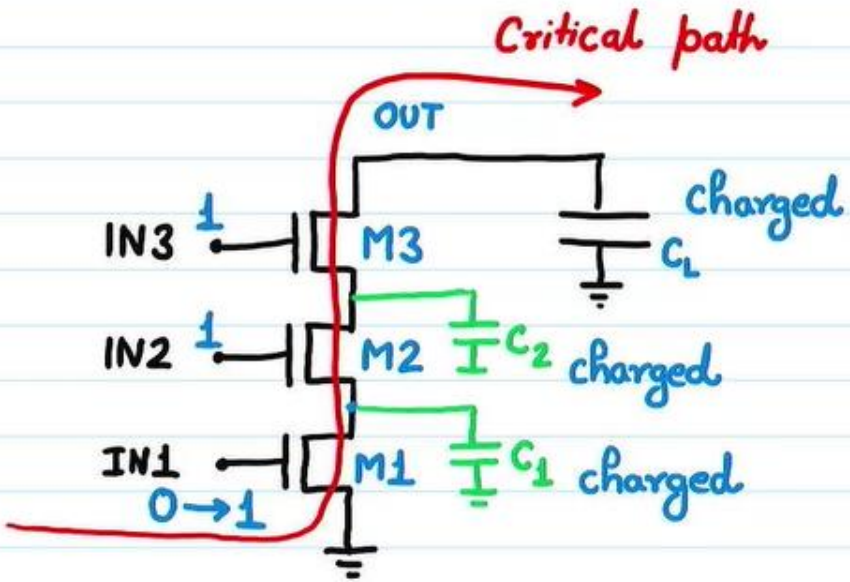
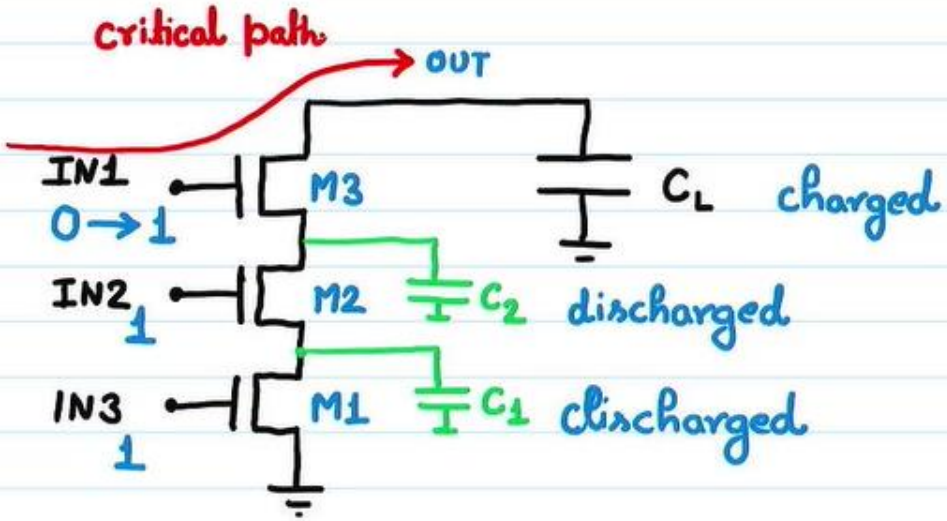
Design Techniques 2 for fast CMOS gates :





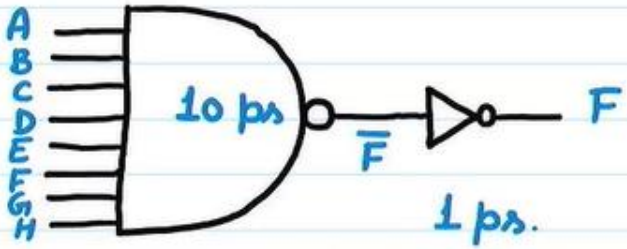
Overall delay is determined by time to discharge C_1, C_2 and C_L.

Overall delay is determined by time to discharge only C_L.

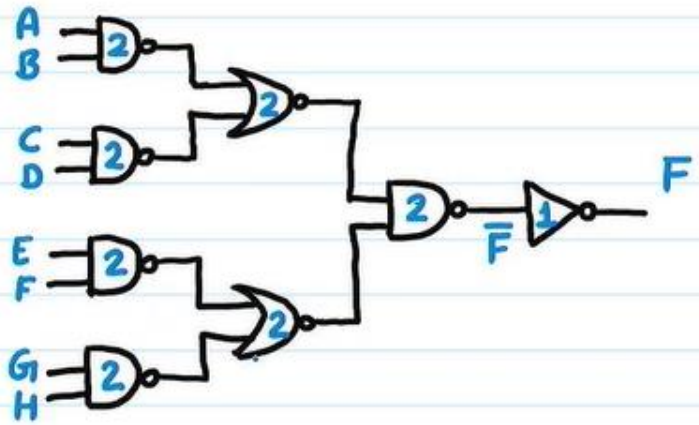
Design techniques 3 for CMOS gates :

- Find alternate logic structures to reduce overall delay.

$F = ABCDEFGH$



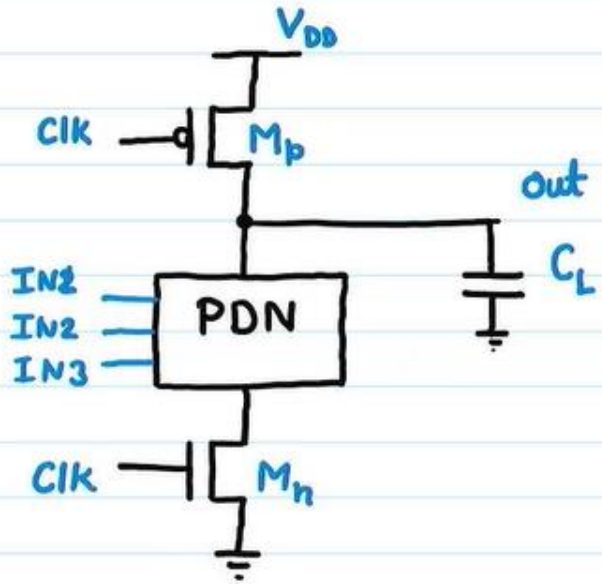
overall delay = 10 + 1 = 11 ps.

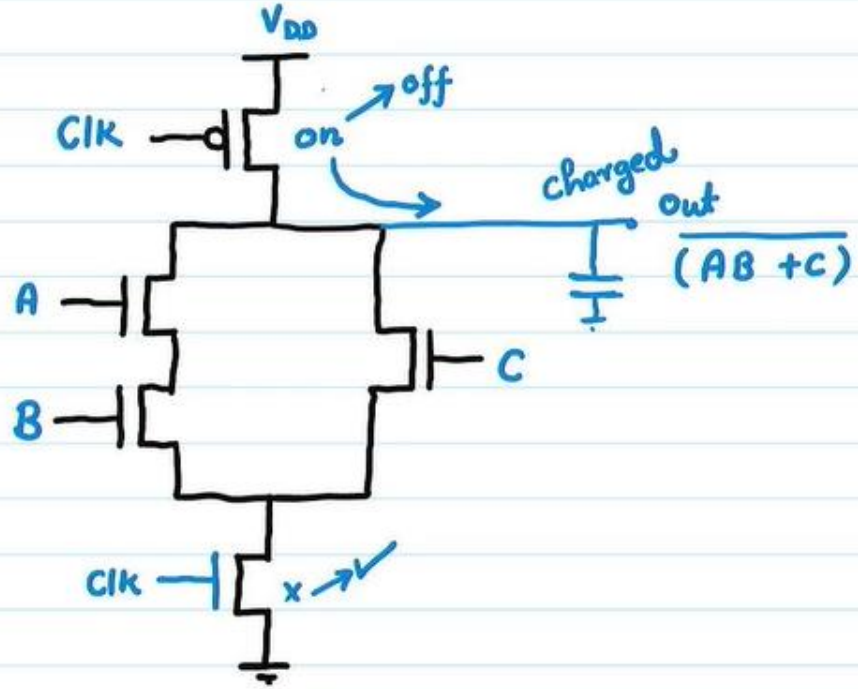


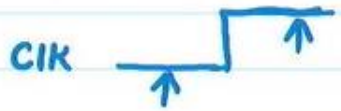
overall delay = 2 + 2 + 2 + 1

= 7 ps.

Dynamic logic Gates :







Two phase operation

Precharge (CIK = 0)

Evaluate (clk = 1)

Properties of Dyamic gates :

- Logic function is implemented by PDN only.
  - No. of transistors needed is $N+2$ ($2N$ in case of static gates)
- Full rail-to-rail output.
- Ratioless design - sizing of device does not affect the logic level.
- Faster switching speed
  1) reduced load capacitance due to lower input capacitance.
  2) reduced load capacitance due to smaller output loading.
  3) I_{sc}. all the current by PDN goes into discharging C_L..

Properties Continued ...

- Overall power dissipation usually higher than static CMOS.
  - Higher transition probabilities.
  - Extra load on clk.
- Needs a pre-charge / evaluate clock.