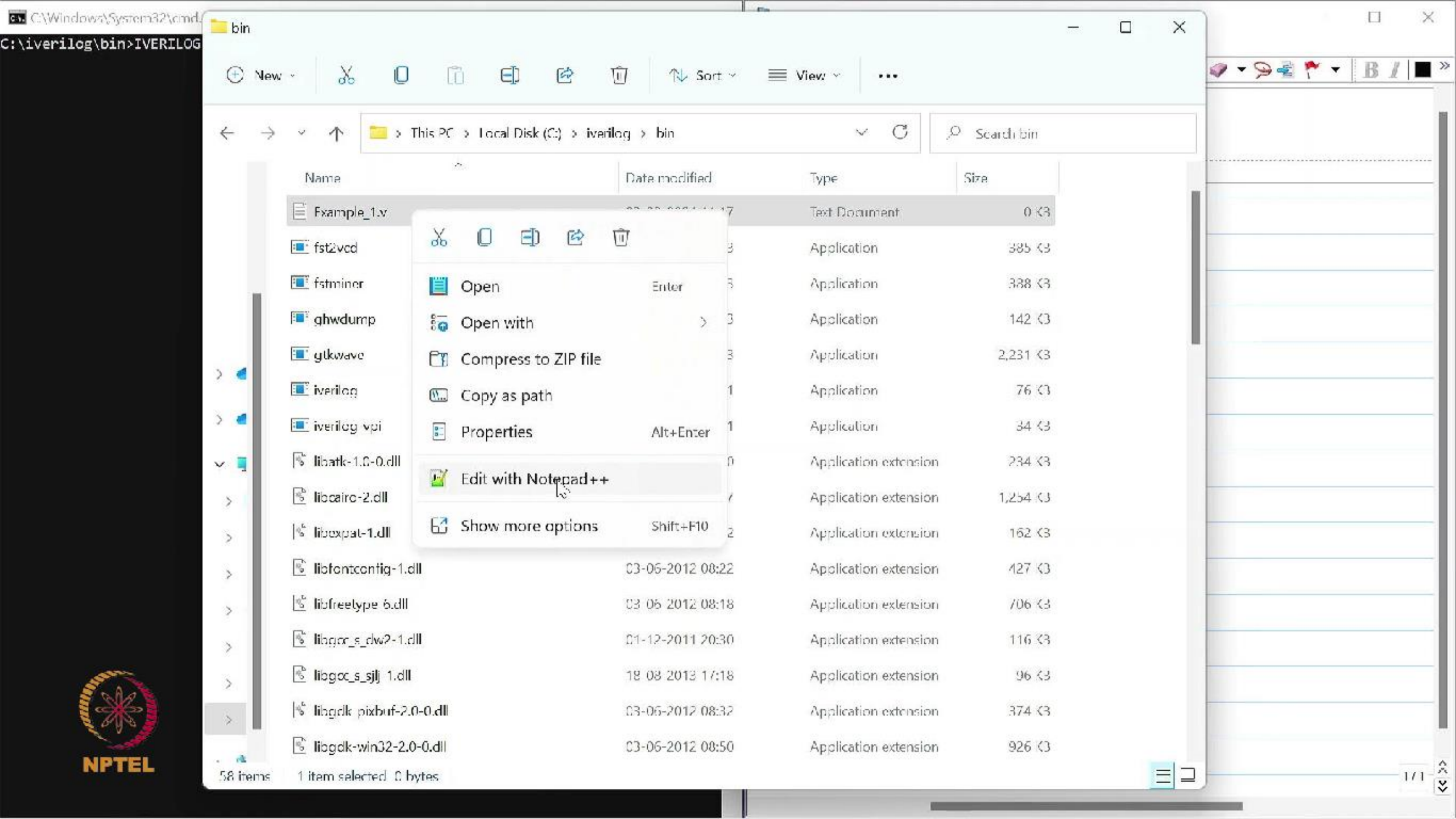

C:\Windows\System32\cmd.
C:\iverilog\bin>IVERILOG
bin
New
Sort
View
This PC › Local Disk (C:) › iverilog › bin
Search bin
Name
Date modified
Type
Size
Example_1.v
Text Document
0 KB
fst2vcd
Application
385 KB
fstminer
Application
338 KB
ghwdump
Application
142 KB
gtkwave
Application
2,231 KB
iverilog
Application
76 KB
iverilog-vpi
Application
34 KB
libatk-1.0-0.dll
Application extension
234 KB
libcairo-2.dll
Application extension
1,254 KB
libexpat-1.dll
Application extension
162 KB
libfontconfig-1.dll
03-06-2012 08:22
Application extension
427 KB
libfreetype-6.dll
03-06-2012 08:18
Application extension
706 KB
libgcc_s_dw2-1.dll
01-12-2011 20:30
Application extension
116 KB
libgcc_s_sjlj-1.dll
18-08-2013 17:18
Application extension
96 KB
libgdk_pixbuf-2.0-0.dll
03-06-2012 08:32
Application extension
374 KB
libgdk-win32-2.0-0.dll
03-06-2012 08:50
Application extension
926 KB
58 items
1 item selected 0 bytes
Open
Enter
Open with
Compress to ZIP file
Copy as path
Properties
Alt+Enter
Edit with Notepad++
Show more options
Shift+F10
NPTEL

C:\iverilog\bin\Example 1.v - Notepad++

File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

Example 1.v

```
1  module example_circuit1 (
2      A,
3      B,
4      C,
5      Z
6  );
7
8      input A, B, C;
9      output Z;
10     wire w1, w2, w3;
11     and G1 (w1, C, B);
12     or G3 (w2, A, w1);
13     and G2 (w3, A, B);
14     or G4 (Z, w2, w3);
15 endmodule
16
```

NPTEL

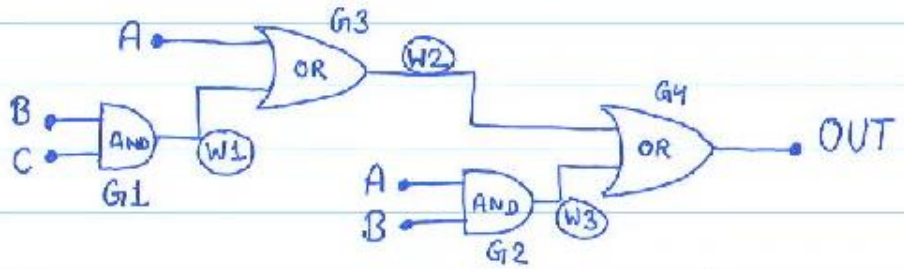
length : 195 lines : 16 Ln : 16 Col : 1 Pos : 196 Windows (CR LF) UTF-8 IN

Note1 - Windows Journal

File Edit View Insert Actions Tools Help

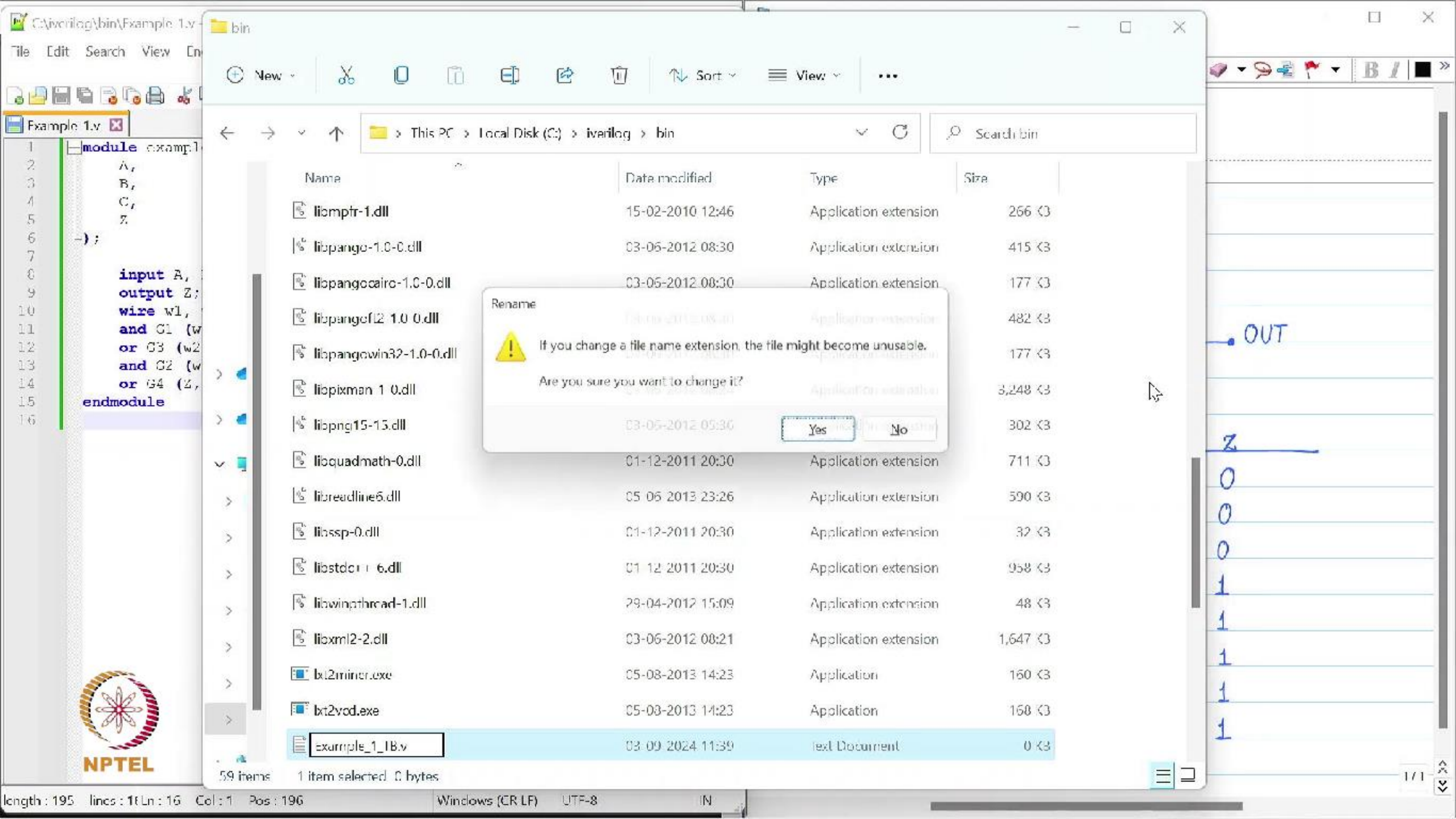
100%

Example :



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1 / 1


bin
New
Sort
View
This PC > Local Disk (C:) > iverilog > bin
Search bin
Name
Date modified
Type
Size
libmpfr-1.dll 15-02-2010 12:46 Application extension 266 KB
libpango-1.0-0.dll 03-06-2012 08:30 Application extension 415 KB
libpangocairo-1.0-0.dll 03-06-2012 08:30 Application extension 177 KB
libpangoft2-1.0-0.dll 482 KB
libpangowin32-1.0-0.dll 177 KB
libpixman-1-0.dll 3,248 KB
libpng15-15.dll 302 KB
libquadmath-0.dll 01-12-2011 20:30 Application extension 711 KB
libreadline6.dll 05-06-2013 23:26 Application extension 590 KB
libssp-0.dll 01-12-2011 20:30 Application extension 32 KB
libwinpthread-1.dll 29-04-2012 15:09 Application extension 48 KB
libxml2-2.dll 03-06-2012 08:21 Application extension 1,647 KB
lxt2miner.exe 05-08-2013 14:23 Application 160 KB
lxt2vcd.exe 05-08-2013 14:23 Application 168 KB
example_1_TB.v 03-09-2024 11:39 Text Document 0 KB
59 items
1 item selected 0 bytes
Rename
If you change a file name extension, the file might become unusable.
Are you sure you want to change it?
Yes
No
Example_1.v
module
input A,
output Z;
wire w1,
and G1 (w
or G3 (w2
and G2 (w
or G4 (Z,
endmodule
NPTEL
length : 195 lines : 16 Ln : 16 Col : 1 Pos : 196
Windows (CR LF) UTF-8 IN
OUT
Z
0
0
0
1
1
1
1
1
1/1

*C:\iverilog\bin\Example 1 TB.v - Notepad++

File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

Example 1.v | Example 1 TB.v

```
1  module example_circuit1_TB;
2      reg A, B, C;
3      wire Z;
4      example_circuit1 M1 (A, B, C, Z);
5      initial begin
6          A = 1'b0;
7          B = 1'b0;
8          C = 1'b0;
9
10         #20 A = 1'b0;
11         B = 1'b0;
12         C = 1'b1;
13
14         #20 A = 1'b0;
15         B
16
```

b0
b1
begin

NPTEL

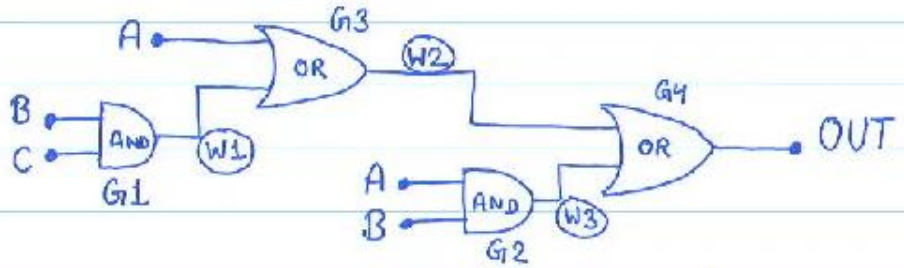
length : 220 lines : 16 Ln : 15 Col : 10 Pos : 217 Windows (CR LF) UTF-8 IN

Note1 - Windows Journal

File Edit View Insert Actions Tools Help

100%

Example :



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1 / 1

C:\iverilog\bin\Example 1 TB.v - Notepad++

File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

Example 1.v | Example 1 TB.v

```
        B = 1'b0;
        C = 1'b0;

        #20 A = 1'b1;
        B = 1'b0;
        C = 1'b1;

        #20 A = 1'b1;
        B = 1'b1;
        C = 1'b0;

        #20 A = 1'b1;
        B = 1'b1;
        C = 1'b1;

        #20 A = 1'b0;
        B = 1'b0;
        C = 1'b0;

    end
    initial begin
        $monitor($time, "A = %b, B = %b, C = %b, Z = %b", A, B, C, Z);
    end
    initial begin
        $dumpfile("example circuit1.vcd");
        $dumpvars(0, example circuit1 tb);
    end
endmodule
```

NPTEL

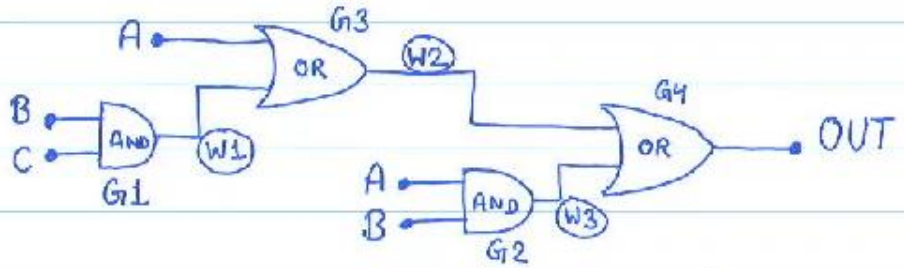
length : 921 lines : 51 Ln : 39 Col : 18 Pos : 659 Windows (CR LF) UTF-8 IN

Note1 - Windows Journal

File Edit View Insert Actions Tools Help

100%

Example :



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1 / 1

C:\Windows\System32\cmd.exe

```
C:\iverilog\bin>iverilog.exe -o example_circuit1 Example_1_TB.v Example_1.v
```

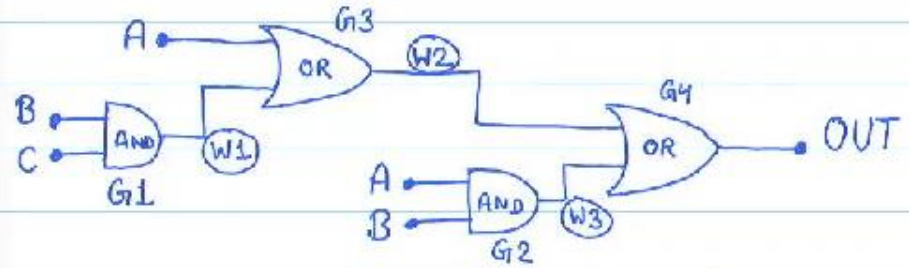
NPTEL

Note1 - Windows Journal

File Edit View Insert Actions Tools Help

100%

Example :



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1 / 1

Select C:\Windows\System32\cmd.exe

```
C:\iverilog\bin>iverilog.exe -o example_circuit1 Example_1_TB.v Example_1.v

C:\iverilog\bin>vvp.exe example_circuit1
VCD info: dumpfile example_circuit1.vcd opened for output.
                   0A = 0, B = 0, C = 0, Z = 0
                  20A = 0, B = 0, C = 1, Z = 0
                  40A = 0, B = 1, C = 0, Z = 0
                  60A = 0, B = 1, C = 1, Z = 1
                  80A = 1, B = 0, C = 0, Z = 1
                 100A = 1, B = 0, C = 1, Z = 1
                 120A = 1, B = 1, C = 0, Z = 1
                 140A = 1, B = 1, C = 1, Z = 1
                 160A = 0, B = 0, C = 0, Z = 0

C:\iverilog\bin>
```

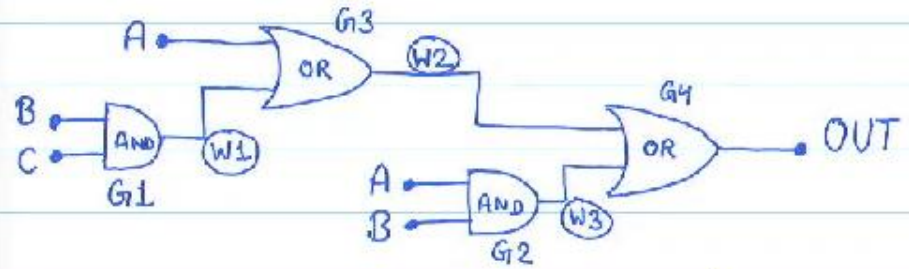
NPTEL

Note1 - Windows Journal

File Edit View Insert Actions Tools Help

100%

Example :



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1 / 1

C:\Windows\System32\cmd.exe

```
C:\iverilog\bin>iverilog.exe -o example_circuit1 Example_1_TB.v Example_1.v

C:\iverilog\bin>vvp.exe example_circuit1
VCD info: dumpfile example_circuit1.vcd opened for output.
                   0A = 0, B = 0, C = 0, Z = 0
                  20A = 0, B = 0, C = 1, Z = 0
                  40A = 0, B = 1, C = 0, Z = 0
                  60A = 0, B = 1, C = 1, Z = 1
                  80A = 1, B = 0, C = 0, Z = 1
                 100A = 1, B = 0, C = 1, Z = 1
                 120A = 1, B = 1, C = 0, Z = 1
                 140A = 1, B = 1, C = 1, Z = 1
                 160A = 0, B = 0, C = 0, Z = 0

C:\iverilog\bin>gtkwave.exe example_circuit1.vcd
```

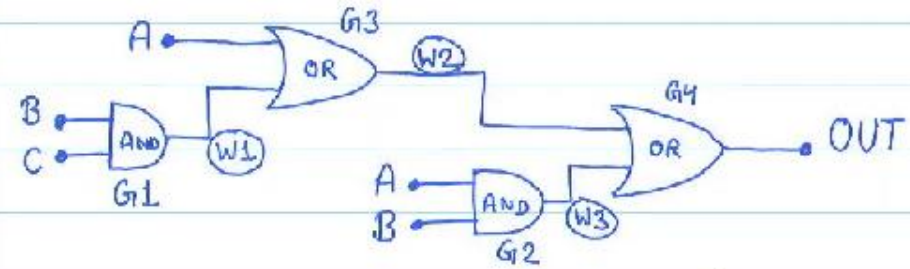
NPTEL

Note1 - Windows Journal

File Edit View Insert Actions Tools Help

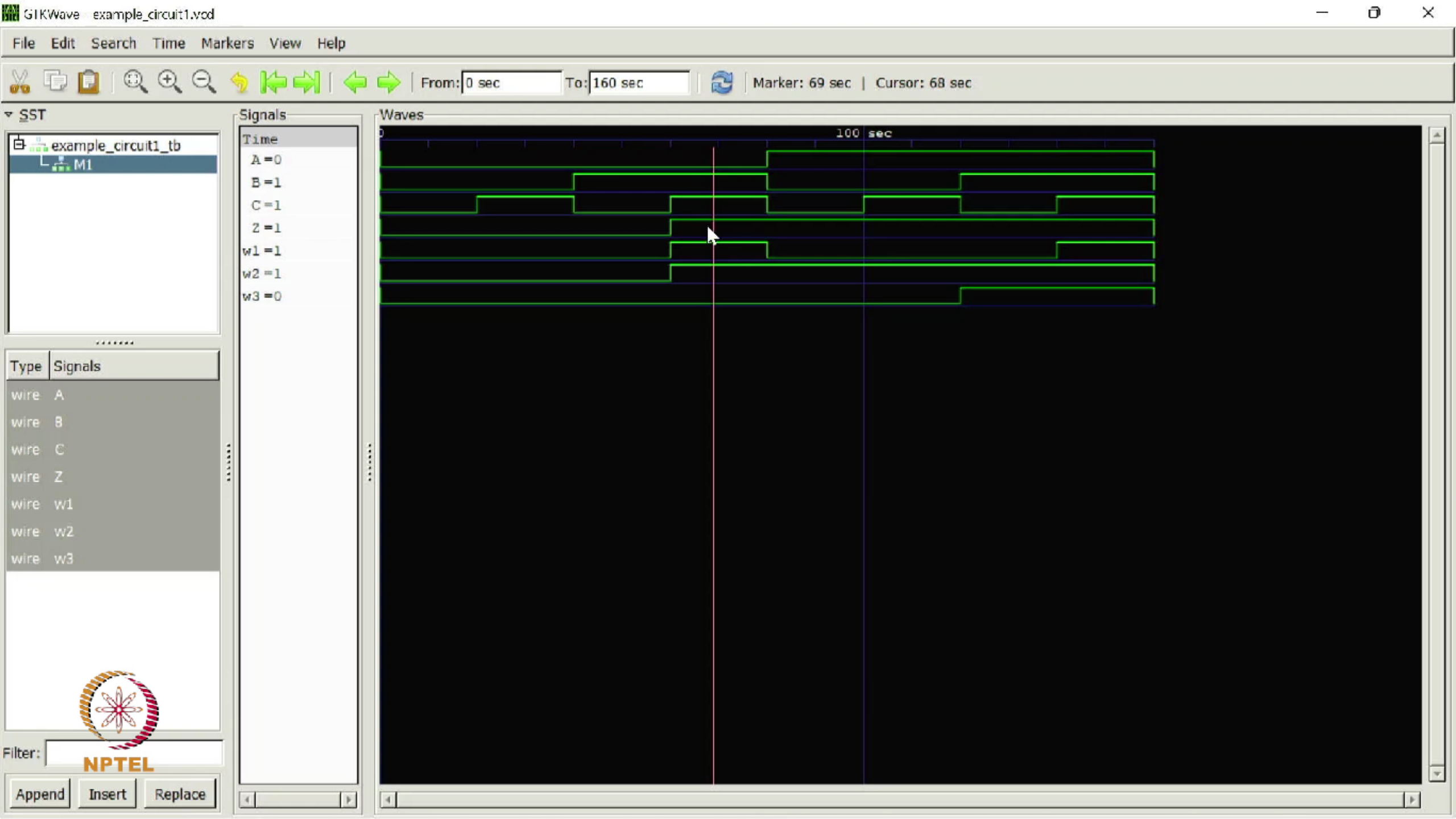
100%

Example :



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1 / 1


GTKWave - example_circuit1.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 160 sec
Marker: 69 sec | Cursor: 68 sec
SST
example_circuit1_tb
M1
Signals
Time
A =0
B =1
C =1
Z =1
w1 =1
w2 =1
w3 =0
Waves
100 sec
Type Signals
wire A
wire B
wire C
wire Z
wire w1
wire w2
wire w3
Filter:
Append
Insert
Replace
NPTEL