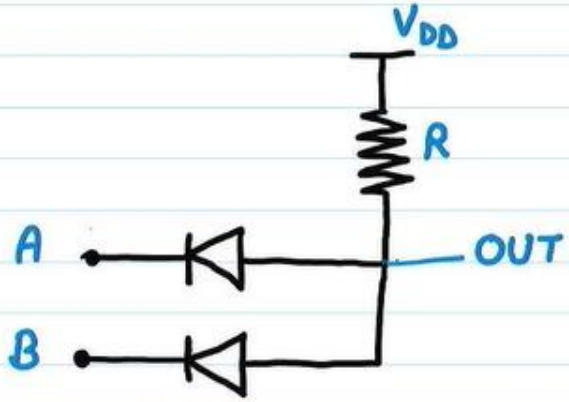
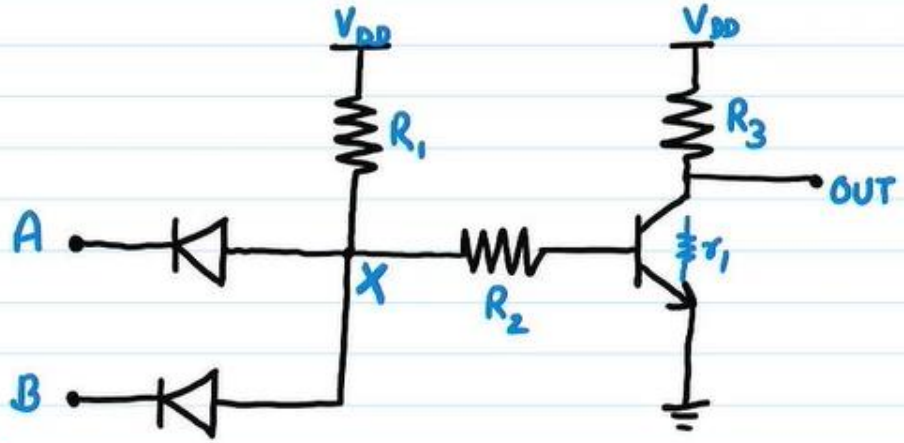
TTL : Transistor - Transistor Logic uses bipolar transistors and diodes.



A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

AND gate



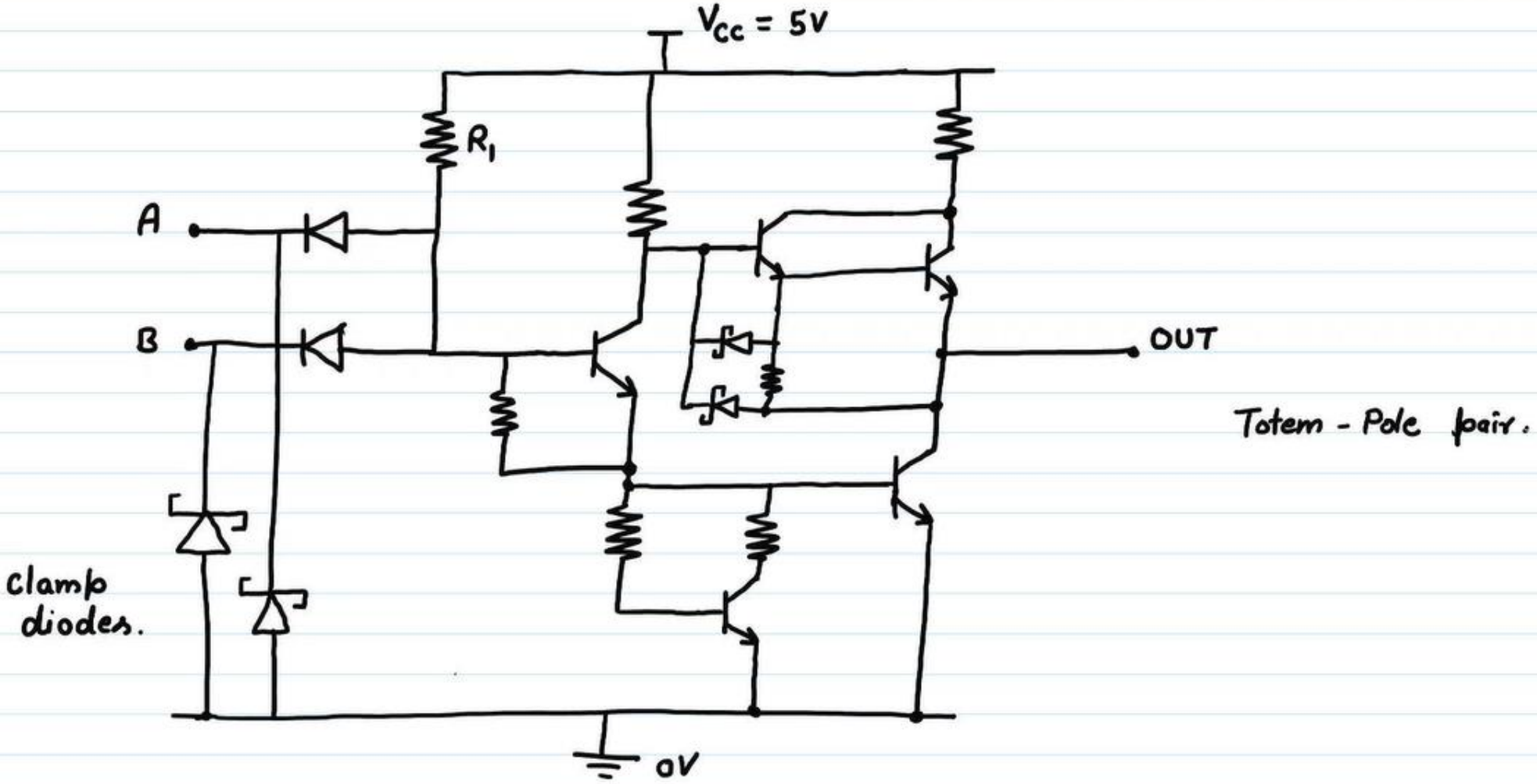
A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate

$OUT = \left(\frac{r_1}{r_1 + r_3}\right) V_{DD}$

$\approx 0V$

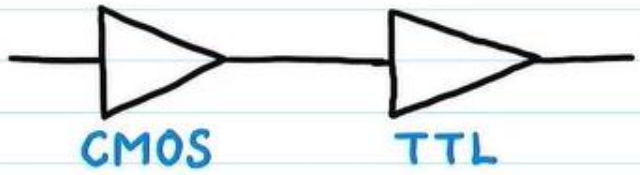
TTL : Practical Realization

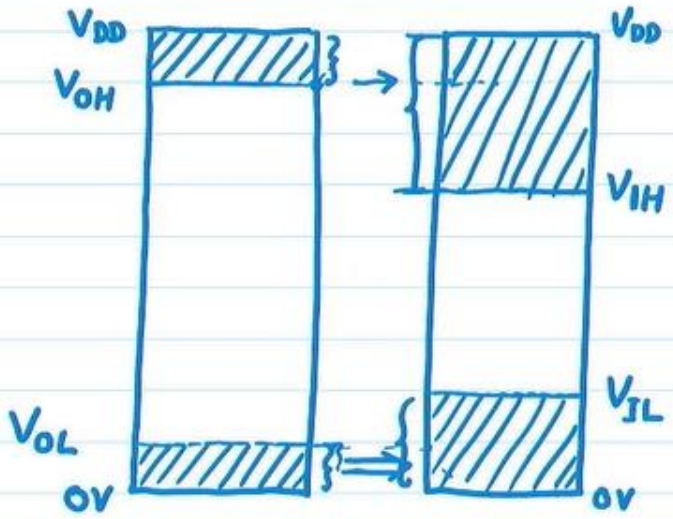


TTL vs CMOS

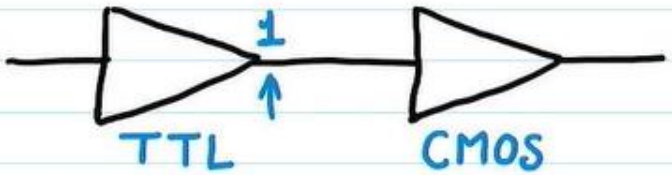
	TTL	CMOS
Noise Margins	0·3 (high) , 0·5 (low)	0·3 V_{cc}
Input Source Currents	High in both cases.	Typically < 1μA in both cases.
Power Consumption	Relatively High	Very Low
Output Drive Current	Asymmetric High 0·4 – 2 mA Low 8 – 20 mA	Symmetric typ. 4 mA.
Power Supply	5V ± 10 %	3V ⟶ 18V
Interconnections.	Can not drive CMOS directly.	Can directly drive TTL.

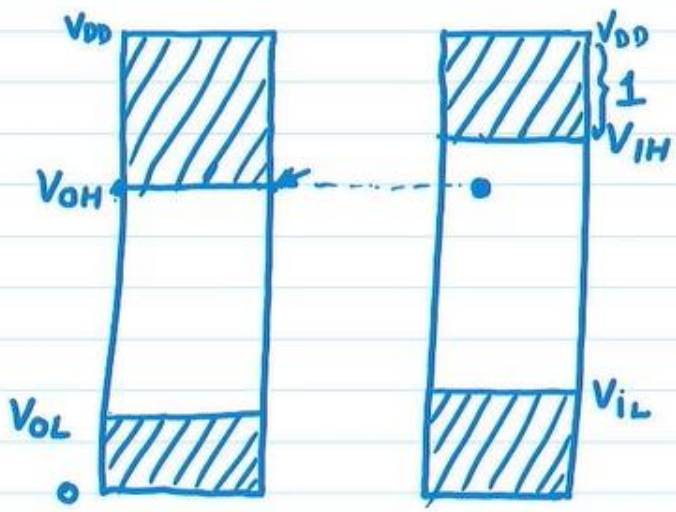
CMOS / TTL Interfacing.





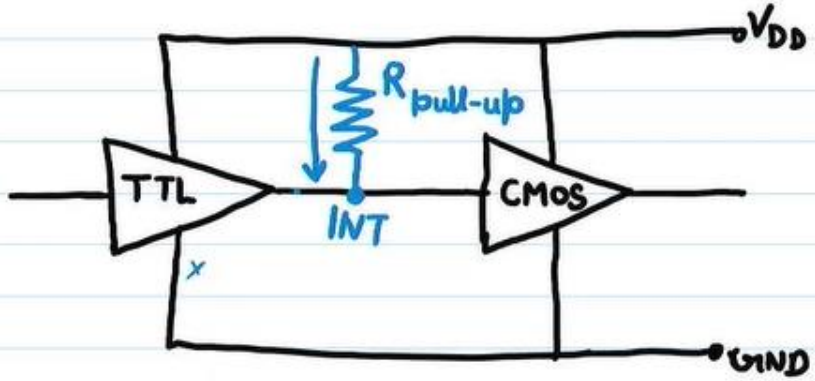
CMOS can directly drive TTL.





TTL can not directly drive CMOS.

Pull - UP resistor :



$R_{pull-up}$: Pull-up resistance.

if $R_{pull-up}$ is very low (< 10 K) : PDN of TTL increases.

if $R_{pull-up}$ is very high (>> 10 K) : Speed decreases.