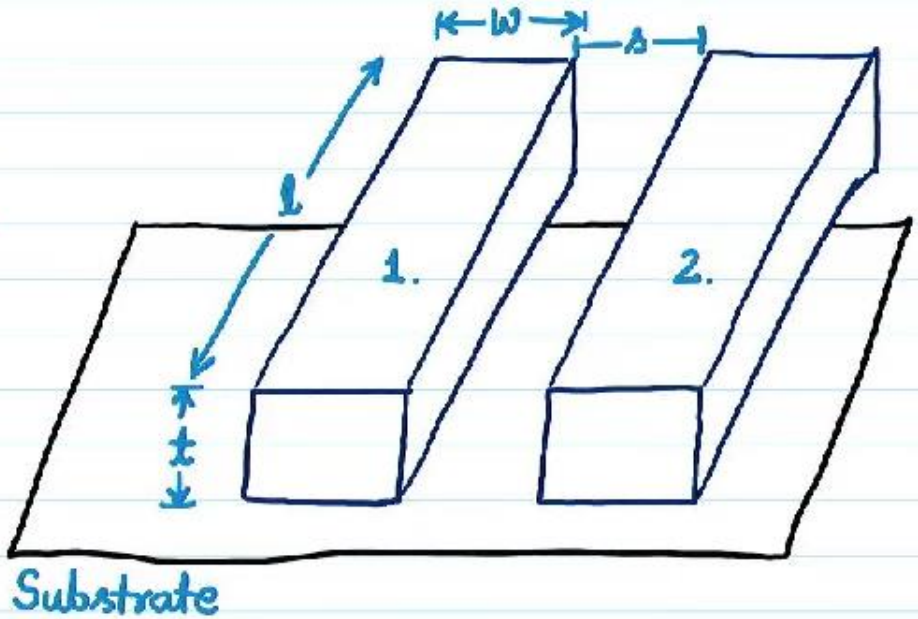
Wire Geometry :

Pitch = $w + s$

Aspect Ratio (AR) = $\frac{t}{w}$

→ in older processes AR << 1,

→ in modern processes AR ≈ 2.



Wire Resistance :

→ ρ : resistivity (Ω * m)

Resistance $R = \frac{\rho L}{t \cdot w}$

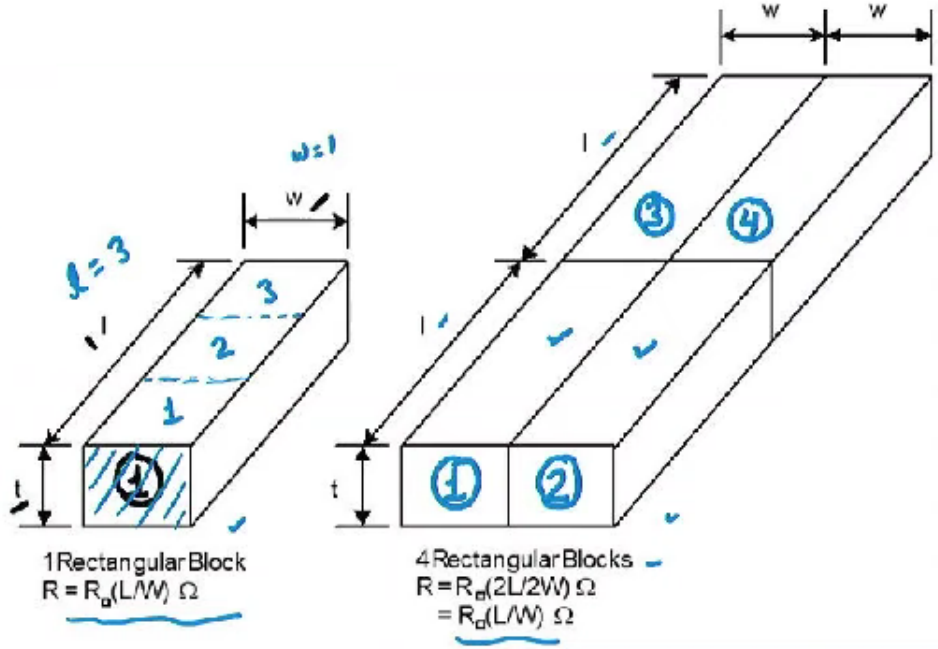
$R = R_{\square} \cdot \frac{L}{w}$

→ $R_{\square}$ = Sheet resistance ($\Omega / \square$)

- $\square$ is a dimentionless unit.

→ Count number of squares

$R = R_{\square} * (\#\ of\ squares)$



NPTEL

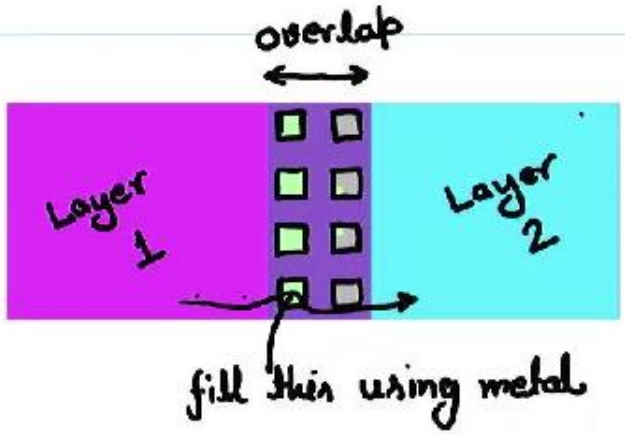
Choice of Metals :

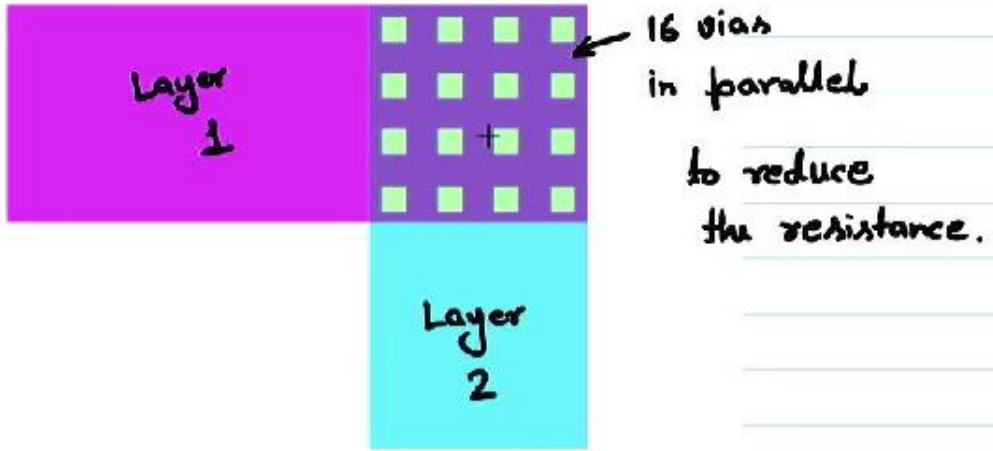
- upto 180 nm technology, most wires were aluminum.
- Modern processes often use copper.
  - Cu atoms diffuse into silicon and damage the FETs.
  - Must be surrounded by a diffusion barrier.

Metal	Bulk Resistivity ($\mu\Omega$-cm)
Silver	1.6
Copper	1.7
Gold	2.2
Aluminum	2.8
Tungsten	5.3
Molybdenum	5.3

Contact Resistance :

- Contacts and vias also have significant resistance (2 - 20 Ω)
- To reduce resistance, use many contacts.
- Many small contacts for current crowding around the periphery.



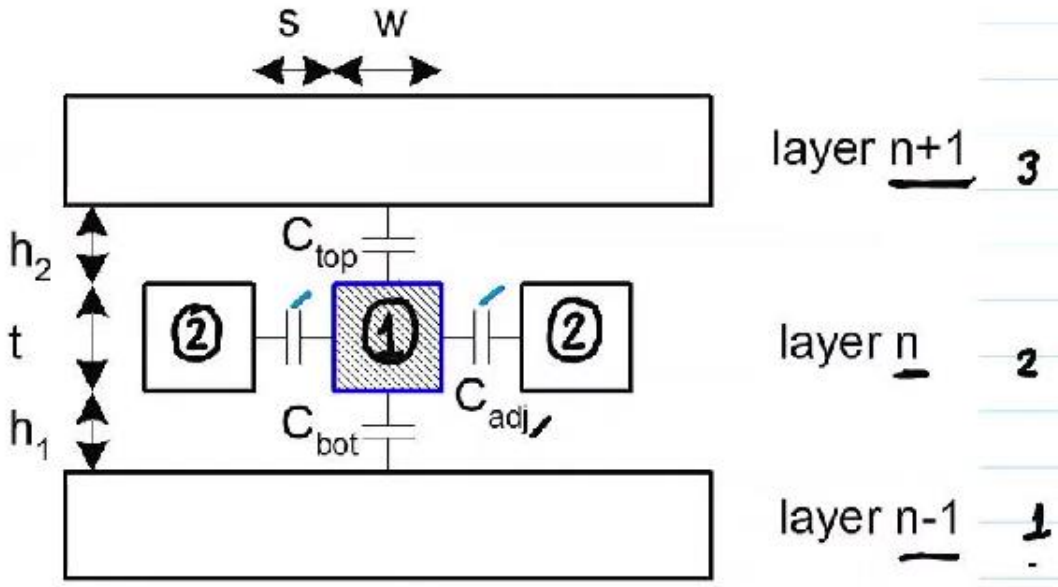


Wire Capacitance :

- Wire has capacitance per unit length.
  - To neighbors.
  - To layers above and below.

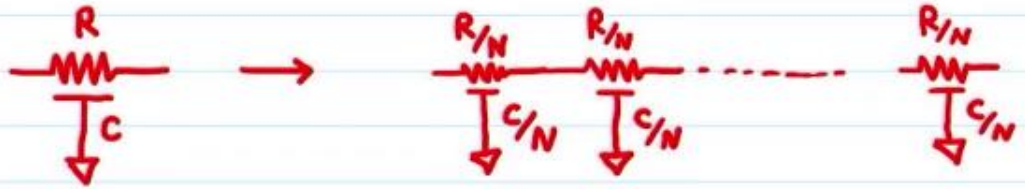
- Total Capacitance :

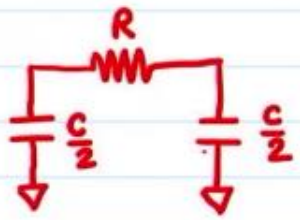
$$C_{Total} = C_{Top} + C_{bot} + 2C_{adj}$$



Lumped Element Models :

- Wires are a distributed system
  - Approximate with lumped element models.



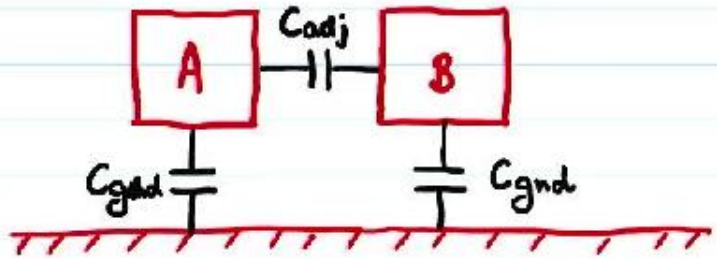


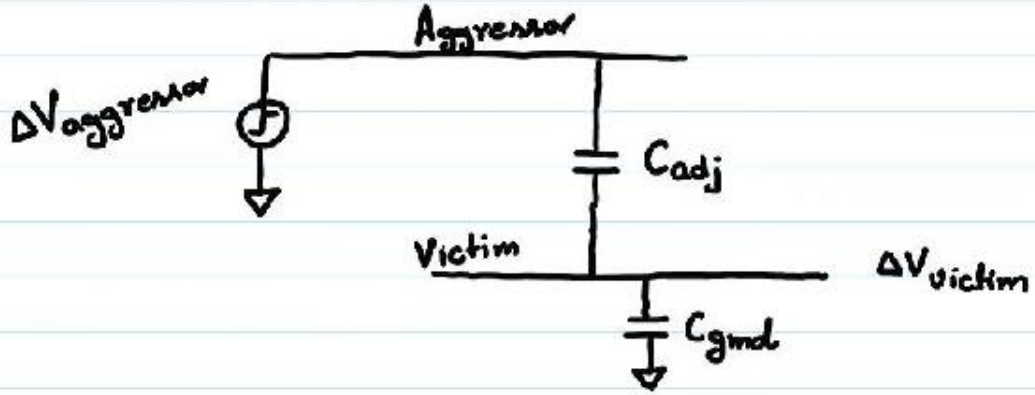
π - model.

- 3 segment π - model is accurate to 3 % in simulation.
-

Cross talk Noise :

- Crosstalk causes noise on nonswitching wires.
- if victim is floating :
  - model as capacitive voltage divider.





$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd} + C_{adj}} * \Delta V_{aggressor}$$