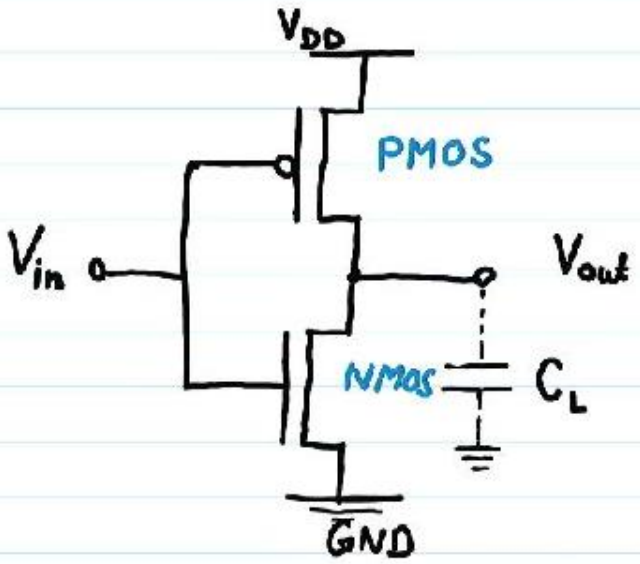
The CMOS Inverter :

- PMOS as well as NMOS.



- Nucleus of ICs
- Same analysis can be extended to study complex gates (NAND , NOR etc.)

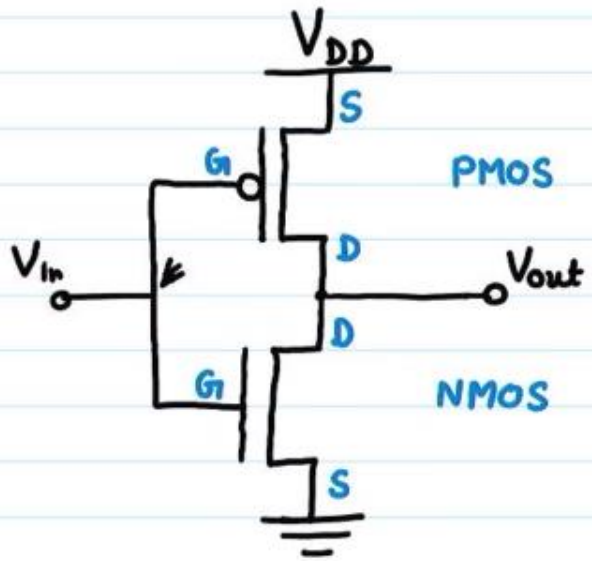
1 - Cost (Area and Complexity)

2 - Robustness (Static behavior)

3 - Performance (Dynamic / Transient response)

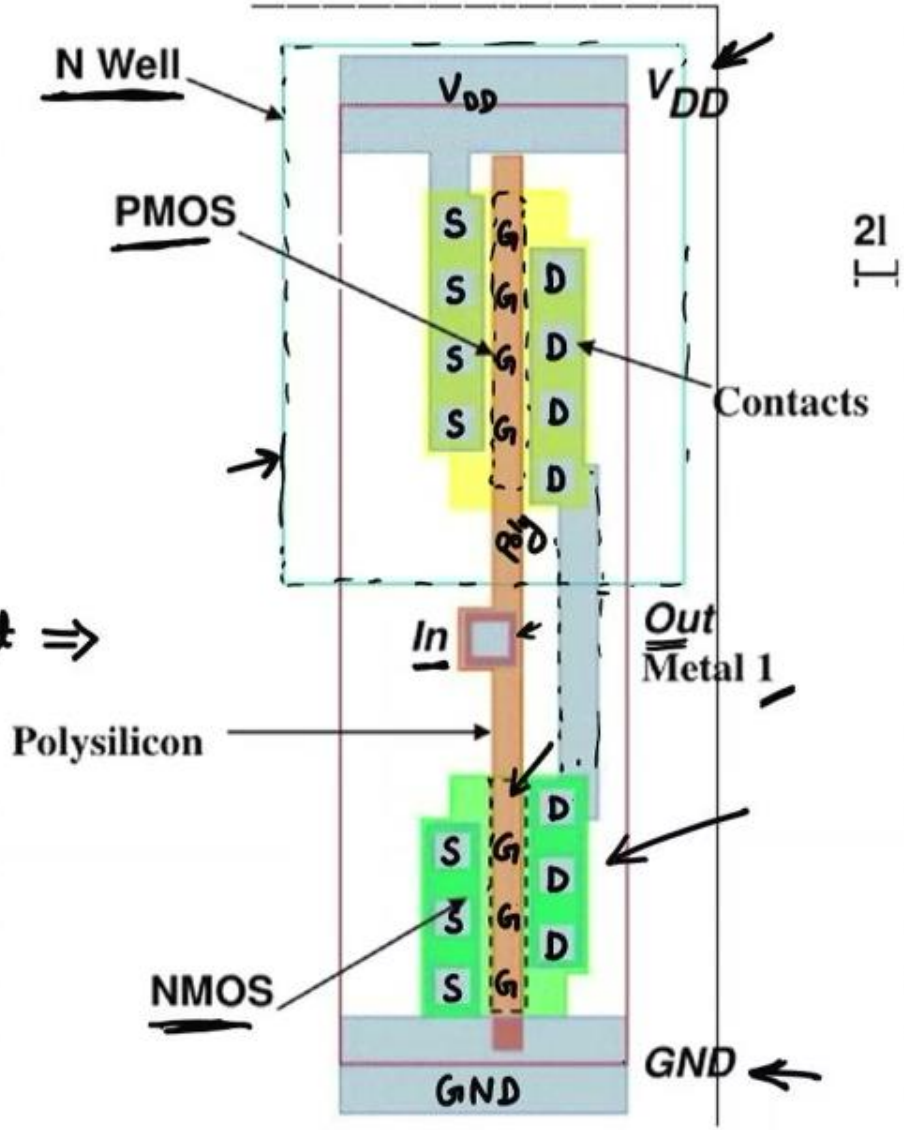
4 - Energy Efficiency (Power consumption)

CMOS Inverter (Schematic vs Layout) :



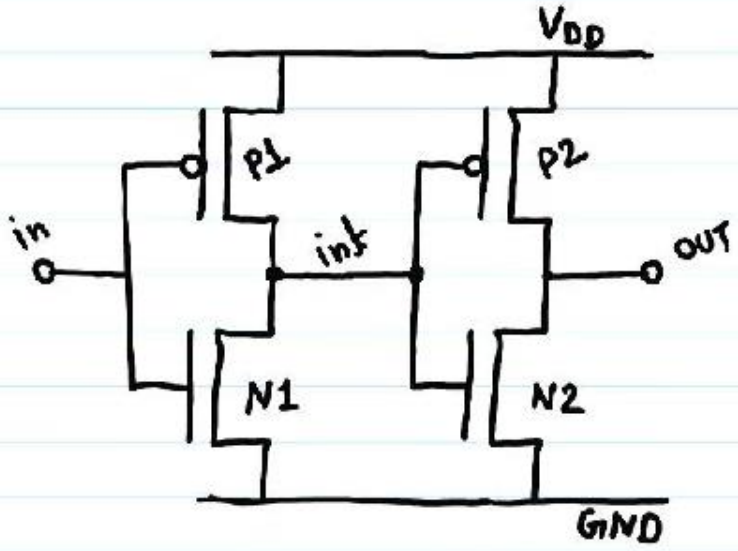
Schematic

Layout ⇒

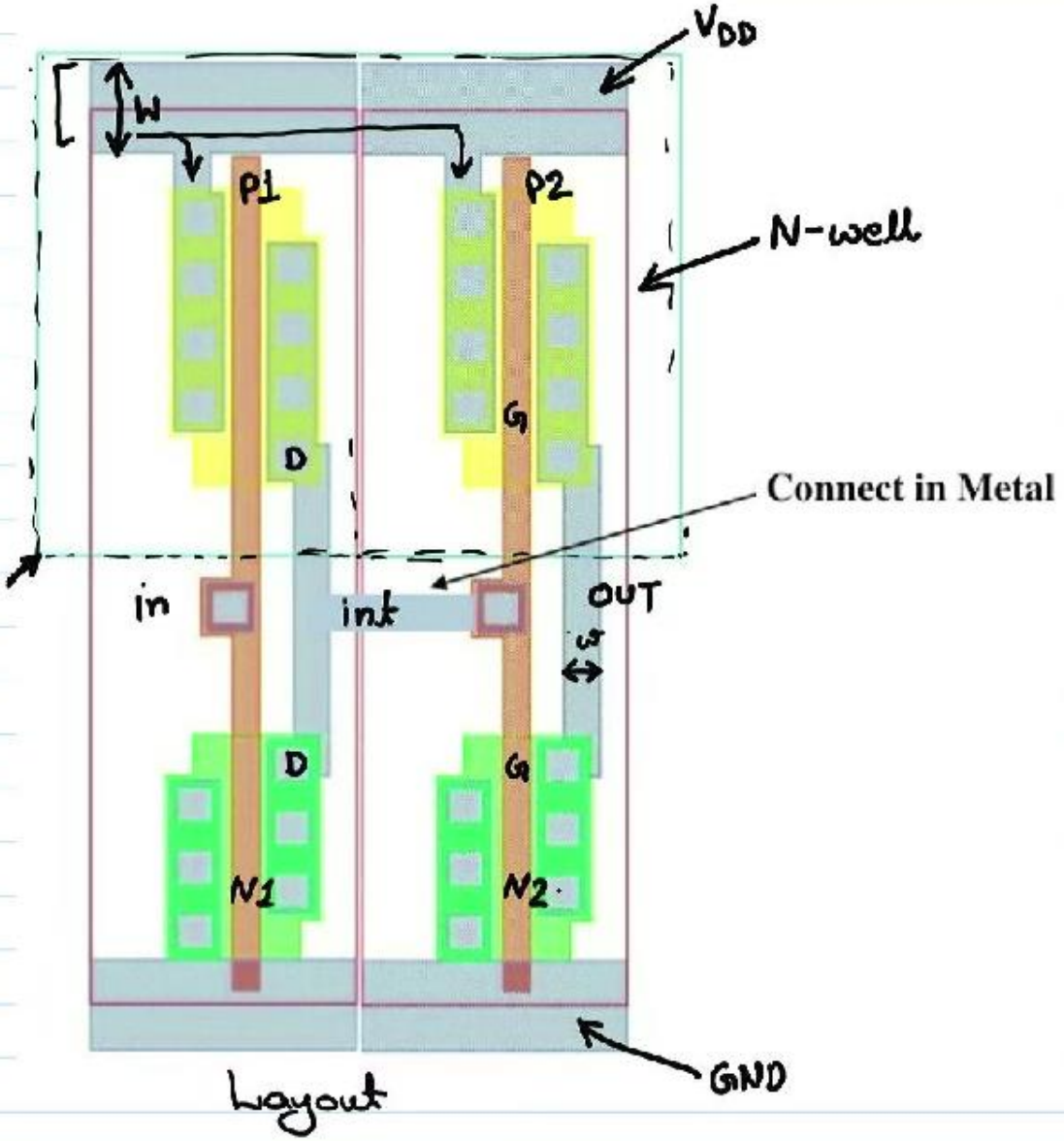


NPTEL

Two Inverters (Schematic vs Layout) :

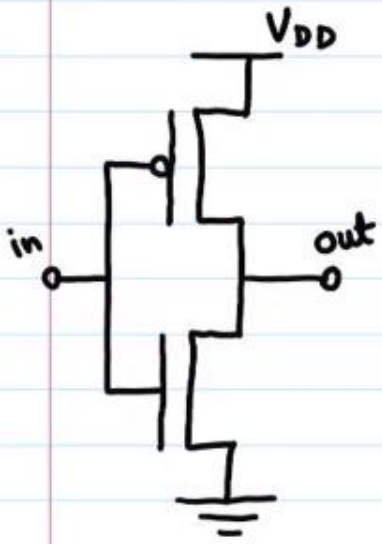


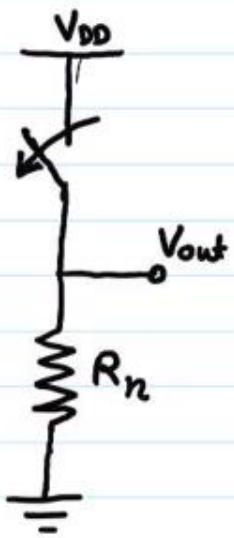
Schematic



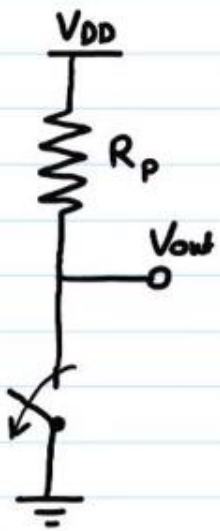
Layout

CMOS Inverter DC Analysis :





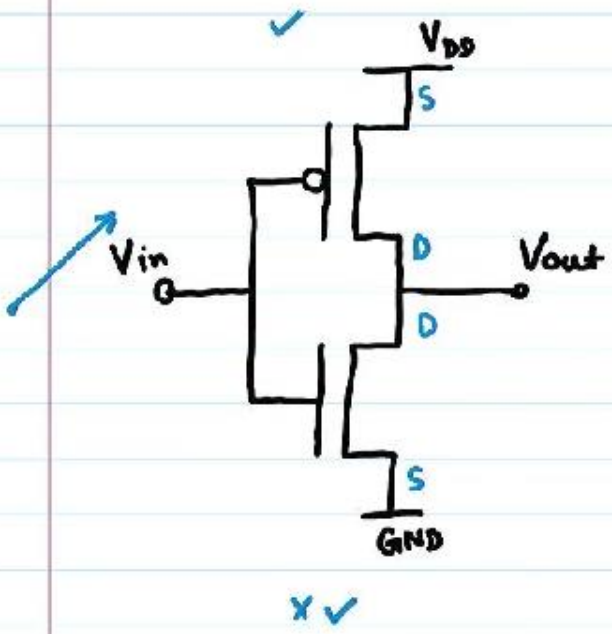
$V_{in} = V_{DD}$

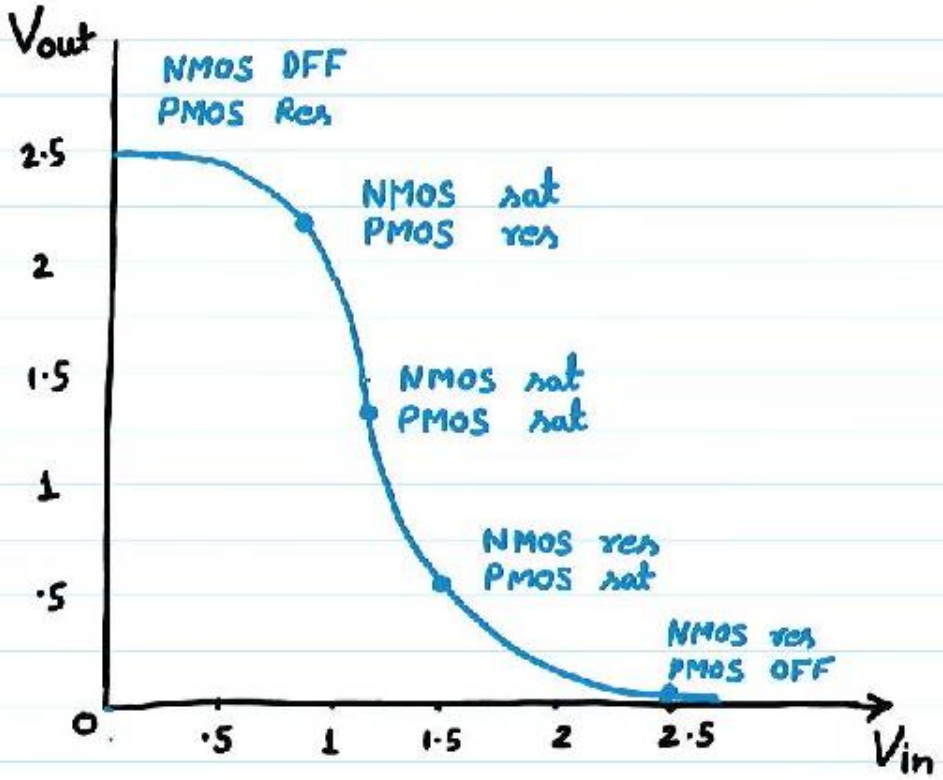


$V_{in} = 0$

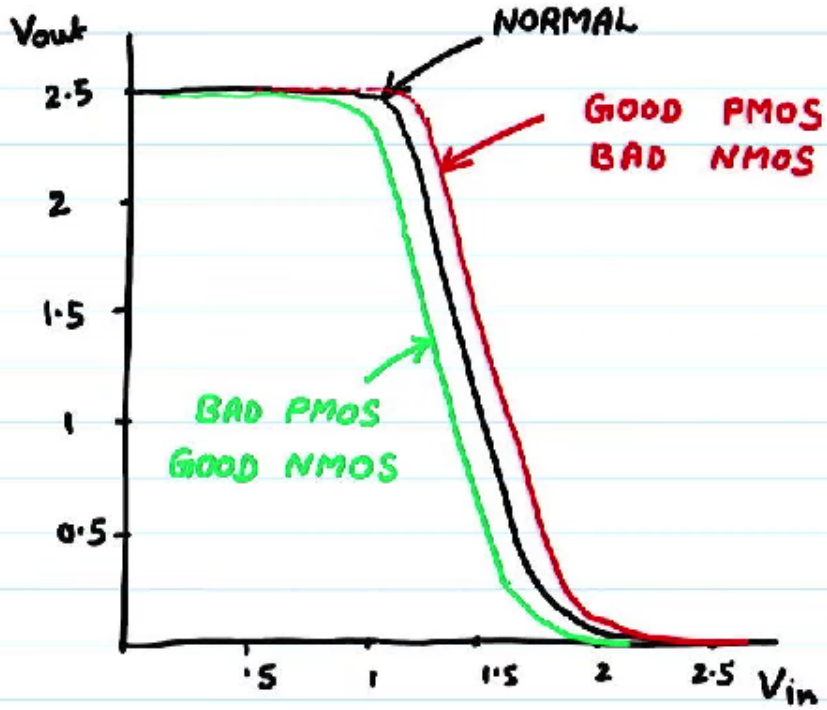
- Low and High levels equal to V_{DD} and GND.
- Ratioless (logic levels do not depend on device sizes)
- V_{out} is always connected to either V_{DD} or GND.
- I/P impedance is very high
- No static power dissipation.

Voltage – Transfer Characteristics :





Impact of Process Variation :



The good device generally has

- Smaller T_{ox}
- Smaller L_g
- Higher W
- Smaller V_{TH}.