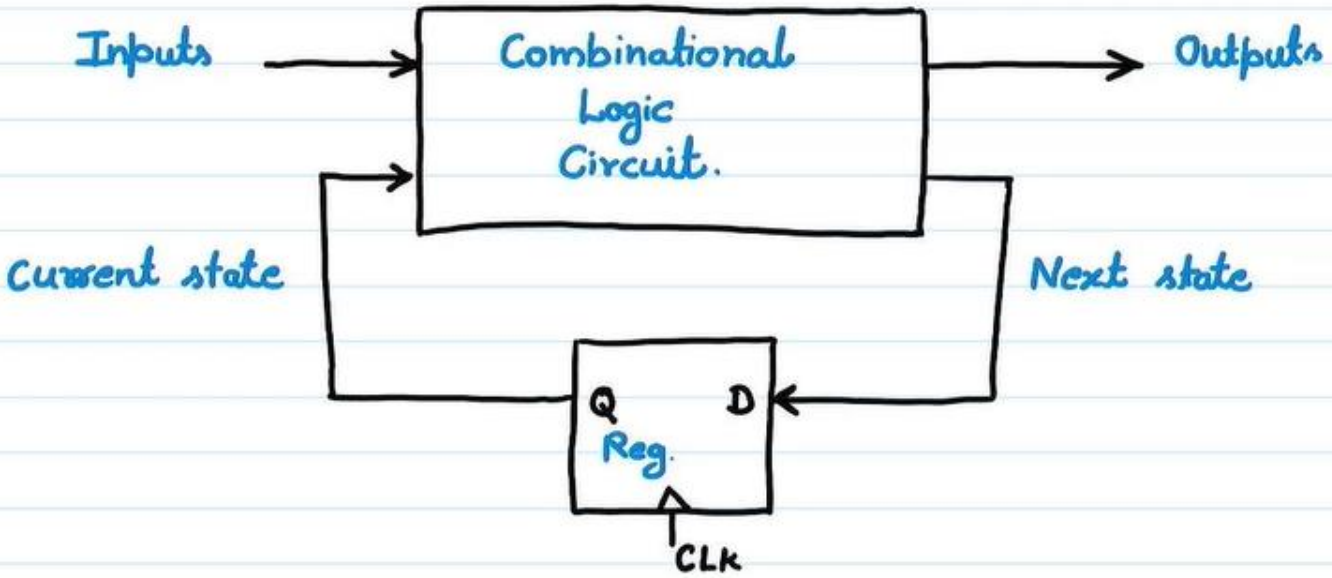
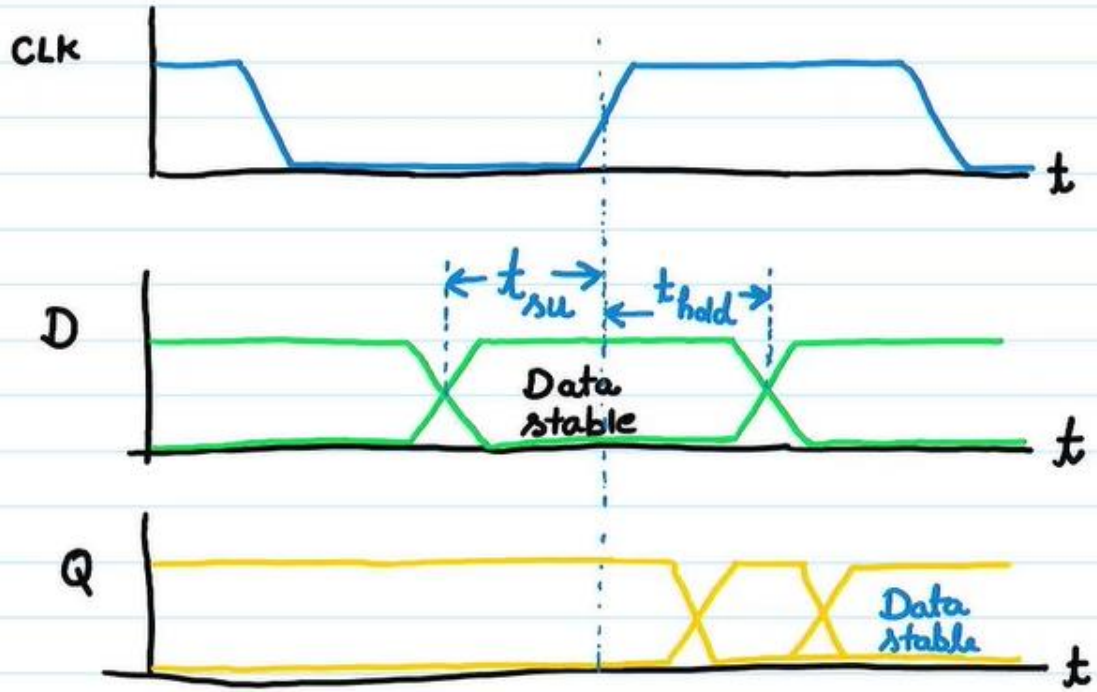
Sequential Logic :

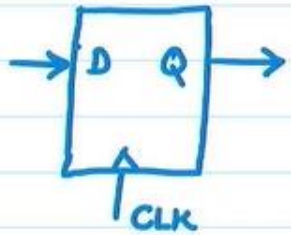


→ A Latch : is level sensitive .

→ A Register : is edge triggered .

Timing Definitions : Timing is synchronized through clock signal.





Setup-Time : The minimum amount of time before the clock edge that the data input must be stable.

Hold-Time : The minimum amount of time after the clock edge that the data input must remain stable.

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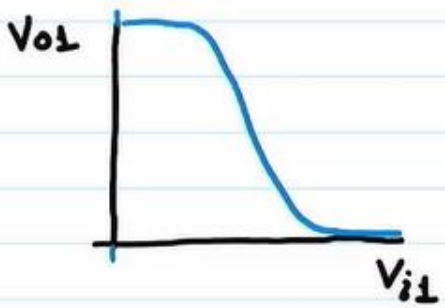
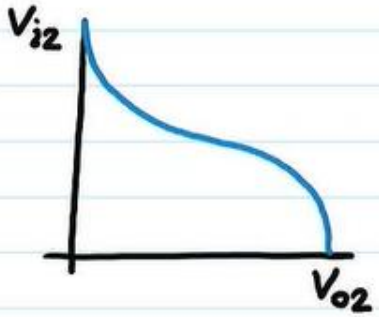
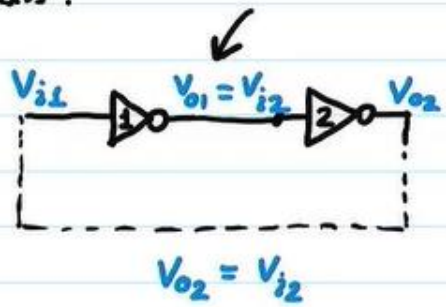
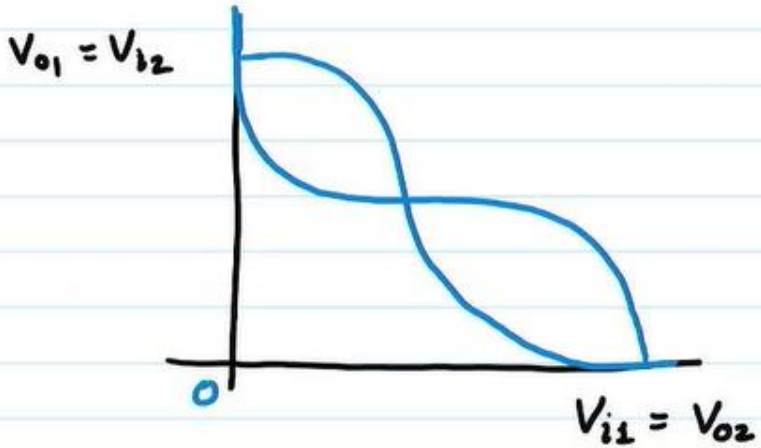
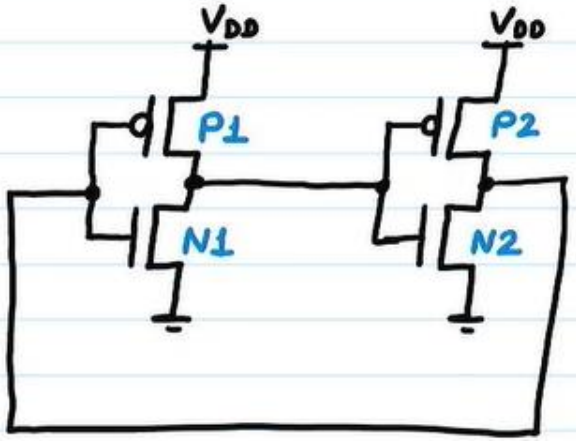
Positive Feedback : Bi - Stability in CMOS circuits.











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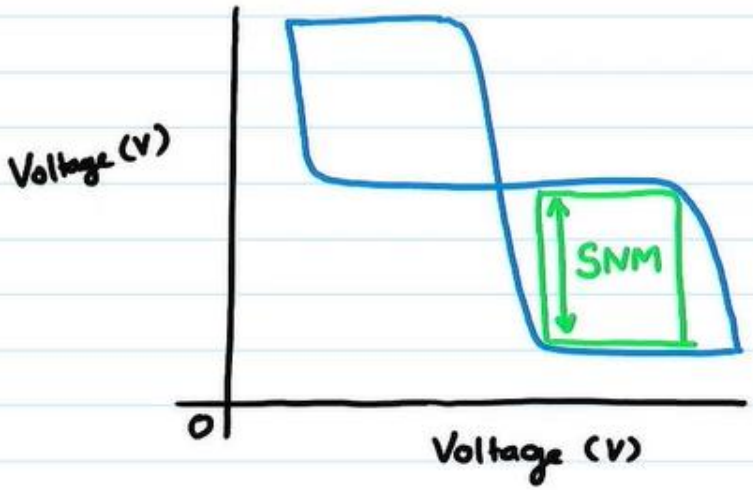
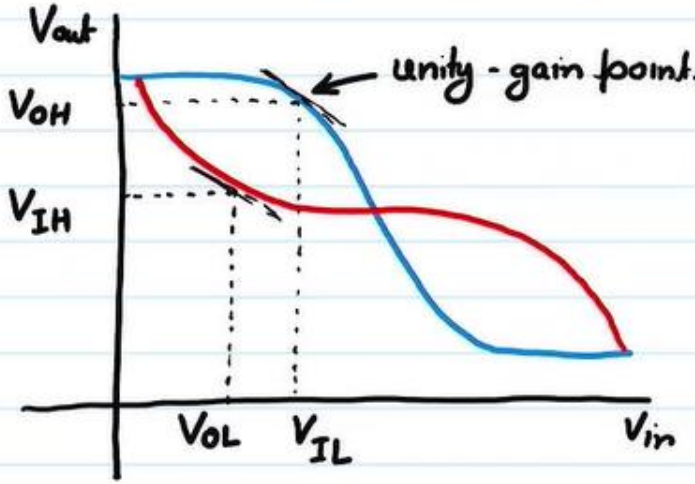
Meta-stability



SNM : Static Noise Margin is a major parameter in the design of a Static Random Access Memory (SRAM) cell.

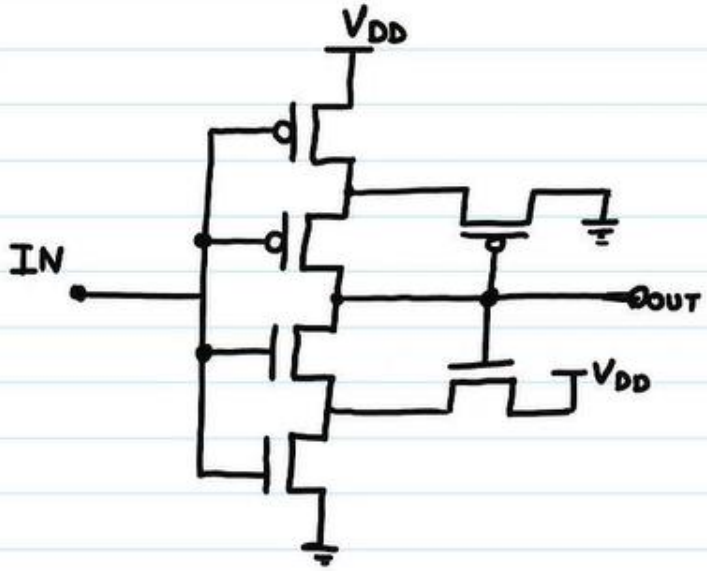
it helps a designer determine the ratio of pull-up, pull-down and passgate transistors.

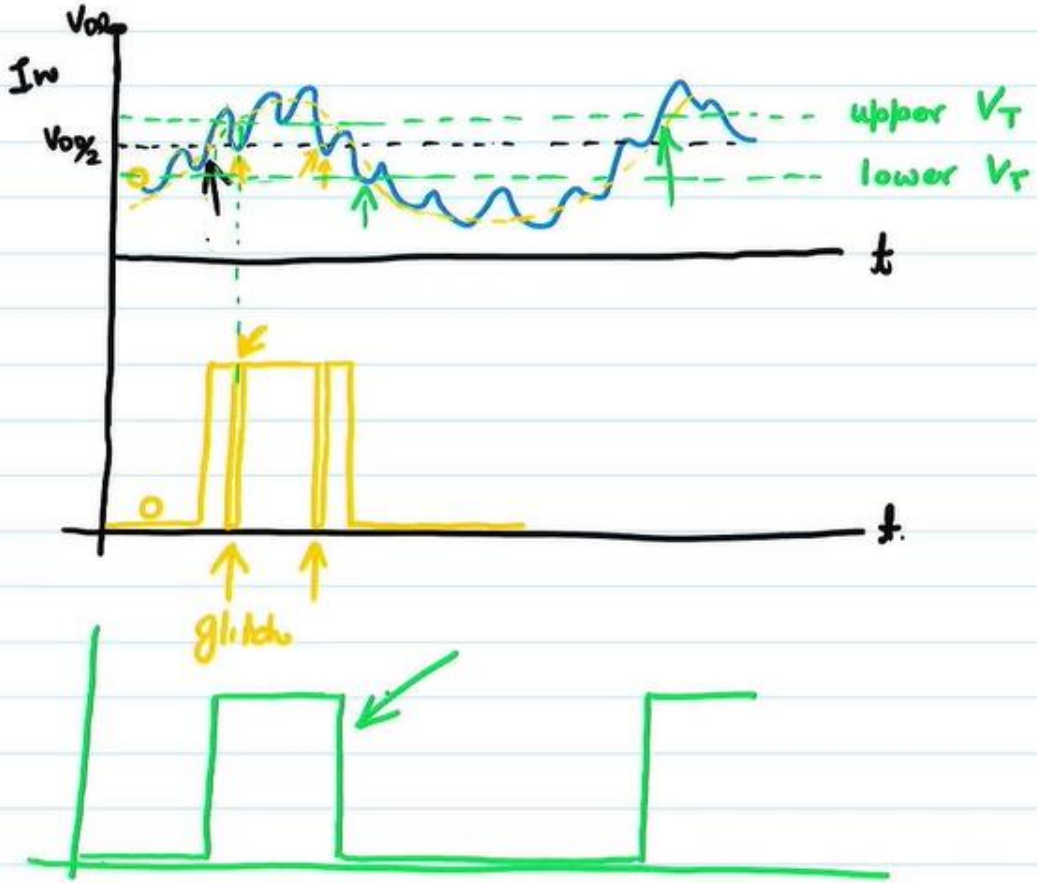


V_{IH} , V_{IL}

V_{OH} , V_{OL}

CMOS Schmitt Trigger :





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