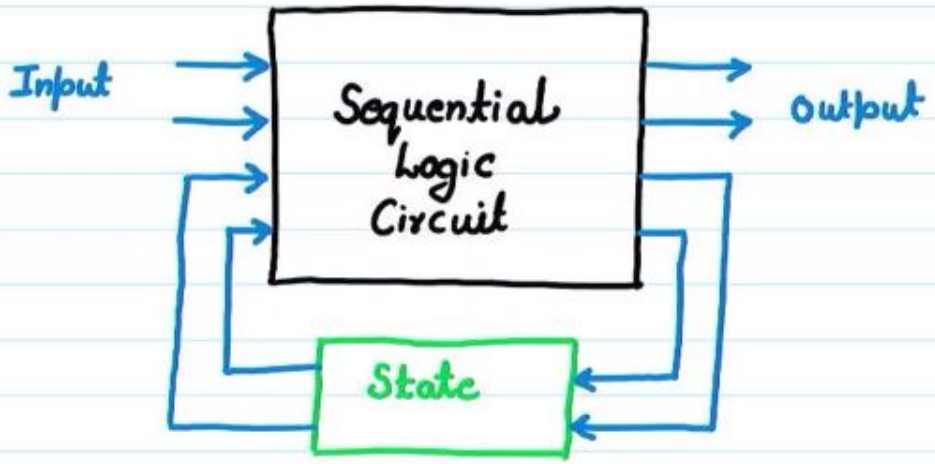
# Combinational and Sequential Logic :


Combinational

Output = f ( Input )




Sequential

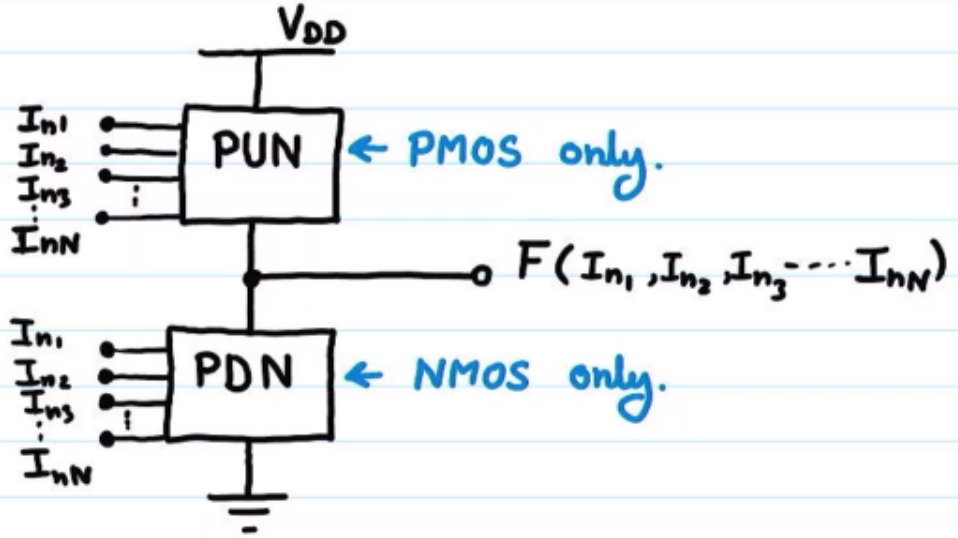
Output = f ( Input , Previous state)

# Static vs Dynamic Logic Gates :

- In static logic gates
  - At every point in time ( except during the switching transients ) each gate output is connected to either $V_{DD}$ or $V_{SS}$ through a low-impedance path.
  - The outputs of the gates assumes at all times the value of boolean function ( i.e. High or Low ).

- In dynamic logic gates
  - This relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes.

# Static Complementary CMOS Logic :




- PUN is dual of PDN.

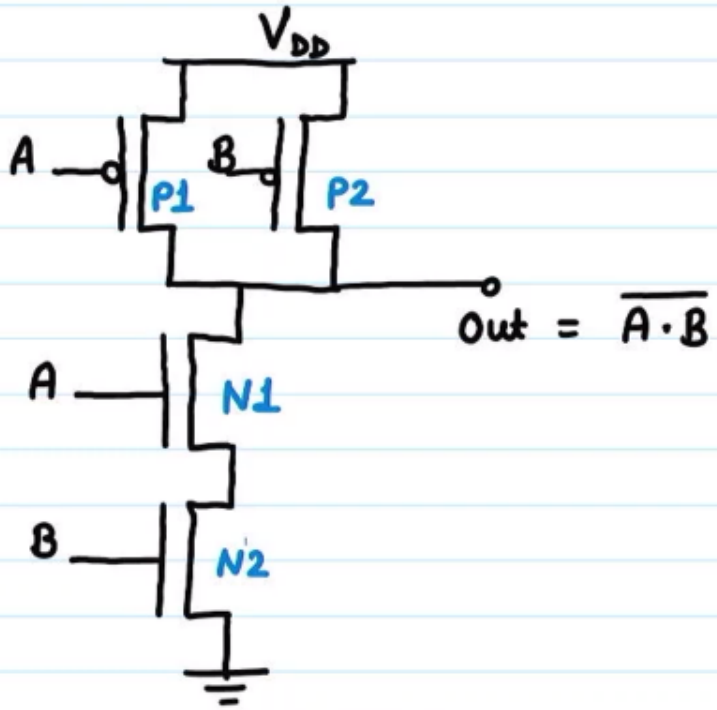
Can be analyze using DeMorgan's Theorem.

$$\overline{A + B} = \bar{A} \cdot \bar{B}$$

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

PUN and PDN are dual logic network.

Example : NAND gate.




| A | B | Out |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Truth-table of 2-INPUT NAND gate.

PDN : $G = A \cdot B$

PUN : $F = \bar{A} + \bar{B} = \overline{A \cdot B}$

$\overline{G(A, B)} = F(\bar{A}, \bar{B})$

## Static CMOS Properties :

- Full rail-to-rail swing ; High Noise Margins.
- Logic levels does not depend upon the relative device sizes ; ratio less.
- Always a path to $V_{DD}$ or Gnd in steady-state ; low output impedance.
- Extremely high input resistance ; nearly zero steady-state input current.
- No direct path between power and ground in steady state ; no static power dissipation.
- Propagation delay is function of load capacitance and resistance of transistors.