IS903

USB3.0 Flash Disk Controller

Specification



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1. Description

IS903 is the USB-3.0 interface Nand Flash Controller. With flexible firmware code supporting, IS903 can support various flash technology including 4k / 8k / 16k page SLC / MLC by different 2xnm / 2ynm / 1xnm process for major flash vendors.

2. Features

2.1 Flash support

2xnm, 2ynm, 1xnm process Flash from various vendors
One Channel / two channel data bus by small footprint package
Up to 4 CEs per channel to support max. 8 Flash CEs
SLC / MLC types Nand Flash supported
ONFI 2.1 spec. interface supported
Toggle DDR interface supported

2.2 USB interface

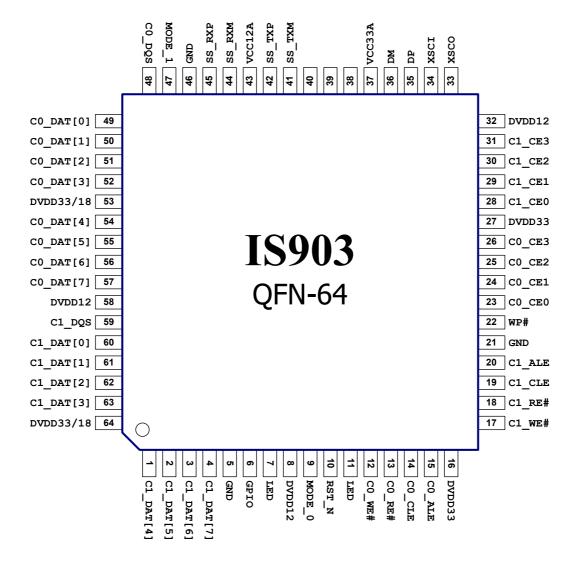
Compliant with USB 3.0 spec. version 1.0
Compliant with USB 2.0 spec. backward compatible with USB1.1
Compliant with USB Mass Storage Class spec. version 1.0

- 2.3 ECC protect 43 bit by 1K bytes
- 2.4 High performance 1T 8051 with hardware acceleration DMA
- 2.5 F/W off-load engine embedded
- 2.6 1.2V low power consumption design
- 2.7 LED indicator to show link status and r/w traffic
- 2.8 Customized VID/ PID with serial number
- 2.9 30Mhz Crystal



3. Pin Assignment

3.1 QFN-64 Pin Assignment





Pin Descriptions (QFN-64)

Pin Name	Pin# (62)	Pin# (64)	Pull up/down	Attribute	Description
C1_DAT[4]	C2	1	down*1	I/O	Flash Channel-1 data
C1_DAT[5]	D1	2	down*1	I/O	Flash Channel-1 data
C1_DAT[6]	E2	3	down*1	I/O	Flash Channel-1 data
C1_DAT[7]	F1	4	down*1	I/O	Flash Channel-1 data
GND	G2	5		GND	GND
GPIO	H1	6	None	0	reserved
LED_1	-	7	None	0	LED to show link status and r/w traffic
DVDD12	J2	8		PWR	1.2V core power supply
MODE0	K1	9	down	I	Test mode pin, tie to GND
RST_N	L2	10	up	I	Chip reset, low active
LED_0	M1	11	None	0	LED to show link status and r/w traffic
C0_WE#	N2	12	None	0	Flash Channel-0 WE#
C0_RE#	P1	13	None	0	Flash Channel-0 RE#
C0_CLE	R2	14	None	0	Flash Channel-0 Command latch
C0_ALE	T1	15	None	0	Flash Channel-0 Address latch
DVDD33	U2	16		PWR	3.3V IO power supply
C1_WE#	V3	17	None	0	Flash Channel-1 WE#
C1_RE#	U4	18	None	0	Flash Channel-1 RE#
C1_CLE	V5	19	None	0	Flash Channel-1 Command latch
C1_ALE	U6	20	None	0	Flash Channel-1 Address latch
GND	-	21		GND	GND
WP#	V7	22	None	0	Flash write protection
C0_CE0	U8	23	None	0	Flash Channel-0 chip enable 0
C0_CE1	V9	24	None	0	Flash Channel-0 chip enable 1
C0_CE2	U10	25	None	0	Flash Channel-0 chip enable 2
C0_CE3	V11	26	None	0	Flash Channel-0 chip enable 3
DVDD33	U12	27		PWR	3.3V IO power supply
C1_CE0	V13	28	None	0	Flash Channel-1 chip enable 0



			I	1	
C1_CE1	V15	29	None	0	Flash Channel-1 chip enable 1
C1_CE2	U14	30	None	0	Flash Channel-1 chip enable 2
C1_CE3	V17	31	None	0	Flash Channel-1 chip enable 3
DVDD12	U16	32		PWR	1.2V core power supply
XSCO	U18	33		0	Crystal 30Mhz output
XSCI	T17	34		I	Crystal 30Mhz input
DP	R18	35		I/O	USB 2.0 differential pin plus
DM	P17	36		I/O	USB 2.0 differential pin minus
VCC33A	N18	37		PWR	3.3V analog power supply
RREF	M17	38		I	Connect the external reference resistor (12.1 k Ω ± 1%) to the analog ground
SSCAP	L18	39		I	Connect to a 2.2nF capacitor, with proper low noise handle
VCC128	K17	40		I	Connect to a 4.7uF capacitor, with proper low noise handle
SS_TXM	J18	41		0	USB 3.0 differential transmit pin negative
SS_TXP	H17	42		0	USB 3.0 differential transmit pin positive
VCC12A	G18	43		PWR	1.2V analog power supply
SS_RXM	F17	44		I	USB 3.0 differential receive pin negative
SS_RXP	E18	45		I	USB 3.0 differential receive pin positive
GND	D17	46		GND	GND
MODE1	C18	47	down	I	Test mode pin, tie to GND
C0_DQS	B17	48	down*1	I/O	Flash Channel-0 strobe data
C0_DAT[0]	A16	49	down*1	I/O	Flash Channel-0 data
C0_DAT[1]	B15	50	down*1	I/O	Flash Channel-0 data
C0_DAT[2]	A14	51	down*1	I/O	Flash Channel-0 data
C0_DAT[3]	B13	52	down*1	I/O	Flash Channel-0 data
DVDD33	A12	53		PWR	3.3V IO power supply
C0_DAT[4]	B11	54	down*1	I/O	Flash Channel-0 data
C0_DAT[5]	A10	55	down*1	I/O	Flash Channel-0 data
C0_DAT[6]	B9	56	down*1	I/O	Flash Channel-0 data



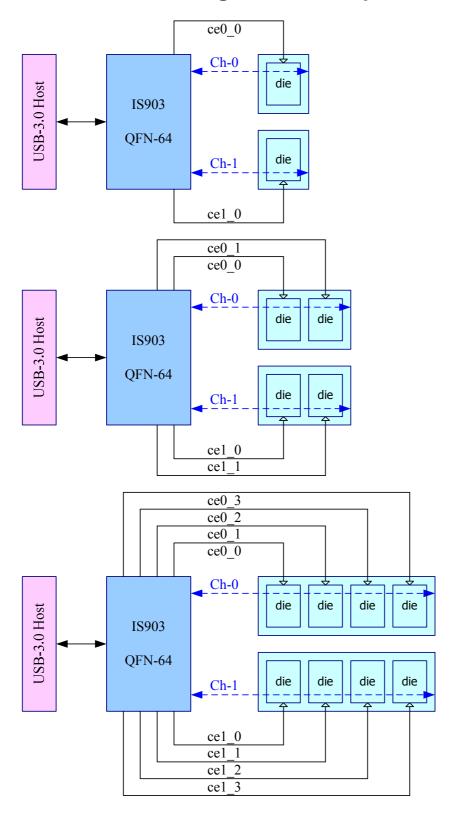
C0_DAT[7]	A8	57	down*1	I/O	Flash Channel-0 data
DVDD12	В7	58		PWR	1.2V core power supply
C1_DQS	A6	59	down*1	I/O	Flash Channel-1 strobe data
C1_DAT[0]	B5	60	down*1	I/O	Flash Channel-1 data
C1_DAT[1]	A4	61	down*1	I/O	Flash Channel-1 data
C1_DAT[2]	В3	62	down*1	I/O	Flash Channel-1 data
C1_DAT[3]	A2	63	down*1	I/O	Flash Channel-1 data
DVDD33	B1	64		PWR	3.3V IO power supply

Note - *1 : Default as pull-down, but it is released when R/W operating.



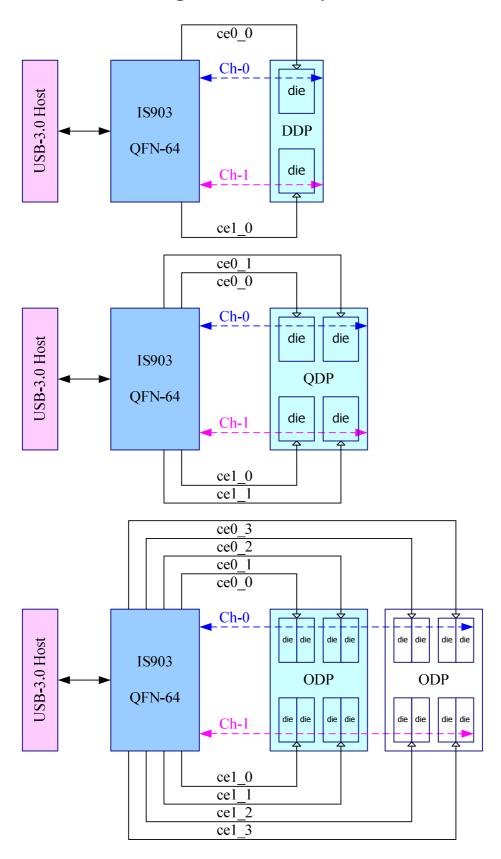
4. System Application Configurations

4.1 QFN-64 configuration example





4.2 QFN-64 configuration examples





5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Symbol Min.		Unit
Storage Temperature	Tstorage	-40	150	С
3.3V supply power	Vin33	-0.3	3.63	V
1.2V supply power	Vin12	-0.3	1.32	V

5.2 Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature	Toperating	0	70	С
USB VBUS	VBUS	3.3	5.5	V
Analog 3.3V power	VCC33A	3.15	3.45	V
Analog 1.2V power	VCC12A	1.14	1.26	V
Digital 3.3V power	DVDD33	2.97	3.63	V
Digital 1.2V power	DVDD12	1.08	1.32	V

5.3 Reference Clock Source and Crystal

Specification

Parameter	Symbol	Min.	Тур.	Max.	Unit
Reference clock	XSCI		30		Mhz
Crystal freq. tolerance		-50		+50	ppm
USB reference resistor	RREF	-1%	12.1	+1%	ΚΩ



5.4 DC Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit
USB bus power	VBUScurrent			900	mA
Analog 3.3V power U3	V33A_cur_u3		TBD		mA
Analog 1.2V power U3	V12A_cur_u3		TBD		mA
Analog 3.3V power U2	V33A_cur_u3		TBD		mA
Analog 1.2V power U2	V12A_cur_u3		TBD		mA
Analog 3.3V Suspend	V33A_cur_sus		TBD		mA
Analog 1.2V Suspend	V12A_cur_sus		TBD		mA
Digital 3.3V power	DVDD33_cur		TBD		mA
Digital 1.2V power	DVDD12_cur		TBD		mA

5.5 DC Characteristics of 3.3V IO

Parameter	Symbol	Min.	Тур.	Max.	Unit
Digital 3.3V power	DVDD33	2.97	3.3	3.63	mA
Input low voltage	Vil			0.8	V
Input high voltage	Vih	2.0			V
Output low voltage	Vol			0.4	V
Output high voltage	Voh	2.4			V
Pull-up resistance	Rpu	40	75	190	ΚΩ
Pull-down resistance	Rpd	30	75	190	ΚΩ



7. Package Information

7.1 QFN-64 package outline dimension

