VIA Labs, Inc.

Super-Speed PCB Design Guide Lines

VIA Labs, Inc.
Revision 1.3 Jul. 2012

VIA Labs, Inc.

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.9	2009/12/28	Initial version.	SI/FAE
1.0	2010/06/01	Add PCIe design rule.	SI/FAE
1.1	2010/09/01	Add Std connector/Pin header suggestion.	SI/FAE
1.2	2010/11/02	1. Add U3 cable soldering pad structure suggestion. 2. Add pcb trace length suggestion for front panel cable and connector.	SI/FAE
1.3	2012/07/11	1. Add cross trace structure. 2. Add 2 Layer suggestion	SI/FAE

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Table of Contents

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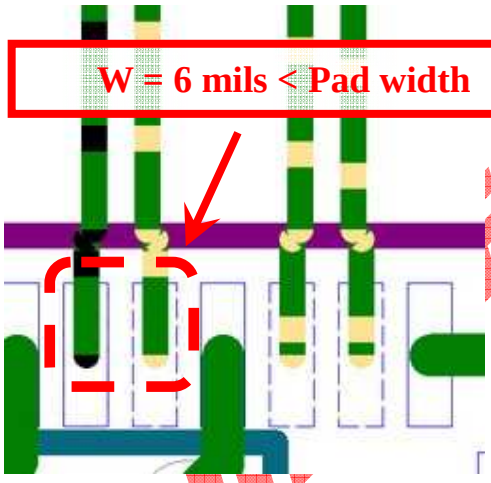
1. Differential Pairs

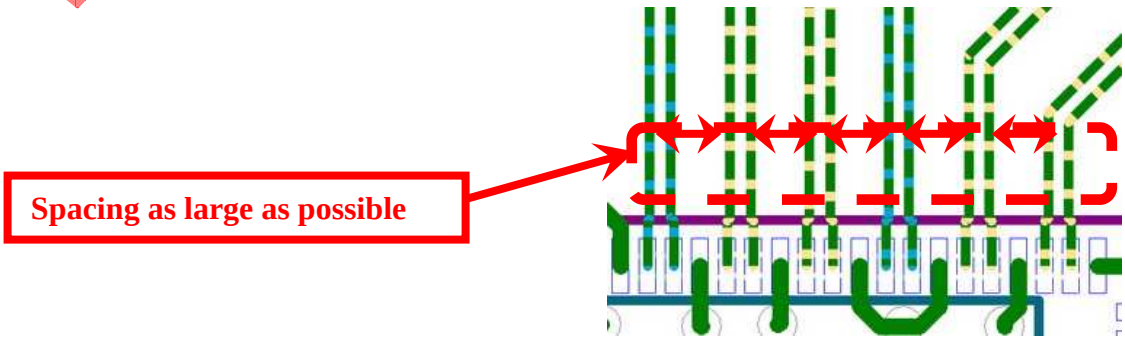
1.1. Differential Pairs - 1 (Diff. Z_0)

- **Characteristic impedance diff. Z_0: 90 +/- 10 % (USB) and 100 +/- 10 % (SATA) ohm**
- **For 4.3-mil FR4 prepreg (DK ~ 3.7), 0.5-mil solder mask (DK ~ 3.5), W-S-W = 6-6-6 mils for 90 ohm, 5-7-5 mils for 100 ohm**
- **Based on the process in PCB house, the trace width and spacing will be changed! Please consult with PCB house**
- **Proper prepreg (top FR4 layer) selection to ensure trace width is less than pad width (10 mils) for the chip pin**

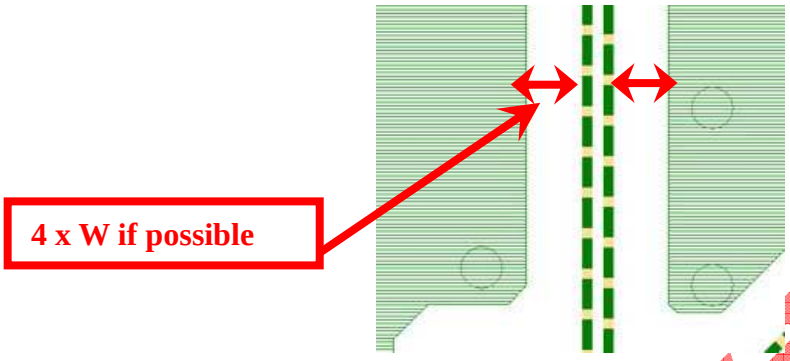


1.2. Differential Pairs - 2 (Trace Spacing)

- **Spacing between diff. pairs must be as large as possible (> 5 x W preferred)**

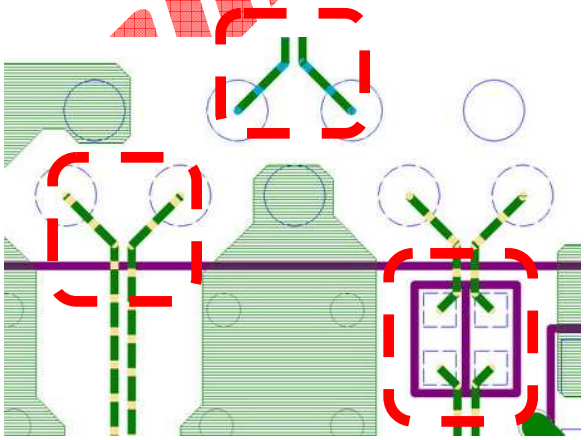


- **Spacing between trace and GND shape, via, and other components must be larger than 3 x W (> 4 x W preferred), except break out region close to chip (trace to via spacing might be smaller)**



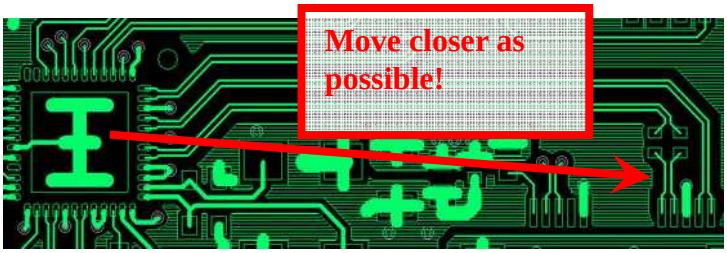
1.3. Differential Pairs - 3a (to Connectors)

- **Traces of tx, rx diff. pairs must be routed symmetrically, including symmetrically connected to connector pins and cap pads. Length tolerance between +/- traces must be less than 8 mils for std. A and B connectors**
- **Trace lengths of tx, rx should be as short as possible**
- **For USB 2 pairs, length tolerance between D+/D- should be less than 50 mils for std. A connector and 70 mils for std. B connector with de-tour routing**
- **If layer change is required, please refer to the via at pp. 5 and solid GND plane must be designed at the adjacent layer (EX. GND plane at L3 must be had for L4 diff. pair)**



1.4. Differential Pairs - 3b (to Connectors)

- Chip location and direction must be close to connector as possible
- Avoid turning high-speed diff. pairs always in the same direction (Skew will be increased obviously)

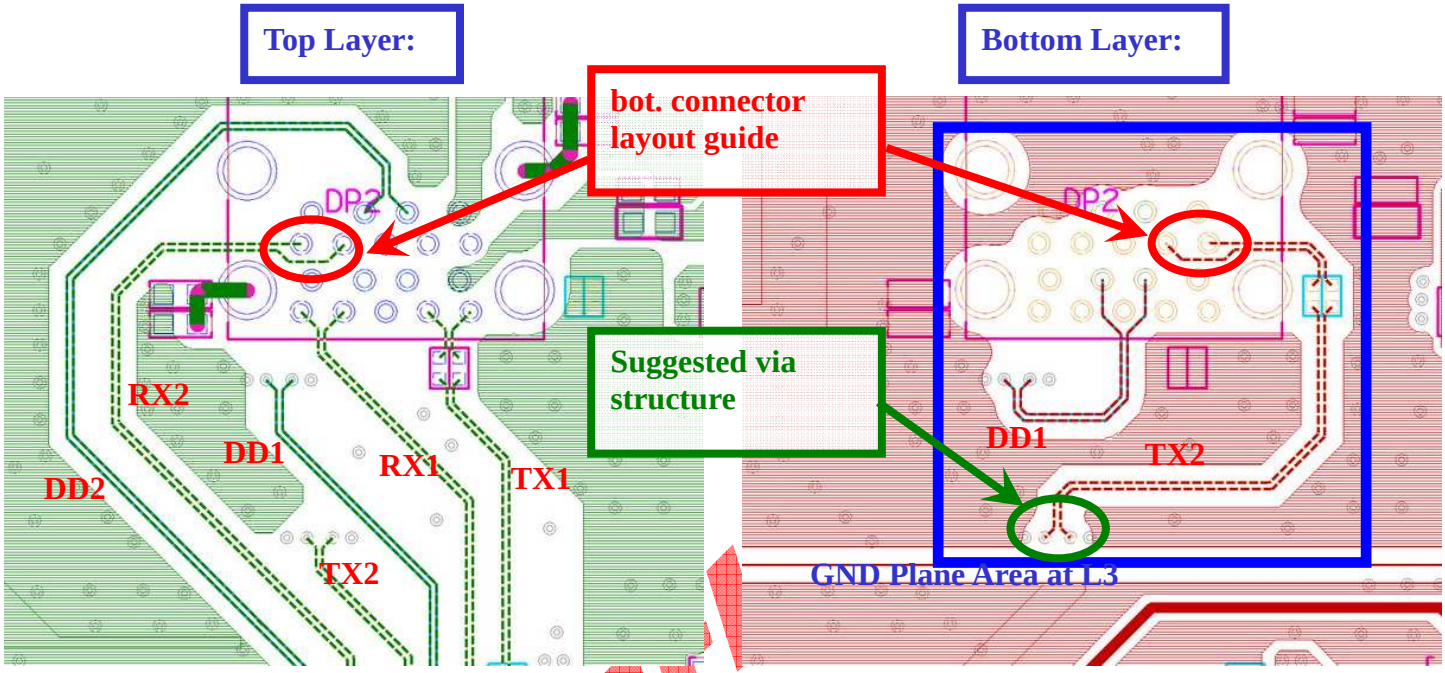


1.5. Differential Pairs - 4 (to Stack Connector)

- Symmetrically routed traces for diff. pairs are still required
- For layout possibility, only tx and rx traces for the bottom connector, and USB 2.0 traces are suggested to have layer changed (use only top and bottom layers for sig.! refer to pp. 5 for the via structure)
- +/- traces of tx, rx for the top one should have length tolerance less than 8 mils
- +/- traces of tx, rx for the bottom one should have length tolerance less than 81 mils (the larger, the larger jitter!)
- For USB 2 pairs, length tolerance between D+/D- should be less than 50 mils with the de-tour routing
- Solid GND plane must be designed adjacent to diff. pair layers (EX. GND plane at L3 must be had for L4 diff. pair)

1.6. Differential Pairs - 5 (Ex. to Stack Connector)

- **One demonstrated example:**



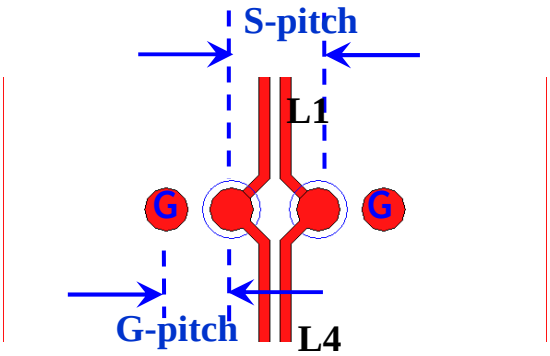
1.7. Structure for 90-Ohm Diff. Via Transition

- **Via spec.:**
  - V10: drill = 10 mil, Pad = 20 mil, antipad = 26 mil
  - V12: drill = 12 mil, Pad = 24 mil, antipad = 28 mil

- **4-via structure (2 GND visa on the opposite sides) is suggested**
- **V10:**
  - S-pitch = 40 mil, G-pitch = 25 mil (G-pitch > 25 mil is still ok for diff. mode, but comm. Mode response will be degraded)
- **V12:**
  - S-pitch = 54 mil, G-pitch = 34 mil
  - S-pitch = 44 mil, G-pitch = 34 mil is ok, but is not as good as the order one!

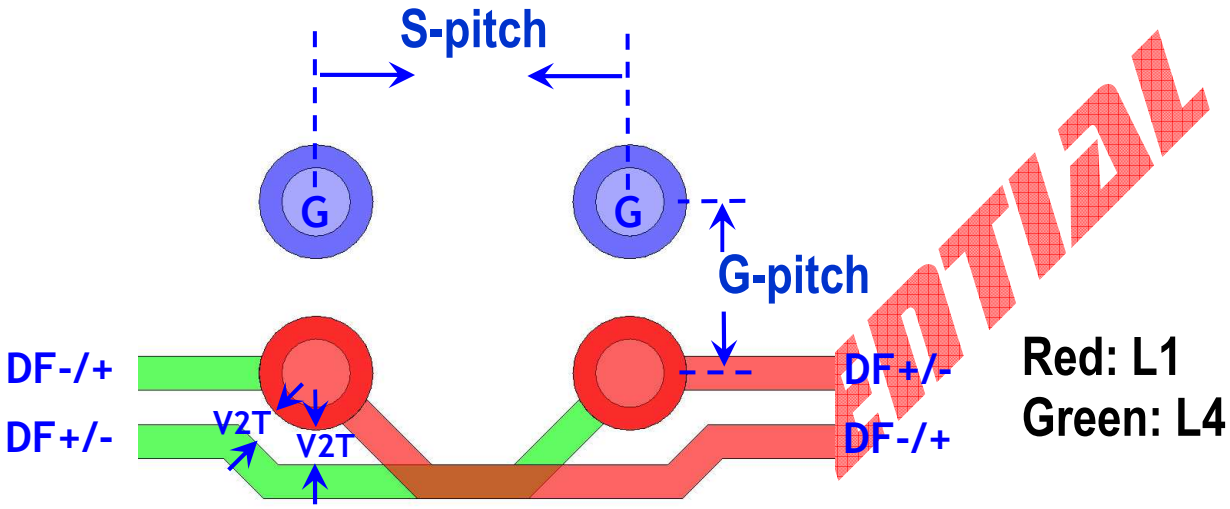
Ex. Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.5 mil
L1		Plating	0.8 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.4 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	0.8 mil
		soldermask	0.5 mil
		Total thickness	63.2 mil
			1.61 mm



1.8. Cross Trace Structure for 90-Ohm Diff. Pair

- **Diff. Pair:**
  - W-S-W = 6-6-6 mils
  - Trace angle: 45 degree
- **Via spec:**
  - v12: drill = 12 mil, pad = 20 mil, antipad = 28 mil
  - S-pitch = 55 mil, G-pitch = 30 mil
  - Minimum via to trace spacing V2T = 6 mil



Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.5 mil
L1		Plating	0.8 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.4 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	0.8 mil
		soldermask	0.5 mil
		Total thickness	63.2 mil
			1.61 mm

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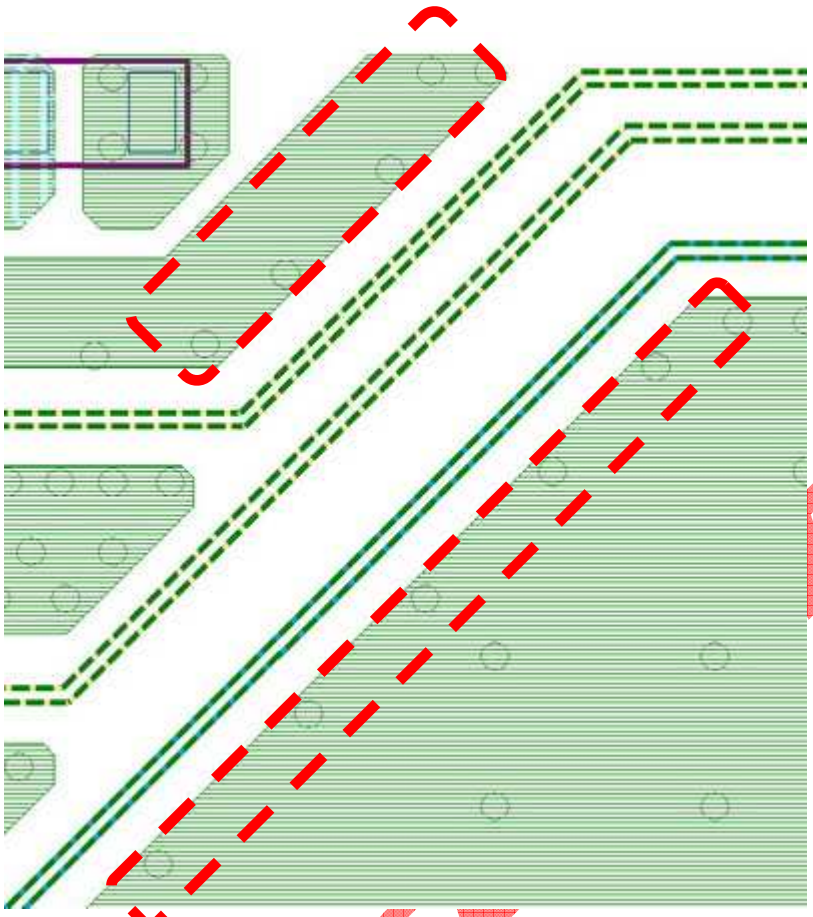
2. Vias on GND Shapes

- **GND vias should be applied to the edge of GND shape adjacent to diff. pairs**
- **Spacing between GND vias should be less than 200 mils, the smaller spacing, the better**
- **Do NOT form protrudent end of the GND shape (GND vias are required at the ends)**



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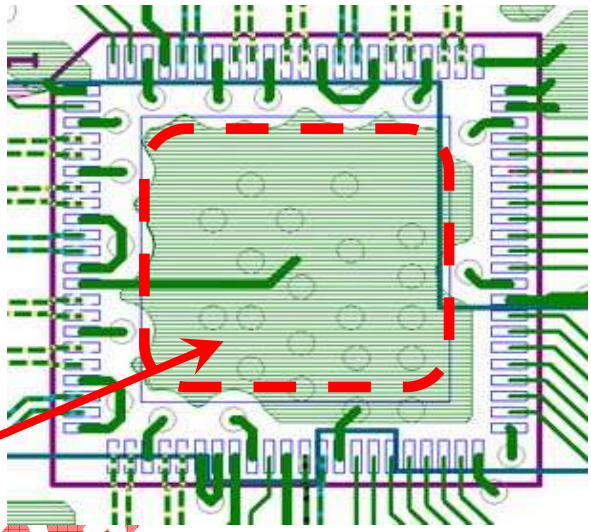
3. GND Pad for Chip Exposed Pad

- **Solid GND pad is required**
- **GND vias in this region should be as many as possible and well distributed**
- **Avoid placing de-caps in this region**



Solid GND and well-distributed vias are required

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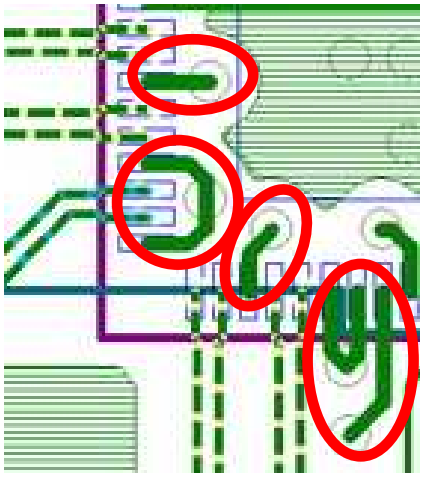
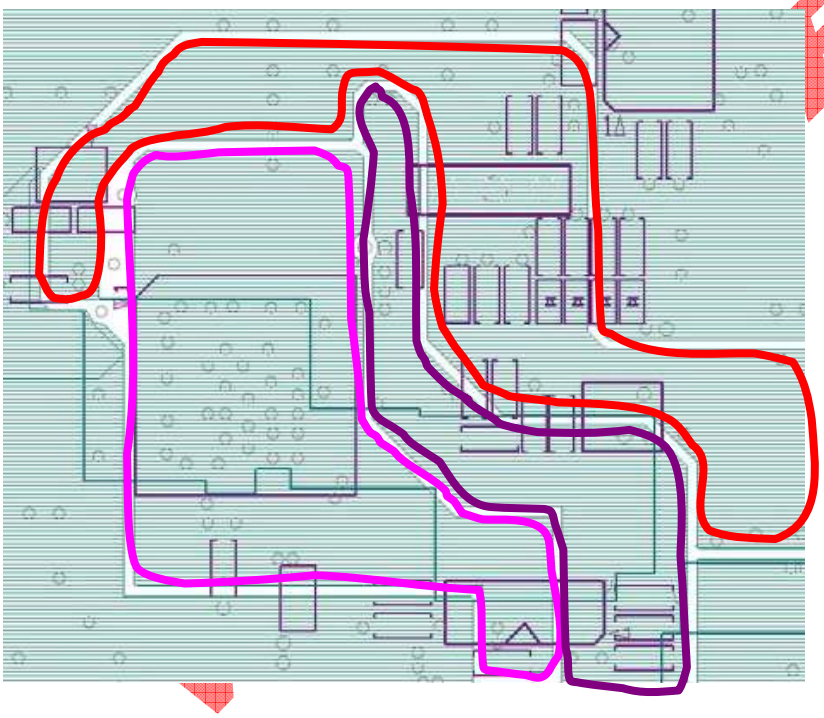
4. Power Planes and Connections

- **Connection between pins and vias must be as short as possible**
- **De-caps must be placed as close to chip as possible**
- **Use power plane design for all powers, and with via connections as much as possible**





5. Guide lines for 2-layer PCB's (Especially for VL812)

5.1. Differential Pairs

- **Diff. Z0 of 1.0 mm FR4 :**
  - W-S-W = 11-5-11 mil
- **Diff. Z0 of 1.6 mm FR4 :**
  - W-S-W = 12-5-12 mil
- **For PCB thickness between above two, use the trace width between above two**
- **Minimum GND shape to trace spacing is 10 mil**
- **After the break out region, keep TX pair to RX pair spacing as large as possible (larger than 1.5*(2W+S) is suggested, at least 1*(2W+S))**

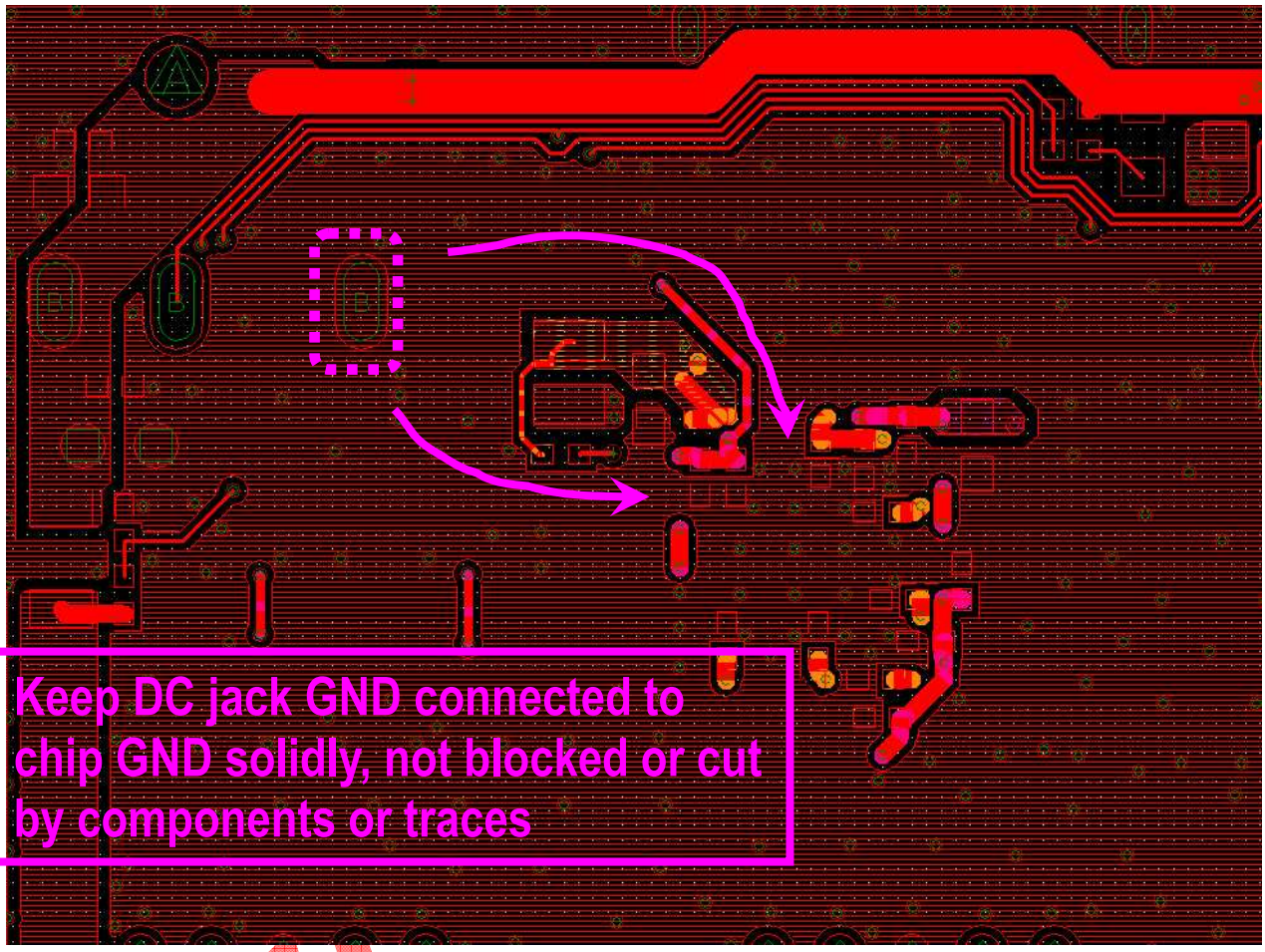
Stackup 1 mm :

Layer	Stackup	Material	Thickness
		soldermask	0.7 mil
L1		Cu + Plating	1.6 mil
		Prepreg	34.2 mil
L2		Cu + Plating	1.6 mil
		soldermask	0.7 mil
		Total thickness	38.8 mil
			0.99 mm

Stackup 1.6 mm :

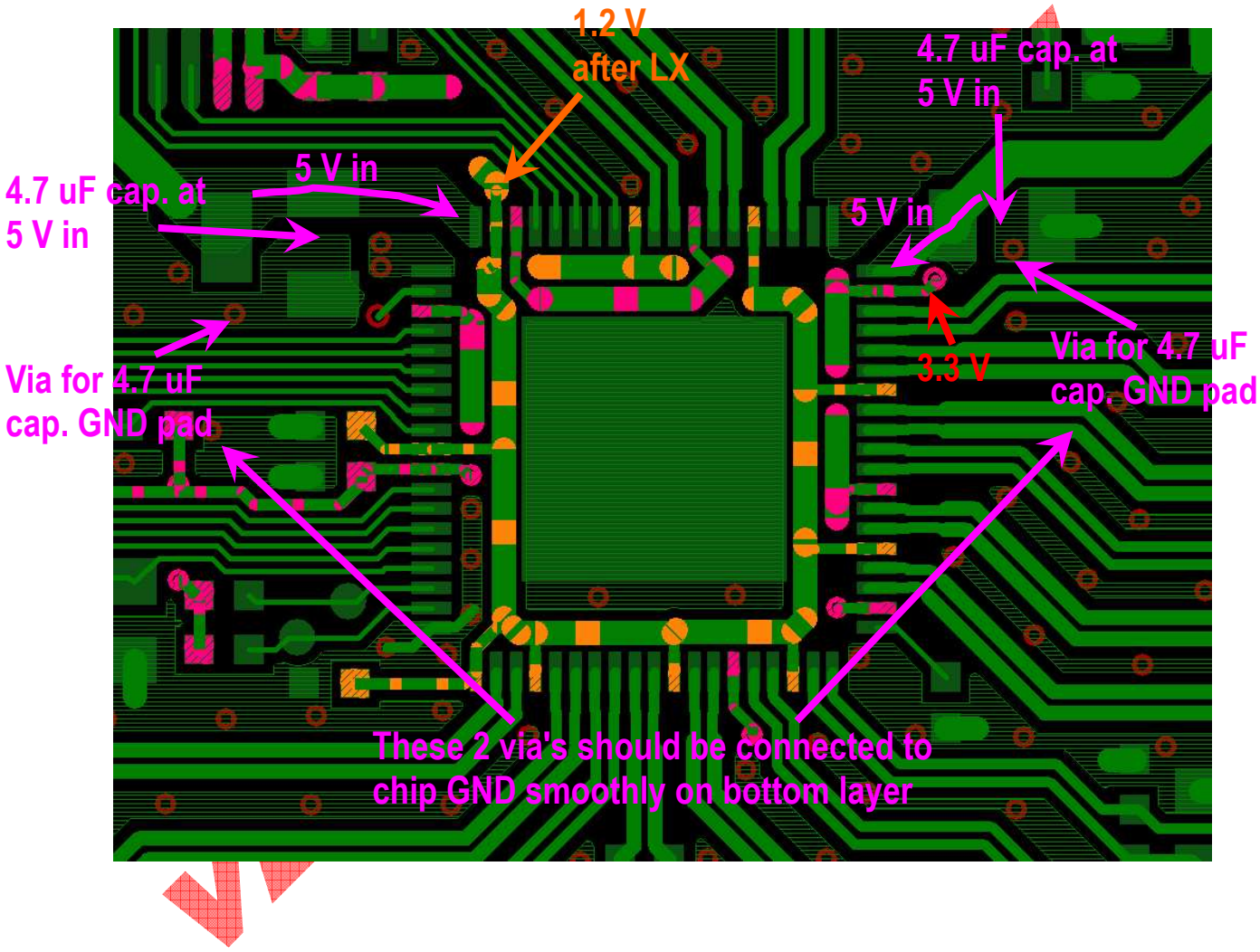
Layer	Stackup	Material	Thickness
		soldermask	0.7 mil
L1		Plating	1.0 mil
		Copper Foil	0.6 mil
		Core	58.0 mil
L2		Copper Foil	0.6 mil
		Plating	1.0 mil
		soldermask	0.7 mil
		Total thickness	62.6 mil
			1.59 mm

5.2. DC Jack GND to Chip GND

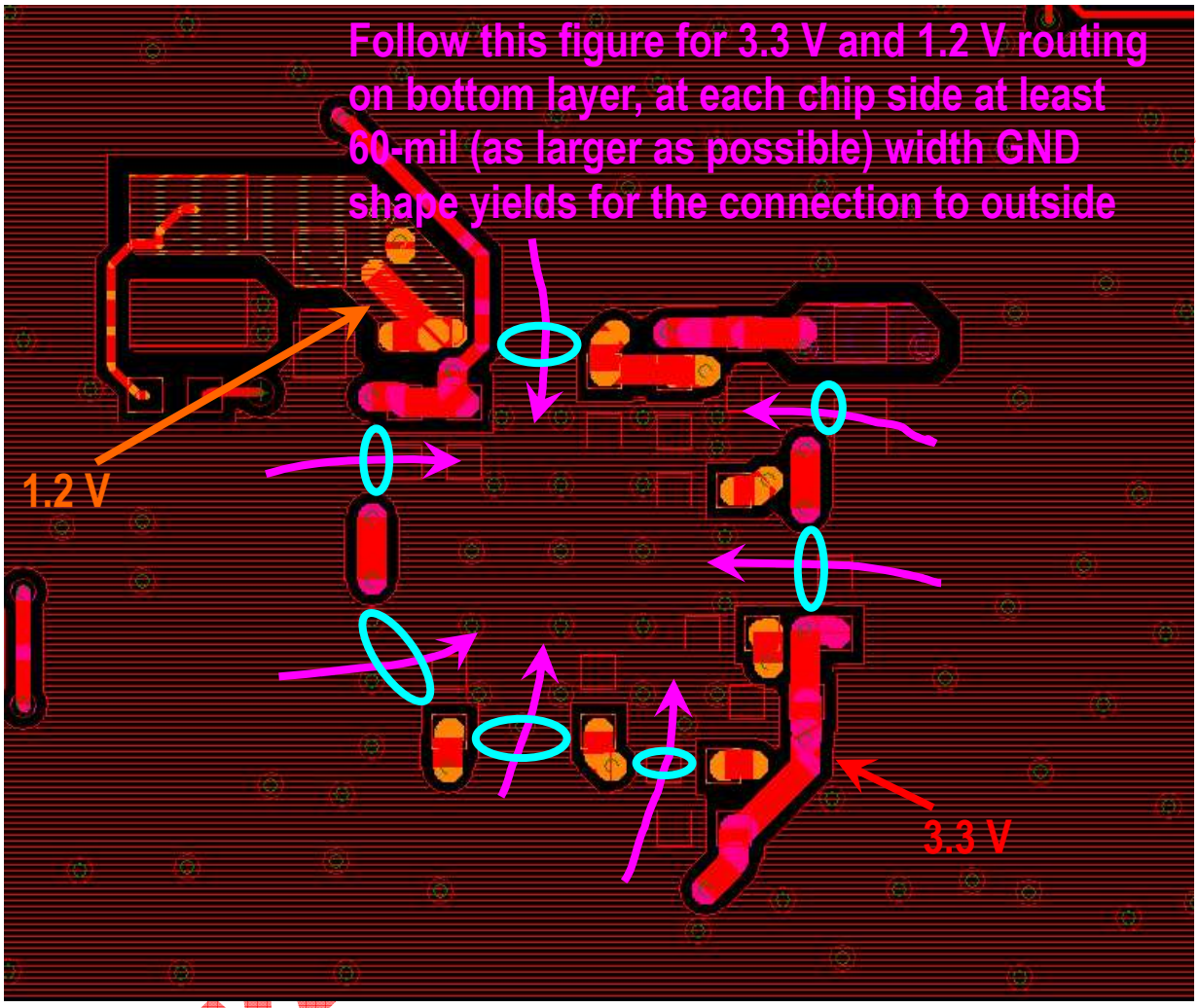


5.3. Keep GND plane solid on Bottom Layer

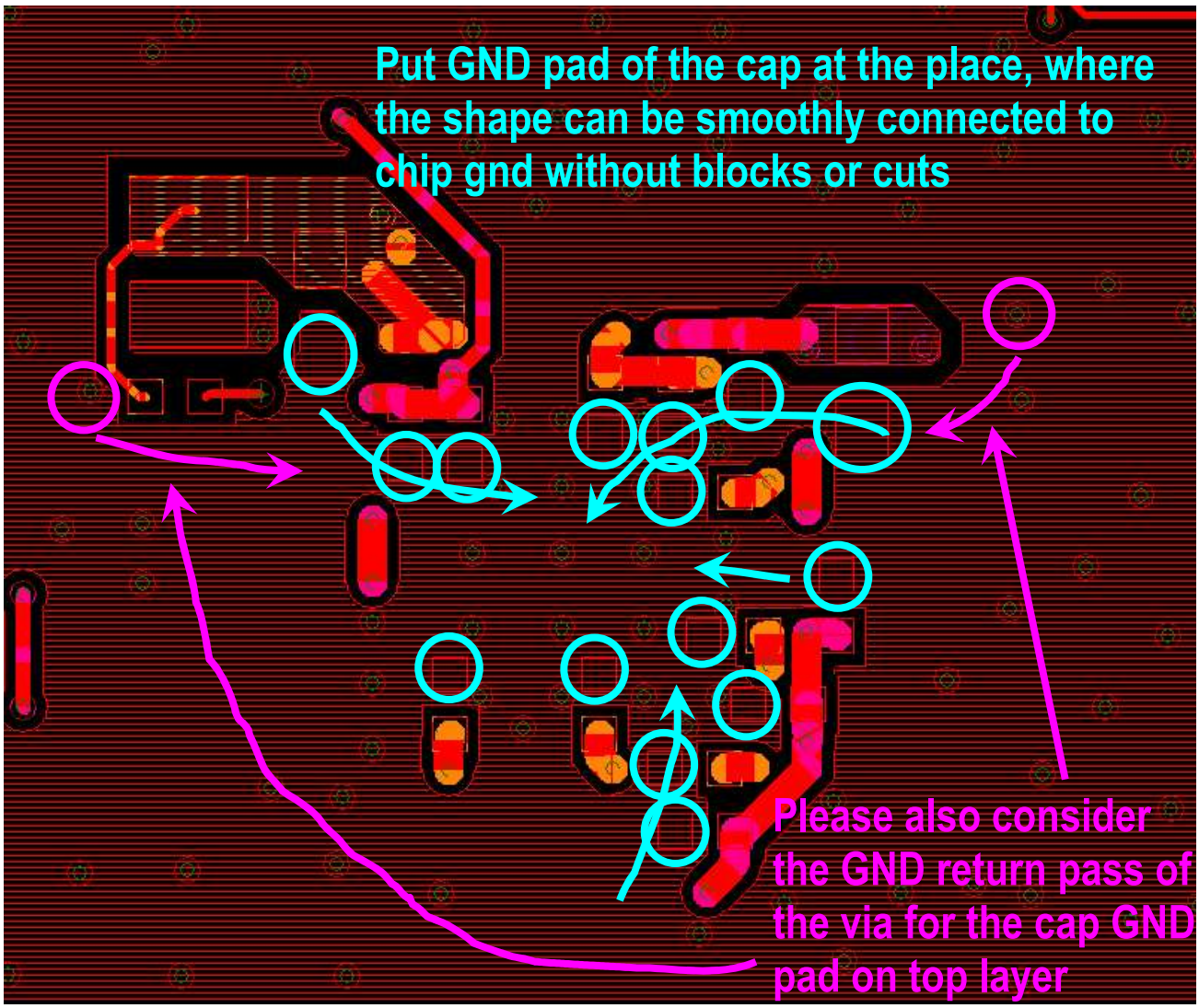
5.4. Power Net Routing on Top Layer



5.5. Power Net Routing on Bottom Layer



5.6. GND Pad Location of De-cap's



6. PCB Footprint for USB 3.0 connectors

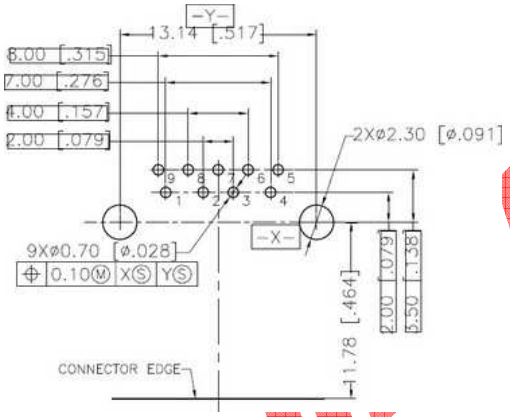
6.1. Footprint for USB 3.0 Std A, Stack A, and Std B Connectors

- **DIP Via for TX/RX pins:**
  - Drill = 28 mil, Pad = 43 mil, Antipad (L2 and L3) = 80 mil
- **Other pins:**
  - Use the default one is fine

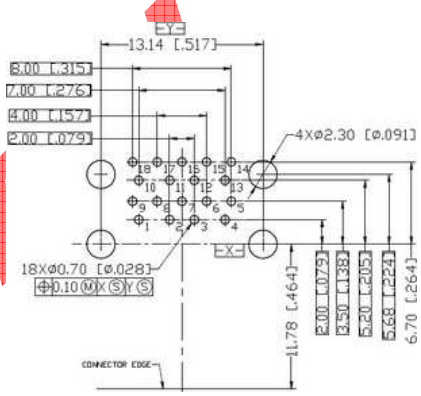
Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.5 mil
L1		Plating	0.8 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.4 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	0.8 mil
		soldermask	0.5 mil
		Total thickness	63.2 mil
			1.61 mm

Std A:



Stack A:



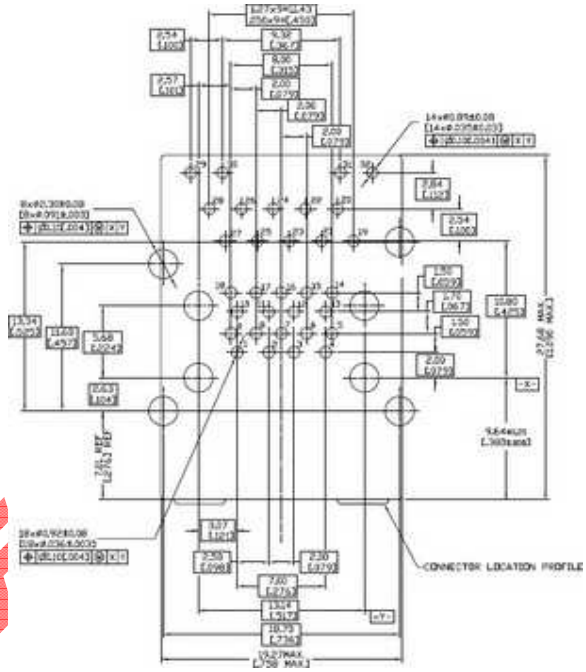
6.2. Footprint for USB 3.0 Stack A with RJ45 Connector

- **DIP Via for TX/RX pins:**
  - Drill = 35 mil, Pad = 50 mil, Antipad (L2 and L3) = 80 mil
- **Other pins:**
  - Use the default one is fine

Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.5 mil
L1		Plating	0.8 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.4 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	0.8 mil
		soldermask	0.5 mil
		Total thickness	63.2 mil
			1.61 mm

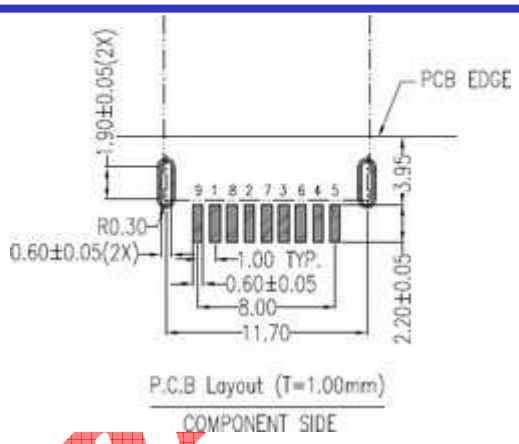
Stack A + RJ45:



6.3. Footprint for USB 3.0 Plug A Connector (WinWin, High-Top)

- **TX/RX pads:**
  - Pad Width = 24 mil
  - Etched GND width on L2 = 30 mil
  - L3 should still be GND
- **Other pins:**
  - Use the default one is fine

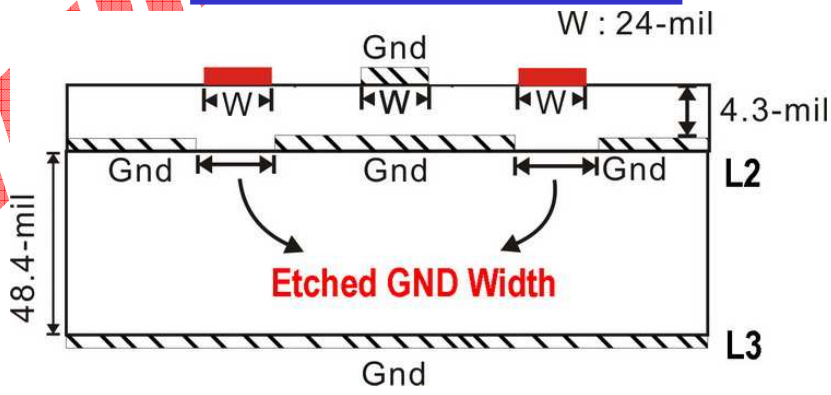
Plug A: (9 pin, equal pitch)



Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.5 mil
L1		Plating	0.8 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.4 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	0.8 mil
		soldermask	0.5 mil
		Total thickness	63.2 mil
			1.61 mm

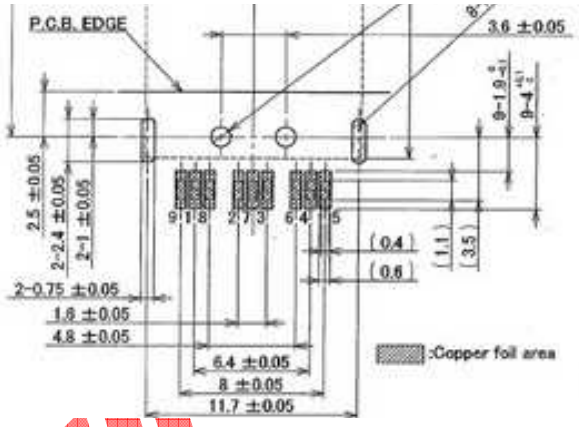
TX/RX Pad Structure:



6.4. Footprint for USB 3.0 Plug A Connector (Hosiden)

- **TX/RX pads:**
  - Pad Width = 24 mil
  - Etched GND width on L2 = 31 mil
  - L3 should still be GND
- **Other pins:**
  - Use the default one is fine

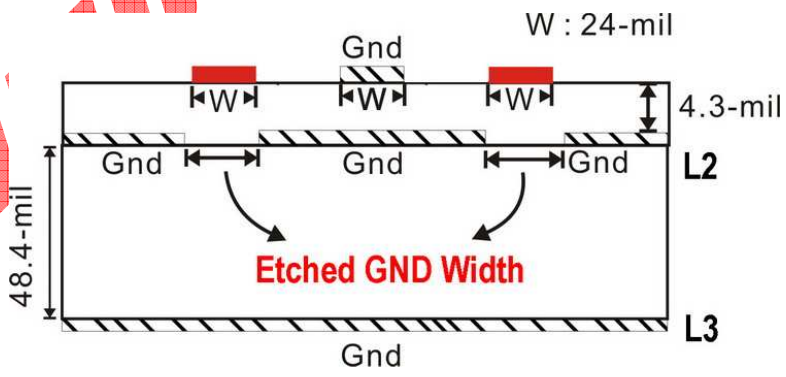
Plug A: (9 pin, non-equal pitch)



Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.5 mil
L1		Plating	0.8 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.4 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	0.8 mil
		soldermask	0.5 mil
		Total thickness	63.2 mil
			1.61 mm

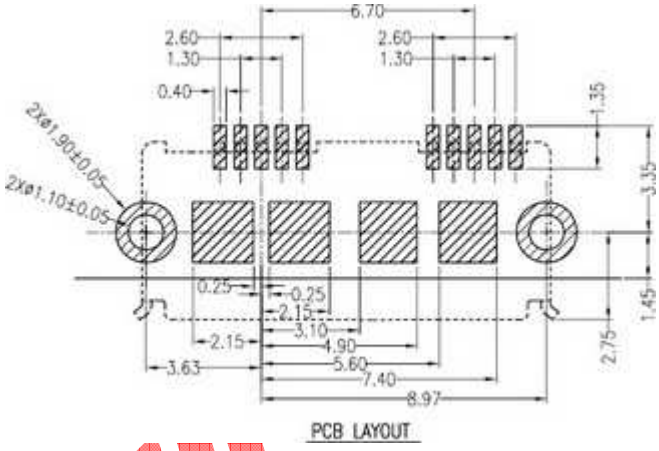
TX/RX Pad Structure:



6.5. Footprint for USB 3.0 uB Connector

- **TX/RX pads:**
  - Pad Width = 20 mil
  - Etched GND width on L2 = 23 mil
  - L3 should still be GND
- **Other pins:**
  - Use the default one is fine

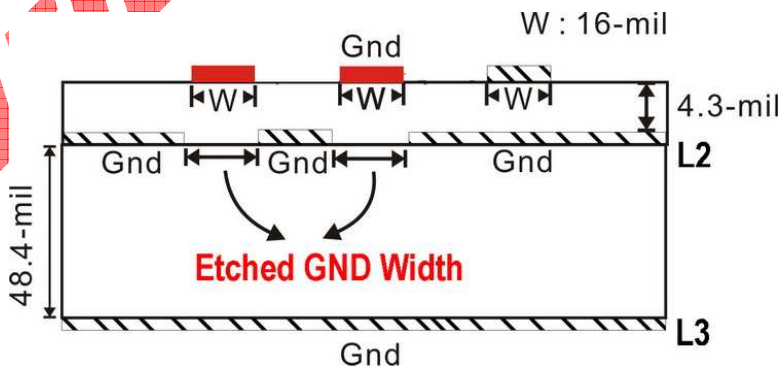
uB:



Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.5 mil
L1		Plating	0.8 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.4 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	0.8 mil
		soldermask	0.5 mil
		Total thickness	63.2 mil
			1.61 mm

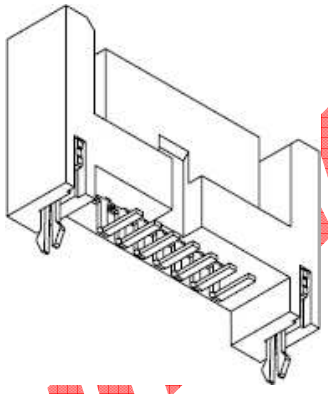
TX/RX Pad Structure:



6.6. Footprint for Vertical SMT SATA Connector

- **Most Well (99G30-180114)**
- **TX/RX pads (diff. 100 ohm):**
  - Pad Width = 28 mil
  - Etched GND width on L2 = 40 mil
  - L3 should still be GND
- **Other pins:**
  - Use the default one is fine

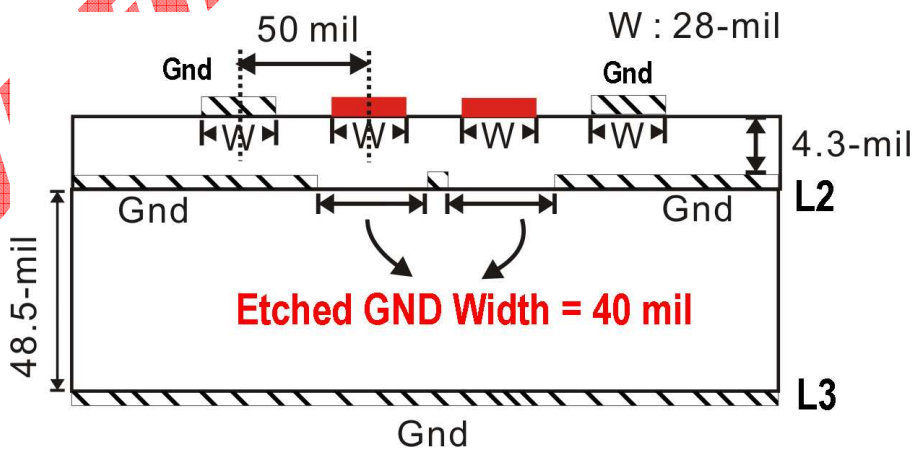
SATA:



Stackup

Layer	Stackup	Material	Thickness
		soldermask	0.7 mil
L1		Plating	1.0 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.5 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	1.0 mil
		soldermask	0.7 mil
		Total thickness	64.1 mil
			1.63 mm

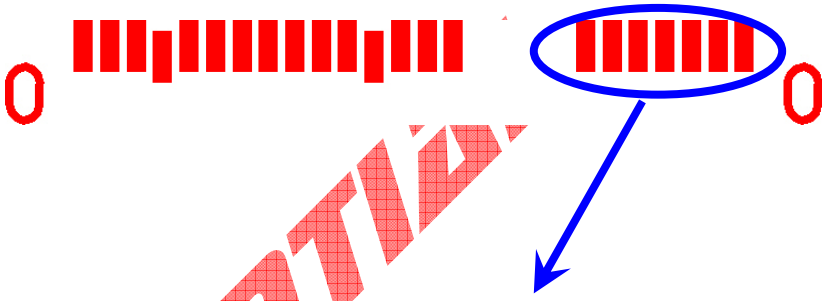
TX/RX Pad Structure:



6.7. Footprint for 22-pin SATA Connector

- **TX/RX pads (diff. 100 ohm):**
  - Pad Width = 33 mil
  - Etched GND width on L2 = 333 mil
  - L3 should still be GND
- **Other pins:**
  - Use the default one is fine

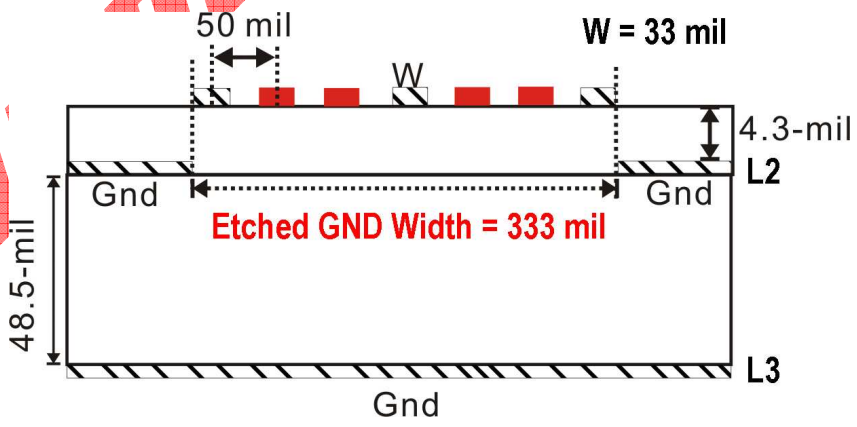
22-pin SATA:



Stackup:

Layer	Stackup	Material	Thickness
		soldermask	0.7 mil
L1		Plating	1.0 mil
		Copper Foil	0.6 mil
		Prepreg	4.3 mil
L2		Copper Foil	1.2 mil
		Core	48.5 mil
L3		Copper Foil	1.2 mil
		Prepreg	4.3 mil
L4		Copper Foil	0.6 mil
		Plating	1.0 mil
		soldermask	0.7 mil
		Total thickness	64.1 mil
			1.63 mm

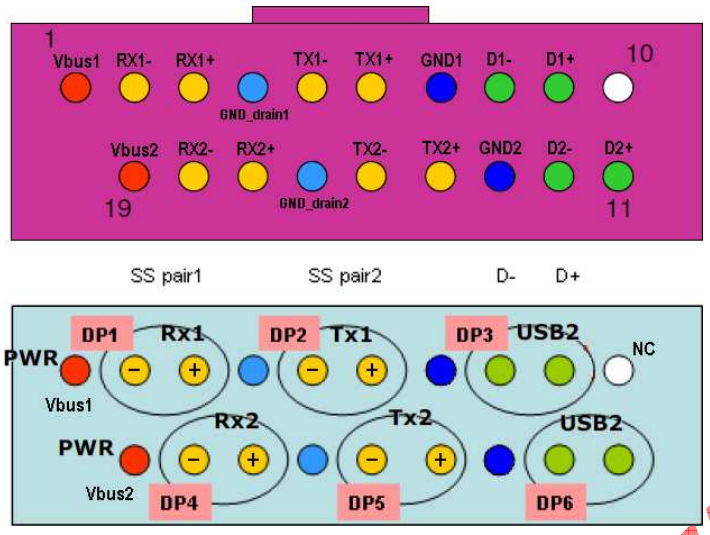
TX/RX Pad Structure:



7. USB 3.0 Internal Connection for Front Panel

- **Pin Header: Lotes GAP-ABA-USB-050 (internal USB 3.0 PLUG)**
- **Cable: Lotes GAP-ABA-USB-061-K01_100325_E (45cm)**
- **Pin Header Foot Print:**

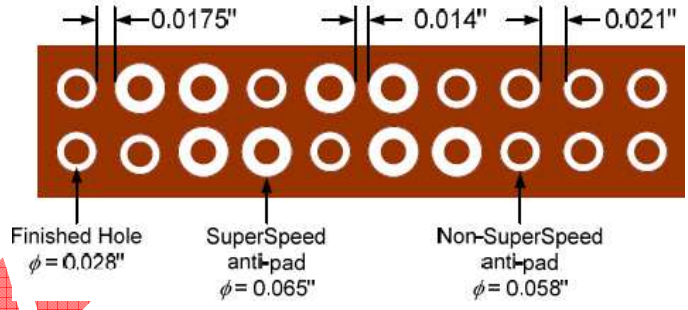
Pin Arrangement:

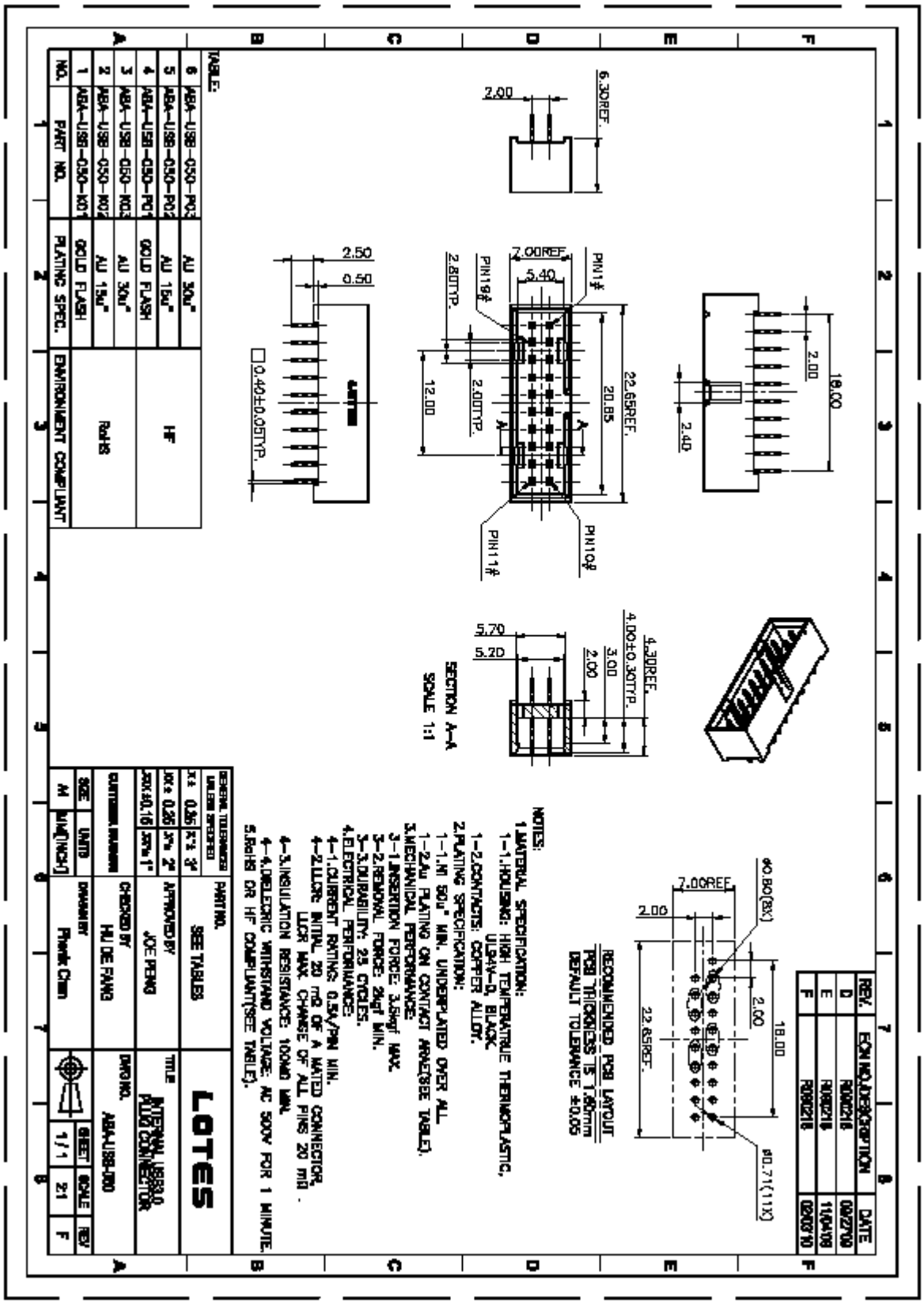


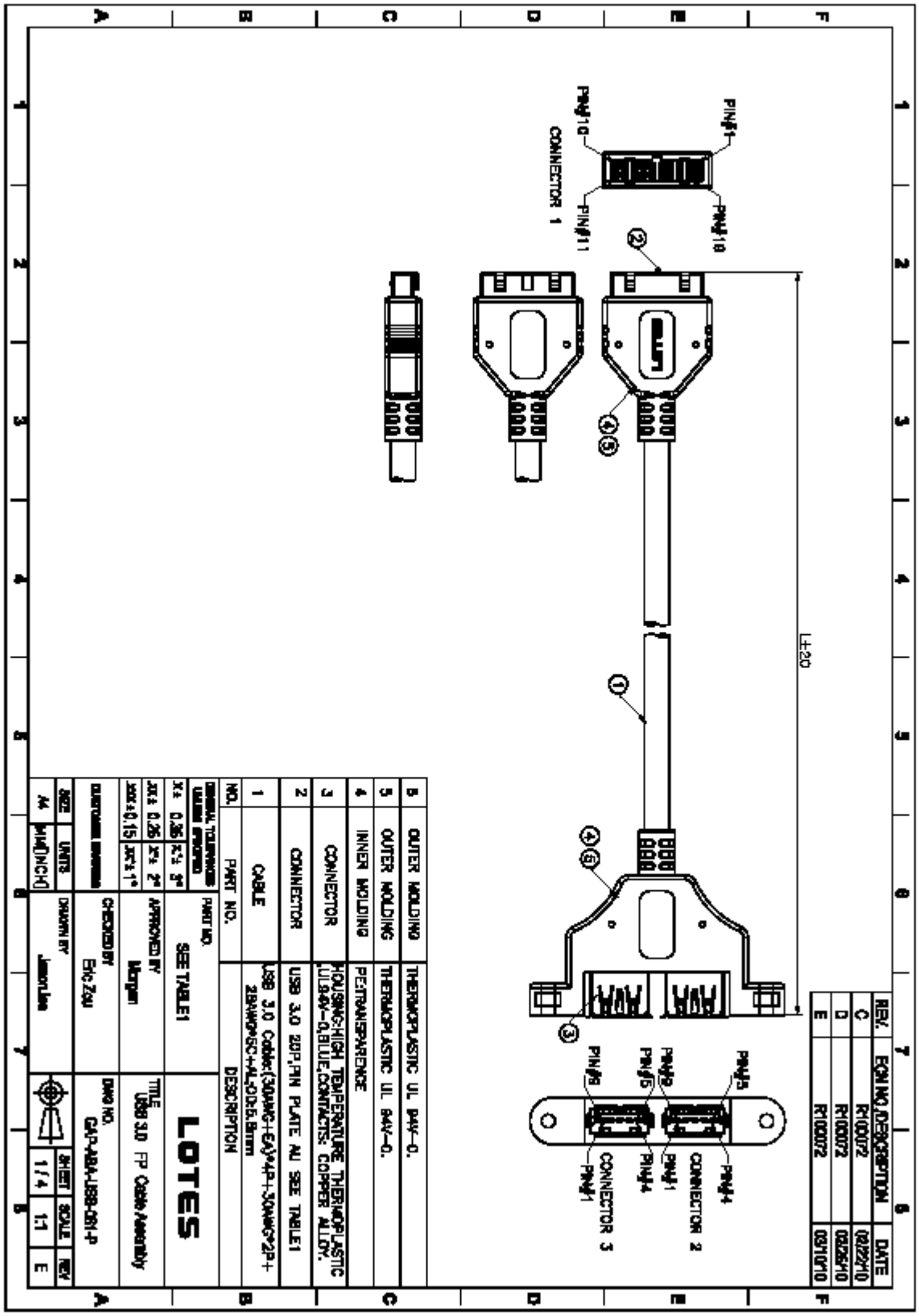
Suggested Footprint by USB-IF:

Via Spec. for SS Pairs:

Drilled hole	0.81mm
Finished hole	0.71mm
Solder pad	1.04mm
Anti-pad	1.65mm





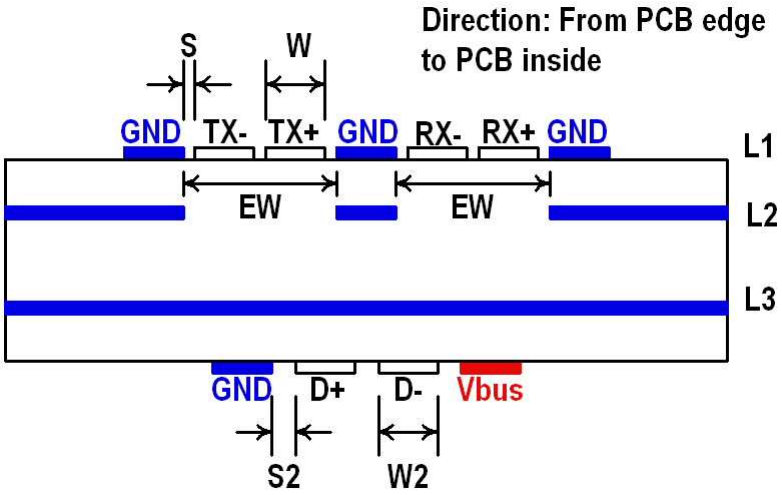


8. PCB Lengths of Front Panel to Pass Compliance Test

- **Mother board only (mother board + 45-CM cable):**
  - PCB trace length to pin header on mother board: < 4 inch
- **Mother and daughter board (mother board + 45-CM cable + daughter board):**
  - PCB trace length to pin header on mother board: < 3 inch
  - PCB trace length from pin header to std. A receptacle connector on daughter board: < 2 inch

9. Soldering Pads for USB 3.0 Cables on PCB

- **2-Layer soldering (top and bot., U3 on chip side):**
- **Pad rules (diff. 90 ohm):**
  - Pad Width W = 47 mil
  - Pad Spacing S = 17.5 mil
  - Etched GND width on L2 EW = 146.5 mil
  - L3 should still be GND
  - W2 and S2 not limited (similar as W and S are fine)



- **1-Layer soldering (on chip side)**
- **Pad rules (diff. 90 ohm):**
  - Pad Width W = 47 mil
  - Pad Spacing S = 17.5 mil
  - Etched GND width on L2 EW = 146.5 mil
  - L3 should still be GND
  - Width and spacing for U2 and Vbus not limited (similar as W and S are fine)