

MODULE I : BJT BIASING

THE OPERATING POINT:

(*) The transistor needs to be operated in an appropriate region of its characteristics depending on the application of the circuit in which it is being used.

(*) The dc currents and voltages in the circuit are established by using a resistive network along with a dc power supply. This process is called "Biasing".

Example: Consider the output characteristics of Common-Emitter npn transistor.

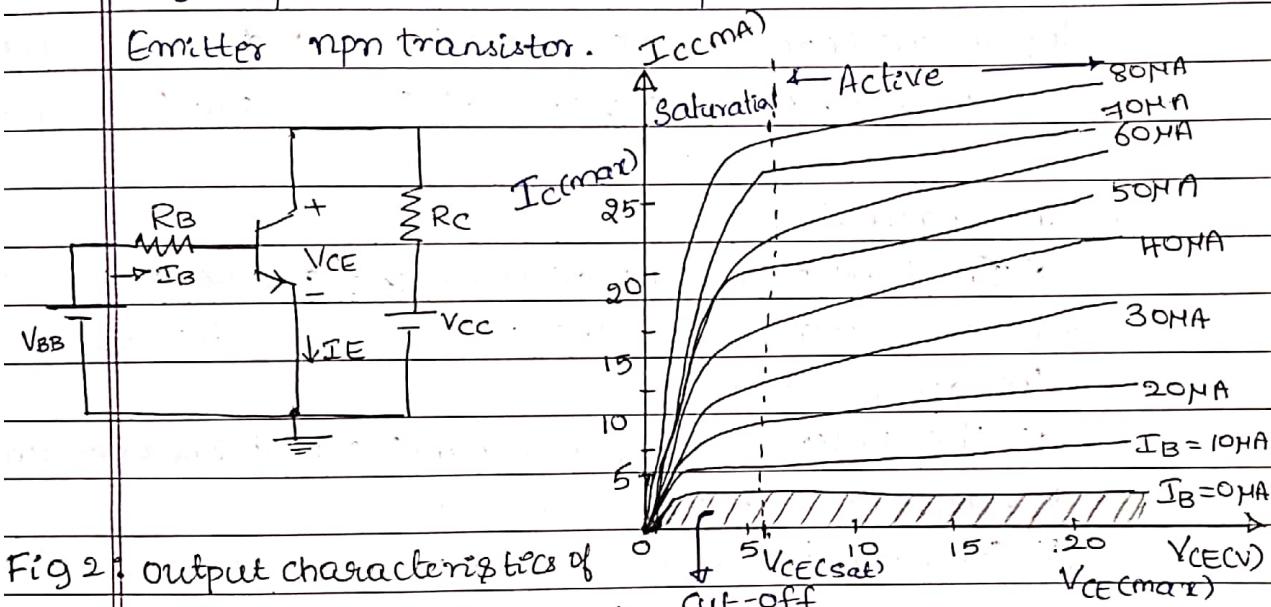


Fig 2: Output characteristics of Common-Emitter Configuration.

(*) The three regions of operation of the transistor are termed as Active region, Cut-off region and Saturation region.

Active Region - It is the region where the collector current increases with increase in Base current.

The BEJ is forward biased while the BCJ is reverse biased.

Cut-off Region - Here the BEJ is RB & CBJ is RB (below 0.1V for Ge and 0 V for Si).

The Emitter current is zero & transistor is non-conducting.

Saturation region - The region close to $V_{CE} = 0$, where all curves appear to merge & fall rapidly to origin is called Saturation Region.

(*) Here Both the EBJ & CBJ is forward Biased.

(*) The transistor is required to be biased from cut-off to saturation and vice versa when being used as a switch.

(*) The BJT must be biased in the active region when being used as an Amplifier.

(*) The transistor functions linearly when its operation is restricted to the active region.

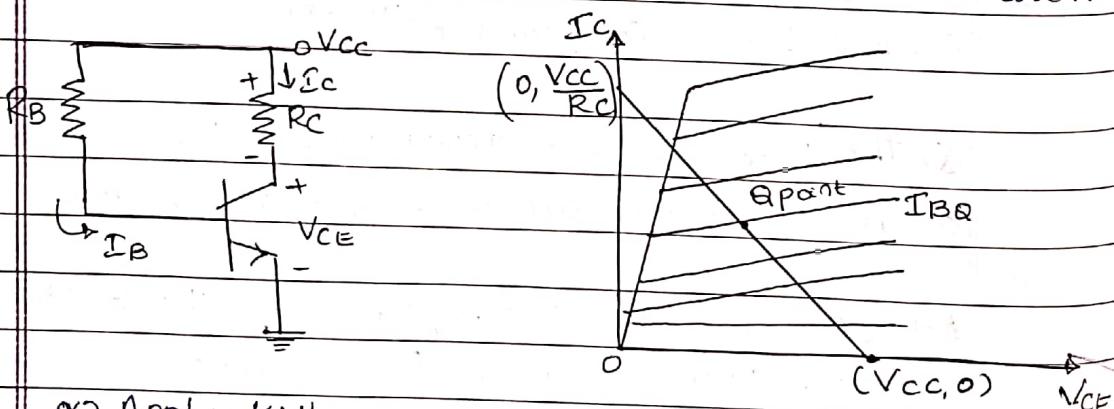
(*) For transistor amplifiers, we need to establish an operating point on the characteristics to define a region of operation by fixing the dc current and voltages.

→ DC Load line

(*) The line called the dc load line can be drawn on the characteristics of the transistor which represents the applied load.

(*) The intersection of the load line with the characteristics will determine the operating point.

(*) Consider the collector circuit of a biased transistor.



(*) Apply KVL. $V_{CC} - I_C R_C - V_{CE} = 0$

$$V_{CE} = V_{CC} - I_C R_C \quad \rightarrow ①$$

(*) To plot dc load line.

(i) Choose $I_C = 0\text{mA}$, specifying the horizontal axis

$$V_{CE} = V_{CC} \Big| I_C = 0\text{mA} \quad \rightarrow ②$$

(ii) Choose $V_{CE} = 0\text{V}$, specifying the vertical axis.

$$I_C = \frac{V_{CC}}{R_C} \Big| V_{CE} = 0\text{V} \quad \rightarrow ③$$

(*) The intersection of this load line with the output characteristics would result in number of possible operating point.

(*) However, the operating point is chosen around the middle of load line to provide an equal swing of I_C & V_{CE} about the point. This would ensure that BJT remains in active region during its entire operation.

BIASING IN

BJT AMPLIFIER CIRCUITS :

major consideration in Bias design.

(i) The biasing problem is that establishing a constant dc current in the collector of the BJT.

(ii) This current has to be calculable, predictable and insensitive to variations in temperature and to the large variations in the value of β .

(iii) Locating the dc bias point in the $I_C - V_{CE}$ plane to allow for maximum output signal swing.

(iv) Consider two biasing arrangements.

(1) Biasing the BJT by fixing the voltage V_{BE} by using a voltage divider across the power supply V_{cc} as shown in Fig(1a), is not a viable/feasible approach.

(*) Because any small and inevitable/unavoidable differences in V_{BE} from the desired value will result in large differences in I_C and in V_{CE} .

(2) Biasing the BJT by establishing a constant current in the Base, where $I_B = (V_{cc} - 0.7)/R_B$ is also not recommended.

$$V_{cc} - I_B R_B - V_{BE} = 0 \Rightarrow I_B R_B = V_{cc} - V_{BE}$$

$$\Rightarrow I_B = \frac{V_{cc} - 0.7}{R_B}$$

(*) Here large variations in the value of β will result in corresponding large variations in I_C and hence V_{CE} .

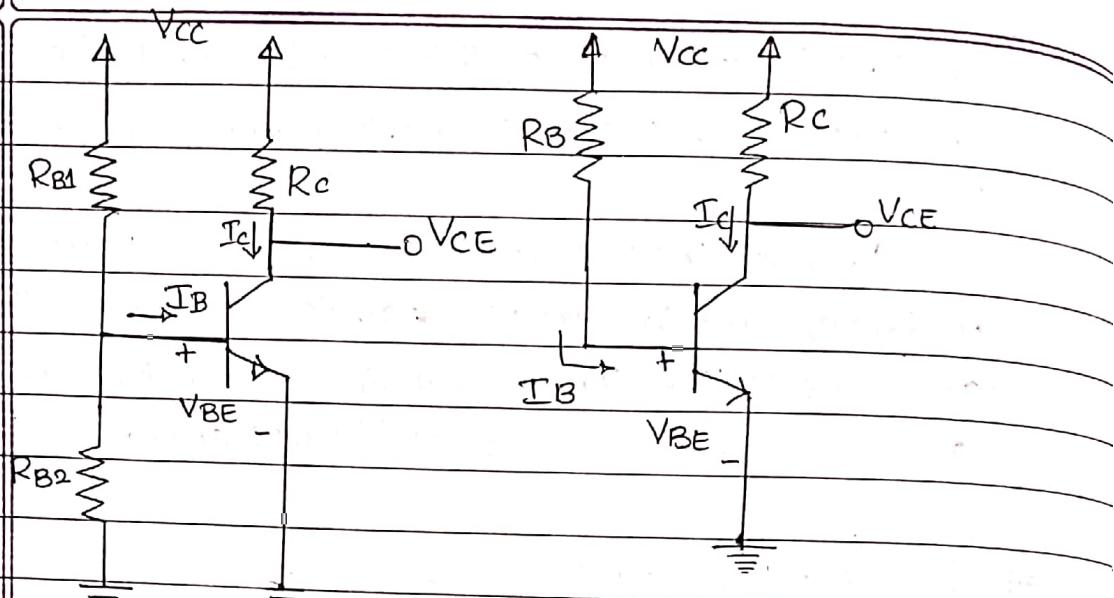


Fig 1: Two Obvious Schemes for biasing the BJT:

- (a) By fixing V_{BE}
- (b) By fixing I_B . Both result in wide variations in I_c and hence in V_{CE} [\therefore Not recommended].

THE CLASSICAL DISCRETE-CIRCUIT BIAS ARRANGEMENT

- (*) In fixed-Bias Scheme, the quiescent values of I_c and V_{CE} i.e., quiescent point is a function of dc current gain β of the transistor.
- (*) β is sensitive to temperature & its values keeps varying.
- (*) A Biasing circuit independent or less dependent on β such as the Voltage divider bias circuit is therefore desirable.
- (*) Fig 2(a) Shows the most commonly used biasing arrangement for discrete-circuit transistor amplifier if only a single power supply is available.
- (*) The technique consists of supplying the base of the transistor with a fraction of the supply voltage V_{CC} through the voltage divider R_1 & R_2 .

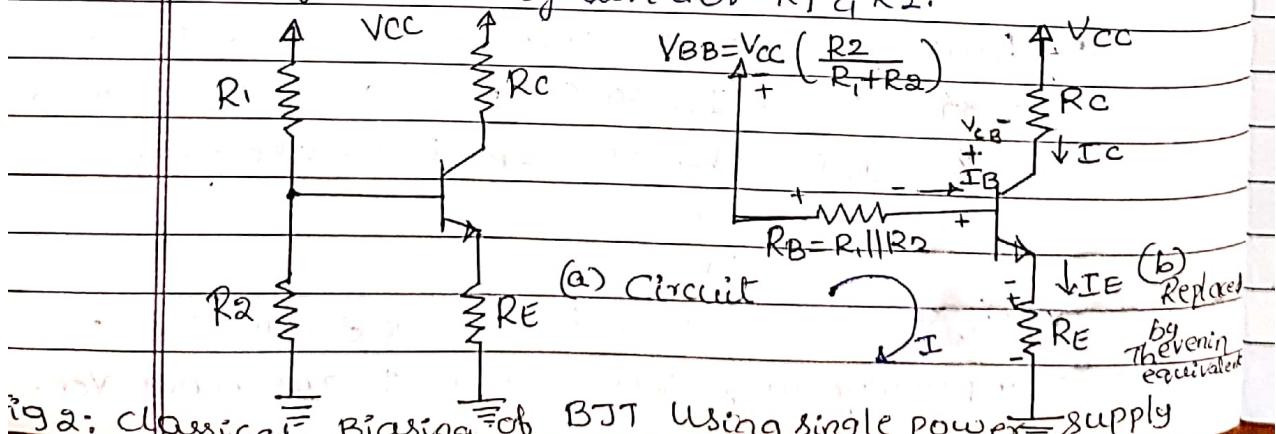
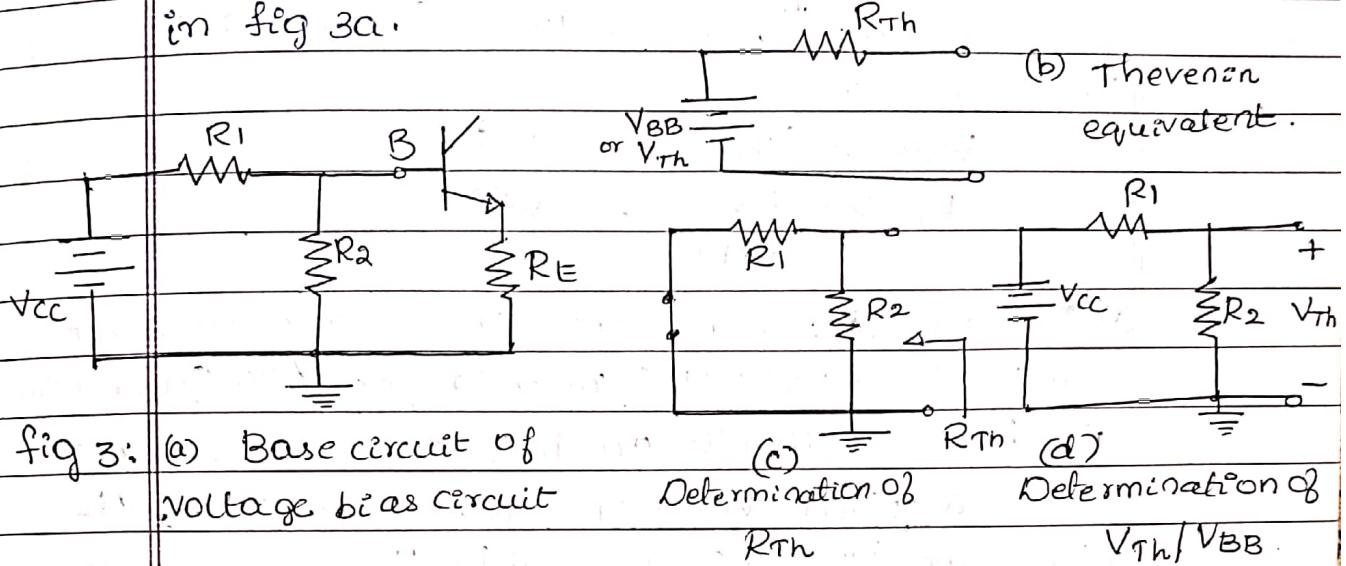


Fig 2: Classical Biasing of BJT Using single power supply

(*) The Input Side of the circuit of fig 2a can be redrawn in fig 3a.



(*) To find the Thevenin resistance R_{Th} , V_{CC} is replaced by short circuit equivalent as shown in fig 3c.

(*) Thevenin resistance R_{Th} :

$$R_{Th} = R_1 \parallel R_2$$

$$\therefore R_{Th} = \frac{R_1 R_2}{R_1 + R_2} \quad \rightarrow ①$$

(*) from fig 3d, Thevenin voltage V_{Th} :

$$V_{Th} \text{ or } V_{BB} = V_{CC} \frac{R_2}{R_1 + R_2} \quad \rightarrow ②$$

(*) The circuit of fig(2a) is redrawn in fig(2b) after substituting the Thevenin equivalent.

(*) Applying KVL to Base-Emitter circuit and substituting $I_B = I_E / (\beta + 1)$:

$$\text{WKT } I_E = I_C + I_B$$

$$\frac{I_C}{I_B} = \beta \Rightarrow I_C = \beta I_B$$

$$I_E = \beta I_B + I_B$$

$$\frac{I_E}{I_B}$$

$$I_E = I_B (1 + \beta)$$

$$\therefore I_B = \frac{I_E}{\beta + 1}$$

$$\text{KVL: } V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{BB} - V_{BE} = I_B R_B + I_E R_E$$

$$V_{BB} - V_{BE} = \frac{I_E R_B + I_E R_E}{\beta + 1}$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B / (\beta + 1)} \quad \rightarrow ③$$

(*) To make I_E insensitive to temperature and β variation, the circuit must satisfy the following two constraints :

$$V_{BB} \gg V_{BE} \longrightarrow ④$$

$$R_E \gg \frac{R_B}{\beta + 1} \longrightarrow ⑤$$

(*) Condition ④ : Ensures that small variation in V_{BE} will be swamped by the much larger V_{BB} (Overwhelm)

(*) There is a limit on how large V_{BB} can be:

↳ For a given value of supply voltage V_{CC} , the higher the V_{BB} , the lower will be the sum of voltage across R_C and collector-base junction (V_{CB}).

↳ On the other hand, the voltage across R_C to be large is desirable to obtain high voltage gain and large signal swing (before transistor cut-off).

↳ V_{CB} (or V_{CE}) to be large is preferable to provide large signal swing (before transistor saturation).

⇒ Therefore the solution must be a compromise.

Thumb rule: (*) one designs V_{BB} about $\frac{1}{3}V_{CC}$, V_{CB} (or V_{CE}) about $\frac{1}{3}V_{CC} + I_C R_C$

$\frac{1}{3}V_{CC}$. (*) condition ⑤: makes I_E insensitive to variations in β & could be satisfied by selecting small R_B .

(*) R_B is lowered by using low values for R_1 and R_2 .

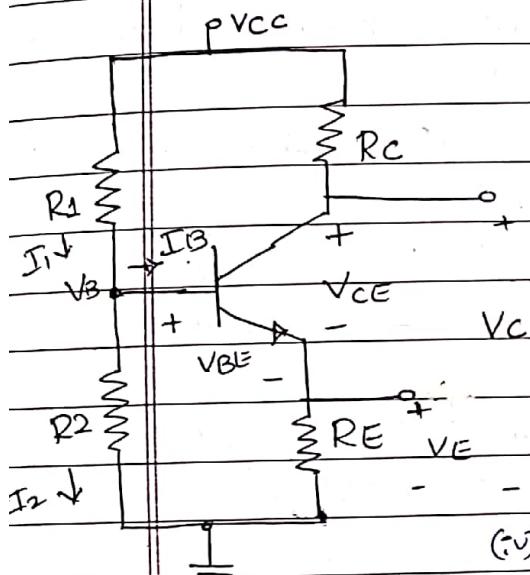
(*) Lower values of R_1 and $R_2 \Rightarrow$ Higher current drain from the power supply & lowers input resistance of the amplifier.

(*) Condition ⑤ means that the base voltage be independent of β and determined solely by the voltage divider.

(*) This is satisfied if the current in the divider is made much larger than the base current.

(*) Typically one selects R_1 and R_2 such that their current is in the range of I_E to $0.1I_E$.

Example: Design the Bias Network of the amplifier in fig 2 to establish a current $I_E = 1 \text{ mA}$ using power supply $V_{CC} = +12 \text{ V}$. Transistor is specified to have $\beta = 100$.



Solution: (i) Rule of thumb

$$V_{BB} = \frac{1}{3} V_{CC} = \frac{1}{3} \times 12 = 4 \text{ V}$$

$$(ii) V_{BE} = V_B - V_E$$

$$V_E = V_B - V_{BE} = 4 - 0.7 = 3.3 \text{ V}$$

$$(iii) R_E = \frac{V_E}{I_E} = \frac{3.3 \text{ V}}{1 \text{ mA}} = 3.3 \text{ k}\Omega$$

(iv) Selecting voltage-divider current as $0.1 I_E$ (Condition 2 from above discussion)

$$V_{CC} = I_1 R_1 + I_2 R_2 \rightarrow (a)$$

KCL at node VB yields

$$I_1 = I_B + I_2 \quad [\text{Neglecting } I_B]$$

$$I_1 \approx I_2$$

$$\therefore \text{eqn } (a) \text{ yields } R_1 + R_2 = \frac{V_{CC}}{I_2}$$

$$R_1 + R_2 = \frac{V_{CC}}{0.1 \text{ mA}} \Rightarrow R_1 + R_2 = \frac{12}{0.1 \text{ mA}}$$

$$\therefore R_1 + R_2 = 120 \text{ k}\Omega \rightarrow (b)$$

$$\frac{R_2 V_{CC}}{R_1 + R_2} = V_{BB}$$

$$\text{i.e. } R_2 = \frac{4 \times 120 \text{ k}\Omega}{12} = 40 \text{ k}\Omega \Rightarrow R_2 = 40 \text{ k}\Omega$$

$$\therefore R_1 + R_2 = 120 \text{ k}\Omega \Rightarrow R_1 = 120 - 40 = 80 \text{ k}\Omega$$

$$\therefore I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B / (\beta + 1)}$$

$$I_E = \frac{4 - 0.7}{3.3 \text{ k} + \frac{80 \text{ k} \parallel 40 \text{ k}}{101}} = 0.93 \text{ mA} \Rightarrow I_E = 0.93 \text{ mA}$$

(*) I_E is bit lower than the value we are aiming [1mA]

(*) Therefore we simply restore that the divider current as I_E .

$$\therefore R_1 + R_2 = \frac{V_{CC}}{I_1} = \frac{12}{1m} = 12k\Omega \quad \therefore R_1 + R_2 = 12k\Omega$$

$$\hookrightarrow \frac{R_2}{R_1 + R_2} V_{CC} = V_{BB} \Rightarrow R_2 = \frac{4 \times 12k}{12} = 4k\Omega \quad \therefore R_2 = 4k\Omega$$

$$\hookrightarrow R_1 + R_2 = 12k\Omega \Rightarrow R_1 = 12 - 4k\Omega \quad \therefore R_1 = 8k\Omega$$

$$\hookrightarrow R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{8k \times 4k}{8k + 4k} = 2.66k\Omega$$

$$\hookrightarrow I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta+1)} = \frac{4 - 0.7}{3.3k + \frac{2.66k}{1021}} = 0.993mA$$

$$\therefore I_E = 1mA$$

R_C can be determined as follows.

$$V_{CC} - V_C = I_C R_C$$

$$V_{CE} = 4V$$

$$R_C = \frac{V_{CC} - V_C}{I_C}$$

$$V_{CE} = V_C - V_E$$

$$4 + 4 = V_C$$

$$R_C = \frac{12 - 8}{1m}$$

$$\therefore V_C = 8V$$

$$\therefore R_C = 4k\Omega$$

$$V_{CB} = V_C - V_B$$

$$4 + 4 = V_C \Rightarrow V_C = 8V$$

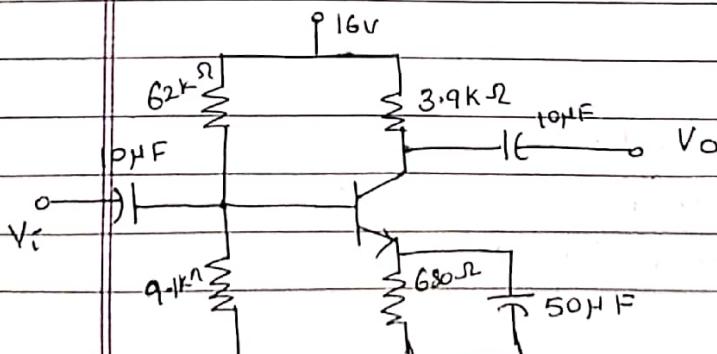
EXAMPLE 2: a) Find the Quiescent Base current, collector current & V_{CE}

for the circuit shown in fig with $V_{BE} = 0.7$ & $\beta = 80$.

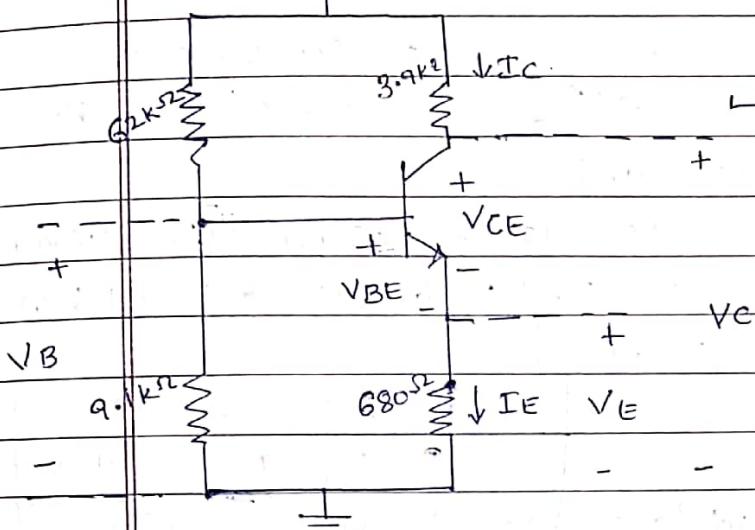
b) Determine values of collector, Emitter & Base voltage wrt ground.

c) Repeat @ for $\beta = 150$.

d) Draw the load line & locate Q-point corresponding to $\beta = 80$ and $\beta = 150$.



16V

Solution:

$$\hookrightarrow R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{62k\Omega \times 9.1k\Omega}{62k\Omega + 9.1k\Omega}$$

$$R_{Th} = 7.94k\Omega$$

$$V_{BB} = \frac{V_{cc} R_2}{R_1 + R_2}$$

$$V_{BB} = \frac{16V \times 9.1k\Omega}{62k\Omega + 9.1k\Omega}$$

$$V_{BB} = 2.05V$$

$$(a) \hookrightarrow V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{BB} - V_{BE} = I_B R_B + I_E R_E$$

$$I_E = I_C + I_B$$

$$V_{BB} - V_{BE} = I_B R_B + (1+\beta) I_B R_E$$

$$I_E = \beta I_B + I_B$$

$$\therefore I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$I_E = (1 + \beta) I_B$$

$$= \frac{2.05V - 0.7V}{7.94 + (80+1) 0.68k\Omega}$$

$$\Rightarrow I_B = 21.42mA$$

$$\hookrightarrow I_C = \beta I_B = 80 \times 21.42mA$$

$$\therefore I_C = 1.71mA$$

$$\hookrightarrow V_{CEQ} = V_{cc} - I_C (R_C + R_E) = 16 - 1.71mA (3.9k + 680)$$

$$V_{CE} = 8.17V$$

(b) Collector to ground voltage \approx

$$V_{cc} - V_C = I_C R_C$$

$$\Rightarrow V_C = V_{cc} - I_C R_C = 16 - (1.71mA \times 3.9k)$$

$$\therefore V_C = 9.33V$$

Emitter to ground voltage \approx

$$V_E = I_E R_E \approx I_C R_E = 1.71mA \times 0.68k\Omega$$

$$\therefore V_E = 1.16V$$

Base to ground voltage \approx

$$V_B = V_{BE} + V_E = 0.7V + 1.16V$$

$$\therefore V_B = 1.86V$$

(c) for $\beta = 150$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{2.05 - 0.7V}{7.94k + (150+1)680\Omega}$$

$$\therefore I_{BQ} = 12.2\text{mA}$$

$$I_{CQ} = \beta I_{BQ} = 150 \times 12.2\text{mA} = 1.83\text{mA} \therefore I_C = 1.83\text{mA}$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E) = 16V - 1.83\text{mA}(3.9k + 680)$$

$$\therefore V_{CEQ} = 7.62\text{V}$$

(d) To plot load line.

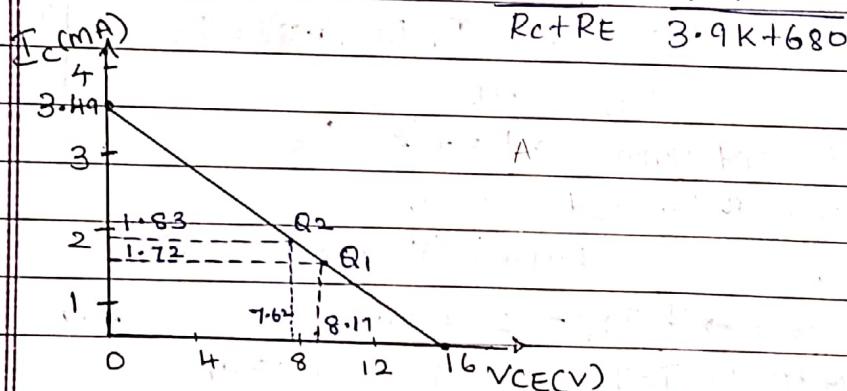
β	I_{BQ}	I_{CQ}	V_{CEQ}
80	21.42mA	1.7mA	8.17V
150	12.2mA	1.83mA	7.62V

Apply KVL to output loop.

$$V_{CC} = V_{CE} + I_C(R_C + R_E)$$

$$\hookrightarrow \text{at } I_C = 0\text{mA} \Rightarrow V_{CE} = V_{CC} = 16V$$

$$\hookrightarrow \text{at } V_{CE} = 0V \Rightarrow I_C = \frac{V_{CC}}{R_C + R_E} = \frac{16V}{3.9k + 680} = 3.49\text{mA}$$



EXAMPLE 3: For the voltage divider bias configuration shown below determine (a) I_C & V_E (b) V_{CC} & V_{CE} (c) V_B & R_1 .

$$\beta = 80.$$

$$V_{CC}$$

$$(a) \hookrightarrow I_C = \beta I_B = 80 \times 40\text{nA} = 3.2\text{mA}$$

$$\sum R_1 \quad \sum 2k\Omega$$

$$\hookrightarrow I_E = I_B + I_C = 40\text{nA} + 3.2\text{mA} = 3.24\text{mA}$$

$$\sum 10V$$

$$\hookrightarrow V_E = I_E R_E = (3.24\text{mA})(1k\Omega) = 3.24V$$

$$V_B \rightarrow 40\text{nA}$$

$$(b) \hookrightarrow V_{CC} = I_C R_C + V_C = (3.2\text{mA})(2k\Omega) + 10V$$

$$10k\Omega \downarrow I_2$$

$$\therefore V_{CC} = 16.4V,$$

$$\sum 1k\Omega$$

$$\hookrightarrow V_{CE} = V_C - V_E = 10V - 3.2V = 6.76V$$

$$(c) \hookrightarrow V_B = V_{BE} + V_E = 0.7V + 3.24V = 3.94V$$

$$\hookrightarrow V_{CC} = I_1 R_1 + V_B$$

$$\rightarrow I_1 = I_B + I_2 \Rightarrow R_1 = V_{CC} - V_B = 16.4V - 3.94V$$

$$\rightarrow I_2 = \frac{V_B}{R_2} = \frac{3.94}{10k} = 0.394\text{mA}$$

$$I_1$$

$$0.434\text{mA}$$

$$\therefore R_1 = 28.7k\Omega$$



BIASING USING A COLLECTOR-TO-BASE FEEDBACK RESISTOR

(*) An improved level of stability can be obtained by introducing a feedback path from collector to Base as shown in fig 4.

(**) fig 4 Shows a simple & effective biasing arrangement suitable for Common-Emitter amplifiers.

(***) The circuit employs a resistor R_B connected between the collector and the Base.

(****) Resistor R_B provides negative feedback, which helps to stabilize the bias point of the BJT.

(*****) The operating point of this circuit is less sensitive to variations in temperature & β when compared to fixed-Bias arrangement.

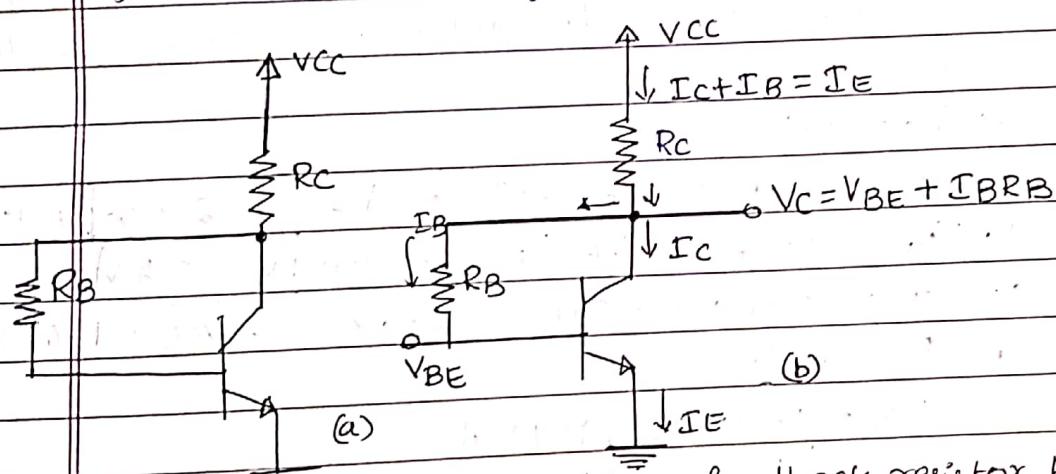


Fig 4 : (a) CE Transistor biased by a feedback resistor R_B .

(b) Analysis of the circuit in (a)

Base-Emitter loop: Apply KVL for the Base-Emitter circuit

$$V_{CC} = I_E R_C + I_B R_B + V_{BE}$$

$$I_C + I_B = I_E$$

$$V_{CC} - V_{BE} = I_E R_C + I_B R_B$$

$$\beta I_B + I_B = I_E$$

$$V_{CC} - V_{BE} = I_E R_C + \frac{I_E R_B}{\beta + 1}$$

$$(1 + \beta) I_B = I_E$$

\therefore Emitter-Bias current,

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B / (\beta + 1)} \quad \rightarrow (4)$$

$$I_B = \frac{I_E}{\beta + 1}$$

(*) This Equation is identical eqn (3) except V_{CC} replace V_{BB} and R_C replaces R_E .

(*) To obtain a value of I_E that is insensitive to variation of β , we select $\frac{R_B}{\beta+1} \ll R_C$

(**) R_B determines the allowable signal swing at the collector.

$$V_{CB} = I_B R_B = \frac{I_E R_B}{\beta+1} \rightarrow (5)$$

(**) Applying KVL to collector-emitter loop, we have

$$V_{CC} = R_C (I_C + I_B) + V_{CE}$$

$$I_C + I_B \approx I_C \quad \& \quad I_E \approx I_C$$

$$\therefore V_{CE} = V_{CC} - I_C R_C \rightarrow (6)$$

EXAMPLE 4: Design the circuit of figure 4 to obtain a dc emitter current of 1mA & to ensure $\pm 2V$ signal swing at the collector i.e. design for $V_{CE} = 2.3V$. Let $V_{CC} = 10V$ and $\beta = 100$.

Soln

$$\hookrightarrow V_C = 4V.$$

$$\hookrightarrow V_{CE} = 2.3V \Rightarrow V_C - V_E = 2.3 \Rightarrow V_E = 4 - 2.3 \Rightarrow V_E = 1.7V$$

$$\hookrightarrow V_{BE} = V_B - V_E \Rightarrow V_B - V_E = 0.7V \Rightarrow V_B = 2.4V$$

$$\hookrightarrow V_{CB} = V_C - V_B = 4 - 2.4 = 1.6V \quad \therefore V_{CB} = 1.6V$$

$$\hookrightarrow I_C = \beta I_B$$

$$I_B = \frac{1mA}{100} = 9.9mA$$

$$\hookrightarrow V_{CB} = I_B R_B \Rightarrow R_B = \frac{V_{CB}}{I_B} = \frac{1.6}{9.9mA} = 162k\Omega$$

$$\therefore R_B = 162k\Omega$$

$$\hookrightarrow I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta+1} \Rightarrow 1mA = \frac{10V - 0.7}{R_C + (\frac{162k}{101})}$$

$$1mA \times R_C + 1.6 = 9.3$$

$$\therefore R_C = 7.7k\Omega$$

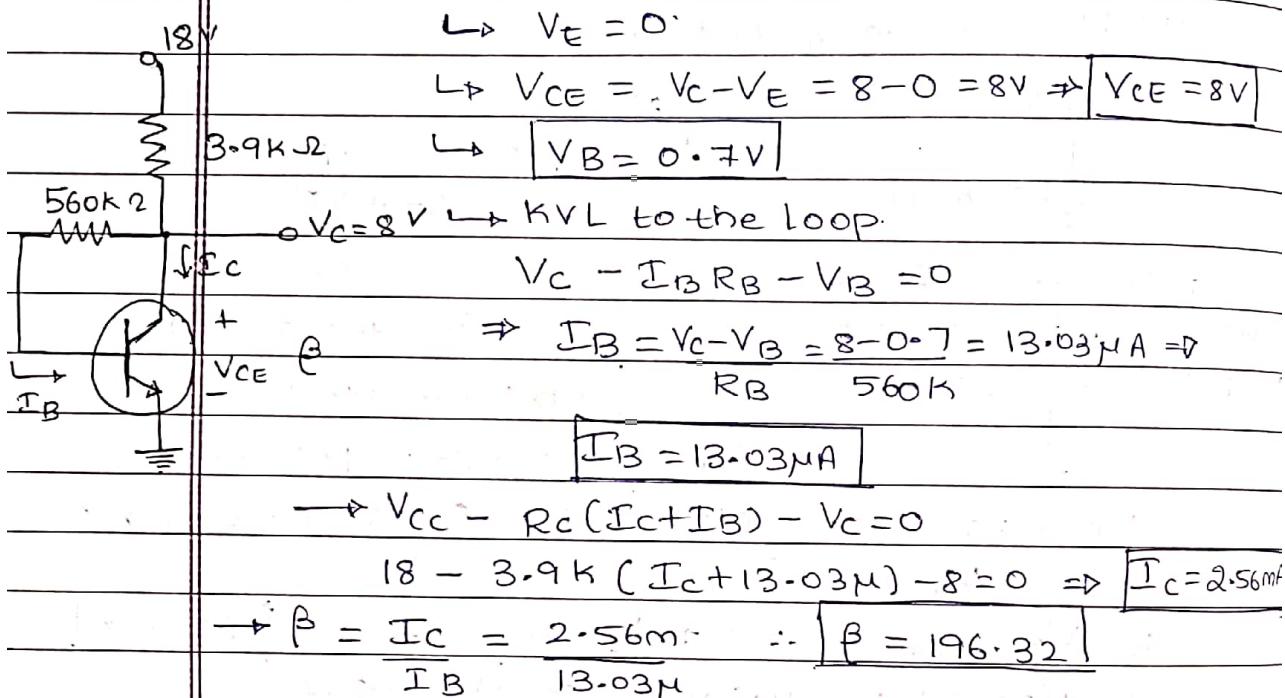
(*) If std 5% resistor values are used, we select

$$R_B = 160k\Omega \text{ and } R_C = 7.5k\Omega$$

This results in $I_E = 1.02mA$ and $V_C = \pm 2.3V$

EXAMPLE 8: Given $V_C = 8V$ for the below network. Determine

- (a) I_B (b) I_C , (c) β , (d) V_{CE}



⇒ SMALL-SIGNAL OPERATION AND MODELS

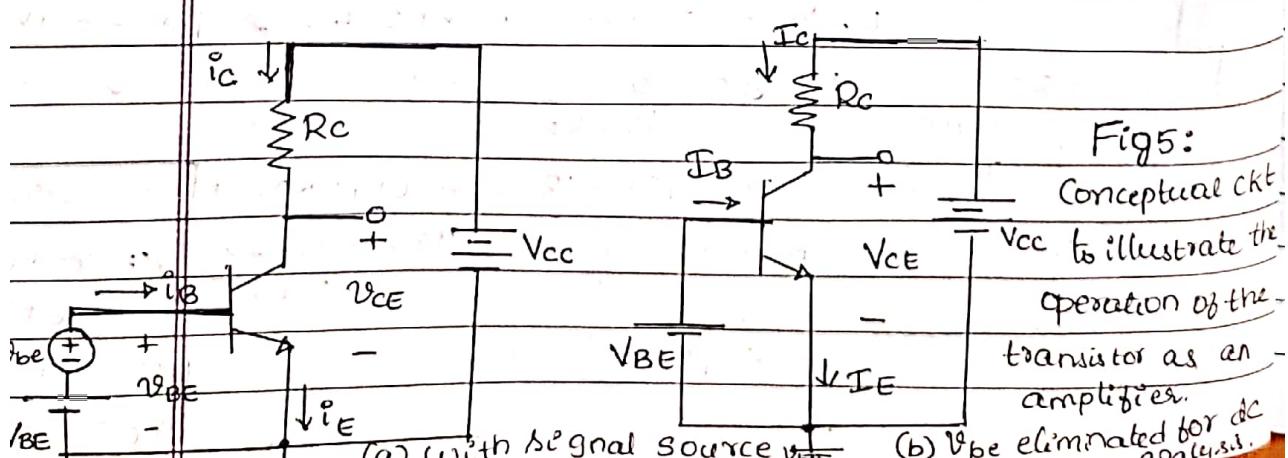
⇒ BJT with Small ac Input signal

(*) Consider the conceptual circuit shown in Fig 5a.

(*) Here the base-Emitter Junction is forward-biased by a dc voltage V_{BE} (battery).

(*) The reverse-bias of the Collector-Base Junction is established by connecting to collector by another power supply V_{CC} through the Resistor, R_C .

(*) The Input signal to be amplified is represented by the voltage source v_{be} that is superimposed on V_{BE} .



(*) The input signal to be amplified is represented by the voltage source v_{be} that is superimposed on V_{BE} .

(*) DC bias conditions by setting signal v_{be} to zero.

(*) The relationships for the dc currents and voltages:

$$I_C = I_S e^{V_{BE}/V_T} \rightarrow \textcircled{7}$$

$$I_E = I_C \rightarrow \textcircled{8}$$

$$I_B = \frac{I_C}{\alpha} \rightarrow \textcircled{9}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C \rightarrow \textcircled{10}$$

$$i_B = I_B + i_b$$

I_B, I_C, I_E - DC currents V_{BE}, V_{CE} - DC voltages

$$i_E = I_E + i_e$$

i_b, i_c, i_e - AC currents V_{be}, V_{ce} - AC voltages

$$i_C = I_C + i_c$$

i_b, i_c, i_e - DC+AC currents V_{BE}, V_{CE} - DC+AC voltages

IIIrd

(*) Small ac signal refers to the input signal (v_{be}) whose magnitude is much smaller than thermal voltage (V_T) i.e. $v_{be} \ll V_T$

Note 1: (*) $V_T = \frac{kT}{q}$ \Rightarrow Voltage produced within the PN junction due to the action of temperature and is called Thermal voltage

$$V_T = 1.38 \times 10^{-23} J/K \times 300K = 26mV. \quad k = 8.617 \times 10^{-5} \text{ eV/K}$$

$$1.609 \times 10^{-19} C \quad k = 1.38 \times 10^{-23} J/K$$

$$\therefore V_T = 26mV$$

$k \rightarrow$ Boltzmann's constant.

(*) The voltage below the base & Emitter is apparently called V_T .

(*) Magnitude of the ac signal applied for amplification must be small so that

\rightarrow The transistor operates in the linear region for the whole cycle of input

\rightarrow The transistor is never driven into saturation or cut-off

(*) On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut-off. This clips the peaks of the input and the amplifier is no longer linear.



Note

The collector current and the Transconductance
Transconductance of an amplifier is defined as
ratio of output current to input voltage fed to amplifier

(*) If the signal v_{be} is applied as shown in fig 5a, the total instantaneous base-emitter voltage V_{BE} becomes

$$v_{BE} = V_{BE} + v_{be} \rightarrow (11) [Total V_{BE} = ac + dc if no signal]$$

(*) Correspondingly, the collector current becomes,

$$\begin{aligned} i_C &= I_S e^{V_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T} \\ &= I_S e^{(V_{BE}/V_T)} e^{(v_{be}/V_T)} \rightarrow (12) \end{aligned}$$

(*) Using eqn (7), yields.

$$i_C = I_S e^{v_{be}/V_T} \rightarrow (13)$$

(*) If $v_{be} \ll V_T$, eqn (13) can be approximated as

NOTE: $e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \dots \infty$

$$i_C \approx I_S \left[1 + \frac{v_{be}}{V_T} \right] \rightarrow (14)$$

(*) This approximation is valid only for $v_{be} < 10mV$
is referred to as the small-signal approximation

(*) Under this approximation, the total collector current
is given by eqn (14) and can be rewritten as.

$i_C = I_C + \frac{I_C v_{be}}{V_T}$	$\rightarrow (15)$
--------------------------------------	--------------------

(*) Thus the collector current is composed of the dc bias value I_C and a signal component i_c ,

$$i_c = \frac{I_C}{V_T} v_{be} \rightarrow (16)$$

(*) Equation (16) relates the signal current in the collector to the corresponding base-Emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be} \rightarrow (17)$$

(*) Where g_m is the transconductance and it is given by

$g_m = \frac{I_C}{V_T}$	$\rightarrow (18)$
-------------------------	--------------------

⇒ Transconductance of the BJT is directly proportional to the collector bias current I_C .

(*) BJTs have relatively high transconductance; [for instance $I_C = 1 \text{ mA}$, $g_m \approx 40 \text{ mA/V}$]

(*) Graphical interpretation for g_m is given in Fig 6. Here g_m is equal to the slope of the $i_C - V_{BE}$ characteristic curve at $i_C = I_C$ (i.e., at the bias point Q). Thus,

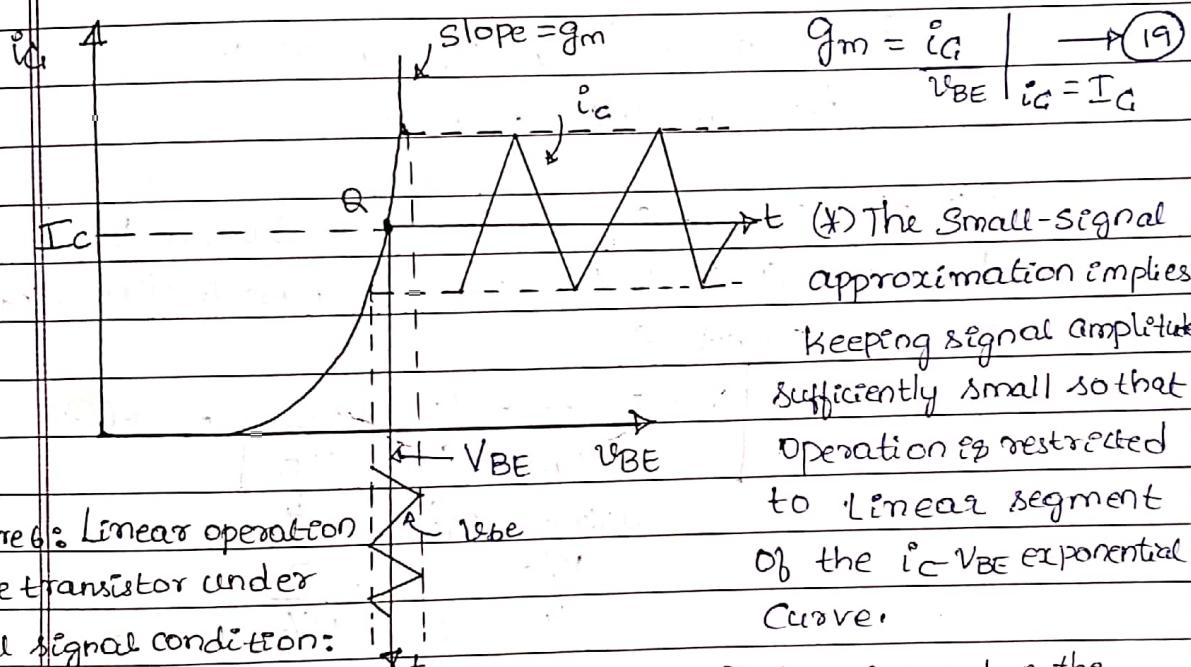


Figure 6: Linear operation of the transistor under small signal condition:

A small signal v_{be} with a triangular waveform is superimposed on the dc voltage V_{be} .

(*) Increasing the signal amplitude will result the collector current having components non-linearly related to v_{be} .

(*) For small signals ($v_{be} \ll V_T$), the transistor behaves as a voltage-controlled current source.

(*) IP port of this controlled source is b/w base & emitter and the OP port is between collector and emitter.

(*) Transconductance of the controlled source is g_m and output resistance is 0.

(*) Collector voltage has no effect on collector current in Active mode.

(*) Practical BJTs have finite OP resistance because of Early effect.

→ The Base current and the Input Resistance at the Base

(*) The total base current i_B using eqn (15)

$$\frac{i_B}{\alpha} = \frac{i_C}{\alpha} + \frac{1}{\alpha} \cdot \frac{I_C v_{be}}{V_T} \quad \rightarrow (20)$$

thus, $i_B = I_B + i_b$

(*) Signal component i_b of base current is given by

$$i_b = \frac{1}{\beta} \cdot \frac{I_C v_{be}}{V_T} \quad \rightarrow (21)$$

(*) Substituting I_C/V_T by g_m gives

$$i_b = \frac{g_m v_{be}}{\alpha} \quad \rightarrow (22)$$

(*) The small-signal input resistance between base and emitter, looking into base is denoted by r_π and defined as

$$r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{V_T}{I_B} \quad \rightarrow (23)$$

using eqn (22)

$$\frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{\beta}{I_C/V_T} = \frac{V_T}{I_C/\beta} = \frac{V_I}{I_B}$$

→ The Emitter Current & Input resistance at the Emitter.

(*) The total Emitter current i_E can be determined from

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_a}{\alpha}$$

(*) Thus $i_E = I_E + i_e \quad \rightarrow (24)$

(*) The signal current i_e is given by

$$i_e = \frac{i_C}{\alpha} = \frac{I_C v_{be}}{\alpha V_T} = \frac{I_E v_{be}}{V_T} \quad \rightarrow (25)$$

(*) The small-signal resistance b/w base & emitter looking into emitter is denoted by r_e and it can be defined as

$$r_e \equiv \frac{v_{be}}{i_e} = \frac{V_T}{I_E} \approx \alpha \quad \rightarrow (26)$$

using eqn (25)

$$\frac{v_{be}}{i_e} = \frac{V_I}{I_E} = \frac{V_I \times \alpha}{I_C} = \frac{\alpha}{g_m} \quad \therefore \frac{I_C}{V_T} = g_m$$

(*) The relationship between γ_{π} and r_e can be found by combining eqns 23 and 26 as

$$V_{be} = i_b \gamma_{\pi} = i_e r_e$$

$$(*) \text{ thus } \gamma_{\pi} = \frac{i_e}{i_b} r_e \rightarrow 27$$

$$(*) \text{ which yields } \gamma_{\pi} = (\beta + 1) r_e \rightarrow 28$$

$$\frac{I_c}{I_B} = \beta$$

$$\frac{I_c + I_B}{I_B} = \beta + 1$$

$$\Rightarrow \frac{I_E}{I_B} = \beta + 1$$

EXAMPLE 9: A BJT having $\beta = 100$ is biased at a dc collector current of 1mA. find the value of g_m , r_e and γ_{π} at bias point

$$\text{soln} \quad \hookrightarrow g_m = \frac{I_c}{V_T} = \frac{1m}{25m} = 40 \text{ mA/V}$$

$$\hookrightarrow I_B = \frac{I_c}{\beta} = \frac{1mA}{100} = 10 \mu A$$

$$\hookrightarrow \gamma_{\pi} = \frac{V_T}{I_B} = \frac{25mV}{10 \mu A} = 2.5 k\Omega$$

$$\hookrightarrow r_e = \gamma_{\pi} = \frac{2.5 k\Omega}{\beta + 1} = 25 \Omega$$

\rightarrow Voltage gain

(*) Before we have established that the transistor senses the base-emitter voltage/signal V_{be} and causes proportional current $g_m V_{be}$ to flow in collector leading high impedance level

(**) Thus, transistor acts as a "voltage-controlled current source".

(**) To obtain an output voltage signal, this current must flow through a resistor.

(*) Then the collector voltage V_C will be

$$\begin{aligned} V_C &= V_{cc} - i_c R_C \\ &= V_{cc} - (I_c + i_c) R_C \\ &= (V_{cc} - I_c R_C) - i_c R_C \\ &= V_C - i_c R_C \end{aligned} \rightarrow 29$$

(*) Here $V_C \rightarrow$ dc bias voltage at the collector and the signal voltage is given by

$$V_C = -i_c R_C = -g_m V_{be} R_C$$

using equation 17

$$V_C = (-g_m R_C) V_{be} \rightarrow 30$$

(*) Thus, the voltage gain of this amplifier A_v is

$$A_v = \frac{V_c}{V_{be}} = -g_m R_C \rightarrow (31)$$

(*) Thus g_m is directly proportional to the collector bias current, the gain will be as stable as the collector bias current is made.

(*) Substituting for g_m from eqn (18)

$$A_v = \frac{-I_C R_C}{V_T} \rightarrow (32)$$

EXAMPLE: In the circuit of fig 5a, V_{BE} is adjusted to yield a dc collector current of 1mA. Let $V_{CC} = 15V$, $R_C = 10k\Omega$ and $\beta = 100$. Find the voltage gain. If $V_{be} = 0.005 \sin \omega t$ find $V_C(t)$ and $i_B(t)$.

Solution:

Given Data:

$$V_{CC} = 15V \quad \hookrightarrow A_v = -\frac{I_C R_C}{V_T} = -\frac{1m \times 10k}{25m} = -400 \text{ V/V}$$

$$I_C = 1mA$$

$$R_C = 10k\Omega \quad \hookrightarrow V_C = V_C - i_C R_C \rightarrow @$$

$$\beta = 100 \quad \text{④ } V_C = V_{CC} - I_C R_C = 15 - 1m \times 10k$$

$$V_{be} = 0.005 \sin \omega t \quad \boxed{V_C = 5V} \quad \text{④ } i_C = I_C V_{be} = \frac{1m \times 0.005}{25m}$$

$$V_{BE} = 0.7V \quad @ \Rightarrow \boxed{V_C = 5 - 2 \sin \omega t \frac{V_T}{mV}}$$

$$\hookrightarrow i_B = \frac{I_C}{\beta} + \frac{I_C V_{be}}{V_T} = \frac{1m}{100} + \frac{1m \times 0.005 \sin \omega t}{25m \times 100}$$

$$\therefore \boxed{i_B = 10 + 2 \sin \omega t \mu A}$$

\rightarrow Separating the Signal and the DC Quantities

(*) The above analysis indicates that every current and voltage in the amplifier circuit is composed of two components: a dc component and a signal component.

(*) For instance, $V_{BE} = V_{BE} + v_{be}$, $I_C = I_C + i_C^s + i_C^d$.

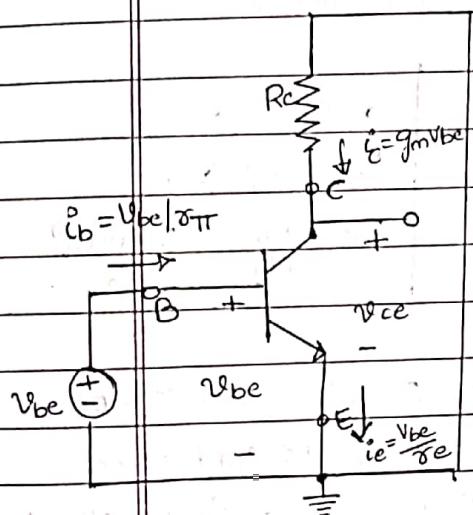
① The dc components are determined from the dc circuit given in Fig 5b, and from eqn (7) to eqn (10).

② On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources as shown in fig 6.

(*) Since the voltage of an ideal dc source/supply does not change, the signal voltage across it will be zero.

DC supply $\Rightarrow V_{CC}$ and V_{BE} are replaced with short circuits.

(*) If the circuit contained ideal DC current sources, these would have been replaced by open circuits.



(*) Fig 6 shows the various signal currents and voltages; it is not an actual amplifier circuit since the dc bias circuits is not shown.

(*) Fig 6 indicates the expressions for the current increments (i_c , i_b & i_e) obtained when a small signal v_{be} is applied.

Figures 6: The amplifier ckt of fig 5a,
With dc Sources (V_{BE} & V_{CC}) eliminated (sc)

(*) These relationships can be represented by a circuit.

(*) Such a circuit should have 3 terminals - C, B & E & should yield the same terminal currents indicated in Fig 6.

(*) The resulting ckt is then equivalent to the transistor as far as small-signal operation is concerned & thus it can be considered an equivalent small-signal circuit model.

The Hybrid- π Model.

(*) An equivalent circuit model for the BJT is shown in fig 7a.

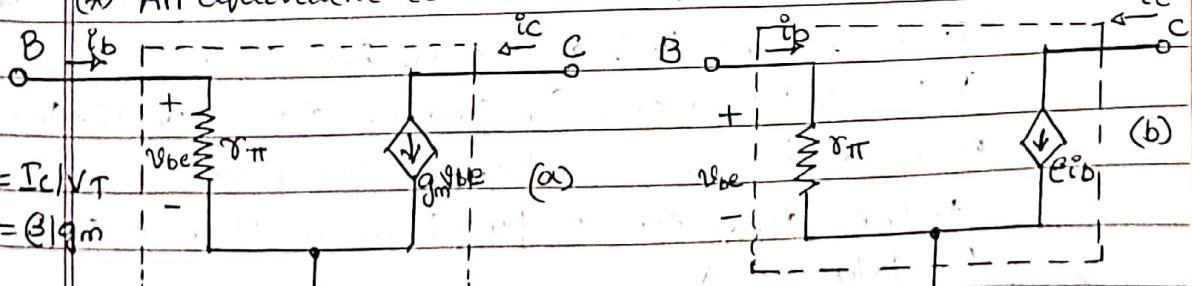


Figure 7: Simplified hybrid π model for small signal operation of the BJT
(a) BJT as VCCS (transconductance amp)
(b) BJT as CCCS (current amp) O E

(*) Fig 7a shows the BJT as a voltage-controlled current source & explicitly includes the I_{L} resistance looking into base, γ_{π} .

(*) This model yields, $i_c = g_m v_{\text{be}}$ and $i_b = v_{\text{be}}/\gamma_{\pi}$.

(*) The model also yields the correct expression for i_e .

(*) At the Emitter node,

$$i_e = \frac{v_{\text{be}}}{\gamma_{\pi}} + g_m v_{\text{be}} = \frac{v_{\text{be}}}{\gamma_{\pi}} (1 + g_m \gamma_{\pi})$$

$$= \frac{v_{\text{be}}}{\gamma_{\pi}} (1 + \beta) = \frac{v_{\text{be}}}{\left(\frac{\gamma_{\pi}}{1+\beta}\right)}$$

$i_e = \frac{v_{\text{be}}}{\gamma_e}$
--

$$g_m \gamma_{\pi} = \beta$$

from eqn 23

$$\gamma_e = \frac{\gamma_{\pi}}{\beta+1} \quad \text{from eqn 28}$$

(*) A slightly different equivalent circuit model can be obtained by expressing the current of the controlled source ($g_m v_{\text{be}}$) in terms of base current i_b as follows:

$$g_m v_{\text{be}} = g_m (i_b \gamma_{\pi}) \\ = (g_m \gamma_{\pi}) i_b$$

$g_m v_{\text{be}} = \beta i_b$

$$\gamma_{\pi} = \frac{v_{\text{be}}}{i_b} \quad \text{from eqn 23}$$

$$\therefore v_{\text{be}} = \gamma_{\pi} i_b$$

$$\text{Also } g_m \gamma_{\pi} = \beta \quad \text{from 23}$$

(*) This results in the alternative

equivalent circuit model shown in Fig 7b.

(*) Here transistor is represented as a current-controlled current source, with control current being i_b .

(*) The two models of Fig 7 are the simplified versions of the hybrid- π model. This is the most widely used model for the BJT.

(*) The small-signal equivalent circuits of Fig 7 model the operation of the BJT at a given bias point.

(*) Model parameters g_m and γ_{π} depend on the value of the dc bias current I_c as indicated in Fig 7.

(*) They apply even to pnp transistor with no change of polarities.

EXAMPLE 1: Determine the voltage gain of the fig below.

Assume $\beta = 100$.

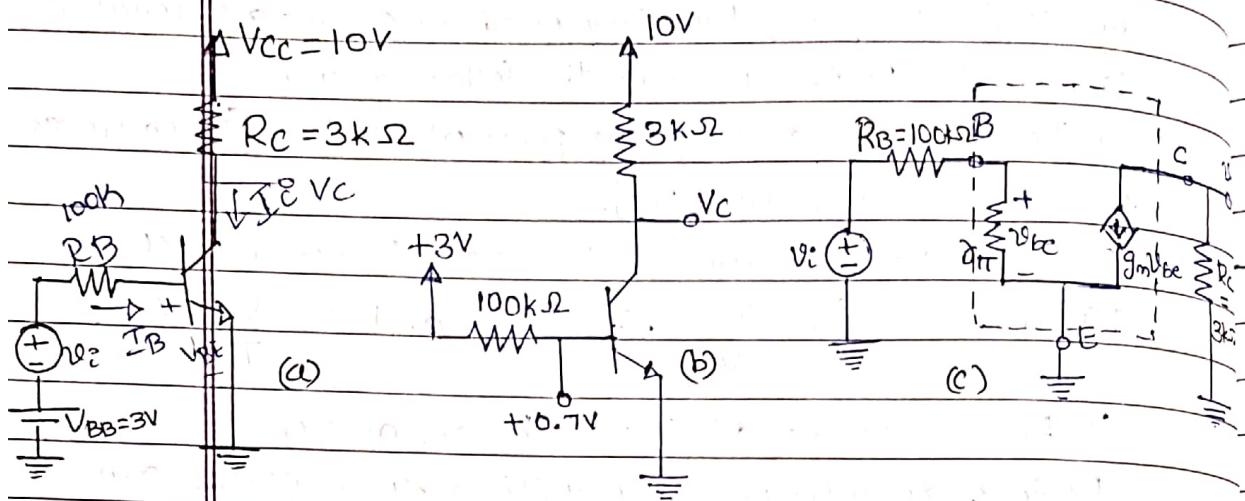


Figure: (a) Example circuit (b) dc analysis (c) Small-signal model.

(i) Determining the quiescent operating point.

$$\rightarrow \text{DC base current } I_B, I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3 - 0.7}{100k} = 0.023\text{mA}$$

$$\rightarrow \text{DC collector current}, I_C = \beta I_B = 100 \times 0.023 \times 10^{-3} = 2.3\text{mA}$$

$$\rightarrow \text{DC voltage at collector}, V_C = V_{CC} - I_C R_C$$

$$= 10 - 2.3 \times 10^{-3} \times 3 \times 10^3$$

$$V_C = 3.1\text{V}$$

$\therefore V_B < V_C \Rightarrow$ The transistor will be operating in Active mode

(ii) Determining the small-signal model parameters:

$$\rightarrow \gamma_e = \frac{V_T}{I_E} = \frac{25\text{mV}}{(2.3/0.99)\text{mA}} = 10.8 \text{ mV} \quad (0) \quad \gamma_e = \frac{\alpha}{g_m} = \frac{1}{92} = 10.8$$

$$\rightarrow g_m = \frac{I_C}{V_T} = \frac{2.3\text{mA}}{25\text{mV}} = 92\text{ mA/V}$$

$$\rightarrow \gamma_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09\text{ k}\Omega \quad (0) \quad \gamma_\pi = \frac{V_T}{I_B} = \frac{25\text{mV}}{0.99\text{mA}} = 1.0$$

(iii) Analysis of the equivalent circuit (c)

$$\rightarrow v_{be} = \frac{v_i \gamma_\pi}{\gamma_\pi + R_{bb}} = \frac{v_i 1.09 \times 10^3}{1.09 \times 10^3 + 100 \times 10^3} = 0.011 v_i$$

→ The output voltage v_o is given by

$$v_o = -g_m v_{be} R_c$$

$$= -92 \times 0.011 v_i \times 3 = -3.04 v_i$$

→ Thus, the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -3.04 \text{ V/V}$$

-ve sign indicates
Phase reversal.

→ BIASING IN MOS AMPLIFIER CIRCUITS

- (*) An essential step in the design of a MOSFET Amplifier circuit is the establishment of an appropriate dc operating point for the transistor.
- (*) This step is known as "Biasing" or "Bias design".
- (*) An appropriate dc operating point is characterized by
 - ↳ a stable and predictable dc drain current I_D and
 - ↳ by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input-signal levels.

① → Biasing by Fixing V_{GS} .

- (*) For biasing a MOSFET, the gate-to-source voltage V_{GS} is fixed to provide the desired I_D .
- (*) V_{GS} can be derived from the power supply voltage V_{DD} , through the use of an appropriate voltage divider.
- (*) Alternatively, it can be derived from another suitable reference voltage that might be available in the system.

↳ Fixing V_{GS} is not a good approach for biasing a MOSFET.

$$(*) \text{ Since, } I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \quad \rightarrow ①$$

(*) Threshold voltage, V_t , the oxide capacitance C_{ox} and the transistor aspect ratio W/L vary widely among devices.

(*) Furthermore, both V_t & μ_n depend on temperature. Hence if we fix the value of V_{GS} , the drain current I_D becomes very much temperature dependent.

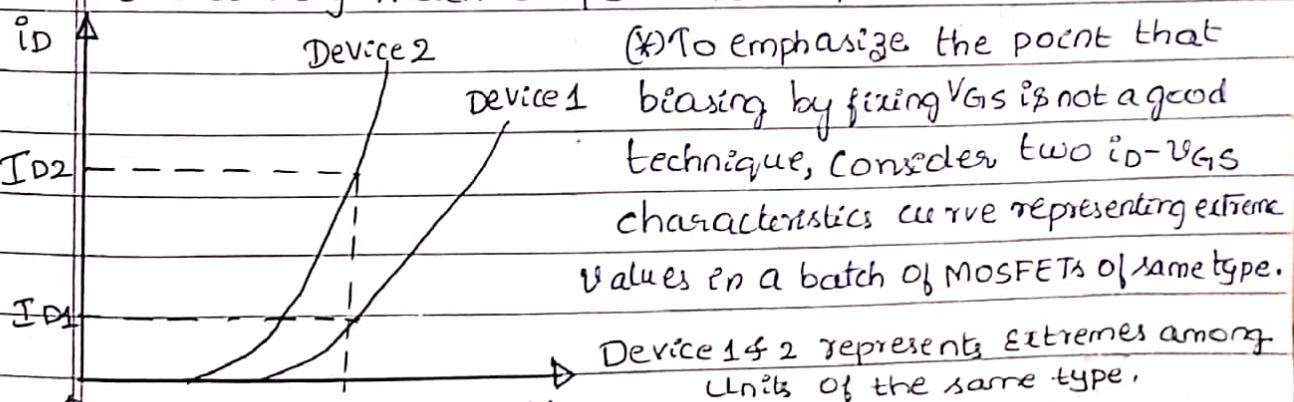


Fig 1: Fixing V_{GS} can result in a large variability in the value of I_D

(*) observe that for fixed value of V_{GS} , the resultant spread in the values of the drain current can be substantial.

② → Biasing by fixing V_G & connecting a Resistance in the Source.

(*) An Excellent biasing technique for discrete MOSFET Circuits consists of fixing the dc voltage at the gate, V_G & connecting a resistance in source lead as shown in fig 2a.

(*) For the circuit,

$$V_G = V_{GS} + R_S I_D \rightarrow ②$$

↳ V_G is much greater than V_{GS} .

↳ I_D is determined by the values of V_G and R_S .

↳ Even if V_G is not much larger than V_{GS} , resistor R_S provides negative feedback which stabilize the value of the bias current I_D .

↳ Suppose when I_D increases. This in turn decrease V_{GS}

(eqn ②) Since V_G is constant. This in turn results in a decrease in I_D , a change opposite to initially assumed.

(*) Thus the action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name "degeneration Resistance".

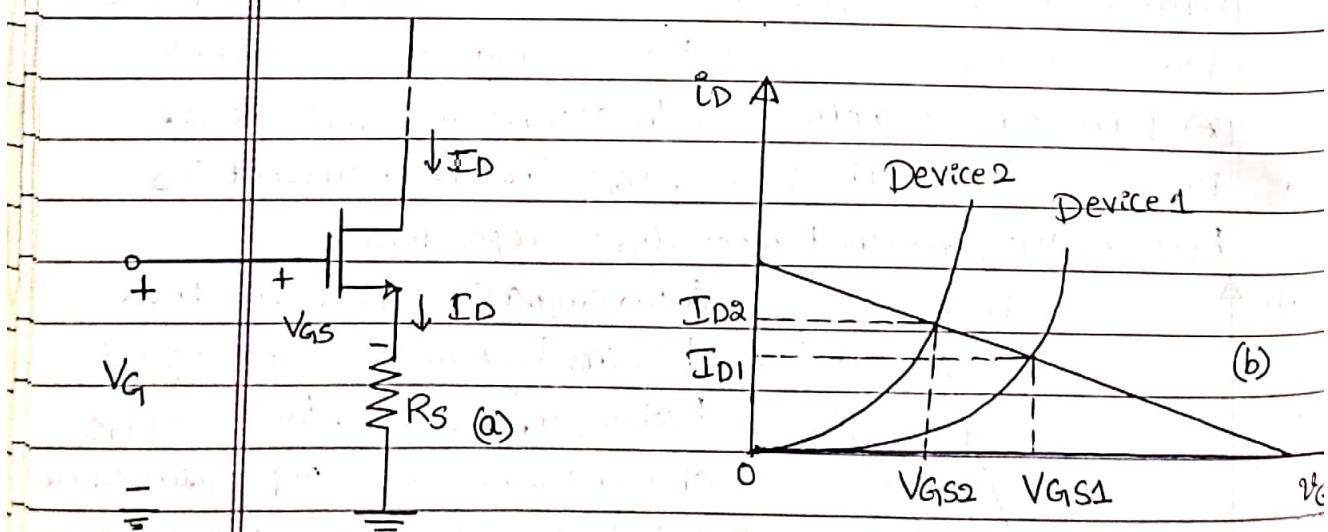
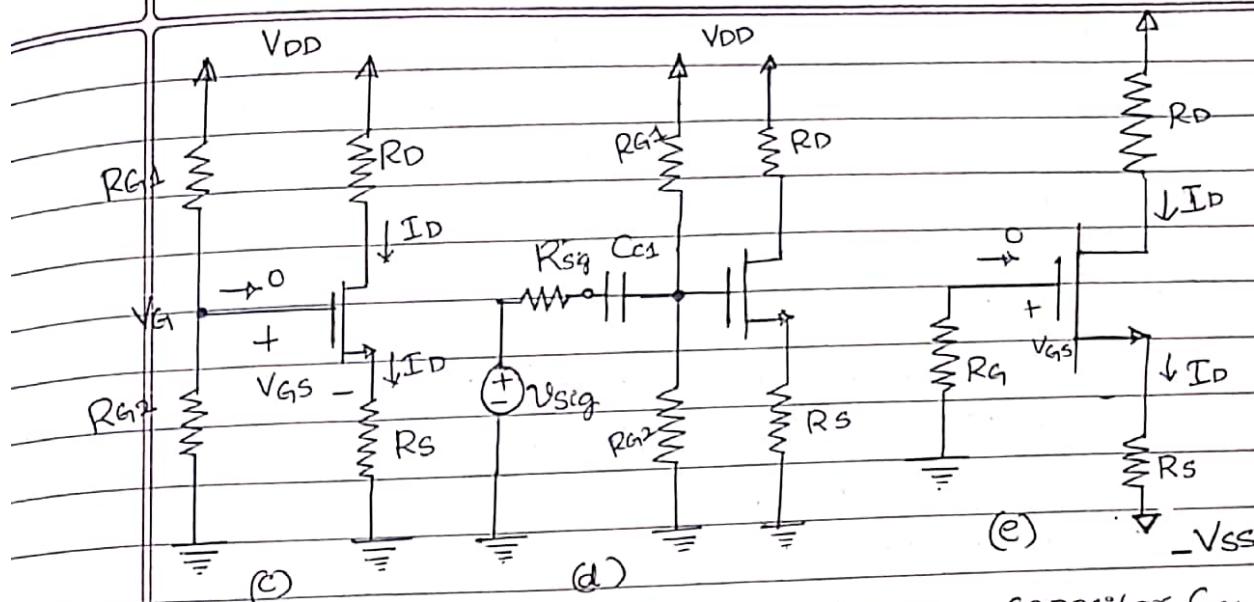


Figure 2: Biasing using fixed V_G and R_S (a) Basic arrangement

(b) reduced variability in I_D (c) practical implementation using



(d) Coupling of a signal source to the gate using a capacitor C_{S1}
 (e) Practical Implementation Using two supplies

- (b) (i) Fig Qb) show the I_D - V_{GS} characteristics for two devices that represent the extremes of a batch of MOSFETs.

(ii) Straight line represents the constraints imposed by the bias circuit [namely eqn ②].

(iii) The intersection of the straight line with I_D - V_{GS} characteristics curve provides the coordinates (I_D & V_{GS}) of bias point.

(iv) comparatively, the variability obtained in I_D is much smaller. Variability decreases as V_G & R_S are made larger. [providing a bias line i.e less steep].

(c) (i) The circuit in fig qc, utilizes one power supply, V_{DD} & derive V_G through a voltage divider (R_{G1} & R_{G2}).

(ii) Since $I_G = 0$, R_{G1} & R_{G2} can be selected very large ($M \gg 1$) allowing the MOSFET to present large input resistance to a signal source that may be connected to the gate through a coupling capacitor as shown in fig qc.

(d) (i) $C_{ci} \rightarrow$ blocks dc & allows us to couple the signal v_{sig} to the amplifier input without disturbing the MOSFET dc bias point.

(ii) The value of C_{ci} should be large so that it approximates as a short-circuit at all signal frequencies of interest.

(*) In the circuit of fig 2c, resistor R_D is selected to be as large as possible to obtain high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

(e) (*) When 2 power supplies are available, the simpler bias arrangement of fig 2e can be utilized.

(*) This Ckt is the implementation of eq 2 with V_G replaced by V_{SS} .

(*) R_G establishes a dc ground at the gate & presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

EXAMPLE 1: Design the circuit of Fig 2c to establish a dc drain current $I_D = 0.5\text{mA}$. The MOSFET is specified to have $V_T = 1\text{V}$ and $k_n' W/L = 1\text{mA/V}^2$. Use power supply, $V_{DD} = 15\text{V}$. Calculate the % change in the value of I_D obtained when MOSFET is replaced with another unit having the same $k_n' W/L$ but $V_T = 1.5\text{V}$

Solution
(a) (*) As a rule of thumb for designing this classical biasing ckt, we choose R_D & R_S to provide $\frac{1}{3}$ power supply voltage V_{DD} as a drop across each of R_D , transistor (i.e V_{DS}) and R_S .

(*) Thus for $V_{DD} = 15\text{V}$,

$$V_D = 10\text{V} \text{ & } V_S = 5\text{V} \text{ is chosen.}$$

→ To find values of R_D & R_S

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5\text{m}} = 10\text{k}\Omega$$

$$\therefore V_{DD} = 15\text{V} \quad I_D = 0.5\text{m}$$

$$R_S = \frac{V_S}{I_S} = \frac{5}{0.5\text{m}} = 10\text{k}\Omega$$

$$\therefore V_D = +10\text{V} \quad \rightarrow V_{GS} \text{ can be determined as follows}$$

$$(*) I_D = \frac{1}{2} k_n' \left(\frac{W}{L} \right) V_{GS}^2$$

$$\therefore 0.5\text{m} = \frac{1}{2} \times 1 \times 1 \text{m} \times V_{GS}^2$$

$$R_S = 10\text{k}\Omega \quad \therefore V_{GS} = 1\text{V}$$

$$(*) V_{GS} = V_T + V_{ov} = 1 + 1 = 2\text{V}$$

(*) Since $V_S = +5V$, V_G must be

$$V_G = V_S + V_{GS} = 5 + 2 = 7V \Rightarrow V_G = 7V$$

(*) To establish this voltage at the gate, select $R_{G1} = 8M\Omega$ and $R_{G2} = 7M\Omega$.

$$\text{Given } V_{DD} R_2 = V_B \Rightarrow 15R_2 = 7R_1 + 7R_2 \Rightarrow R_2 = \frac{7}{8} R_1$$

$$\text{Hence } R_2 = 0.875 R_1$$

$$(*) \text{ If } R_1 = 8M\Omega \text{ then } R_2 = 7M\Omega$$

(b) If nMOS transistor is replaced by another having $V_T = 1.5V$ new I_D is determined as.

$$\hookrightarrow I_D = 0.5m \times (V_{GS} - 1.5)^2 \rightarrow (a)$$

$$\hookrightarrow V_G = V_{GS} + I_D R_S \Rightarrow 7 = V_{GS} + 10I_D \rightarrow (b)$$

$$7 = V_{GS} + 5(V_{GS} - V_T)^2$$

$$7 = V_{GS} + 5(V_{GS}^2 + V_T^2 - 2V_{GS}V_T)$$

$$7 = V_{GS} + 5V_{GS}^2 + 11.25 - 15V_{GS}$$

$$5V_{GS}^2 - 14V_{GS} + 4.25 = 0$$

$$\therefore V_{GS} = 2.45 \text{ or } 0.35V$$

$$\hookrightarrow I_D = \frac{7 - V_{GS}}{10} = \frac{7 - 2.45}{10} = 0.455 \text{ mA}$$

$$\hookrightarrow \text{Change in } I_D \text{ is } \Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

$$\hookrightarrow \text{Percentage change } -0.045 \times 100 / 0.5 = -9\% \text{ change}$$

③ → Biasing Using a Drain-to-Gate feedback Resistor,

(*) A simple and effective biasing arrangement utilizing a feedback resistor connected b/w the drain & gate is shown in fig 3. Large Feedback resistance R_F ($M\Omega$) range forces the

$\uparrow V_{DD}$ dc V_G at the gate be equal to drain
(because $I_G = 0$)

$$(*) \text{ thus } V_{GS} = V_{DS} = V_{DD} - I_D R_D \rightarrow (3)$$

which can be rewritten as

$$V_{DD} = V_{GS} + I_D R_D \rightarrow (4)$$

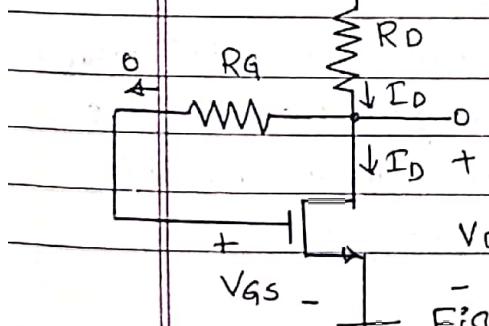


Figure 3: Biasing using large drain-to-gate feedback

- (*) If I_D increases then (eqⁿ indicates) V_{GS} must decrease. The decrease in V_{GS} in turn decrease I_D , a change opposite to originally assumed.
- (*) Thus the -ve feedback or degeneration provided by R_G keep the value of I_D as constant as possible.
- (*) The circuit of Fig 3 can be utilized as a CS amplifier by applying the I_{Op} voltage signal to the gate via a coupling capacitor so as not to disturb dc bias conditions already established.
- (*) The amplified o/p signal at the drain can be coupled to another part of the circuit again via a capacitor.

EXAMPLE 2: Design the circuit in Fig 3 to operate at a dc drain current of 0.5mA . Assume $V_{DD} = 5\text{V}$, $k_n \frac{W}{L} = 1\text{mA/V}^2$, $V_T = 1\text{V}$ and $\lambda = 0$. Use standard 5% resistance value for R_D & give the actual values obtained for I_D & V_D .

Solution:

$$\hookrightarrow I_D = \frac{1}{2} k_n \left(\frac{W}{L} \right) V_{DD}^2$$

$$0.5\text{m} = 0.5 V_{DD}^2 \Rightarrow V_{DD}^2 = 1\text{mV}$$

$$\hookrightarrow V_{GS} = V_{DD} + V_T = 1 + 1 = 2\text{V} \quad \therefore V_{GS} = 2\text{V}$$

$$\hookrightarrow V_{GS} = V_{DD} - I_D R_D$$

$$\hookrightarrow R_D = \frac{V_{DD} - V_{GS}}{I_D} = \frac{5 - 2}{0.5\text{m}} = 6.2\text{k}\Omega = 6.2\text{k}\Omega$$

$$\hookrightarrow I_D = \frac{V_{DD} - V_{GS}}{R_D} = \frac{5 - 2}{6.2\text{k}} = 0.49\text{mA}$$

$$\hookrightarrow V_{DD} - V_D = I_D R_D \quad \therefore V_D = V_{DD} - I_D R_D$$

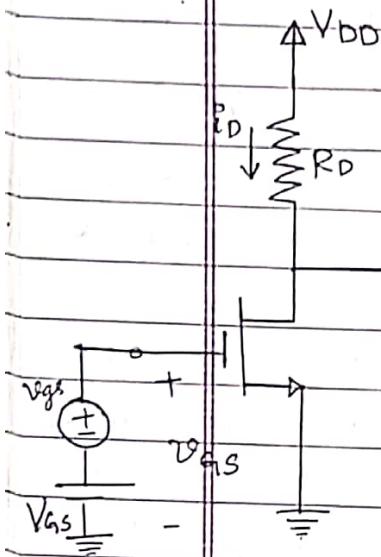
$$V_D = 5 - (0.49\text{m})(6.2\text{k})$$

$$\therefore V_D = 1.96\text{V}$$

⇒ SMALL-SIGNAL OPERATION AND MODELS

(*) Linear amplification can be obtained by biasing the MOSFET to operate in the saturation region and by keeping the input signal small.

(*) Consider the common-source amplifier circuit shown in figure 5.



(*) Here MOS transistor is biased by applying a dc voltage V_{GS} .

(*) The input signal to be amplified v_{GS} is superimposed on the dc bias voltage V_{GS} .

(*) The output voltage is taken at the drain

Figure 5: Conceptual circuit to study the operation of a MOSFET as a small-signal amplifier.

→ THE DC BIAS POINT

(*) The dc bias current I_D is found by setting the signal v_{GS} to zero, thus

$$I_D = \frac{1}{2} k_n' W \left(V_{GS} - V_t \right)^2 \rightarrow ⑨$$

(*) Channel length modulation is neglected ($\lambda = 0$).

(*) The dc voltage at the drain, V_D or V_o will be

$$V_D = V_{DD} - I_D R_D \rightarrow ⑩$$

(*) To ensure saturation region operation, we must

$$V_D > V_{GS} - V_t \rightarrow ⑪$$

(*) Since the total voltage at the drain will have a signal component superimposed on V_D .

(*) V_D has to be sufficiently greater than $(V_{GS} - V_t)$ to allow required signal swing.

→ THE SIGNAL CURRENT IN THE DRAIN TERMINAL

(*) The total instantaneous gate-to-source voltage will be.

$$v_{GS} = V_{GS} + v_{gs} \quad \rightarrow (12)$$

(*) Resulting in a total instantaneous drain current i_D ,

$$i_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2} k_n \frac{W}{L} [(V_{GS} - V_t) + v_{gs}]^2$$

$$i_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2 + \frac{1}{2} k_n \frac{W}{L} v_{gs}^2 + k_n \frac{W}{L} (V_{GS} - V_t) v_{gs} \quad \rightarrow (13)$$

(*) Consider the RHS of eqⁿ (13)

↳ First term can be recognized as the dc bias current I_D .

↳ Second term represents a current component that is proportional to the square of the input signal.

↳ Third term represents a current component that is directly proportional to the input signal v_{gs}

(*) Second term is undesirable because it represents non-linear distortion.

(*) To reduce the non-linear distortion introduced by MOSFE the input signal should be kept small so that

$$\frac{1}{2} k_n \frac{W}{L} v_{gs}^2 \ll k_n \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

(*) resulting in, $v_{gs} \ll 2(V_{GS} - V_t) \rightarrow (14)$

(*) equivalently, $v_{gs} \ll 2V_{ov} \rightarrow (15)$

(*) where V_{ov} is the overdrive Voltage at which transistor is operating.

(*) If this small-signal condition is satisfied, we neglect the 2nd term of eqⁿ (13) and express i_D as

$$i_D = I_D + i_d$$

$$\text{where } i_d = k_n \frac{W}{L} (V_{GS} - V_t) v_{gs} \rightarrow (16)$$

(*) The parameter that relates i_d & v_{gs} is the MOSFET transconductance g_m ,

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n \frac{W}{L} (V_{GS} - V_T) \rightarrow (17)$$

(*) In terms of the overdrive voltage V_{ov} ,

$$g_m = k_n \frac{W}{L} V_{ov} \rightarrow (18)$$

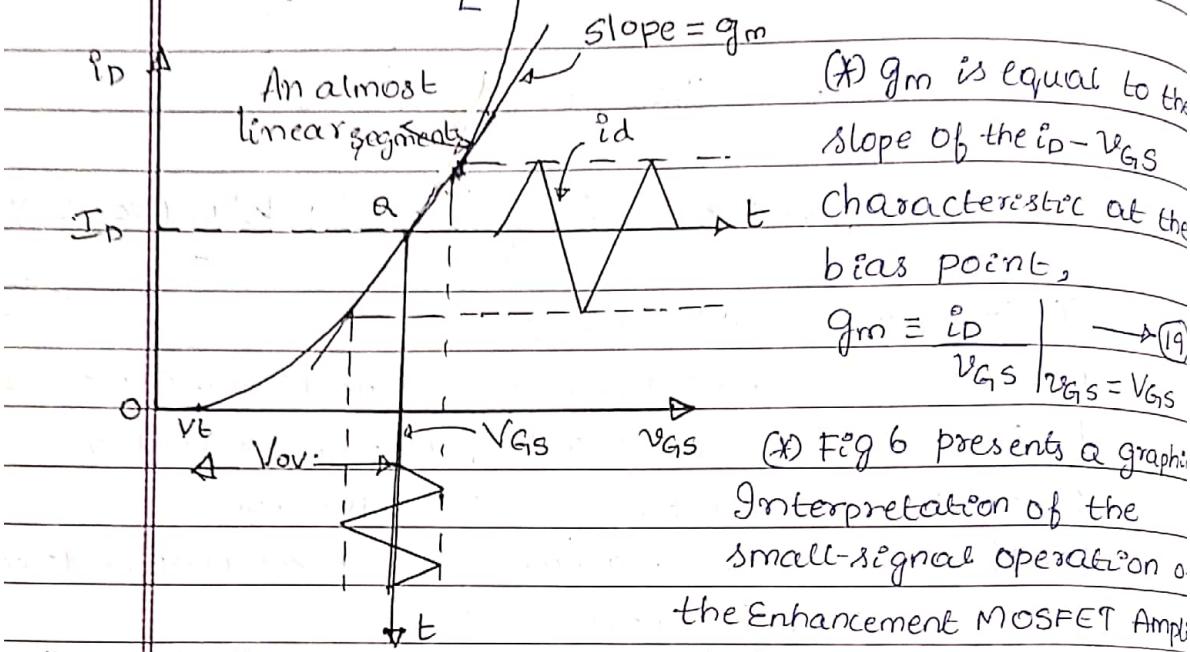


Figure 6: Small-signal operation of the Enhancement MOSFET Amplifier

→ THE VOLTAGE GAIN

(*) The instantaneous drain voltage v_D is [from fig 5]

$$v_D = V_{DD} - i_D R_D$$

(*) Under small-signal condition, we have

$$v_D = V_{DD} - R_D (I_D + i_d)$$

(*) Which can be rewritten as

$$v_D = V_{DD} - I_D R_D - i_d R_D$$

$$v_D = V_D - i_d R_D$$

(*) Thus, the signal component of the drain voltage is

$$v_d = -i_d R_D = -g_m v_{gs} R_D \rightarrow (20)$$

(*) The voltage gain is given by

$$Av \equiv \frac{v_d}{v_{gs}} = -g_m R_D \rightarrow (21)$$

(*) -ve sign indicates the output signal v_d is 180°

out of phase wrt input signal v_{gs} .

(*) This is illustrated in figure 7, which shows V_{GS} and V_D .

(*) The o/p signal is assumed to have a triangular waveform with an amplitude much smaller than $2(V_{GS} - V_t)$, the small signal

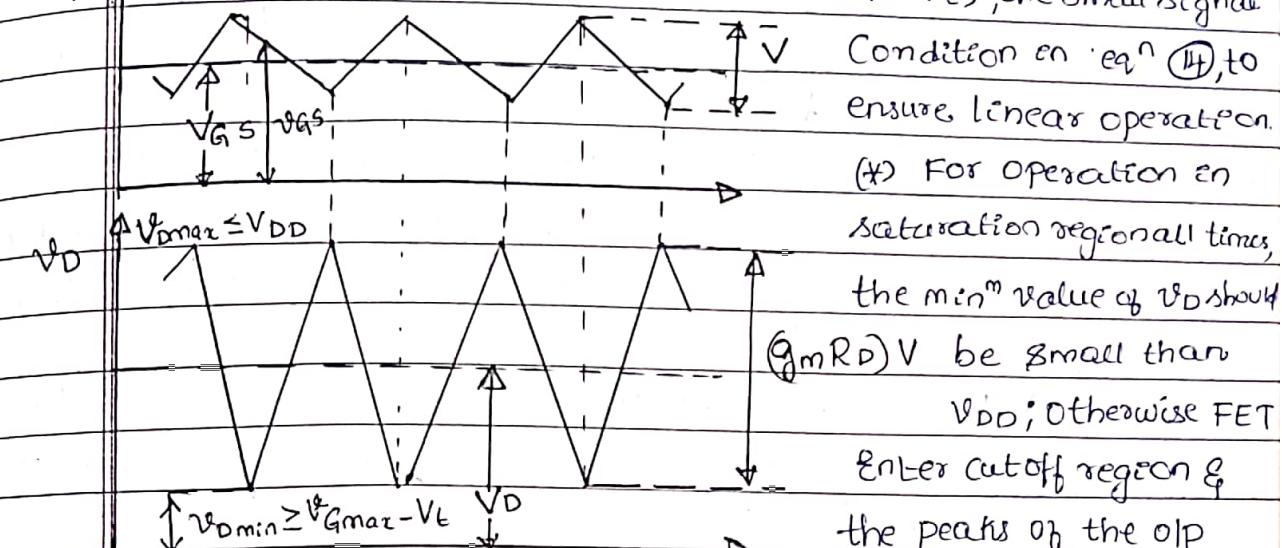


Figure 7: Total Instantaneous voltages V_{GS} and V_O for the circuit of fig 5. Signal will be clipped off.

→ SEPARATING THE DC ANALYSIS AND THE SIGNAL ANALYSIS

(*) Under small-signal approximation, signal quantities are superimposed on dc quantities.

(*) For instance, the total drain current i_D equals the dc current I_D plus the signal current i_d ; the total drain voltage $V_D = V_D + v_d$ and so on.

(*) The analyses and design can be greatly simplified by separating dc or bias calculations from small-signal calculations.

(*) It means once a stable dc operating point has been established & all dc quantities calculated, then signal analysis is performed by ignoring dc quantities.

→ SMALL-SIGNAL EQUIVALENT - CIRCUIT MODELS

(*) MOSFET behaves as a Voltage Controlled Current Source.

(*) It accepts signal v_{GS} between gate and source and provides a current " $g_m v_{GS}$ " at the drain terminal.

(*) Input resistance of this controlled source is very high- ∞ .

(*) Output resistance, looking into drain - is high

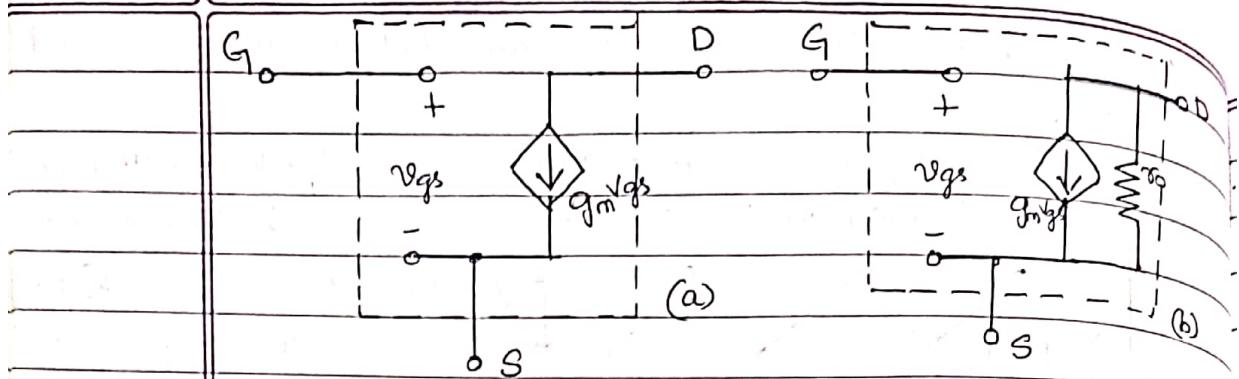


Figure 8: Small-signal models of the MOSFET. (a) neglecting the dependence of i_D on v_{DS} in saturation ($\lambda = 0$) (b) including the effect of channel-length modulation, $r_o = |V_A| / I_D$.

(*) Fig 8a represents the small-signal operation of the MOSFET and thus a small-signal model or a small-signal equivalent circuit.

(*) In the analysis of a MOSFET amplifier circuit, the transistors can be replaced by the equivalent model shown in fig 8a.

(*) Rest of the circuit remains unchanged except that ideal constant dc voltage sources are replaced by short circuits. This is due to the fact that

- the voltage across ideal ^{constant} dc voltage does not change
- thus there will always be zero voltage signal across a constant dc voltage.

(*) The constant dc current sources; namely signal current of an ideal constant dc current source will be zero & hence it is replaced by open-circuit in small-signal equivalent circuit of the amplifier.

(*) The shortcoming of small-signal model of fig 8a is that it assumes drain current in saturation is independent of drain voltage.

(*) But the fact is drain current depend on v_{DS} in a linear manner,

(*) Such dependencies is modelled by finite resistance between drain and source, given by

$$\gamma_0 = \frac{|V_A|}{I_D} \rightarrow (22) \text{ where } V_A = \frac{1}{\lambda}$$

(*) For a given process-technology, $V_A \propto$ to the MOSFET channel length.

(*) Drain current without channel-length modulation is given as $I_D = \frac{1}{2} k_n \frac{W}{L} V_{ov}^2 \rightarrow (23)$

(*) $\gamma_0 \rightarrow$ Range of $10\text{ k}\Omega$ to $1000\text{ k}\Omega$

(*) Including γ_0 improves the accuracy of the small-signal model.

(*) The small-signal model parameters g_m & γ_0 depend on the dc bias point of the MOSFET.

(*) For small-signal model of fig 8b, the voltage gain is

$$A_v = \frac{v_d}{v_{gs}} = -g_m (R_D || \gamma_0) \rightarrow (23)$$

(*) Thus, finite output resistance γ_0 results in reduction in the magnitude of the voltage gain.

→ THE TRANSCONDUCTANCE, g_m

(*) From eqn (17)

$$① g_m = k_n \left(\frac{W}{L} \right) (V_{GS} - V_t) = k_n \left(\frac{W}{L} \right) V_{OL} \rightarrow (24)$$

(*) $g_m \propto$ the process transconductance parameter, $k_n' = \mu_n C_{ox}$ & $g_m \propto \frac{W}{L}$ of the mos transistor.

(*) Hence to obtain Large g_m , the device must be short & wide

(*) Also for a given device the $g_m \propto$ to the Overdrive Voltage, $V_{ov} = V_{GS} - V_t$, the amount by which the bias voltage V_{GS} exceeds the threshold voltage V_t .

(*) But increasing g_m by biasing device at larger V_{GS} is disadvantageous since it reduces allowable voltage signal swing at the drain.

$$I_D = \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2$$

$$\Rightarrow V_{GS} - V_t = \sqrt{2 I_D / k_n' \left(\frac{W}{L} \right)}$$

$$\therefore g_m = k_n' \left(\frac{W}{L} \right) \times \sqrt{2ID}$$

$$② \Rightarrow g_m \sqrt{2k_n' \sqrt{W/L} \sqrt{ID}} \rightarrow ②⑤$$

(*) This expression shows that:

1. For a given MOSFET, $g_m \propto$ square root of the dc bias current.

2. At a given bias current, $g_m \propto$ to $\sqrt{W/L}$

(*) In contrast, g_m of BJT is \propto bias current & is independent of physical size & geometry of the device.

(*) Another expression for g_m of the MOSFET can be obtained as follows:

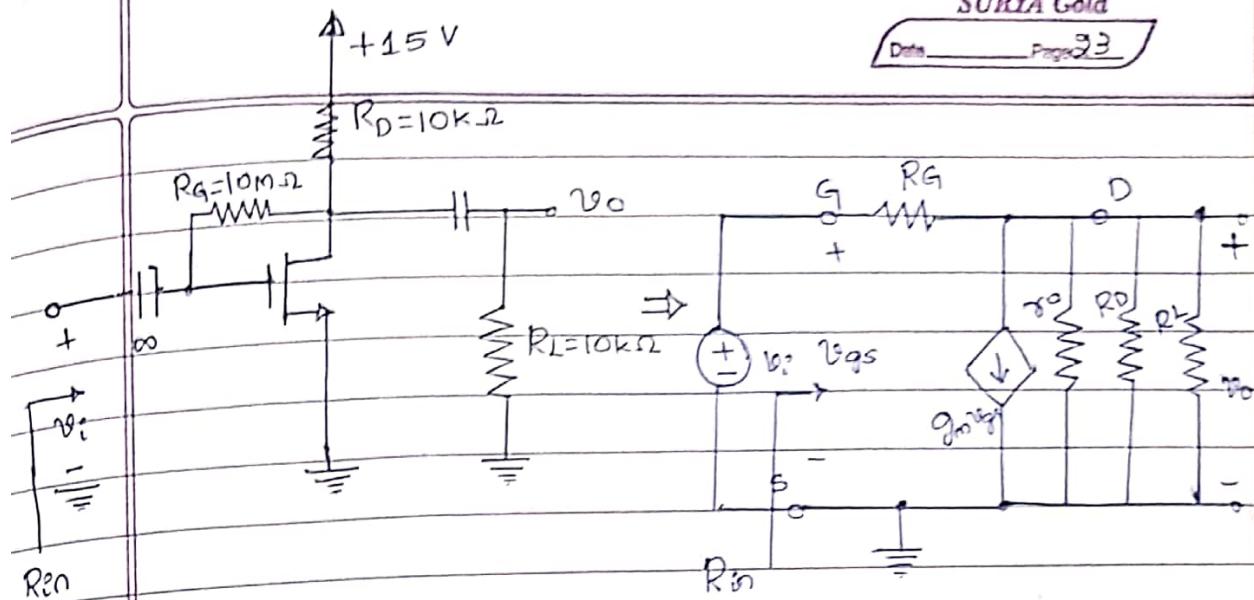
$$k_n' \left(\frac{W}{L} \right) = 2ID \\ (V_{GS} - V_T)^2$$

$$④ \Rightarrow ③ \quad g_m = \frac{2ID}{V_{GS} - V_T} = \frac{2ID}{V_{ov}} \rightarrow ④⑥$$

(*) From three different relationships for determining g_m , there are 3 design parameter $-(W/L)$, V_{ov} and I_D & any two of which can be chosen independently.

(*) i.e., designer may choose to operate the MOSFET with a certain overdrive voltage V_{ov} & at a particular I_D ; the required W/L can be found & resulting g_m is determined.

EXAMPLE 3: Consider the below circuit, the input signal v_i is coupled to the gate via a large capacitor & output signal at the drain is coupled to the load resistance via large capacitor. Determine its small signal voltage gain & its input resistance & allowable input signal. The transistor has $V_T = 1.5V$, $k_n' \frac{W}{L} = 0.25 \text{ mA/V}^2$, and $V_A = 50 \text{ V}$.



$$\hookrightarrow I_D = \frac{1}{2} \times k_n' w \frac{(V_{GS} - V_t)^2}{L}$$

$$I_D = \frac{1}{2} \times 0.25 (V_{GS} - 1.5)^2 \rightarrow \textcircled{a}$$

(*) Since dc gate current = 0, there is no voltage drop across R_g , thus $V_{GS} = V_D$,

$$\therefore I_D = 0.125 (V_D - 1.5)^2 \rightarrow \textcircled{b}$$

$$(\textcircled{c}) \text{ Also, } 15 - I_D R_D = V_D$$

$$V_D = 15 - 10 I_D \rightarrow \textcircled{c}$$

(*) Solving eqns \textcircled{b} & \textcircled{c} together gives,

$$\textcircled{b} \Rightarrow I_D = 0.125 (15 - 10 I_D - 1.5)^2$$

$$I_D = 0.125 (13.5 - 10 I_D)^2$$

$$I_D = 0.125 (182.25 + 100 I_D^2 - 270 I_D)$$

$$I_D = 22.78 + 12.5 I_D^2 - 33.75 I_D$$

$$\Rightarrow 12.5 I_D^2 - 34.75 I_D + 22.78 = 0$$

$$\Rightarrow I_D = 1.72 \text{ mA or } I_D = 1.05 \text{ mA}$$

$$V_D = -2.2 \text{ V or } V_D = 4.5 \text{ V } \checkmark$$

$$\therefore I_D = 1.05 \text{ mA } \& V_D = 4.5 \text{ V}$$

$$\hookrightarrow g_m = k_n' w \frac{(V_{GS} - V_t)}{L} = 0.25 (4.4 - 1.5)$$

$$g_m = 0.725 \text{ mA/V}$$

\hookrightarrow Output resistance r_o is given by,

$$r_o = \frac{|V_A|}{I_D} = \frac{50}{1.05} = 47 \text{ k}\Omega \therefore r_o = 47 \text{ k}\Omega$$

→ for small-signal equivalent circuit of the amplifier
 Coupling capacitors have been replaced with short circuits
 & dc power supply is replaced with short circuits to ground
 → R_G is very large ($10M\Omega$), the current through it can be neglected.

→ output voltage is given by

$$V_O \approx -g_m V_{GS} (R_D || R_L || r_o)$$

$$V_{GS} = V_i$$

↳ Voltage gain, $A_v = \frac{V_O}{V_i} = -g_m (R_D || R_L || r_o)$

$$A_v = -0.725 (10 || 10 || 47)$$

$$A_v = -0.725 \times 4.52$$

$$A_v = -3.3 V/V$$

$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$\frac{1}{R_T} = \frac{1}{10} + \frac{1}{10} + \frac{1}{47}$$

$$\frac{1}{R_T} = 0.2212$$

↳ Input resistance R_{in} , the input

current i_i is given by,

$$i_i = \frac{(V_i - V_O)}{R_G}$$

$$= V_i \left[1 - \frac{V_O}{V_i} \right] = \frac{V_i \cdot 4.3}{R_G}$$

↳ Thus, $R_{in} \equiv V_i / i_i = R_G = \frac{10}{4.3} = 2.33 M\Omega \therefore R_{in} = 2.33 M\Omega$

↳ The largest allowable input signal \hat{V}_i is determined by the need to keep the MOSFET in saturation at all times

$$V_{DS} \geq V_{GS} - V_T$$

$$V_{DSmin} = V_{GSmax} - V_T$$

$$V_{DS} - |A_v| \hat{V}_i = V_{GS} + \hat{V}_i - V_T$$

$$4.4 - 3.3 \hat{V}_i = 4.4 + \hat{V}_i - 1.5$$

$$\hat{V}_i + 3.3 \hat{V}_i = 1.5$$

$$\hat{V}_i = 0.34 V$$

$$A_v = V_O = V_{DS}$$

$$V_i = V_{GS}$$

$$V_{DS} = |A_v| V_i$$