Synthesis using Genus

- For running the combinational circuit, sel_sense.v through Genus, use sample commands from the script script_sel_sense.tcl and use the PDK: “Cadence_RAK_18.1_blockImplementation” to run Synthesis. The demo for this design is in Week3_lec1 and Week3_lec2.
- LIBS/lib/ contains lib files
- LIBS/lef contains lef files
- This demo is not done on our lab machine. So, pls follow guidelines in the “login” section below, to understand how to login and access Cadence tools in our lab
- Note that you will need to modify paths, commands etc in the tcl file before running.
- For running the sequential circuit counter.v**,** use script_counter.tcl and the PDK counter_design_database_45nm. The demo for this design is in Week3_lec3_seq
  - **constrains_counter.sdc -- has the constraint commands**

Login

- **Login or ssh to the VLSI lab machine**
- **If you are not on campus, you should first vpn into the iiitb network and then do ssh to the lab machine**
- cd to home directory, using the command “cd”
- Do “source cshrc_hub” to source the paths of the tools installed. The cshrc_hub text file is posted on lms. You need to copy this to the home directory of you lab machine
- Note that you need to have the PDK downloaded in the lab machine to run the tool
- **Launch Genus using the command**
  - genus -legacy_ui
  - Type in each of the Synthesis commands shown in the demo at the command prompt of genus
  - **Hit quit to exit Genus. Do not do Ctrl+C, you will be holding up licenses**
- How to run the .tcl script
  - Type in each of the Synthesis commands shown in the script at the command prompt of genus
    **OR**
  - To source the whole script file at once, **source script.tcl. This will run the entire script at once, without pausing at each step. If you want to pause at any moment, use a “suspend” command in the script.**

- Write out a template script:
    - write_template -simple -outfile simple_template.txt
    - write_template -power -outfile template_power.tcl
    - write_template - → different optimisation templates
    - Type man followed by command to search for help regarding the command: Eg: man write_template
- Command to view schematics in GUI mode: gui_show
- After you run all commands: a genus.cmd and genus.log are created in the same directory. The command file has a history of all commands.

Constraints: sdc file contents:
**//Period is in nanoseconds. Manual says picoseconds. Verify this yourself once!**

Create_clock -name clk -period 1 - -waveform {0 5} [get+ports “clk”]
Set clock_transition -rise 0.1 [get clocks “clk”]
Set clock_transition -fall 0.1 [get clocks “clk”]
Set clock_uncertainty 0.01  [get clocks “clk”]
Set_input_delay -max 1.0  [get clocks “rst”] -clock  [get clocks “clk”]
Set output_delay -max 1.0  [get clocks “count”] -clock  [get clocks “clk”]

**Synthesis Outputs:**

- **Sdc file - important for the next step**
- **Synthesized Netlist  - important for the next step**
- **Area, timing, power reports**