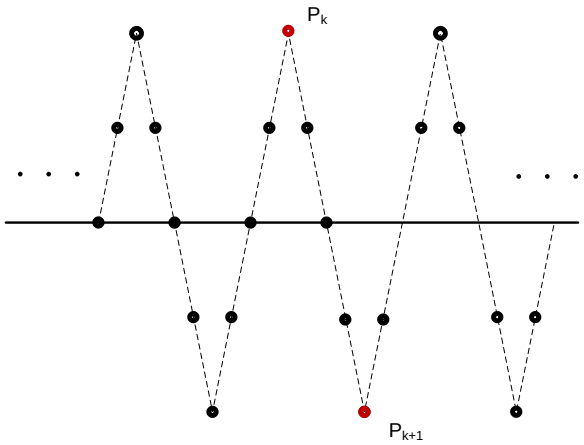
Amplitude Equalizer

Design a digital circuit that performs amplitude equalisation of a triangle wave signal. The wave is sampled by an ADC, which outputs signed samples represented on 8 bits. The sampling frequency of the ADC is 8 times that of the input signal. Suppose that sampling is carried out in such a way as to have for each period of the input signal also the sample on the peaks of the triangular wave (see figure below).



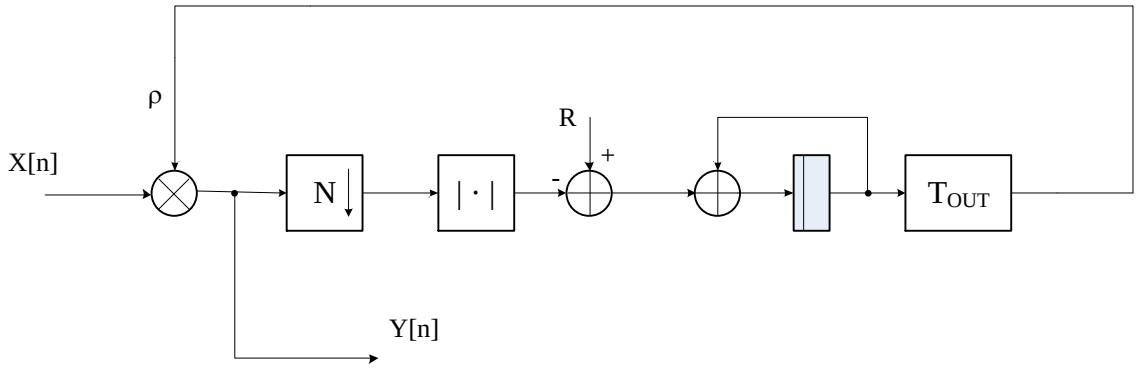
Equalisation must be done by multiplying the samples output by the ADC by a correction factor represented with sign on 8 bits. This factor is obtained recursively according to the equation:

$$\rho_{k+1} = \rho_k + (R - |P_k \cdot \rho_k|)$$

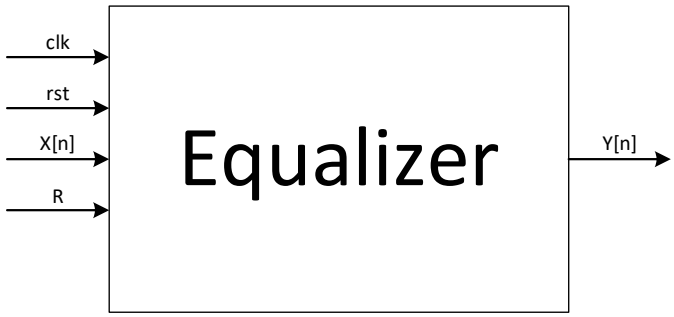
Where ρ_k is the value of the correction factor at step k, P_k is the sample on the peak at step k and R is the reference at which the amplitude on the peak of the output triangular wave must reach. Keep in mind that for each period of the input signal there are two peaks (one positive and one negative), both of which can be exploited to perform the updating of the factor ρ for which the index k is updated with a frequency equal to twice that of the input signal.
For the reference consider:

$$R = 2^{10} - 1$$

In the following a possible high-level architecture for the circuit. Set the size of the accumulator to 20 bits. The output of the accumulator must then be truncated to 12 bits to obtain the 8-bit signal.



The interface of the circuit to be designed is as follows:



You are requested to deal with the various possible error situations, documenting the choices made.

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions