DIGITAL SYSTEM AND LOGIC DESIGN PROJECT

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Submitted to :-Prof. V.K.Sambhe

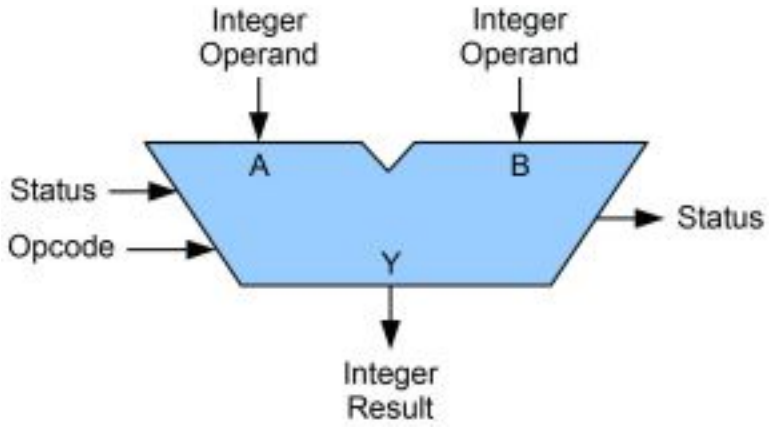
Topic :

A 4-bit Arithmetic Logic Unit.

Introduction :

An ALU stands for Arithmetic and Logic unit. It is a digital circuit that performs arithmetic, logical and bitwise operations. It is the fundamental building block of the central processing unit. It performs arithmetic operations like add, subtract, increment, decrement, comparison, etc. shifting operations like logical shift, arithmetic shift, rotate, etc. bitwise operations like AND, OR, XOR, XNOR, NOR, NAND, 1's complement, etc.

Basic Block Diagram :



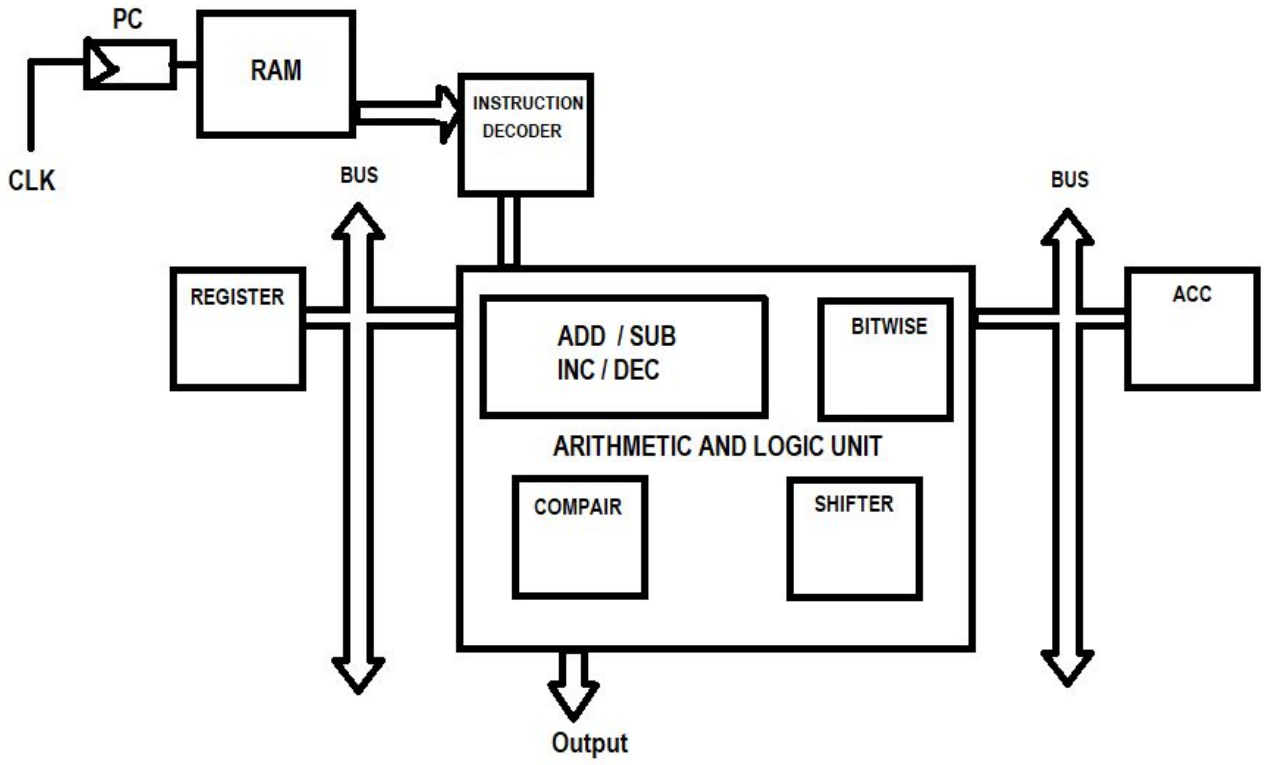
Components required:

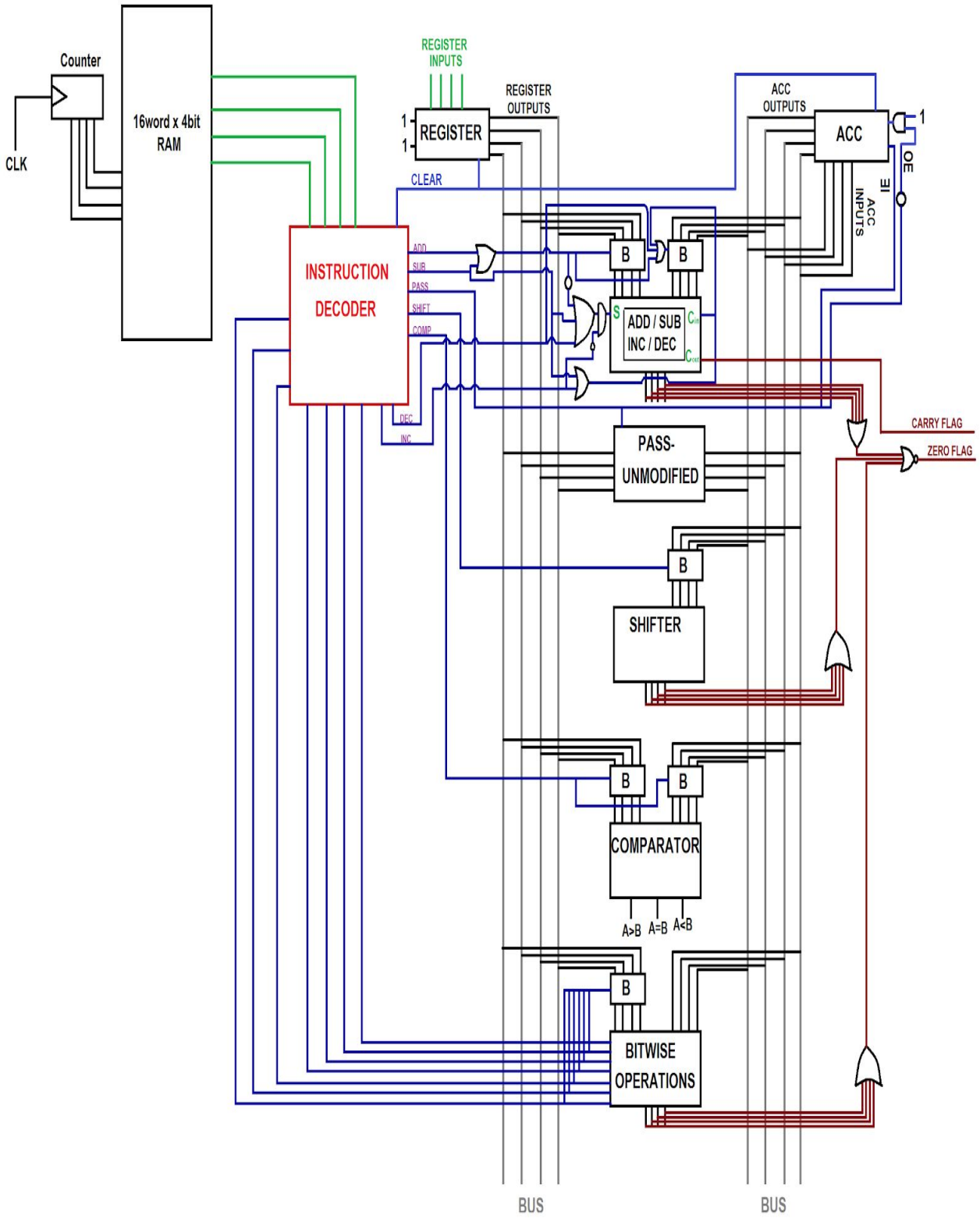
Component	Description	Cost
Breadboard	It is a construction base for prototyping of electronics.	Rs.80
330 ohm Resistor	Used to limit the current through the LEDs	Rs.3 /piece
IC 74283	It is a 4-bit fast adder ic with look-ahead-carry. Datasheet	Rs.120
IC 7485	It is a 4-bit comparator with outputs as A>B, A<B, A=B Datasheet	Rs.105
IC 7408, IC 7432, IC 7404, IC 7486, IC 7400, IC 7402	The ics are quad 2 input AND gate,quad 2 input OR gate, NOT gate, quad 2 input XOR gate, quad 2 input NAND gate and quad 2 input NOR gate respectively	All costs nearly Rs.15 each
IC 74LS195	It is a universal shift register Datasheet	Rs.22

IC 74243	It is a 4-bit tri state buffer Datasheet	Rs.60

IC 74LS173	It is a 4-bit d type register Datasheet	Rs.115
IC 74LS154	It is a 4-16 line decoder Datasheet	Rs.85
Jumper wires	For communication	Rs.50
IC 74LS189	16word x 4bit RAM	Rs.90
IC 7493	4bit binary counter	Rs.30

Block Diagram

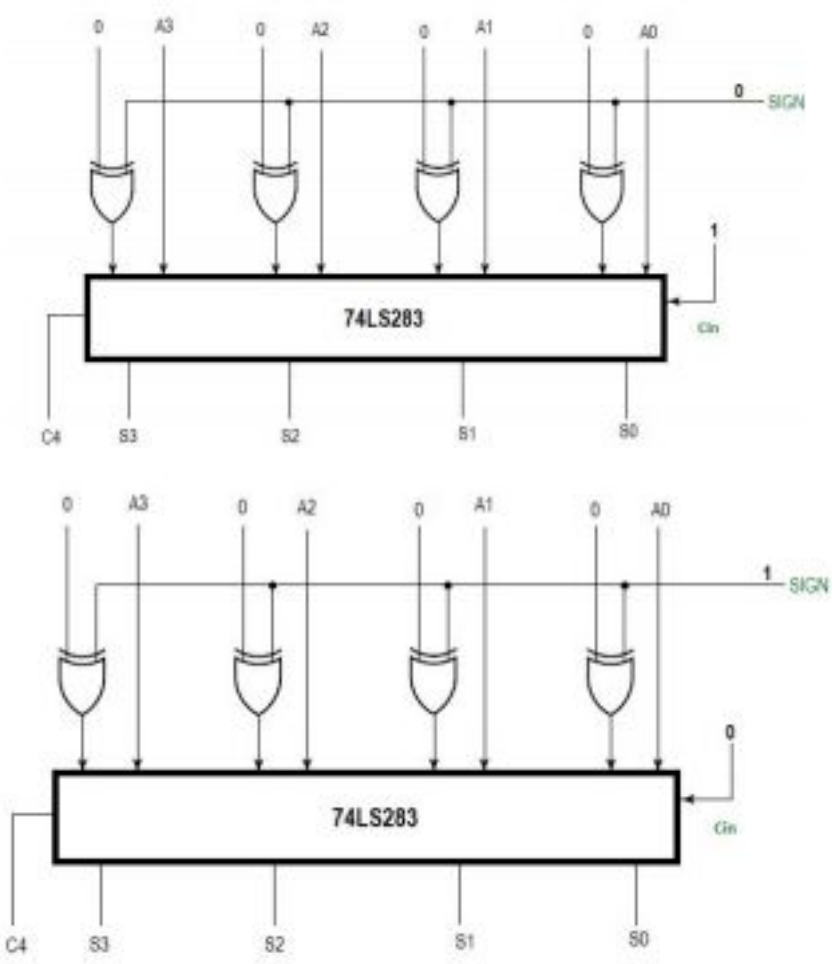

PC
RAM
CLK
INSTRUCTION
DECODER
BUS
BUS
REGISTER
ACC
ADD / SUB
INC / DEC
BITWISE
ARITHMETIC AND LOGIC UNIT
COMPAIR
SHIFTER
Output



Circuit Diagram

Explaination:

- **There are 2 buses for data transfer. One is for the data register and other is for accumulator.**
- **An instruction decoder decodes the 4-bit instruction and activates one of the unit.**
- **The first unit performs the add / subtract / increment / decrement operations.**
  - **For addition and subtraction a full adder with XOR inverter logic is used.**
  - **For increment and decrement :**



- **The pass unmodified unit loads the value of the register to the accumulator. It is done using a tri-state buffer. ● The shift**

unit shifts the content of the accumulator.

- **The compare unit compares the values of the register and the accumulator and produces the output on the lines for A>B, A<B and A=B.**
- **The bitwise unit performs the bitwise operations.**
- **The tri-state buffers are used for activating and deactivating the units.**
- **There is a clear signal to clear the values of both the register and the accumulator.**
- **There are 2 flags zero and carry.**
- **There is a manually pulse generator, which generates pulse.**
- **A 4 bit binary counter is used as a program counter.**
- **Its output is fed into the input of a 16-word x 4-bit RAM as address.**
- **Instructions are stored at these addresses, these instructions will be input to the 4 to 16 line instruction decoder.**
- **As a result the decoder will activate one of the 16 lines.**
- **Instructions:**

INSTRUCTION	OPCODE	DESCRIPTION
LDA	0001	Load the content of register to accumulator
ADD	0010	Add the contents of register and accumulator
SUB	0011	Subtract the contents of register and accumulator
COMP	0100	Compare the contents of register and accumulator
SHIFT	0101	Shift the contents of accumulator by 1 bit
INCRE	0110	Increments the content of accumulator
DECRE	0111	Decrements the content of accumulator
CLR	1000	Clear the contents of both, the register and the accumulator
AND	1001	ANDs the contents of register and accumulator
OR	1010	ORs the contents of register and accumulator
NOT	1011	NOTs the content of accumulator
NOR	1100	NORs the contents of register and accumulator
NAND	1101	NANDS the contents of register and accumulator
XOR	1110	XORs the contents of register and accumulator
X-NOR	1111	X-NORs the contents of register and accumulator

- **Program example:**

LDA 0010	**Loads the R to ACC**
ADD 0001	**Adds the 0001 with the ACC**
SHIFT	**Shifts the ACC**
DECRE	**Decrements ACC**

CLR	**Clears both th R and ACC**

Novelty:

Though ALU has been implemented earlier, the uniqueness of this project is that it a single adder-subtractor unit can perform 4 operations. Also the circuit is unique and easy to implement. Further more unit can be compressed and the number of operations can be increased. Instructions can be increased. A RAM can be introduced ot store the programs, while executing. Also a program counter can be introduced.

The State of art :

State of the art of this project is the ics used. They are the key components. Using combination of these ics we can also perform some advanced programs. The cost of the components is also considerably low. **For processing 8bit on a 4 bit processor data we can use ic 74ls157. It allows the bits in the group of 4 bits.**

Future Scope:

There are many microcontroller available in the market with lot more functionality.

But we need to study those microcontroller's syntax and then we can implement some projects.

By designing our own microcontroller we can add the functionality we want.
A recent article is also published that in future AI will be trained on 4 bit computers.
Link:https://www.technologyreview.com/2020/12/11/1014102/ai-trains-on-4-bit-computers/

Conclusion:

- In this project we design a 4-bit ALU(4-bit in the sense it can operate on 4 bits).
- List the required components.
- We design instructions.
- Execute programs.