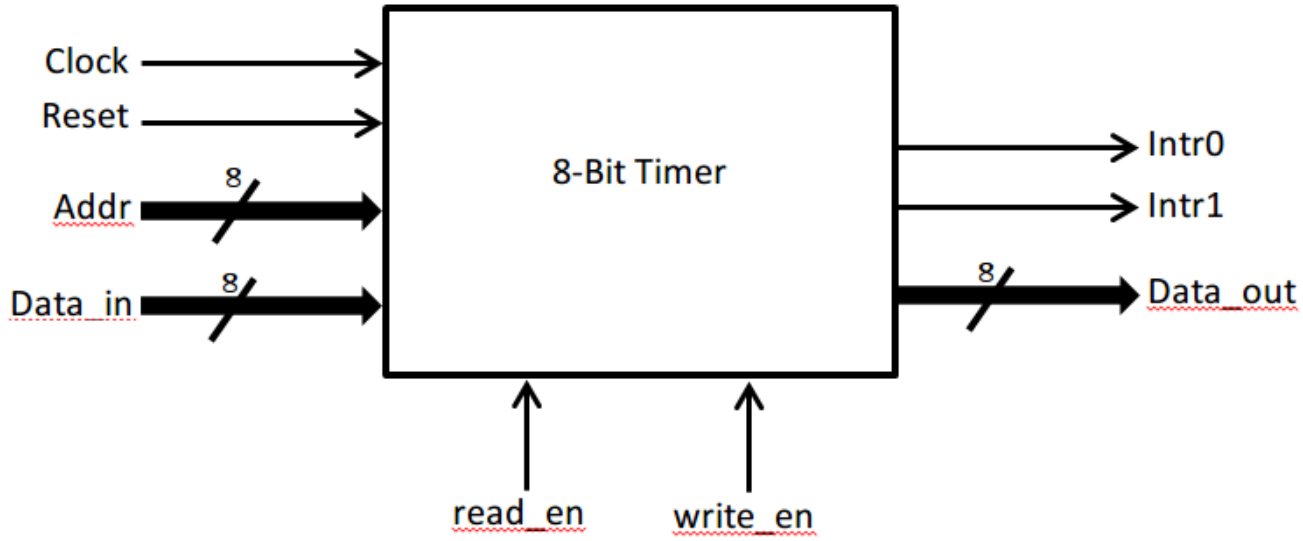
8-Bit Timer Counter Module

Features:

- This is an 8-bit incrementing counter. It continues incrementing after sending interrupts.
- It has a private 8-bit comparator that is used to assert an interrupt when the timer has reached the comparator value.
- There is one more interrupt line for an overflow event, i.e., whenever timer value reaches 0xFF, in the next increment it will start counting from 0x0 and raise an interrupt line corresponding to overflow interrupt.
- The timer is clocked by CLK.



Register Block:

S.No.	Offset	Reg Name	Reset Value	Width	Access	Description
1.	0x0	timer_cntrl	0x00	8	rw	Timer control register
2.	0x4	timer_val	0x00	8	ro	Timer value register
3.	0x8	timer_cmp	0x00	8	rw	Timer compare register
4.	0xC	timer_intr_status	0x00	8	w1c	Timer interrupt status register

Register Description:

Note: 8-bit access is allowed.

1) Timer control Register

Reserved	OV	CMP	EN

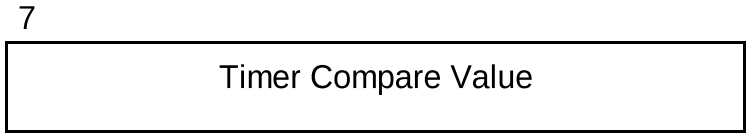
Bits	Name	Function
[0]	EN	Timer Enable bit 0 - Timer is disable and counter does not increment All register can still be read and written 1 - Timer is enabled and counter will increment normally. Timer counter will be incremented every clock cycle.
[1]	CMP	Timer compare Interrupt Enable 0 - Compare interrupt is disabled 1 - Compare interrupt is enable. if enabled then whenever timer counter value reaches to compare value it will raise the interrupt line(INT0).
[2]	OV	Overflow Interrupt Enable 0 - Overflow interrupt is disabled 1 - Overflow interrupt is enable. if timer counter value reaches to 0xFF, in the next clock cycle it will update start counting from zero, and raise the interrupt line(INT1) corresponding to overflow interrupt.

2) Timer Value Register

7 0

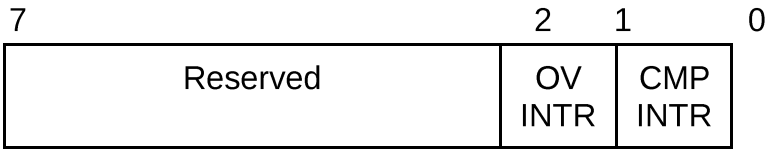
This is a read only register, Whenever timer is enabled it will start incrementing value of this register.

3) Timer Compare Register



This register can be used to store the comparison value for timer counter register. If timer compare interrupt is enable, then it will assert an interrupt line INT0 whenever timer value matches with the timer compare value.

4) Timer Interrupt status Register



This is a write one clear interrupt status register. If timer is enabled then whenever timer counter value reaches a comparator value or an overflow occurs then it will update the corresponding status bit if related interrupt is enable.
Writing a 1 will clear the corresponding interrupt.