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22EC10057

Assignment1 : CMOS Inverter

**Use 65nm PTM CMOS Model ,
Simulate CMOS inverter with square pulses of
period 1ns and amplitude 1V, Vdd =1V.
Use rise-time and fall time of square pulse
~50ps**

**Obtain the plot of pmos and nmos current
along with input and output waveforms.**

Use W, L of PMOS W=0.5u, L=65nm

NMOS W=0.25u, L=65nm

In this task, a CMOS inverter with the following specifications has been made:

PMOS specifications :

W = 0.5u

L = 45nm

NMOS specifications :

W = 0.25u

$L = 45\text{nm}$

Input voltage:

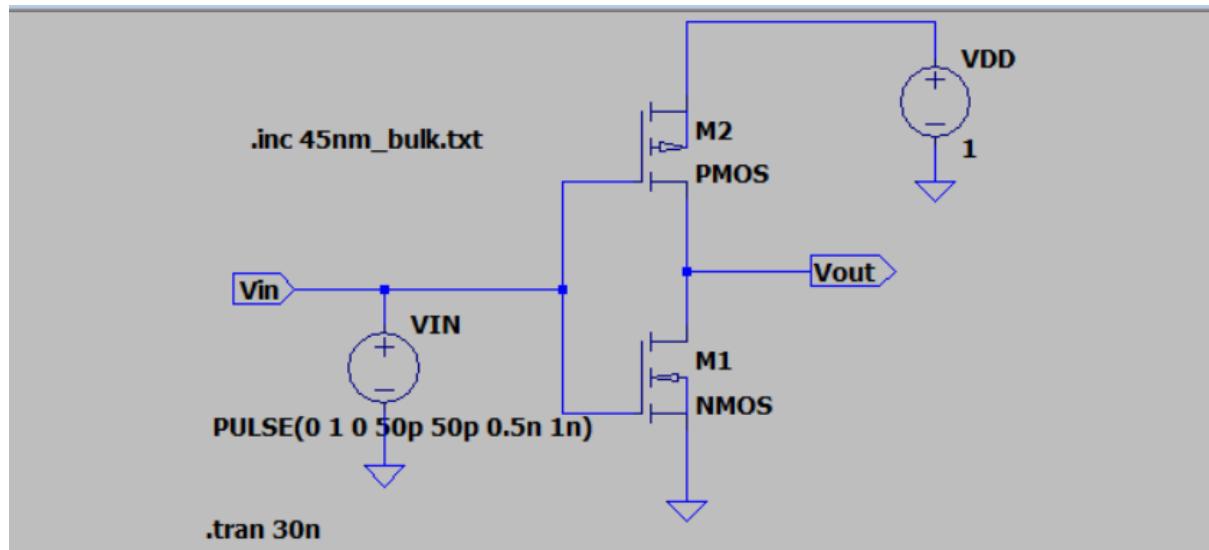
Square voltage of period 1ns and amplitude 1V
(rise time and fall time are 50ps, 50ps)

Input DC voltage (V_{dd}) = 1V

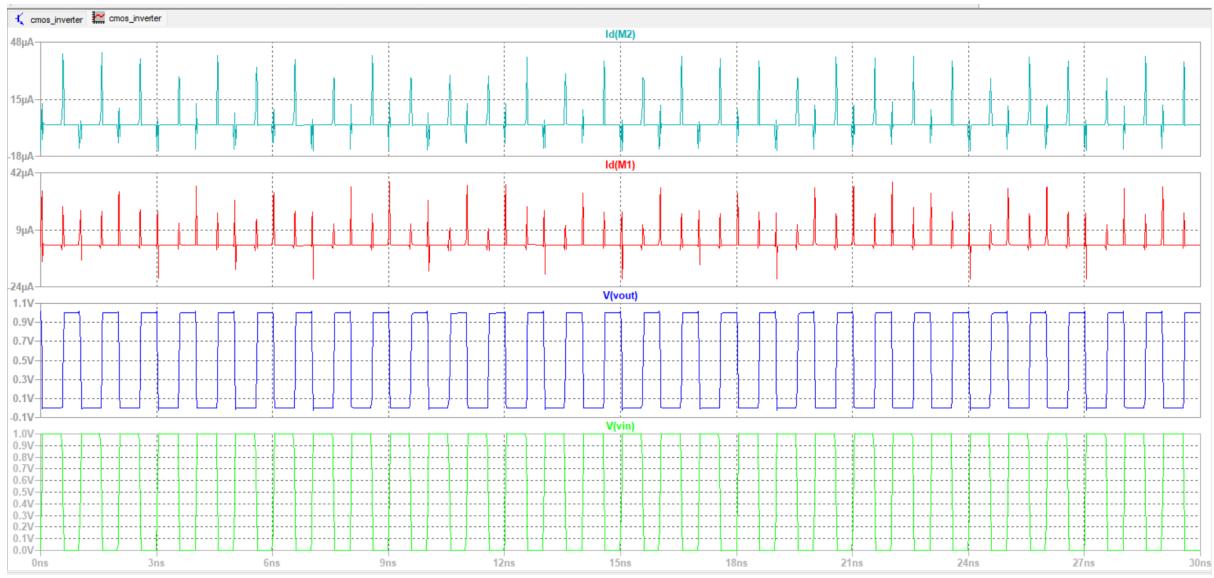
Model:

45nm CMOS model: [Model Files – Learning Microelectronics](#)

Circuit Diagram :



Simulation waveforms:

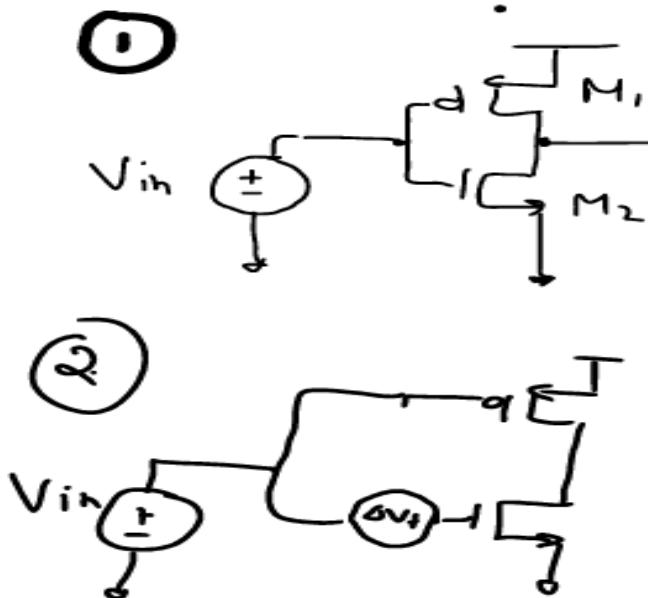


Discussions:

From the waveforms, it is evident that the circuit is acting as a NOT gate or inverter. Current in MOS basically depends on V_{ds} (drain to source voltage). A parasitic capacitor can be imagined at the output(as a load capacitor). During the charging of this capacitor, PMOS is ON ($V_{in}=0V$) and that's why current through PMOS only appears during the transition of V_{in} from 1V to 0V. Similarly, during the discharging of this capacitor, NMOS is ON ($V_{in}=1V$) and that's why current through NMOS only appears during the transition of V_{in} from 0V to 1V. Both PMOS and NMOS can't be simultaneously ON or OFF.

Assignment 2 VLSI :

(N.B.: channel length is 45nm everywhere)

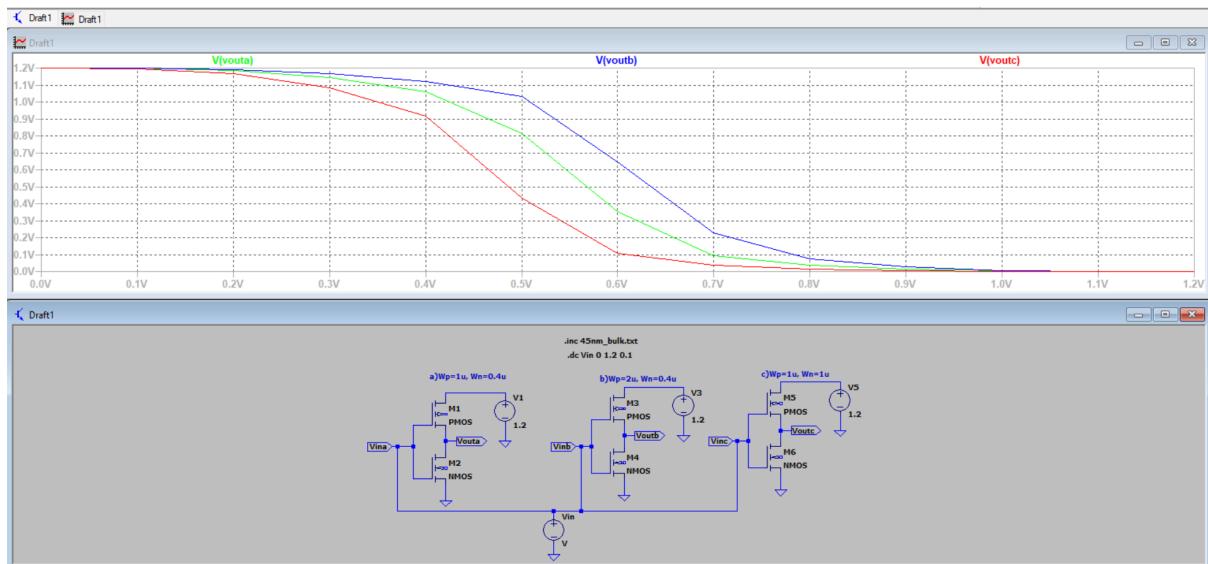


1. Obtain the transfer characteristics of the inverter as shown in the figure for the following dimensions (minimum L for both M₁ and M₂) (a) W_p = 1u, W_n = 0.4u, (b) W_p = 2u, W_n = 0.4u, (c) W_p = 1u, W_n = 1u
Obtain the rise-time and fall time of the output for each case (90% to 10% transition time).

2. Use two inverters in series and figure out which combination gives worst change in duty cycle of output with respect to input. (different possible combinations: 1st inverter-size(1a) & 2nd inverter-size(1b) and so on.

3. As shown in fig., add a DC voltage of 50mV in series with gate terminal of NMOS. Note that, this is equivalent to using an NMOS with threshold voltage lower by 50mV. Check the effect on transfer characteristics. Change the polarity of the DC voltage and obtain the DC characteristics. Now move the DC voltage source to gate of PMOS and repeat the above two steps. Save the snaps of the characteristics thus obtained.

Task1:



a) $W_p=1\mu, W_n=0.4\mu$

For Square voltage of period 1ns and amplitude 1V (rise time and fall time are 50ps, 50ps),

Rise time : 0.022ns

Fall time : 0.021ns

b) $W_p=2u$, $W_n=0.4u$

For Square voltage of period 1ns and amplitude 1V (rise time and fall time are 50ps, 50ps),

Rise time : 0.024ns

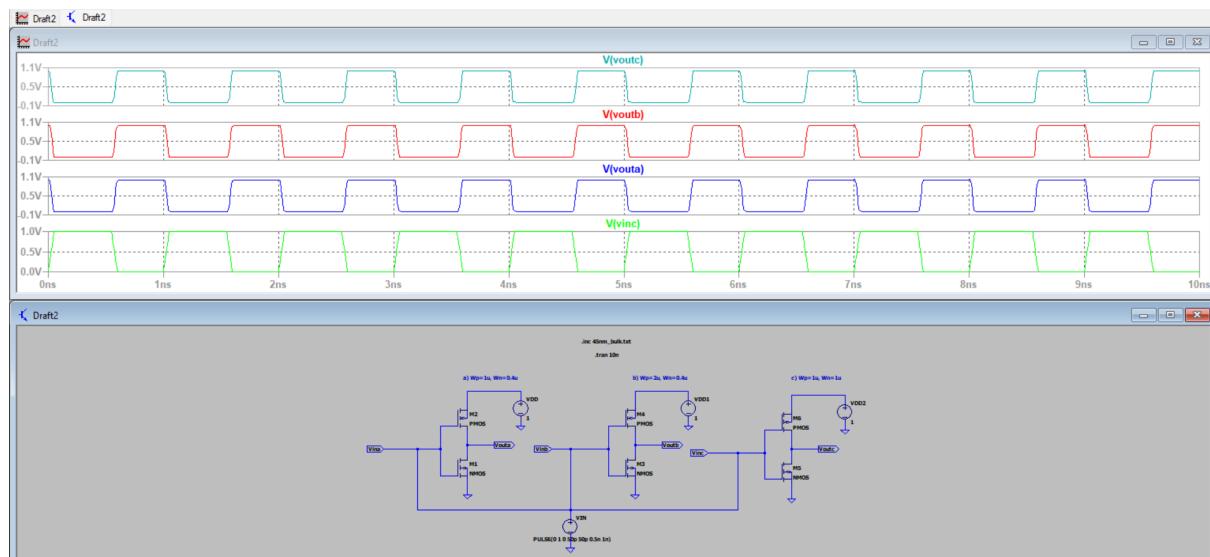
Fall time : 0.022ns

c) $W_p=1u$, $W_n=1u$

For Square voltage of period 1ns and amplitude 1V (rise time and fall time are 50ps, 50ps),

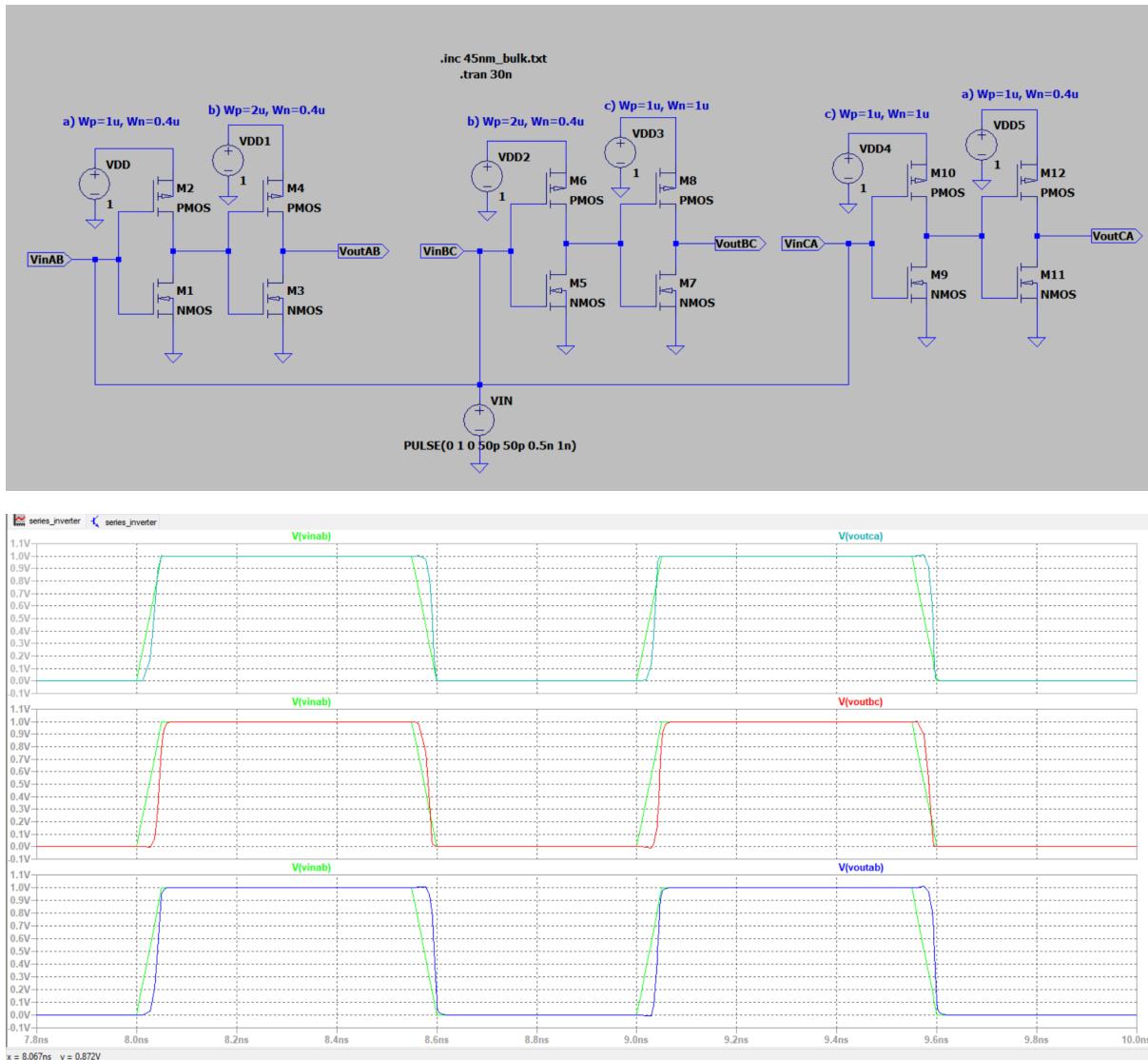
Rise time : 0.027ns

Fall time : 0.021ns



Task2:

For Square voltage of period 1ns and amplitude 1V (rise time and fall time are 50ps, 50ps & duty cycle 50%)



a) $W_p=1\mu$, $W_n=0.4\mu$ & b) $W_p=2\mu$, $W_n=0.4\mu$

Propagation delay: 0.017ns

Average Output duty cycle: 55.4%

b) $W_p=2\mu$, $W_n=0.4\mu$ & c) $W_p=1\mu$, $W_n=1\mu$

Propagation delay: 0.021ns

Average Output duty cycle: 53.9%

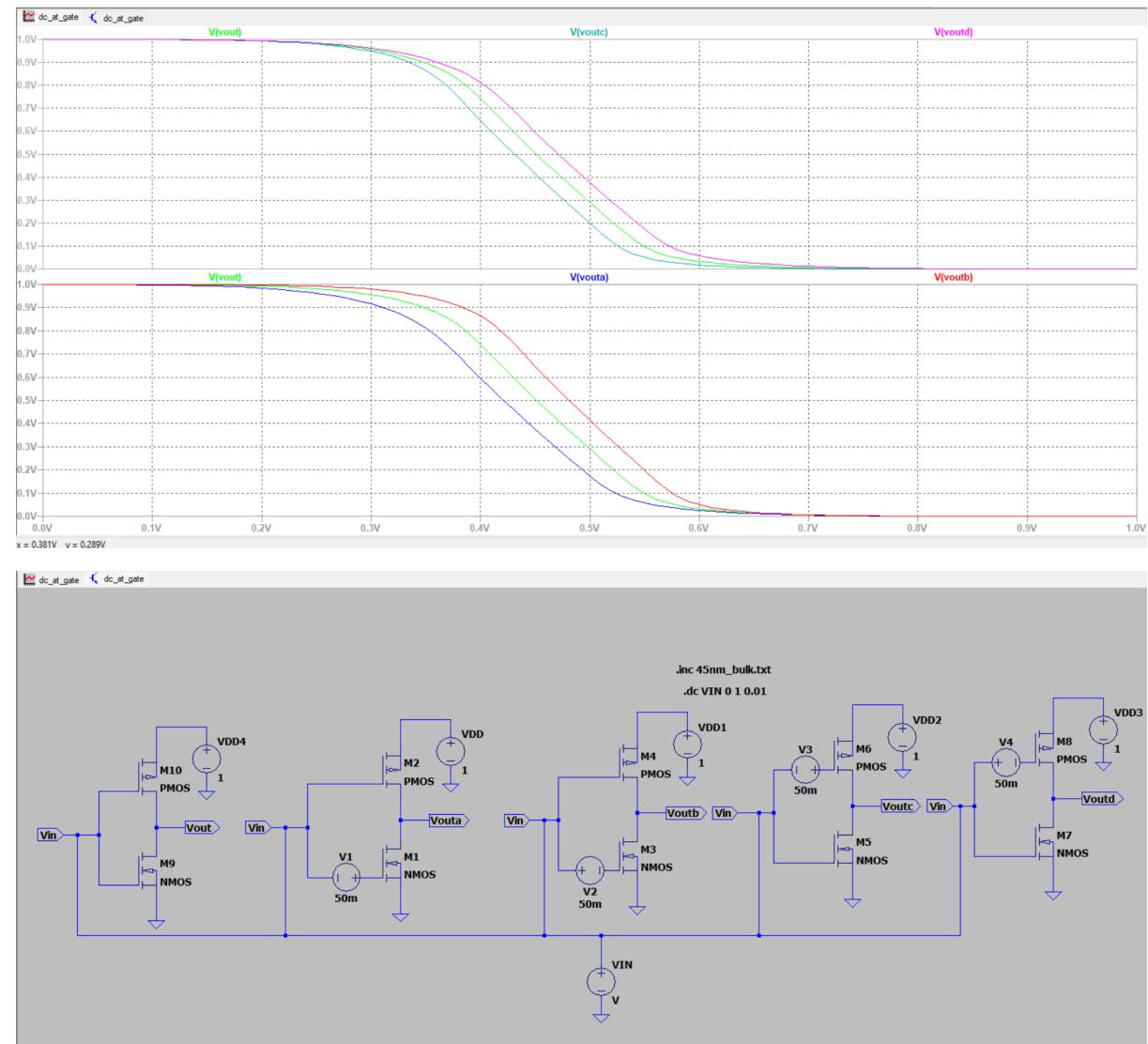
c) Wp=1u, Wn=1u & a) Wp=1u, Wn=0.4u

Propagation delay: 0.009ns

Average Output duty cycle: 55.7%

Last one gives the worst change in duty cycle.

Task3:



In the above diagram,
Vout : Output voltage of CMOS inverter

Vouta : Output voltage of CMOS inverter having a 50 mV dc voltage at NMOS gate

Voutb : Output voltage of CMOS inverter having a 50 mV dc voltage at NMOS gate with reverse polarity

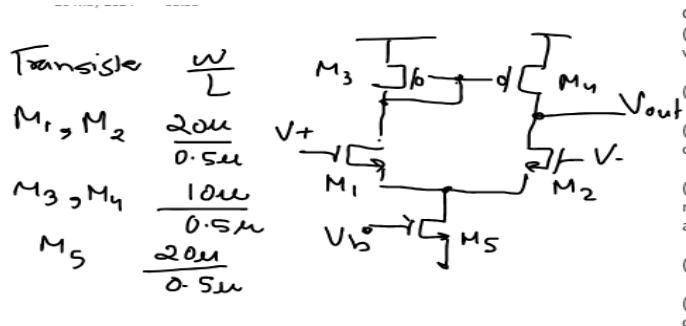
Voutc : Output voltage of CMOS inverter having a 50 mV dc voltage at PMOS gate

Voutd : Output voltage of CMOS inverter having a 50 mV dc voltage at PMOS gate with reverse polarity

When DC voltage source is added to NMOS gate, we need lesser input voltage to get the same output voltage. So, the curve (Vouta) will shift leftwards. When DC voltage source is added to NMOS gate with reverse polarity, we need higher input voltage to get the same output voltage. So, the curve (Voutb) will shift rightwards. Similarly, when DC voltage source is added to PMOS gate, the curve (Voutc) will shift leftwards & when DC voltage source is added to PMOS gate with reverse polarity, the curve (Voutd) will shift rightwards.

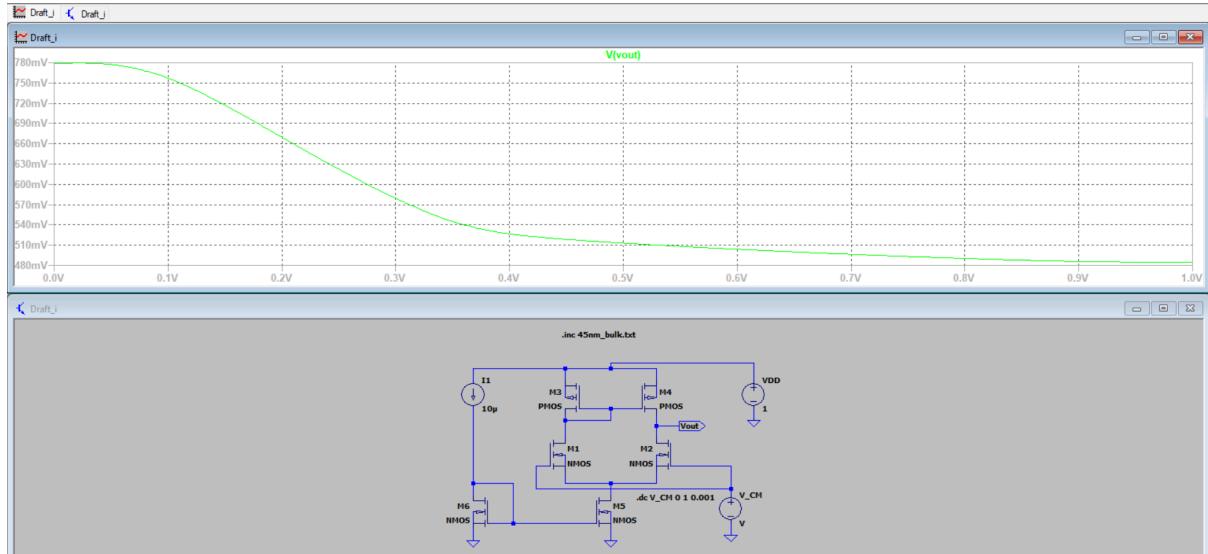
Assignment 3 VLSI :

Q: Bias the differential amplifier with a current of 10uA using current mirror



Here, I took $V_{dd}=1V$ & 45nm cmos ss model

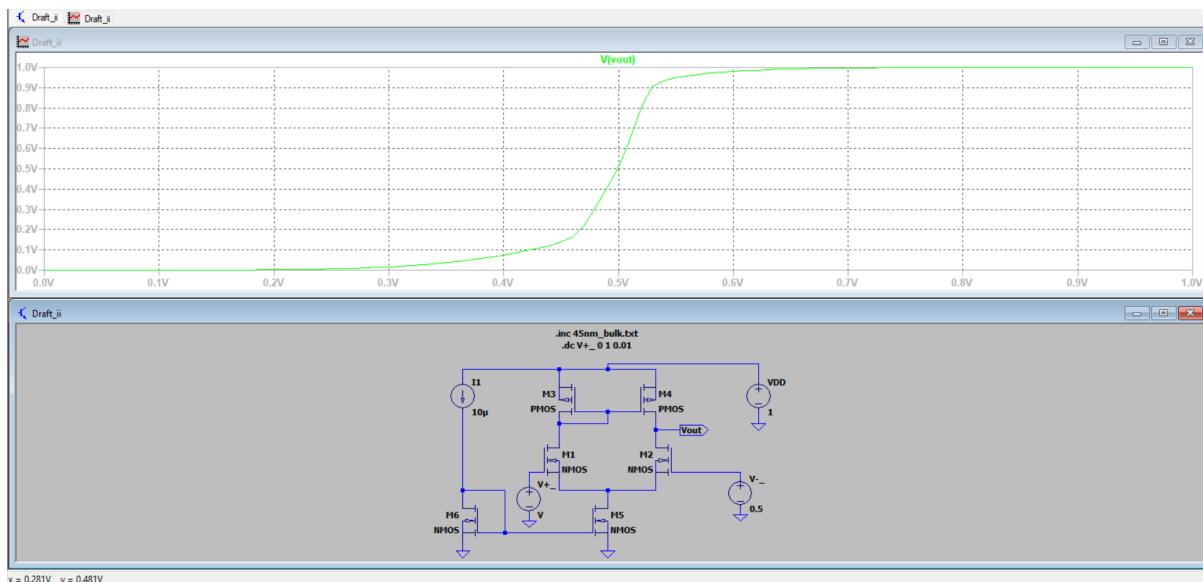
(i) Plot V_{out} as a function of V_{in_cm} (common-mode input) swept from zero to v_{dd} . Obtain the ICMR (input common-mode range).



Vout vs Vcm plot

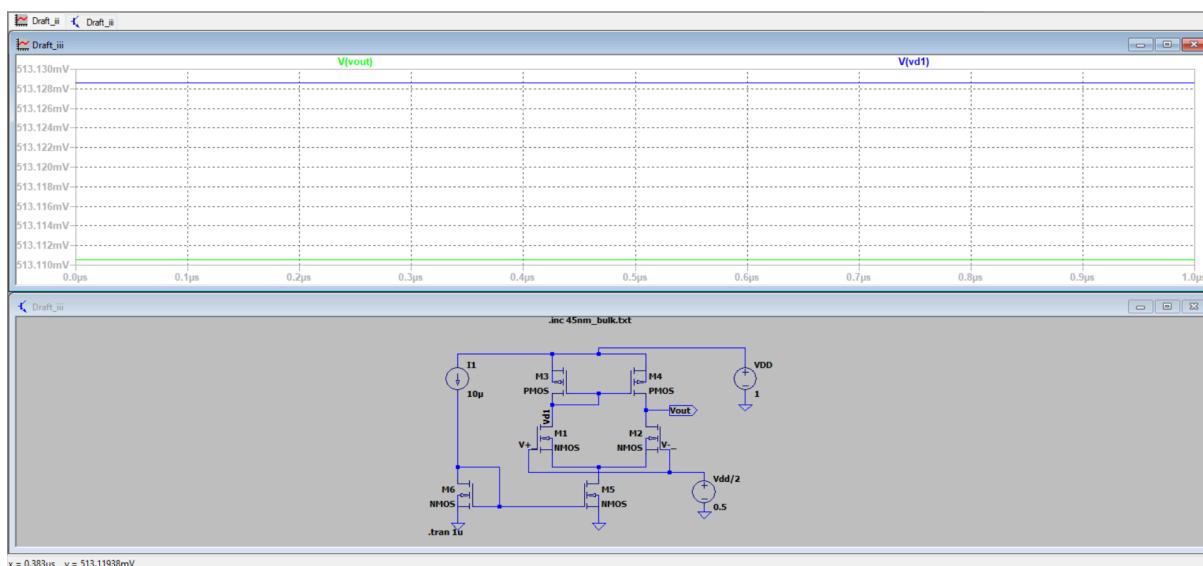
ICMR: In the above circuit, ICMR (range of common mode voltage where gain is constant or above curve is almost linear i.e. both NMOS is in saturation) is around 82 mV - 388 mV .

(ii) Plot Vout as a function of V+, while fixing V- at 0.5Vdd



Vout vs V+

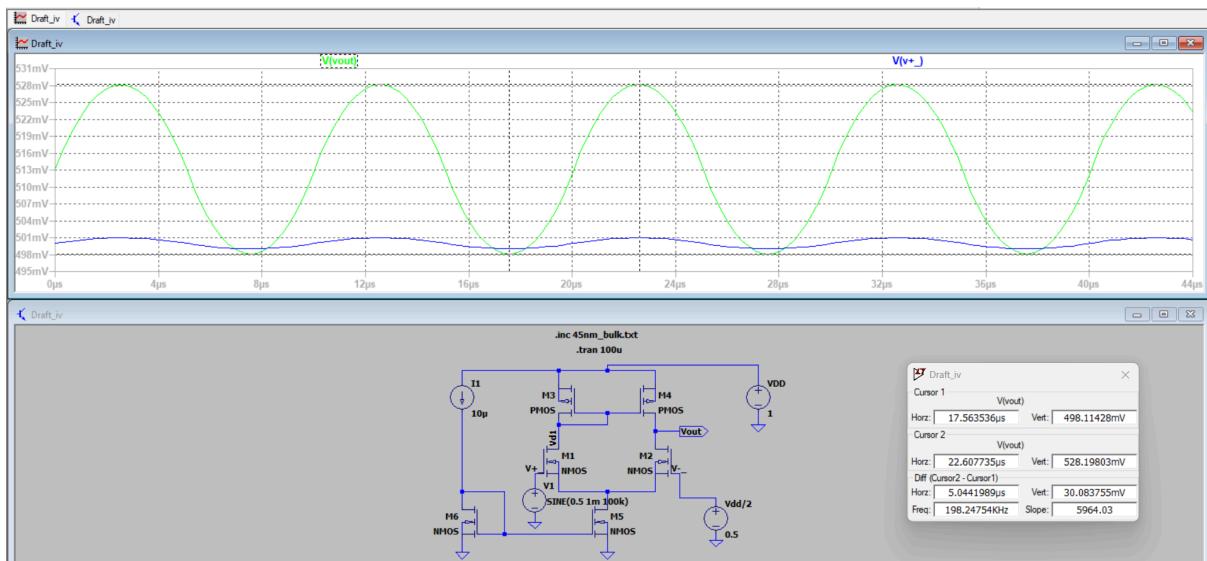
(iii) For V+ = V- = 0.5VDD, find the output DC level, compare it with drain voltage of M1.



$$V_{out} = 513.11 \text{ mV}, V_{d1} = 513.13 \text{ mV}.$$

So, the output DC level & drain voltage of M1 are almost equal.

(iv) For the bias condition in (iii), obtain the transient plot for 100KHz signal of magnitude 1mV (You can fix one input to DC and apply 1mV signal to the other) and report the gain.



$$V_{in(pp)} = 2 \text{ mV}$$

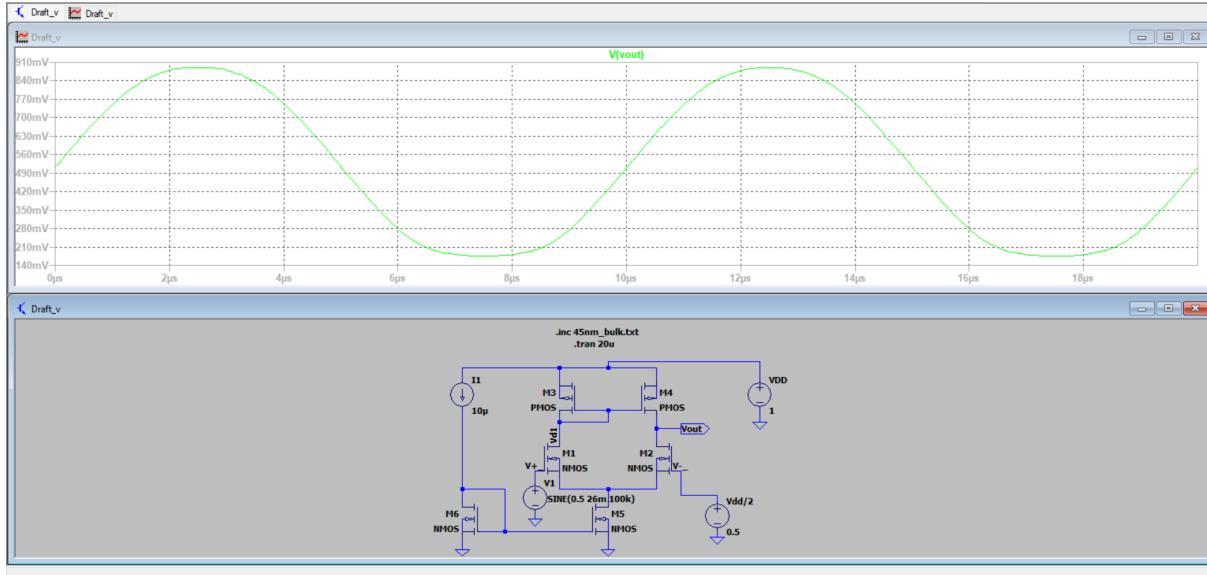
$$V_{out(pp)} = 30.084 \text{ mV}$$

$$\text{Gain} = 15.042$$

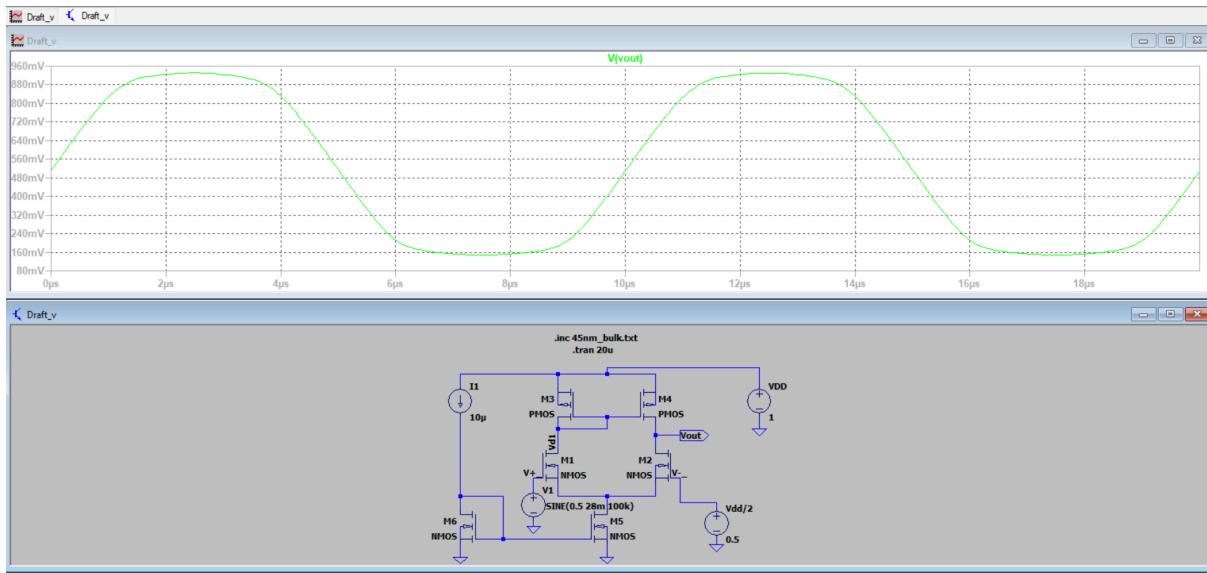
(v) Find the maximum peak to peak differential signal applicable.

Upto 26 mV (amplitude) or 52 mVpp input voltage, output has non-distorted sinusoid.

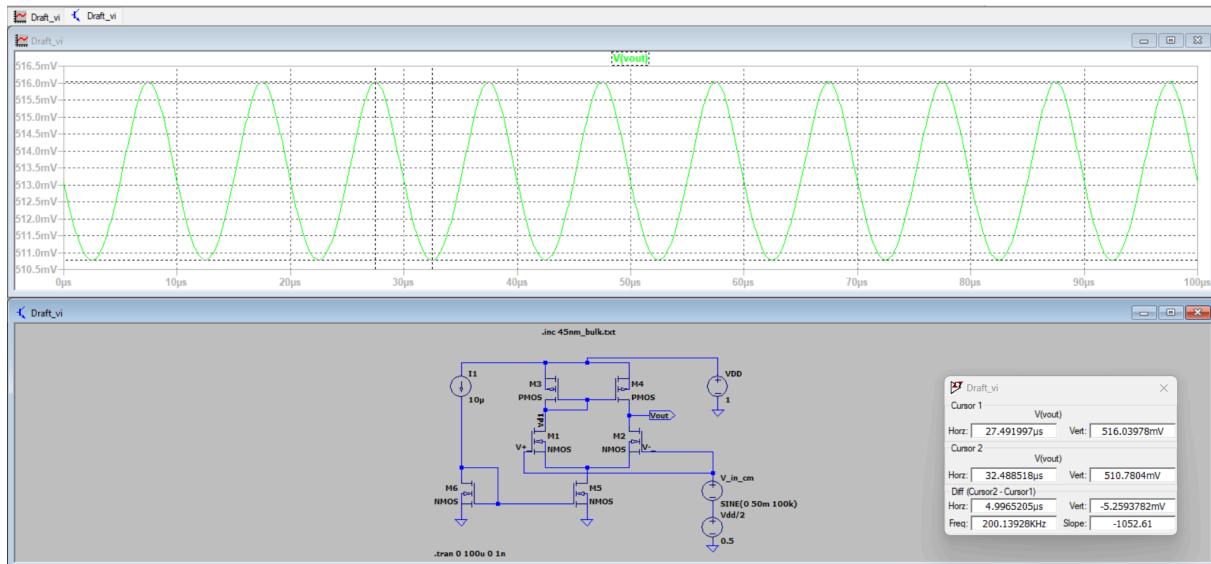
So, maximum peak to peak differential signal is 52mVpp sinusoid with 100kHz frequency.



After 52mVpp, sinusoid is distorted.

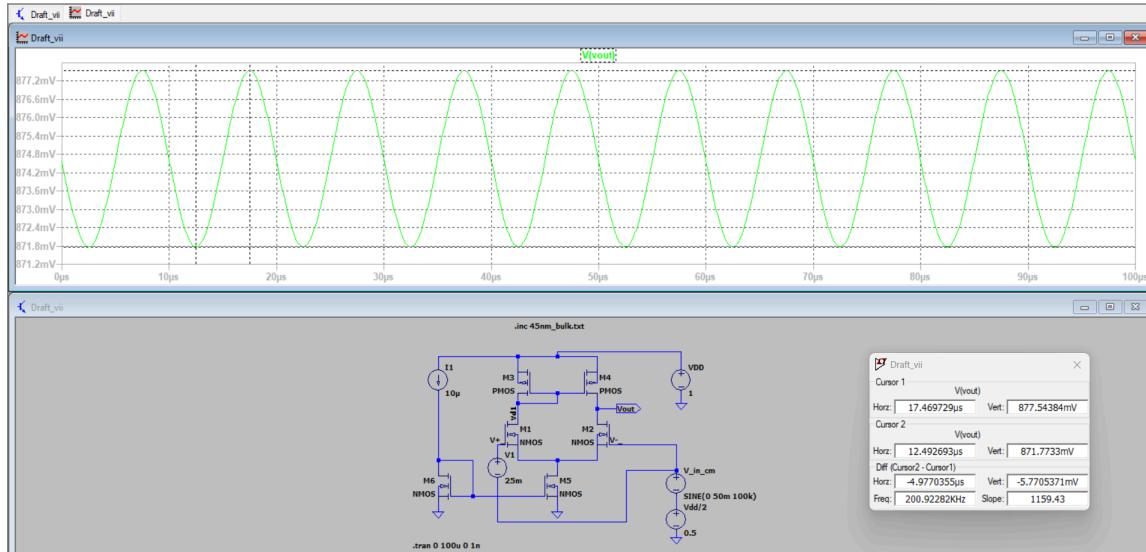


(vi) Find the common mode gain for bias condition in (iii), by applying a 50mV common-mode AC signal at the input. Plot the waveform.



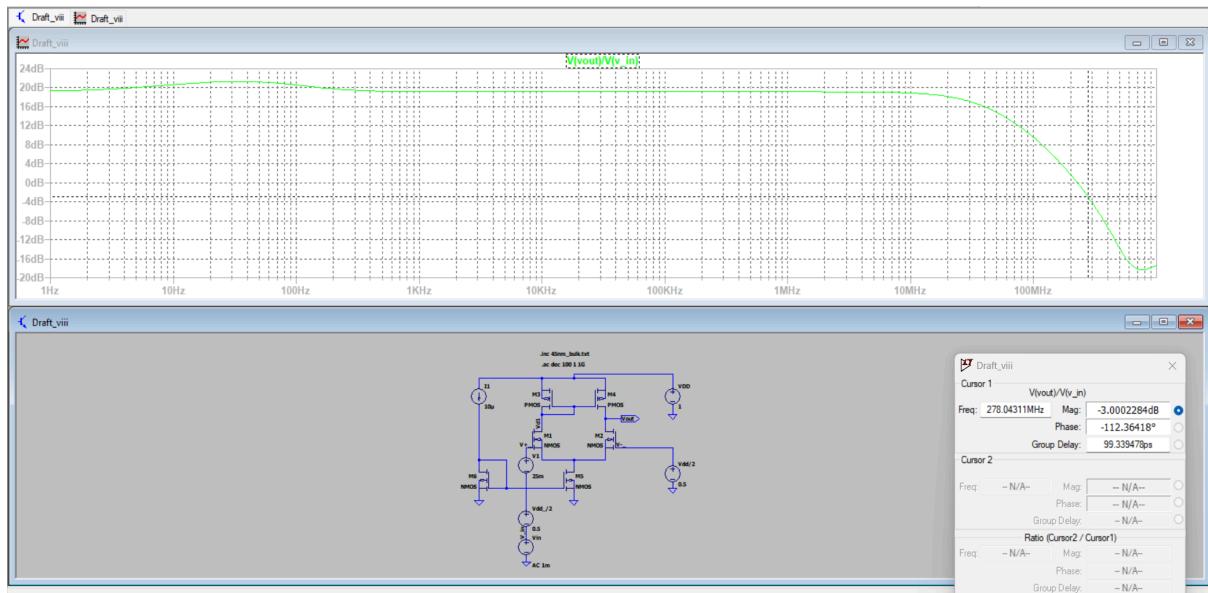
$$\text{Common mode gain} = 0.05259$$

(vii) Add a DC voltage of 25mV in series with gate of M1, emulating a v_{th} mismatch, find the common mode gain again. Plot the waveform.



Common mode gain = 0.05771

(viii) Obtain the AC gain magnitude plot and find the 3dB cutoff frequency.



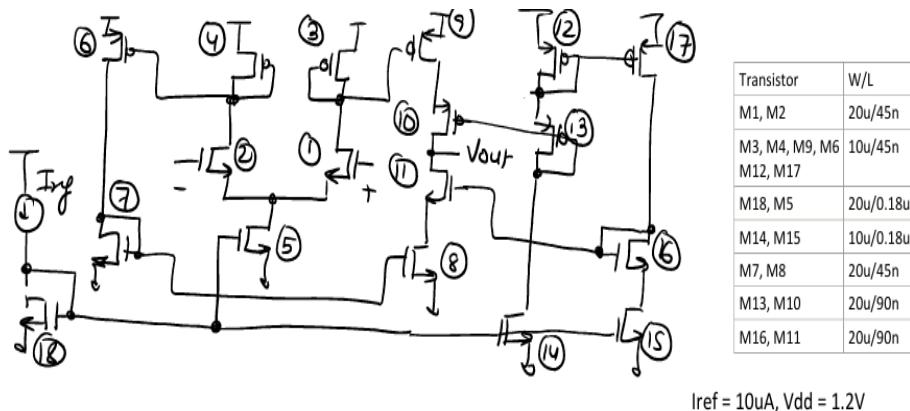
AC gain plot

Gain = 19.15 dB

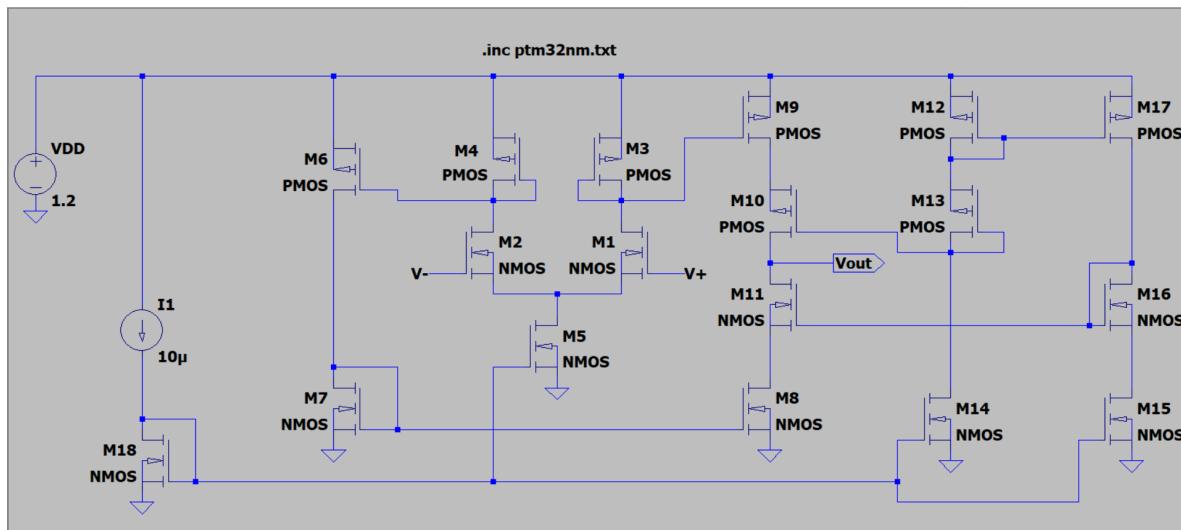
3 dB cut-off frequency = 278.043 MHz

(ix) Adjust the circuit design parameters (you can change bias current as well as device sizes) Increase the gain by at least 4x and obtain the modified 3dB cutoff frequency.

Assignment 4 VLSI :

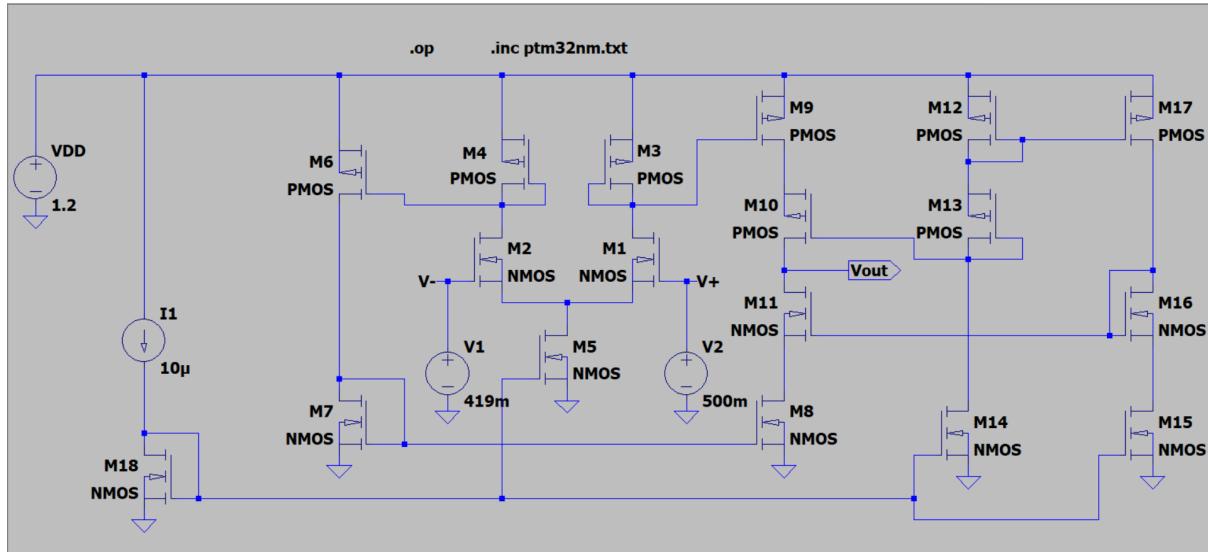


a) Design the 2-stage OPAMP as shown in the figure, with specified sizes



b) Select the input common-mode DC such that the output DC is close to 0.5VDD. Check the DC currents and voltages and ensure that biasing is consistent in all branches.

Here, I selected $V+ = 500mV$ & $V- = 419mV$



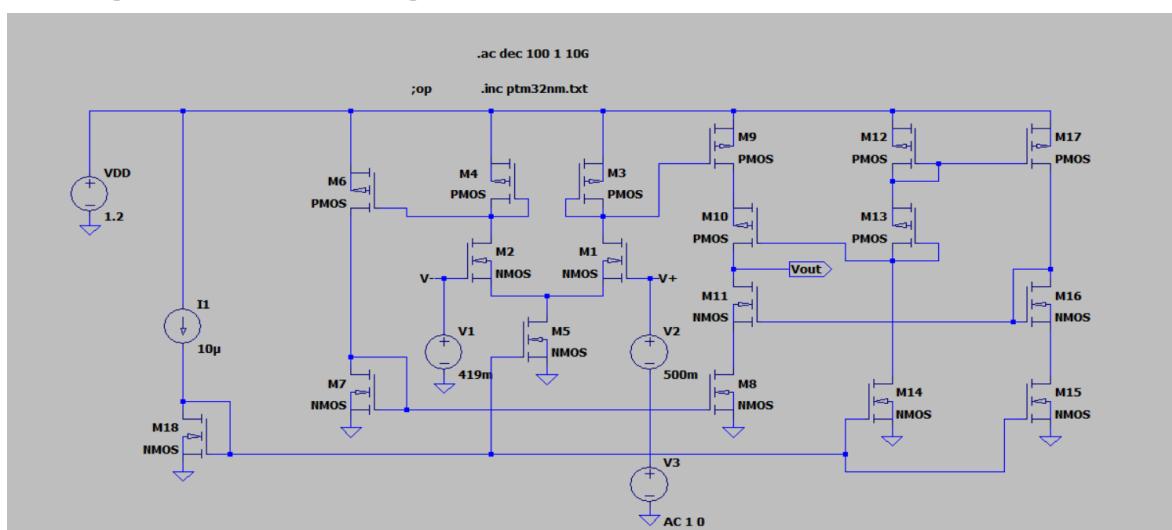
--- Operating Point ---

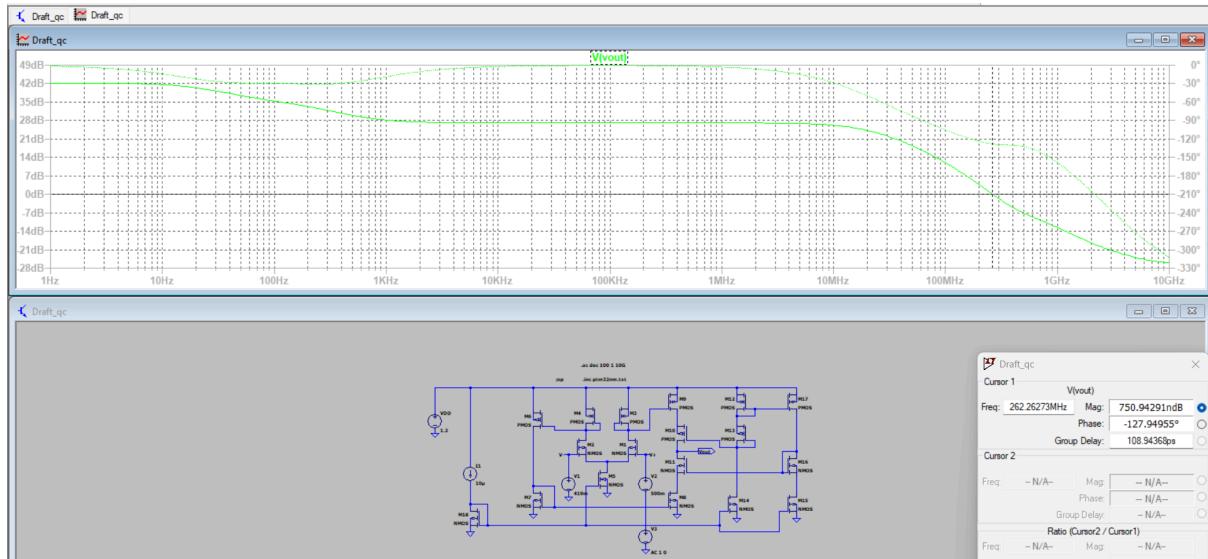
V(n005) :	0.845043	voltage	V (m1#dbody) :	0.358075	voltage
V(v+) :	0.5	voltage	V (m1#sbody) :	0.358075	voltage
V(n018) :	0.258806	voltage	V (m2#dbody) :	0.36168	voltage
V(n017) :	0.358075	voltage	V (m2#sbody) :	0.36168	voltage
V(v-) :	0.419	voltage	V (m3#dbody) :	0.132507	voltage
V(n010) :	0.916095	voltage	V (m3#sbody) :	0.132507	voltage
V(n016) :	0.36168	voltage	V (m4#dbody) :	0.0815981	voltage
V(n001) :	1.2	voltage	V (m4#sbody) :	0.0815981	voltage
V(n008) :	1.0756	voltage	V (m5#dbody) :	0.119249	voltage
V(n007) :	1.0775	voltage	V (m5#sbody) :	0.119249	voltage
V(n022) :	0.349351	voltage	V (m6#dbody) :	0.531233	voltage
V(n023) :	0.132507	voltage	V (m6#sbody) :	0.531233	voltage
V(n021) :	0.236732	voltage	V (m7#dbody) :	0.144787	voltage
V(n009) :	1.0651	voltage	V (m7#sbody) :	0.144787	voltage
V(n026) :	0.0815981	voltage	V (m8#dbody) :	0.144787	voltage
V(n024) :	0.519322	voltage	V (m8#sbody) :	0.144787	voltage
V(n027) :	0.119249	voltage	V (m9#dbody) :	0.14772	voltage
V(n011) :	0.882848	voltage	V (m9#sbody) :	0.14772	voltage
V(n002) :	1.0764	voltage	V (m10#dbody) :	0.574513	voltage
V(n014) :	0.493616	voltage	V (m10#sbody) :	0.574513	voltage
V(vout) :	0.633794	voltage	V (m11#dbody) :	0.136624	voltage
V(n012) :	0.764809	voltage	V (m11#sbody) :	0.136624	voltage
V(n015) :	0.851614	voltage	V (m12#dbody) :	1.0651	voltage
V(n019) :	0.531233	voltage	V (m12#sbody) :	1.0651	voltage
V(n006) :	0.863553	voltage	V (m13#dbody) :	1.0764	voltage
V(n003) :	1.07614	voltage	V (m13#sbody) :	1.0764	voltage
V(n013) :	0.743752	voltage	V (m14#dbody) :	0.764809	voltage
V(n028) :	0.144787	voltage	V (m14#sbody) :	0.764809	voltage
V(n025) :	0.542982	voltage	V (m15#dbody) :	1.07614	voltage
V(n029) :	0.14772	voltage	V (m15#sbody) :	1.07614	voltage
V(n020) :	0.574513	voltage	V (m16#dbody) :	0.743752	voltage
V(n004) :	1.07589	voltage	V (m16#sbody) :	0.743752	voltage
V(n030) :	0.136624	voltage	V (m17#dbody) :	1.07589	voltage
			V (m17#sbody) :	1.07589	voltage

Id (M1) :	8.36896e-06	device_current	Id (M3) :	8.36896e-06	device_current
Ig (M1) :	-3.86302e-10	device_current	Ig (M3) :	-2.23113e-14	device_current
Id (M1) :	-3.58088e-13	device_current	Id (M3) :	-1.07557e-12	device_current
Is (M1) :	-8.36857e-06	device_current	Is (M3) :	-8.36896e-06	device_current
Id (M2) :	1.35118e-06	device_current	Id (M4) :	1.35118e-06	device_current
Ig (M2) :	-1.07432e-09	device_current	Ig (M4) :	-1.13662e-14	device_current
Id (M2) :	-3.61691e-13	device_current	Id (M4) :	-1.07745e-12	device_current
Is (M2) :	-1.35011e-06	device_current	Is (M4) :	-1.35118e-06	device_current
Id (M5) :	9.71868e-06	device_current	Id (M6) :	4.54423e-06	device_current
Ig (M5) :	8.19781e-11	device_current	Ig (M6) :	4.99635e-14	device_current
Id (M5) :	-1.32499e-13	device_current	Id (M6) :	-1.06503e-12	device_current
Is (M5) :	-9.71876e-06	device_current	Is (M6) :	-4.54423e-06	device_current
Id (M7) :	4.54445e-06	device_current	Id (M9) :	7.89439e-06	device_current
Ig (M7) :	1.55268e-11	device_current	Ig (M9) :	-2.23918e-14	device_current
Id (M7) :	-8.15918e-14	device_current	Id (M9) :	-1.07638e-12	device_current
Is (M7) :	-4.54446e-06	device_current	Is (M9) :	-7.89439e-06	device_current
Id (M8) :	7.89446e-06	device_current	Id (M10) :	7.89439e-06	device_current
Ig (M8) :	-2.34875e-10	device_current	Ig (M10) :	-1.6869e-13	device_current
Id (M8) :	-1.19248e-13	device_current	Id (M10) :	-7.64806e-13	device_current
Is (M8) :	-7.89422e-06	device_current	Is (M10) :	-7.89439e-06	device_current
Id (M11) :	7.89439e-06	device_current	Id (M12) :	5.26803e-06	device_current
Id (M11) :	7.21796e-11	device_current	Ig (M12) :	-1.8736e-14	device_current
Id (M11) :	-5.31267e-13	device_current	Id (M12) :	-1.07606e-12	device_current
Is (M11) :	-7.89446e-06	device_current	Is (M12) :	-5.26803e-06	device_current
Id (M14) :	5.26803e-06	device_current	Id (M13) :	5.26803e-06	device_current
Ig (M14) :	6.3469e-12	device_current	Ig (M13) :	-1.39354e-13	device_current
Id (M14) :	-1.44789e-13	device_current	Id (M13) :	-7.43763e-13	device_current
Is (M14) :	-5.26803e-06	device_current	Is (M13) :	-5.26803e-06	device_current
Id (M15) :	5.3673e-06	device_current	Id (M17) :	5.36737e-06	device_current
Ig (M15) :	-1.75274e-11	device_current	Ig (M17) :	-1.86983e-14	device_current
Id (M15) :	-1.47727e-13	device_current	Id (M17) :	-1.07578e-12	device_current
Is (M15) :	-5.36728e-06	device_current	Is (M17) :	-5.36737e-06	device_current
Id (M16) :	5.36725e-06	device_current	I (I1) :	1e-05	device_current
Ig (M16) :	4.66479e-11	device_current	I (Vdd) :	-4.27942e-05	device_current
Id (M16) :	-5.74499e-13	device_current	I (V1) :	1.07432e-09	device_current
Is (M16) :	-5.3673e-06	device_current	I (V2) :	3.86302e-10	device_current

Above are all the operating values of currents and voltages

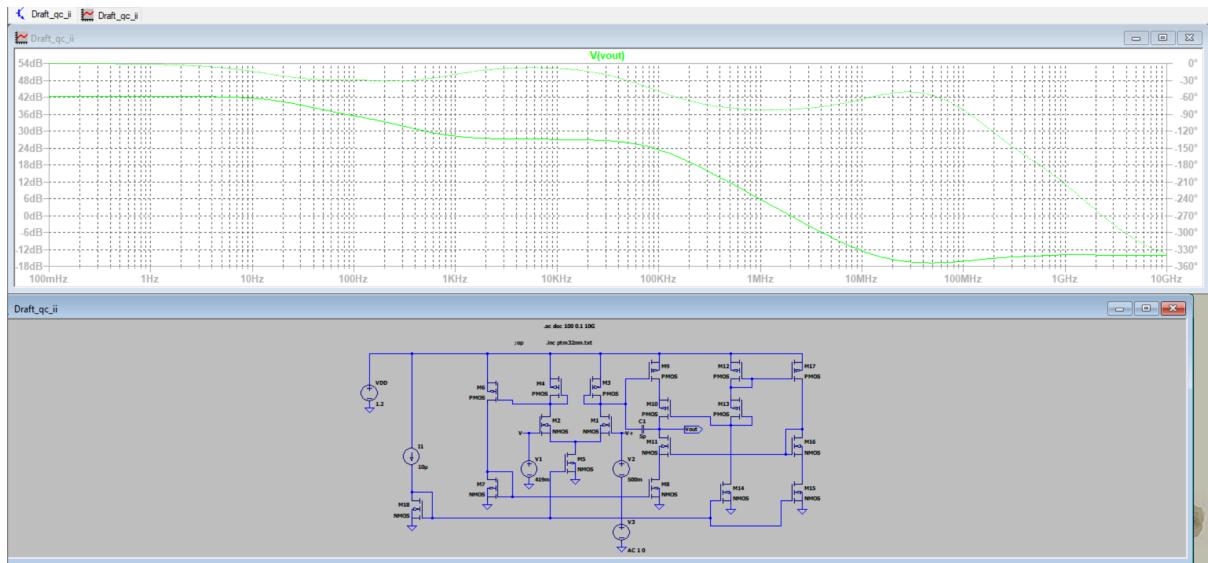
c) Apply a small signal AC and check the gain magnitude plot. Find the phase margin. Use compensation cap at output to obtain phase margin of 45 degrees.



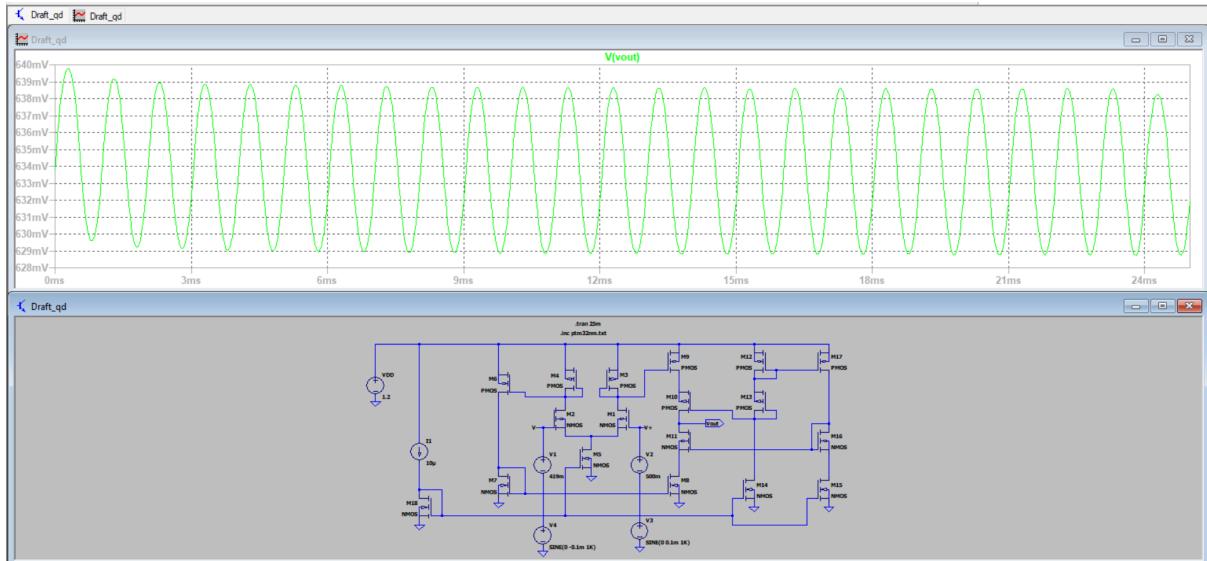


Phase margin = 127.9 degrees

After using compensation capacitor 5pF, I got phase margin 81 degrees but not less than that



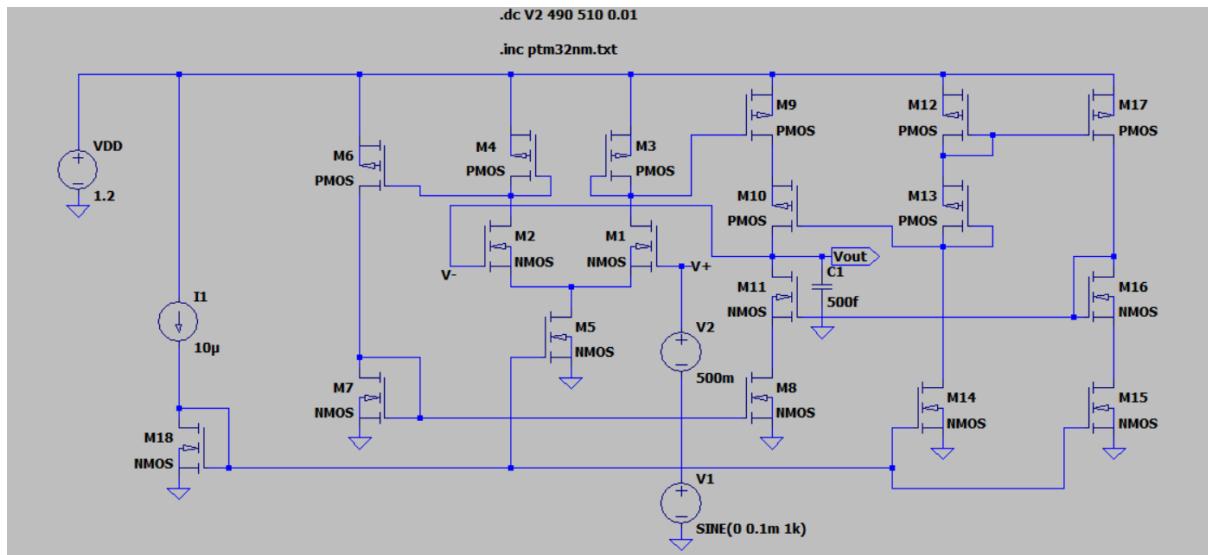
d) Apply an appropriate sinusoid signal at input and plot the output for a frequency of 1KHz.



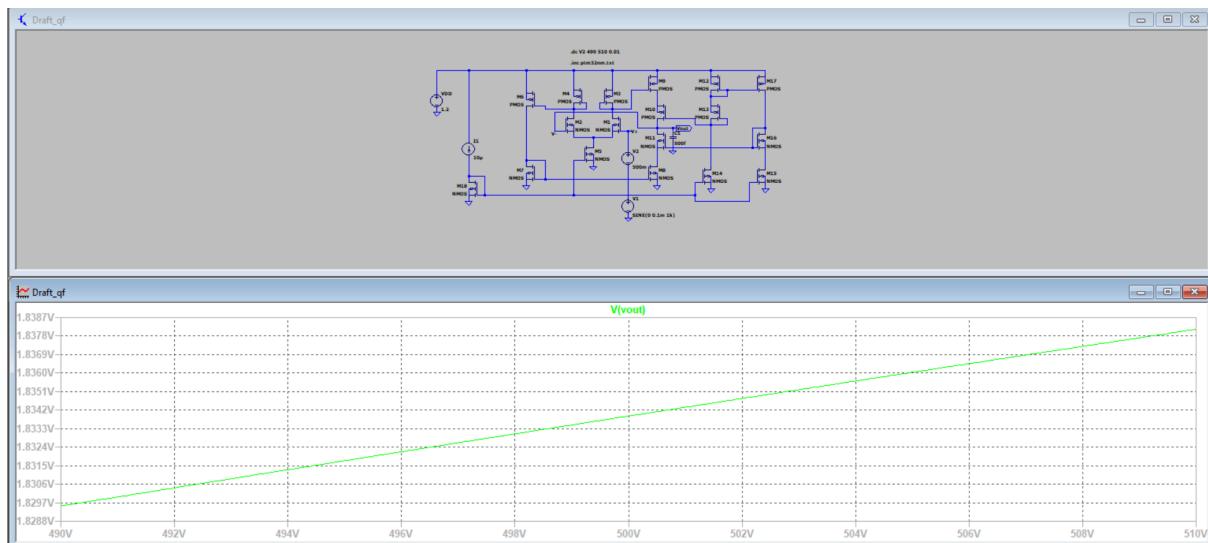
Here, I applied differential signal of 0.1mV amplitude with previous DC biases.

e) Try to increase the open loop gain by at least 4x by modifying the sizes.

f) Connect the amplifier in unity gain configuration and obtain the input output characteristics for unity gain operation.



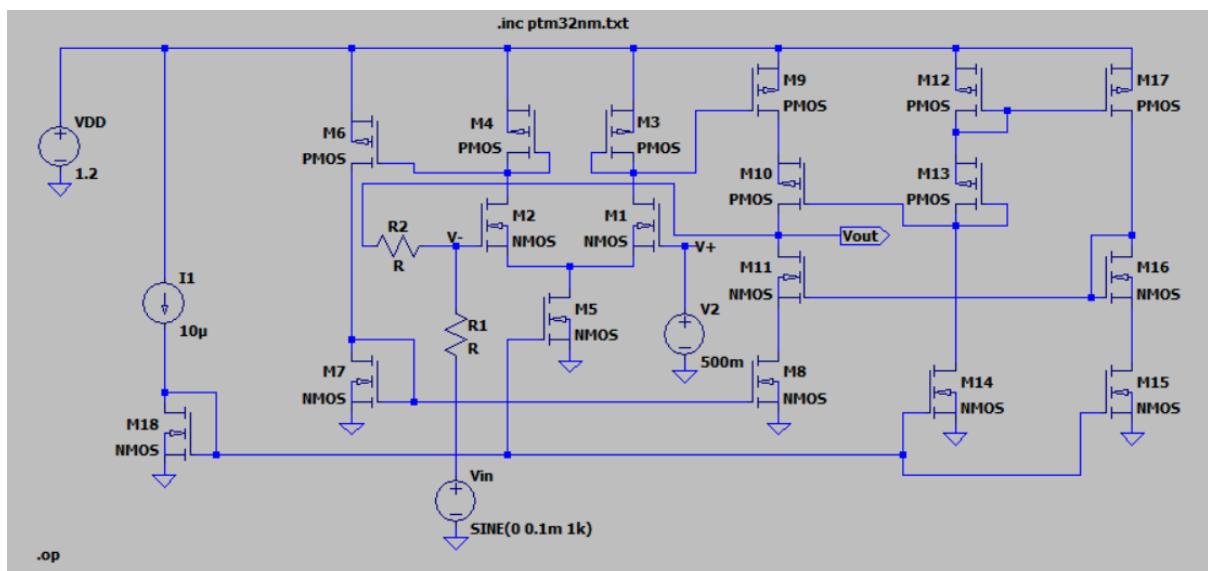
Unity gain configuration



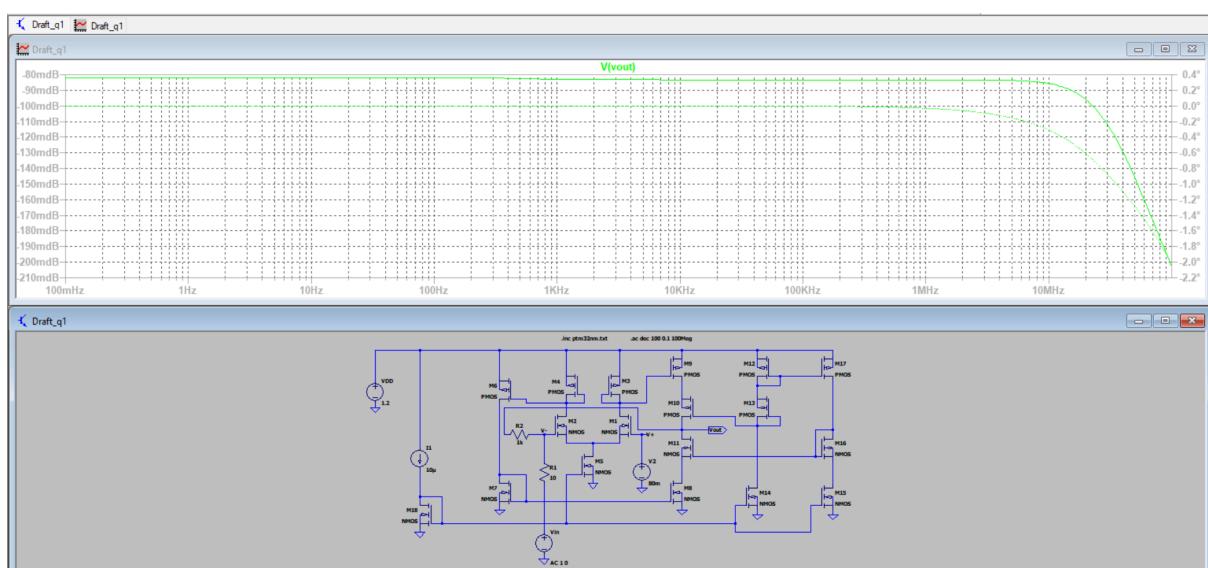
Input Output Characteristics for Unity Gain Operation

Assignment 5 VLSI :

1. Design negative feedback amplifier with resistive load and try to establish the right DC point for input. Check the effect of change in input DC point on the out DC and gain.

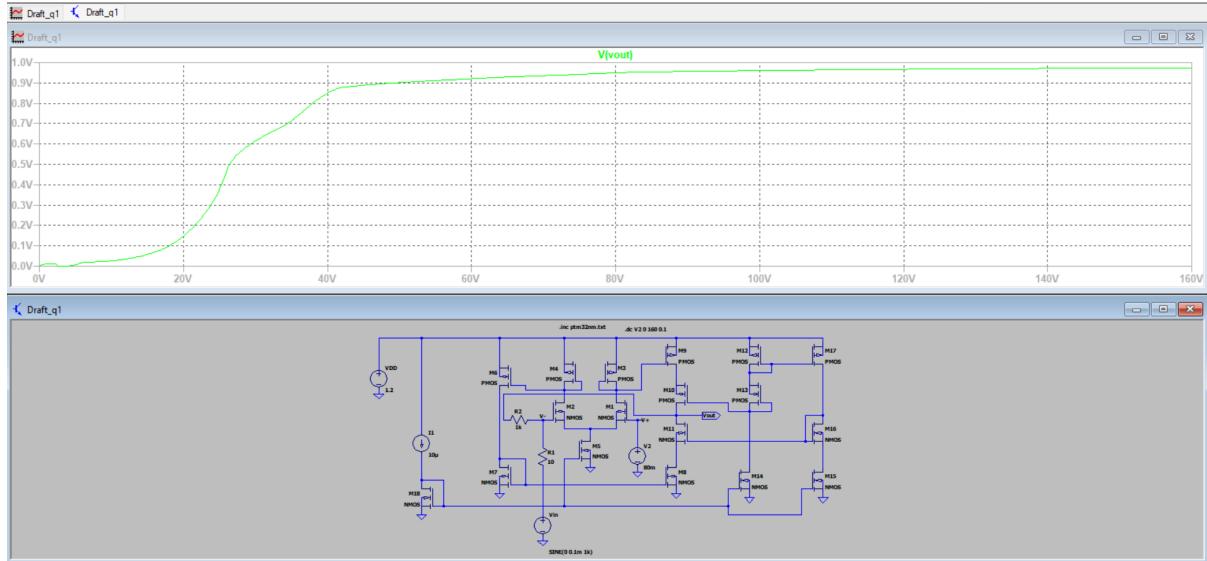


Negative feedback amplifier with resistive load



Gain with small signal AC analysis

On increasing input DC, gain slightly increases. Also, output voltage follows the below trend with input DC.



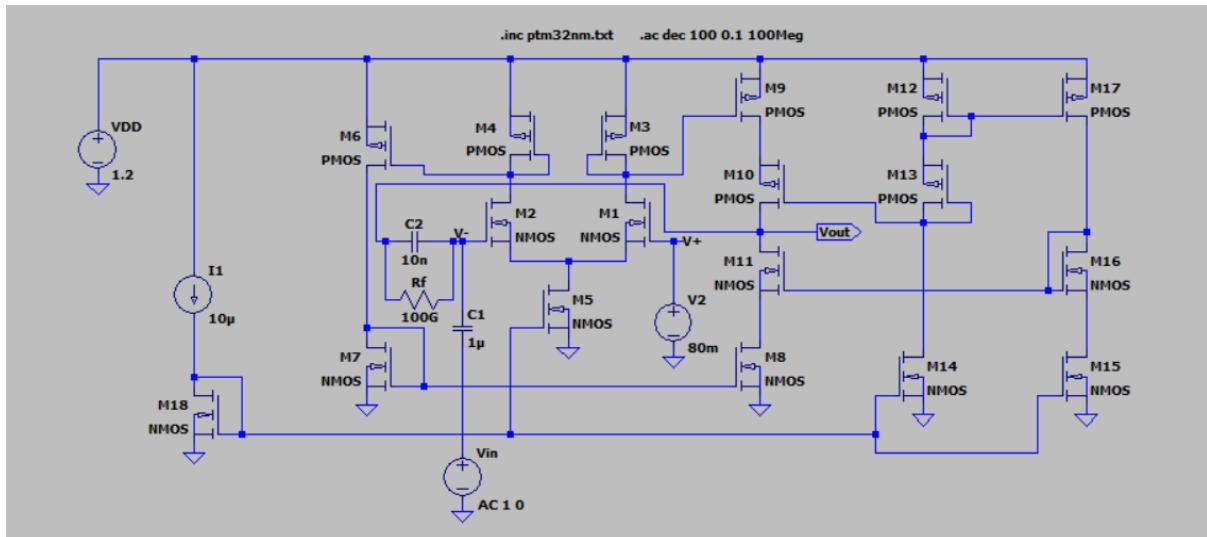
--- Operating Point ---

$V(n005)$:	0.964887	voltage	$V(m1\#dbody)$:	0.144086	voltage
$V(v+)$:	0.08	voltage	$V(m1\#sbody)$:	0.144086	voltage
$V(n018)$:	0.00151599	voltage	$V(m2\#dbody)$:	0.146387	voltage
$V(n017)$:	0.144086	voltage	$V(m2\#sbody)$:	0.146387	voltage
$V(n010)$:	1.02423	voltage	$V(m5\#dbody)$:	0.0916616	voltage
$V(v-)$:	5.52561e-06	voltage	$V(m5\#sbody)$:	0.0916616	voltage
$V(n016)$:	0.146387	voltage	$V(m7\#dbody)$:	0.0541728	voltage
$V(n001)$:	1.2	voltage	$V(m7\#sbody)$:	0.0541728	voltage
$V(n008)$:	1.07868	voltage	$V(m8\#dbody)$:	0.0101956	voltage
$V(n007)$:	1.08013	voltage	$V(m8\#sbody)$:	0.0101956	voltage
$V(n022)$:	0.349351	voltage	$V(m11\#dbody)$:	0.278821	voltage
$V(n023)$:	0.0916616	voltage	$V(m11\#sbody)$:	0.278821	voltage
$V(n021)$:	0.147449	voltage	$V(m14\#dbody)$:	0.144787	voltage
$V(n009)$:	1.06351	voltage	$V(m14\#sbody)$:	0.144787	voltage
$V(n026)$:	0.0541728	voltage	$V(m15\#dbody)$:	0.147532	voltage
$V(n024)$:	0.000544788	voltage	$V(m15\#sbody)$:	0.147532	voltage
$V(n027)$:	0.0101956	voltage	$V(m16\#dbody)$:	0.571726	voltage
$V(n011)$:	0.762053	voltage	$V(m16\#sbody)$:	0.571726	voltage
$V(n002)$:	1.07451	voltage	$V(m18\#dbody)$:	0.136624	voltage
$V(n014)$:	0.493617	voltage	$V(m18\#sbody)$:	0.136624	voltage
$V(vout)$:	0.00054448	voltage	$V(m3\#dbody)$:	1.07868	voltage
$V(n012)$:	0.637904	voltage	$V(m3\#sbody)$:	1.07868	voltage
$V(n015)$:	0.848163	voltage	$V(m4\#dbody)$:	1.08013	voltage
$V(n019)$:	0.278821	voltage	$V(m4\#sbody)$:	1.08013	voltage
$V(n006)$:	0.863554	voltage	$V(m6\#dbody)$:	1.06351	voltage
$V(n003)$:	1.07614	voltage	$V(m6\#sbody)$:	1.06351	voltage
$V(n013)$:	0.743752	voltage	$V(m9\#dbody)$:	1.07451	voltage
$V(n028)$:	0.144787	voltage	$V(m9\#sbody)$:	1.07451	voltage
$V(n025)$:	0.539702	voltage	$V(m10\#dbody)$:	0.637904	voltage
$V(n029)$:	0.147532	voltage	$V(m10\#sbody)$:	0.637904	voltage
$V(n020)$:	0.571726	voltage	$V(m12\#dbody)$:	1.07614	voltage
$V(n004)$:	1.07582	voltage	$V(m12\#sbody)$:	1.07614	voltage
$V(n030)$:	0.136624	voltage	$V(m13\#dbody)$:	0.743752	voltage
$V(n031)$:	0	voltage	$V(m13\#sbody)$:	0.743752	voltage
			$V(m17\#dbody)$:	1.07582	voltage
			$V(m17\#sbody)$:	1.07582	voltage

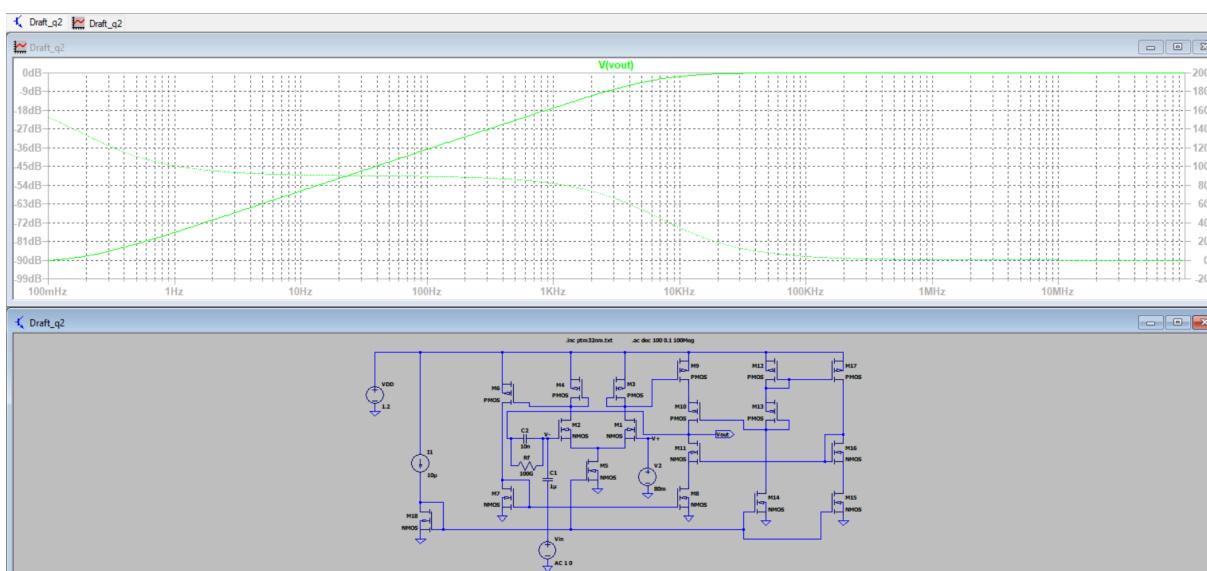
Id(M1) :	3.60418e-07	device_current	Is(M18) :	-9.99986e-06	device_current
Ig(M1) :	-7.49338e-09	device_current	Id(M3) :	3.60419e-07	device_current
Ib(M1) :	-1.44086e-13	device_current	Ig(M3) :	-6.66457e-15	device_current
Is(M1) :	-3.52925e-07	device_current	Ib(M3) :	-1.07866e-12	device_current
Id(M2) :	6.81899e-08	device_current	Is(M3) :	-3.60418e-07	device_current
Ig(M2) :	-1.36066e-08	device_current	Id(M4) :	6.81912e-08	device_current
Ib(M2) :	-1.46389e-13	device_current	Ig(M4) :	-2.62899e-15	device_current
Is(M2) :	-5.45832e-08	device_current	Ib(M4) :	-1.08008e-12	device_current
Id(M5) :	4.07508e-07	device_current	Is(M4) :	-6.81901e-08	device_current
Ig(M5) :	1.4873e-10	device_current	Id(M6) :	3.87613e-07	device_current
Ib(M5) :	-9.16607e-14	device_current	Ig(M6) :	2.01609e-13	device_current
Is(M5) :	-4.07657e-07	device_current	Ib(M6) :	-1.06348e-12	device_current
Id(M7) :	3.87606e-07	device_current	Is(M6) :	-3.87612e-07	device_current
Ig(M7) :	1.84087e-12	device_current	Id(M9) :	5.08419e-07	device_current
Ib(M7) :	-5.41726e-14	device_current	Ig(M9) :	-5.06342e-15	device_current
Is(M7) :	-3.87608e-07	device_current	Ib(M9) :	-1.07441e-12	device_current
Id(M8) :	4.93677e-09	device_current	Is(M9) :	-5.08418e-07	device_current
Ig(M8) :	3.71866e-12	device_current	Id(M10) :	5.08418e-07	device_current
Ib(M8) :	-1.01958e-14	device_current	Ig(M10) :	-1.80081e-14	device_current
Is(M8) :	-4.94047e-09	device_current	Ib(M10) :	-6.37859e-13	device_current
Id(M11) :	-3.05369e-08	device_current	Is(M10) :	-5.08417e-07	device_current
Ig(M11) :	3.54739e-08	device_current	Id(M12) :	5.26799e-06	device_current
Ib(M11) :	-2.78816e-13	device_current	Ig(M12) :	-1.87355e-14	device_current
Is(M11) :	-4.93677e-09	device_current	Ib(M12) :	-1.07619e-12	device_current
Id(M14) :	5.26799e-06	device_current	Is(M12) :	-5.26799e-06	device_current
Ig(M14) :	6.34612e-12	device_current	Id(M13) :	5.26799e-06	device_current
Ib(M14) :	-1.44785e-13	device_current	Ig(M13) :	-1.39354e-13	device_current
Is(M14) :	-5.268e-06	device_current	Ib(M13) :	-7.43775e-13	device_current
Id(M15) :	5.36081e-06	device_current	Is(M13) :	-5.26799e-06	device_current
Ig(M15) :	-1.56638e-11	device_current	Id(M17) :	5.39629e-06	device_current
Ib(M15) :	-1.47536e-13	device_current	Ig(M17) :	-1.86864e-14	device_current
Is(M15) :	-5.3608e-06	device_current	Ib(M17) :	-1.07574e-12	device_current
Id(M16) :	5.36077e-06	device_current	Is(M17) :	-5.39629e-06	device_current
Ig(M16) :	4.65481e-11	device_current	I(I1) :	1e-05	device_current
Ib(M16) :	-5.71725e-13	device_current	I(R1) :	5.52561e-07	device_current
Is(M16) :	-5.36081e-06	device_current	I(R2) :	-5.38954e-07	device_current
Id(M18) :	9.99978e-06	device_current	I(Vdd) :	-2.19889e-05	device_current
Ig(M18) :	7.65525e-11	device_current	I(V2) :	7.49338e-09	device_current
Ib(M18) :	-1.36623e-13	device_current	I(Vin) :	5.52561e-07	device_current
Is(M18) :	-9.99986e-06	device_current			

DC operating points

2. Design capacitive feedback amplifier with very large ideal Rf (100Gohm) , check the AC gain. Check the effect of changing Rf on AC response.



capacitive feedback amplifier with very large ideal Rf (100Gohm)



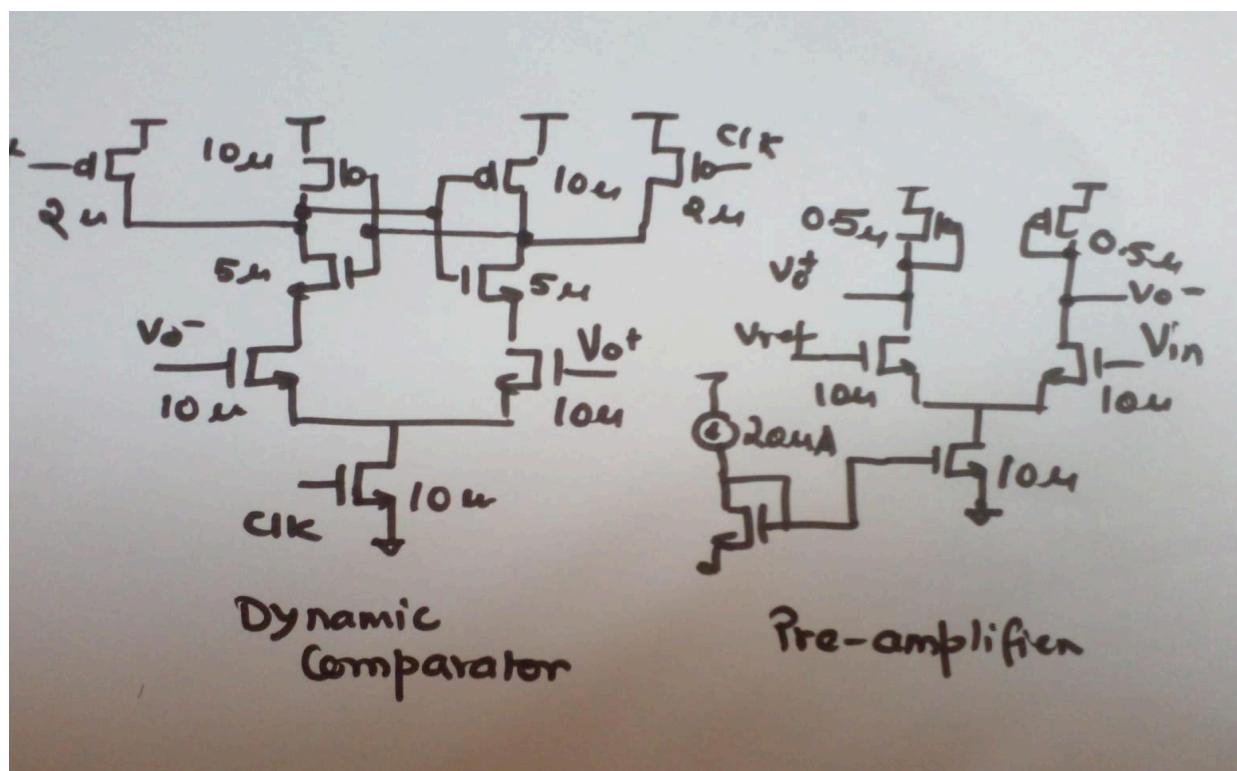
AC gain with small signal (AC) response

Gain almost remains same with different Rf, but the curve slightly shifted leftwards with higher resistance

Assignment 6 VLSI :

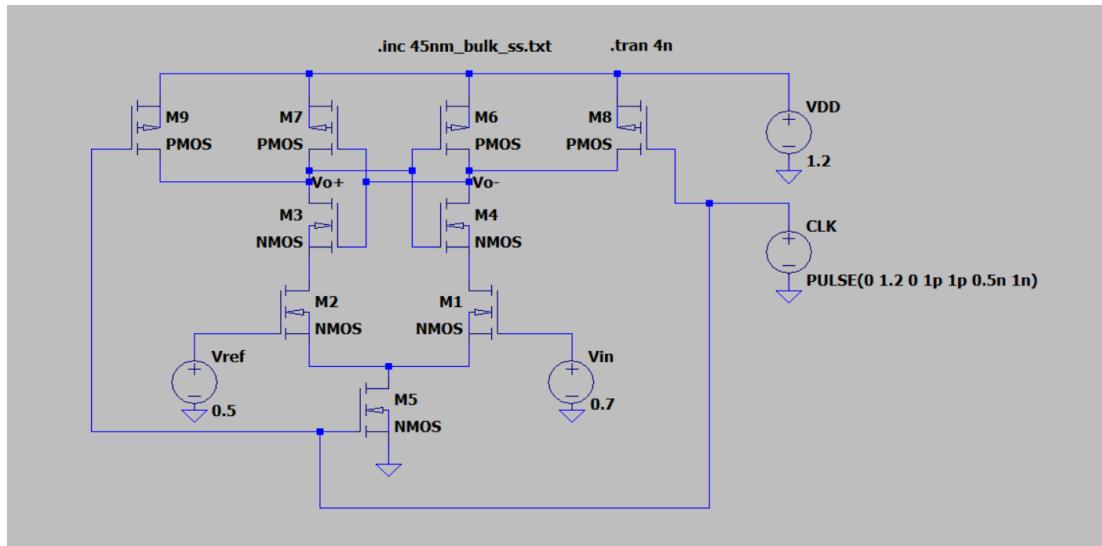
Simulate a dynamic comparator with and without a pre-amplifier.

Try to observe the resolution in both cases.
Also, obtain the max speed of operation.

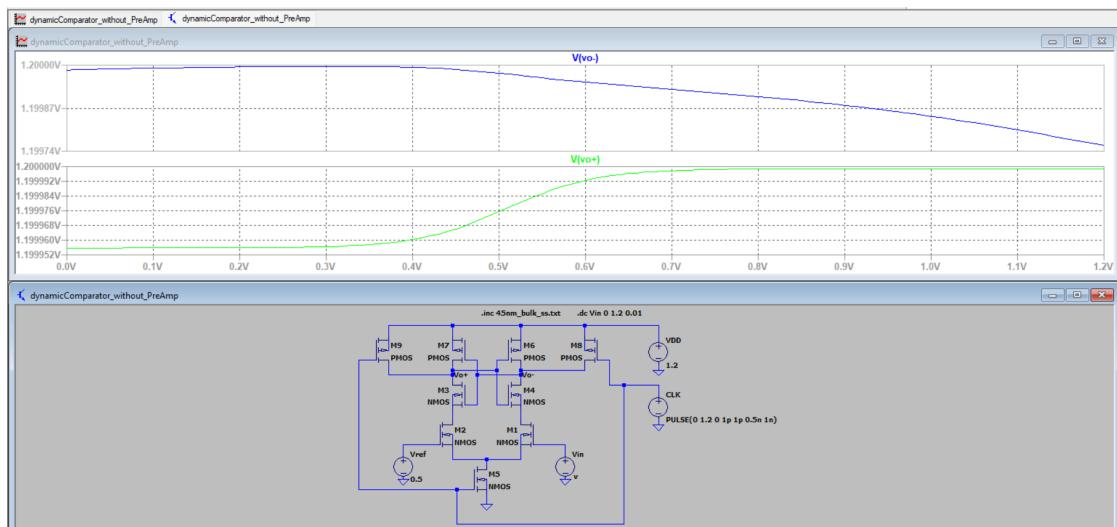


All L values minimum

Dynamic Comparator Without Pre-Amplifier

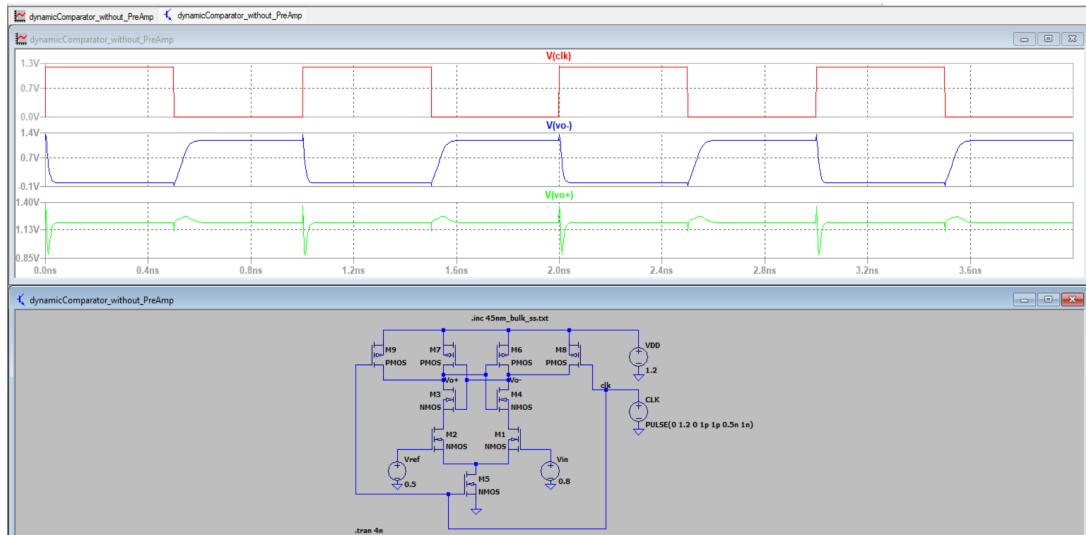


Schematic of the circuit

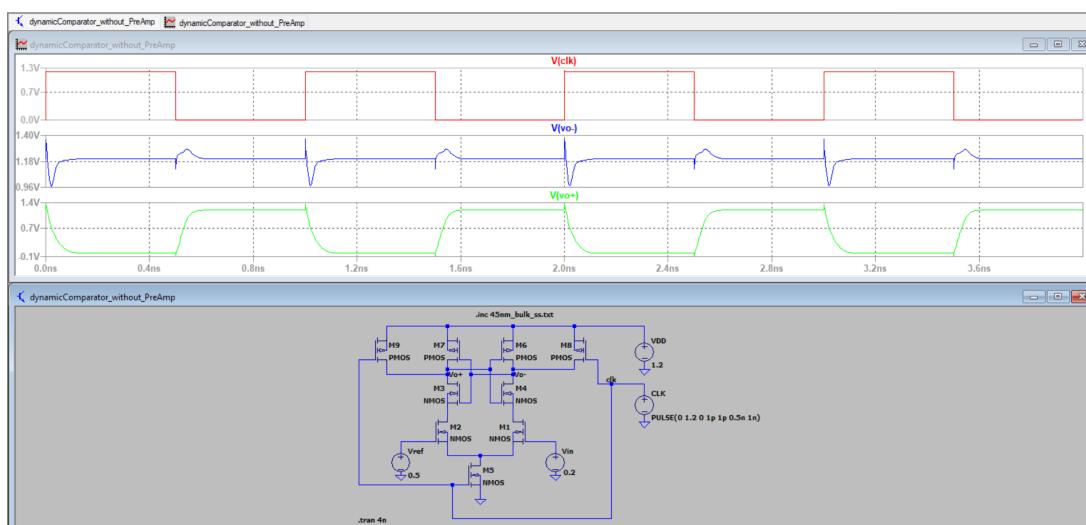


Characteristics Curve

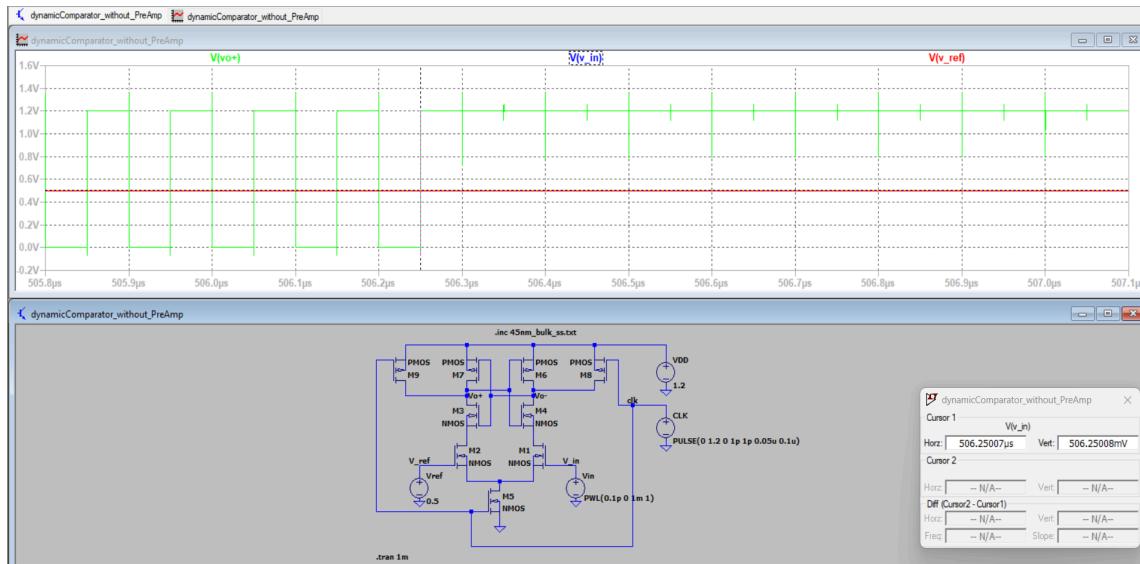
When $V_{in} > V_{ref}$,



When $V_{in} < V_{ref}$,

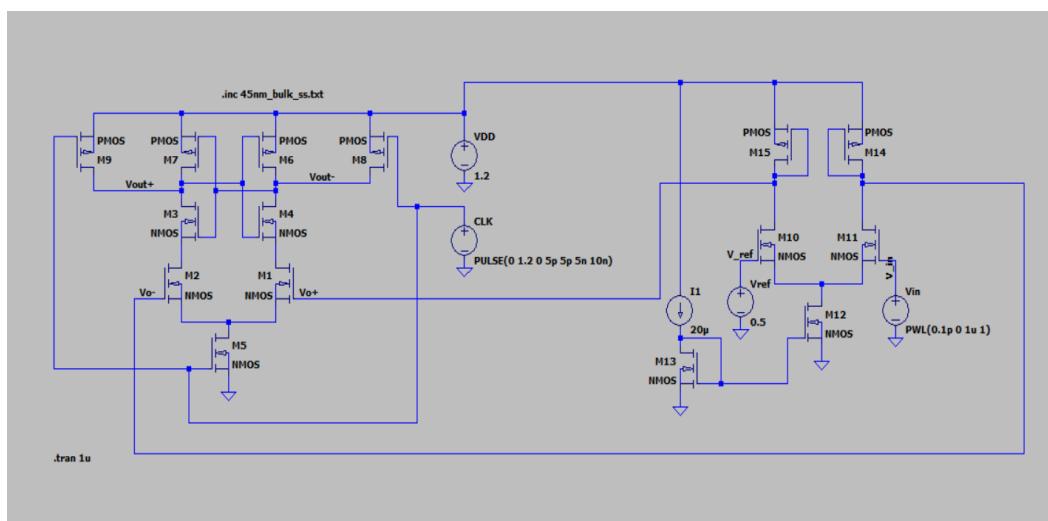


Resolution & Maximum speed of operation,

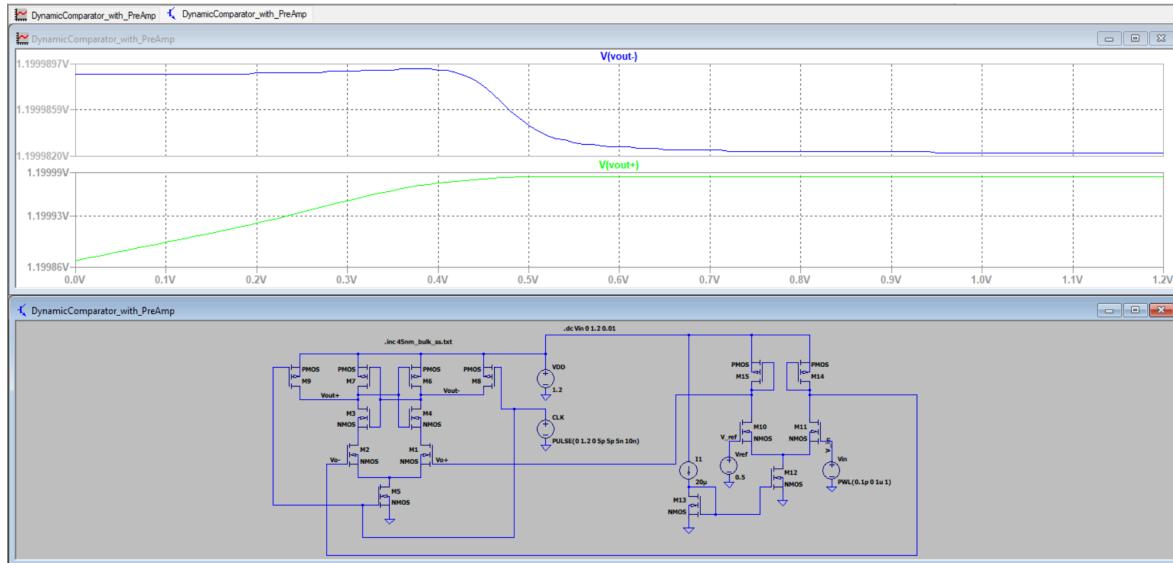


Here, We got the maximum speed of operation at 10 MHz. Resolution at that frequency is 6.25 mV.

Dynamic Comparator Without Pre-Amplifier

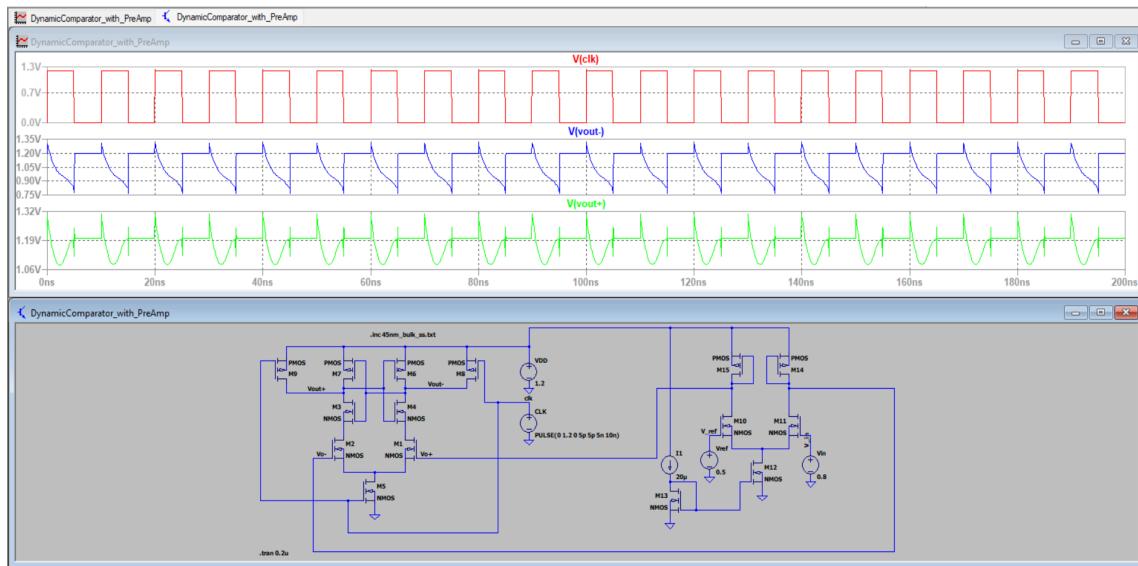


Schematic of the circuit

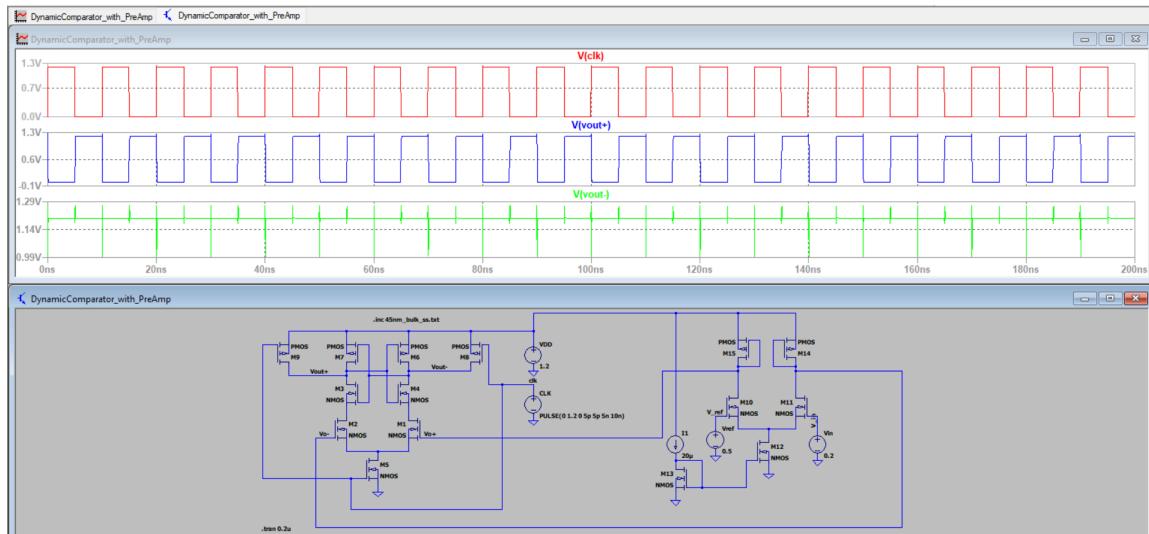


Characteristics Curve

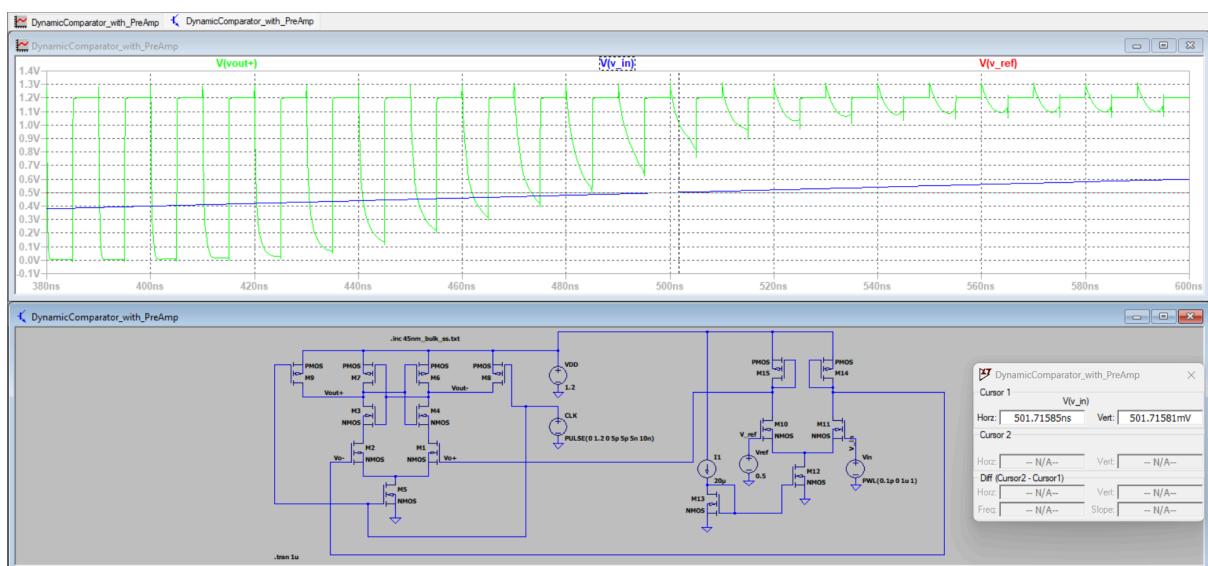
When $V_{in} > V_{ref}$,



When $V_{in} < V_{ref}$,



Resolution & Maximum speed of operation,



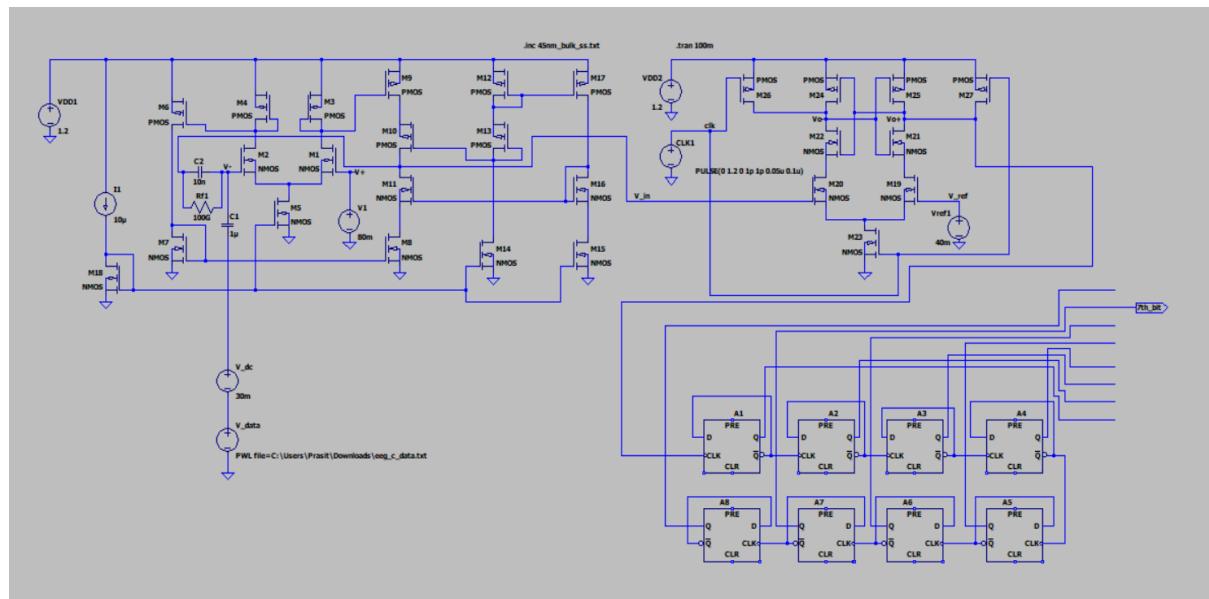
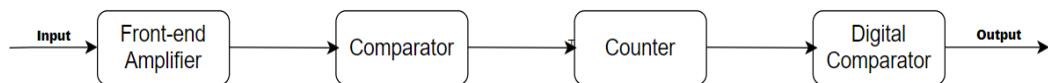
Here, we got the maximum speed of operation at 100MHz. Resolution at that frequency is 1.72 mV.

Assignment 7 VLSI :

Designing of a seizure detection circuit :

Here, I made the circuit using an Amplifier followed by a Comparator and Digital Counter and then a Digital Comparator (in-built in LTSpice).

The block diagram of the circuit is given below:



Schematic of the circuit

This circuit has following specifications:

Amplifier gain = 100

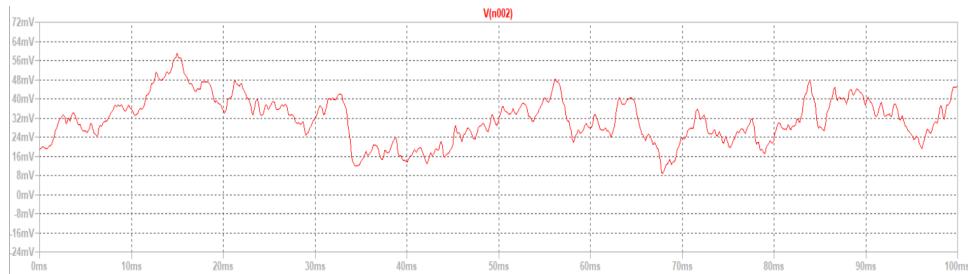
Reference voltage of comparator = 40 mV

Clock frequency of comparator = 100MHz

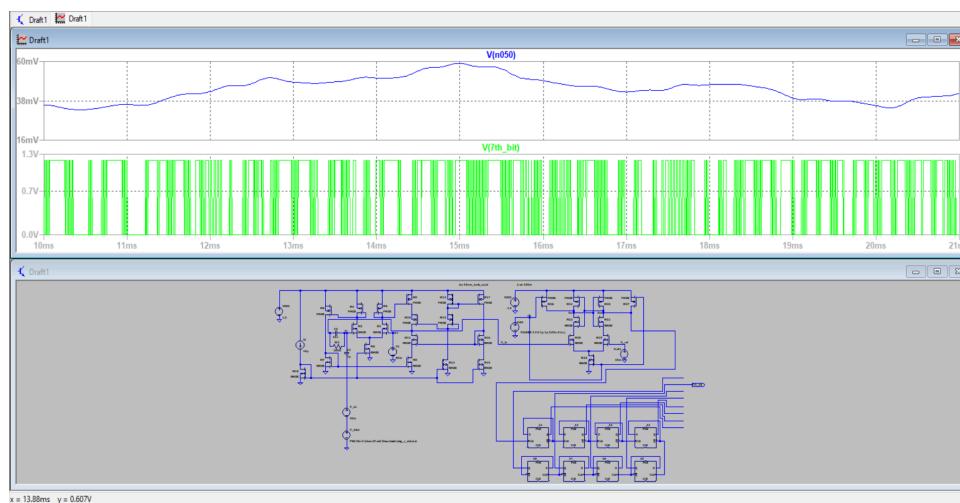
Vdd = 1.2 V

Reference count = 100

Evaluation time = 100 ms



EEG Signal



Output Waveform

In this circuit, we first amplify the input signal which is given using an EEG signal dataset in the form of a PWL file in LTSpice. Then we used a comparator to compare the signal with a pre-specified threshold value. Counter then counts the number of instances when the input signal is greater than the specified value in a pre-defined evaluation time and digital comparator compares the count with a reference count. If the count is higher than the reference count, the output will be high & we can assume that epileptic seizure signal is detected.