Experiment 2: Combinational Circuit 2

Prateek Garg
20D070060
EE-214, WEL, IIT Bombay
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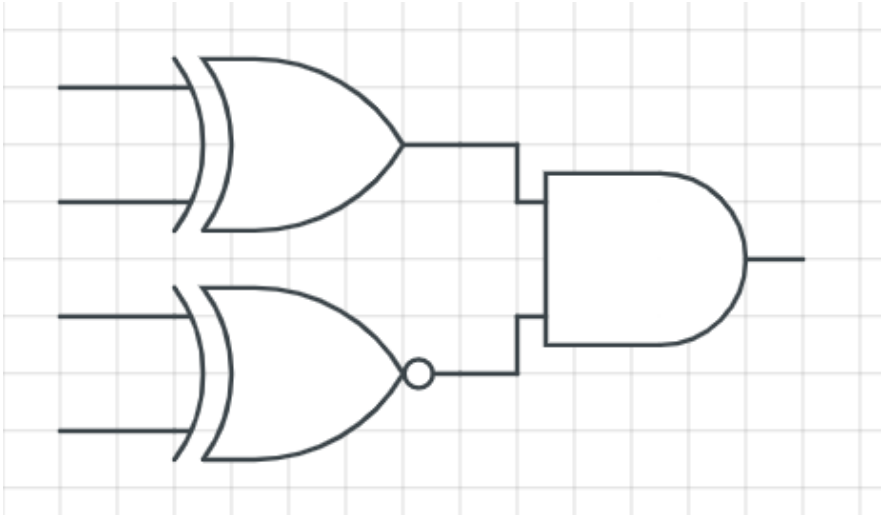
Overview of the experiment:

Objective: Representation of first 16 letters of the English alphabets (i.e. A to P), 0000 represents A, 0001 represents B and so on is provided as input.
Design a system that gives output as '1' when a given alphabet has 3 points, and '0' in other cases. in accordance with the points scores provided in the game Scrabble.

The task is done using VHDL with the software Quartus. Structural modelling was used which means components were instantiated and port mapping is used to describe connections. All the designs were then simulated using ModelSim checked against every possible testcase.

Approach to the experiment:

Design:



First of all, a minterm expression on 4 bits was made which was then subsequently reduced using K' map and boolean algebra. The final expression needed 1 XNOR, 1 XOR and 1 AND gate.
Circuit is drawn using online tool: www.circuitlab.com

Design document and VHDL code:

Architecture:

```
architecture Struct of Scrabble is
  component AND_2 is
   port (A, B: in std_logic; Y: out std_logic);
  end component ;

  component XOR_2 is
   port (A, B: in std_logic; Y: out std_logic);
  end component ;

  component XNOR_2 is
   port (A, B: in std_logic; Y: out std_logic);
  end component ;

  signal t0,t1: std_logic;
begin

  xnor1: XNOR_2 port map(A => X0, B => X1, Y => t0);
  xor1 : XOR_2  port map(A => X2, B => X3, Y => t1);
  and1 : AND_2  port map(A => t0, B => t1, Y => Y);

end Struct;
```

RTL View:

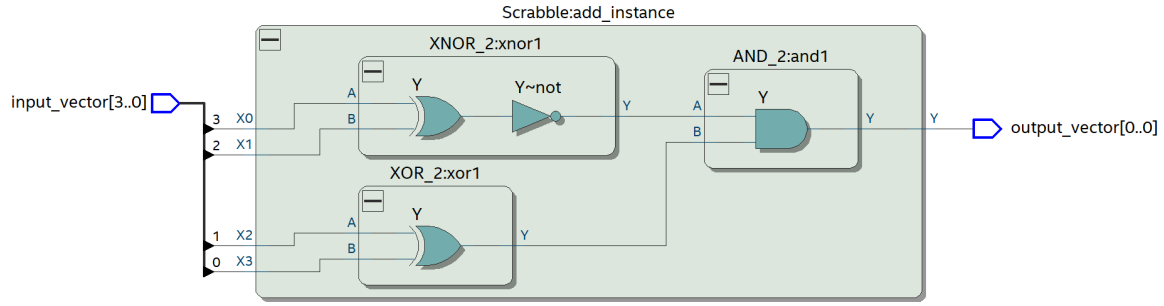


Fig: RTL View.

DUT Input/Output Format:

Port map:

```
--input map
X0 => input_vector(3),
X1 => input_vector(2),
X2 => input_vector(1),
X3 => input_vector(0),

--output map
Y => output_vector(0)
```

Some test cases from TRACEFILE:
TRACEFILE format

<x3 x2 x1 x0> <Y> 1

```
0000 0 1
0001 1 1
0010 1 1
0011 0 1
0100 0 1
0101 0 1
0110 0 1
0111 0 1
1000 0 1
1001 0 1
1010 0 1
1011 0 1
1100 0 1
1101 1 1
1110 1 1
1111 0 1
```

Truth Table:

X3	X2	X1	X0	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

RTL Simulation:

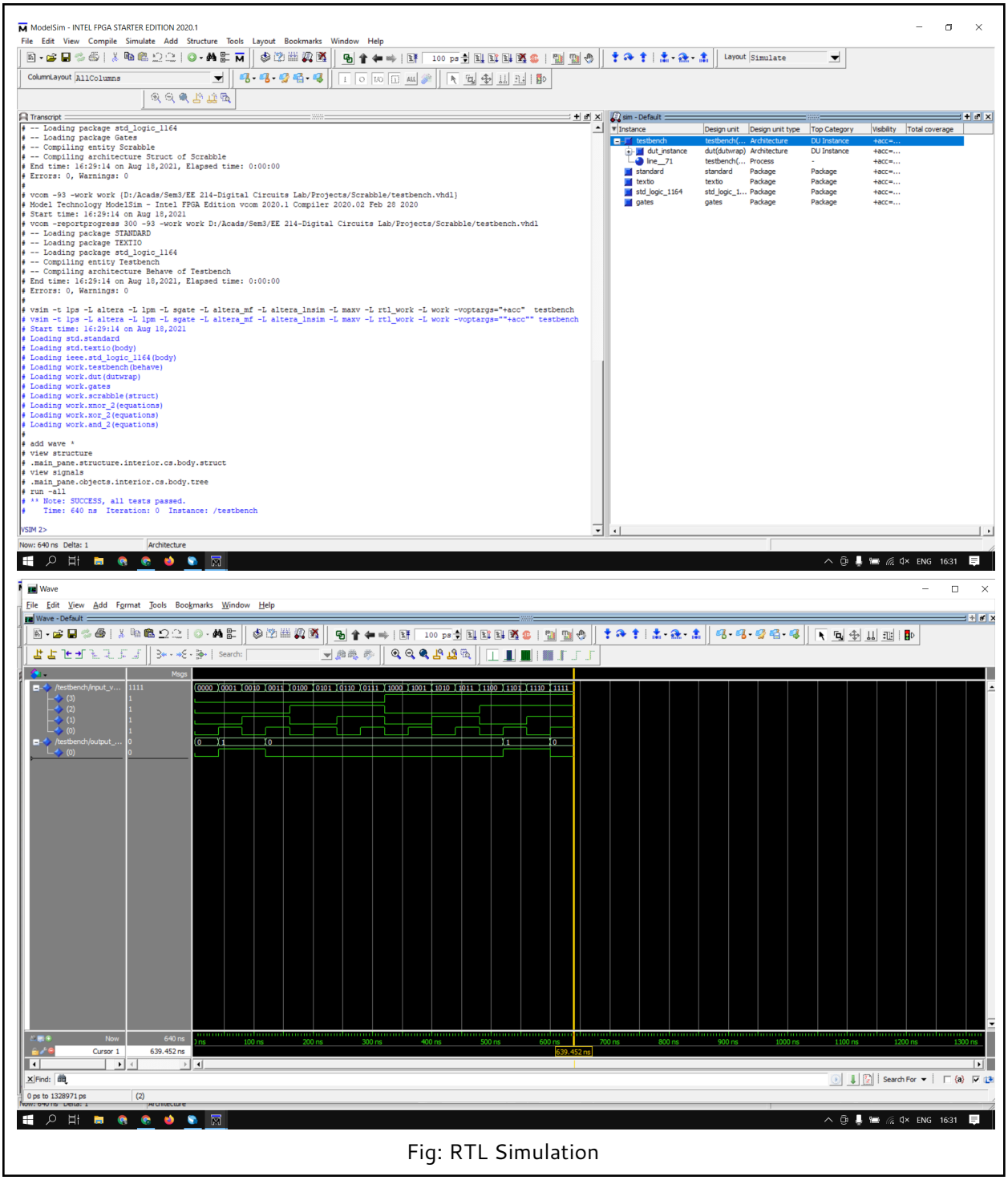


Fig: RTL Simulation

Gate-level Simulation:

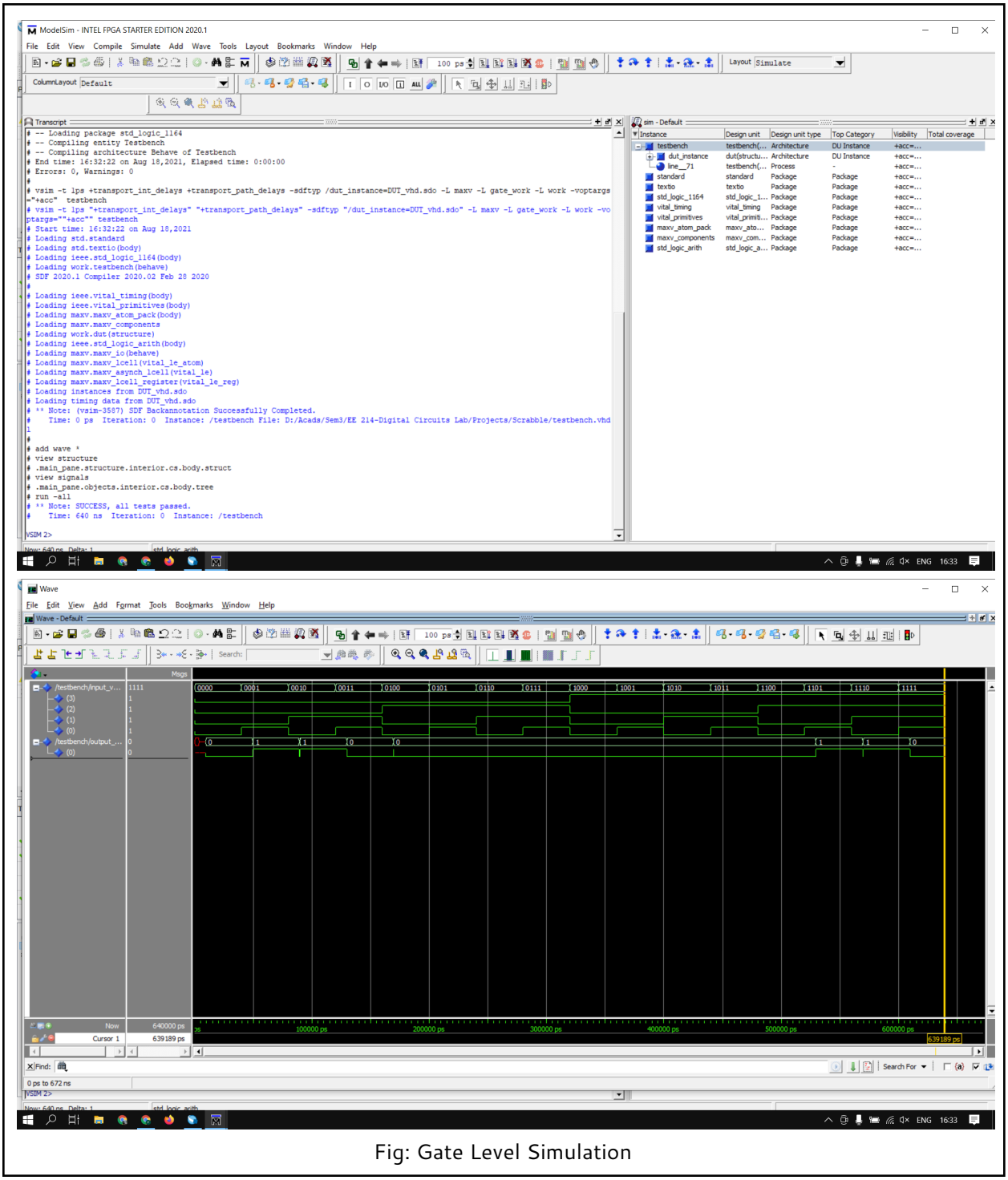


Fig: Gate Level Simulation

References:

1. J.F.Wakerly: Digital Design, Principles and Practices,4th Edition,Pearson Education, 2005