EE230: Lab-2
Unregulated DC Power Supply Learning

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1 Overview of the experiment

1.1 Aim of the experiment

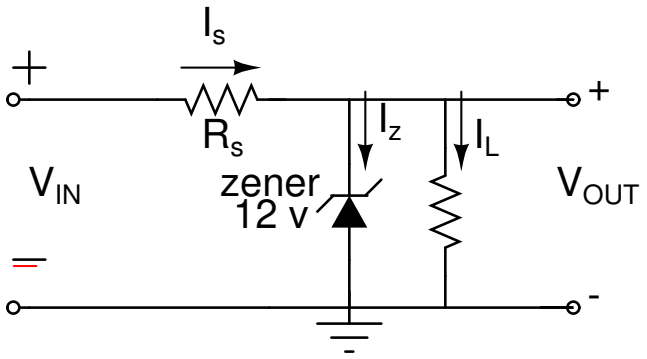
1. Understanding the limits of performance of a Zener regulator
2. Understanding a BJT based series voltage regulator to appreciate the basic blocks of an IC voltage regulator.

1.2 Methods

We start by analysing the circuits and then simulating in ngspice to check against theoretical expectations.

2 Design

2.1 Zener Regulator



In non conduction region :

$$I_z = 0$$

$$V_{out} < 12V$$

$$V_{out} = \frac{V_{in}}{R_s + R_l}$$

In conduction region : Using $R_z = 125\Omega$ and V_z=12V

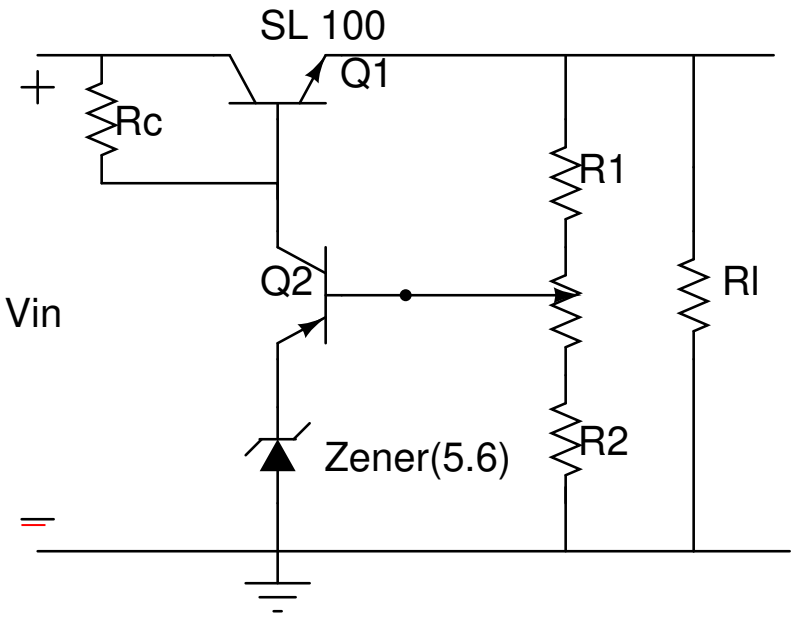
$$V_{out} \geq 12V$$

$$V_{out} = (V_{in}/R_s + 12/125)/(1/R_s + 1/R_z + 1/R_l)$$

$$I_s = (V_{in} - V_{out})/R_s$$

$$I_z = (V_{out} - 12)/125$$

2.2 BJT Series Regulator



3 Simulation results

3.1 Zener Regulator

3.1.1 Code snippet

```
Zener Regulator Circuit

*Defining zener Subckt
.MODEL DF D ( IS=27.5p RS=0.620 N=1.10 CJO=78.3p VJ=1.00 M
   =0.330 TT=50.1n)
.MODEL DR D ( IS=5.49f RS=50 N=1.77 )
.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 10.8
.ENDS

*describe circuit
* <element-name> <nodes> <value/nodel>
Vin 1 0 dc 20

Vrs 2 3 dc 0
Rs  1 2 470

x3 4 3 ZENER_12
Viz 4 0 dc 0

RL 3 5 1k
Vil 5 0 dc 0

*analysis commandx

.op

.control
run

*display cmd
print v(3) i(Vrs) i(Vil) i(Viz)
*end control mode
.endc

*end netlist
.end
```

3.1.2 Simulation results

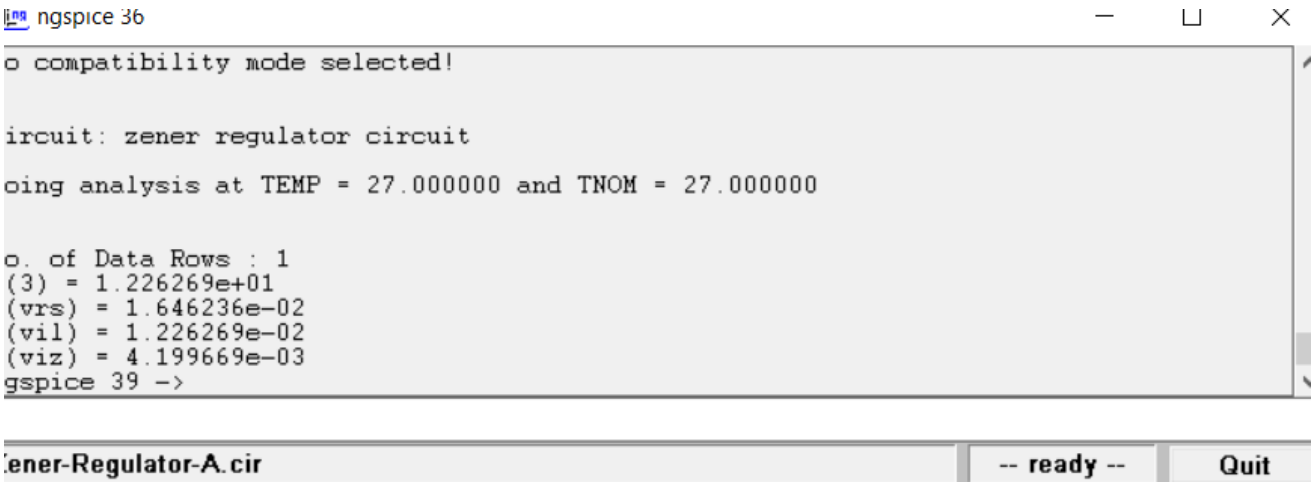
3.2 BJT Series Regulator

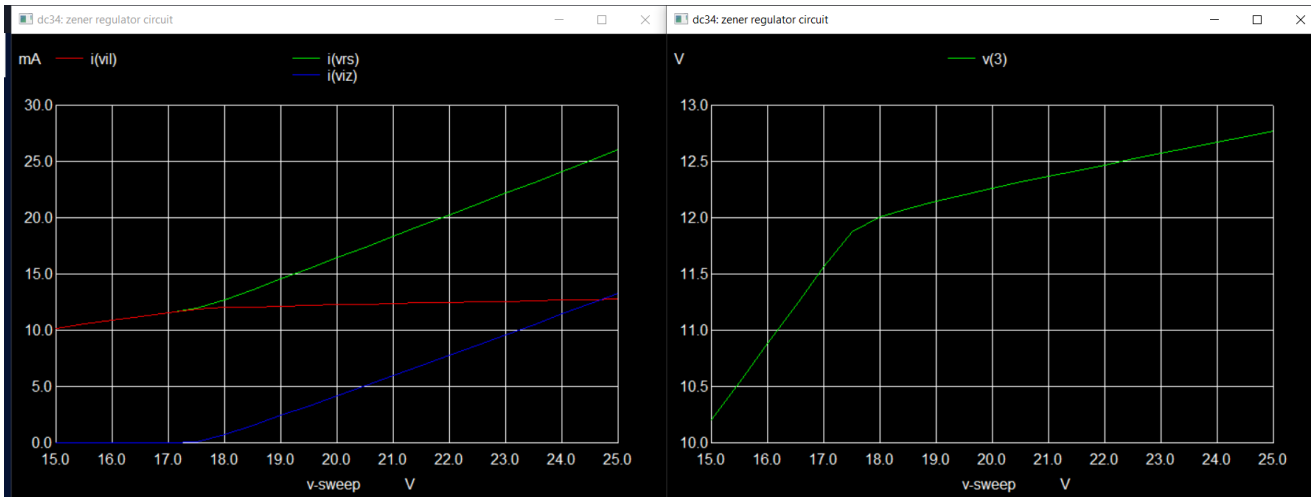
3.2.1 Code snippet

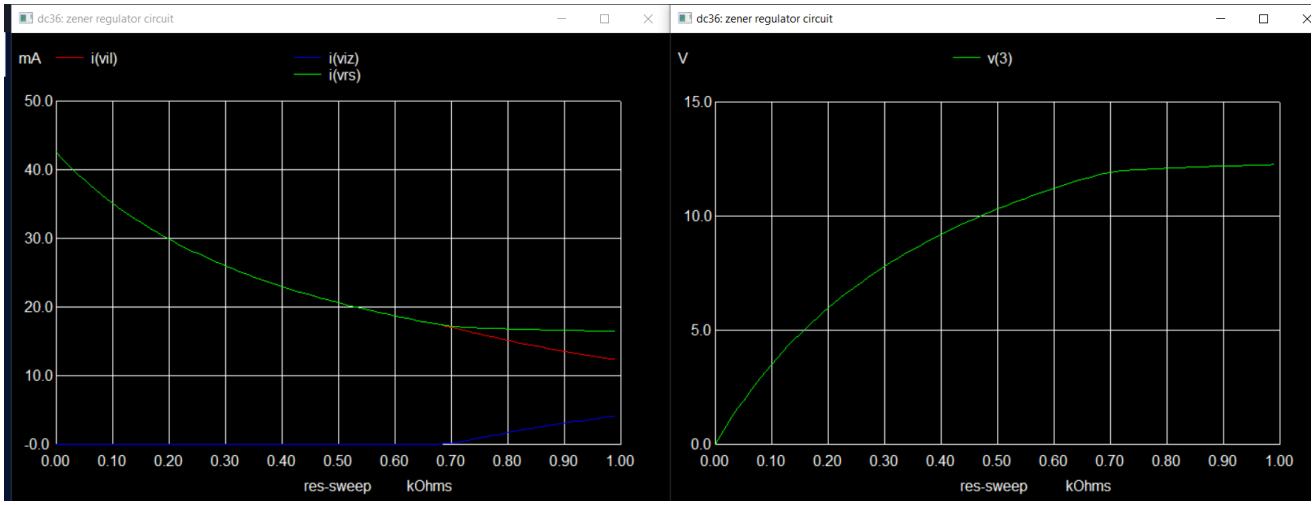
```
BJT Regulator Circuit

.include zener_B.txt
*Defining Models
.model bc547a NPN (IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc
    =0.33 kf=2f)

.model SL100 NPN (IS=100f BF=80 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=100 RE=1 RC=10
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc
    =0.33 kf=2f)

*describe circuit
* <element-name> <nodes> <value/nodel>
Vin 1 0 dc 20
RC 1 3 1K
Q1 1 3 2 SL100
Q2 3 4 5 bc547a
xz 0 5 DI_1N4734A
R1 2 4 12.5K
R2 0 4 12.5K
RL 2 0 1k

*analysis commandx
.op

.control
run

*display cmd
print v(1) v(2) v(3) v(4) v(5)
*end control mode
.endc

*end netlist
.end
```

3.2.2 Simulation results

Zener Regulator

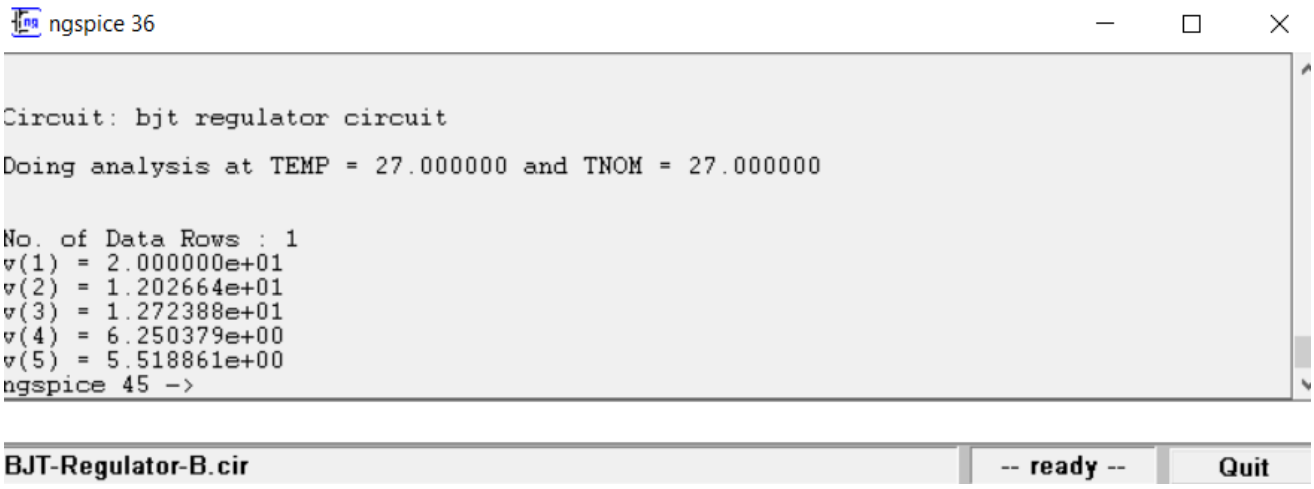


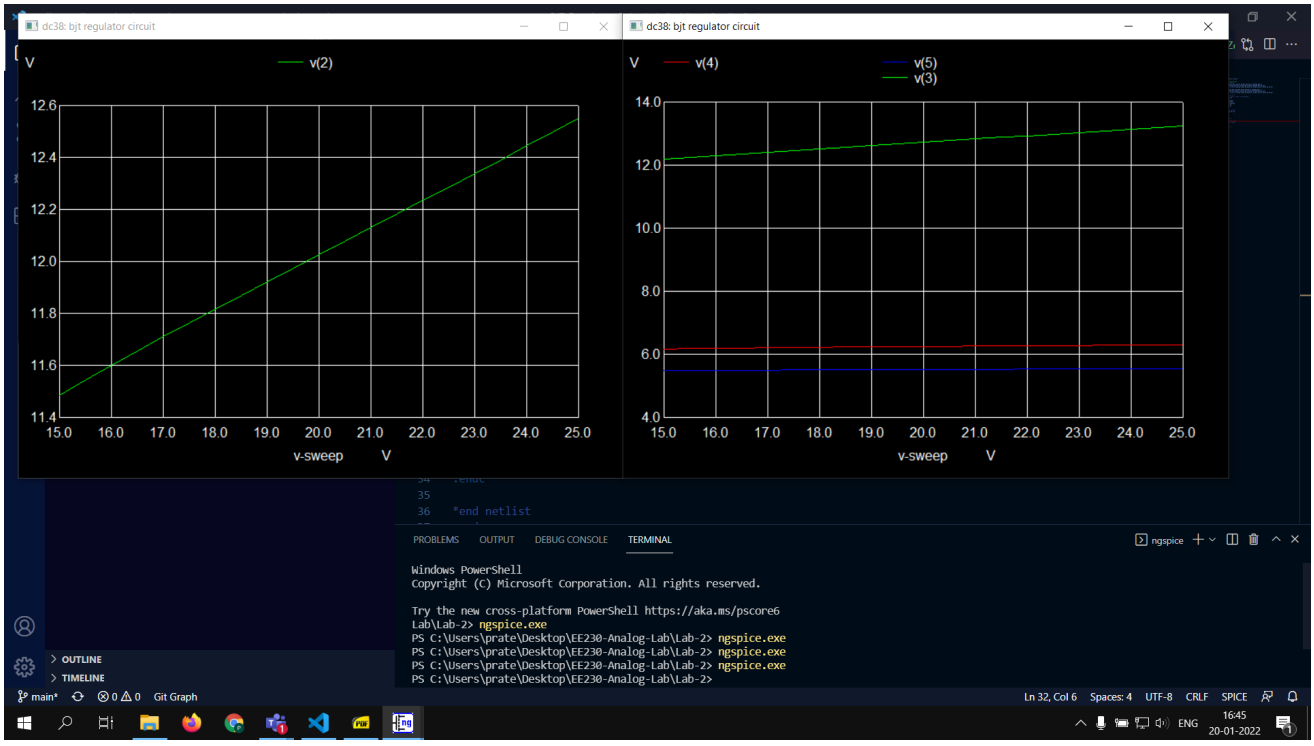




BJT Series Regulator

```
ngspice 36

Circuit: bjt regulator circuit

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 1
v(1) = 2.000000e+01
v(2) = 1.304369e+01
v(3) = 1.374712e+01
v(4) = 6.235345e+00
v(5) = 5.512430e+00
ngspice 44 ->
```


ngspice 36
Circuit: bjt regulator circuit
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
No. of Data Rows : 1
v(1) = 2.000000e+01
v(2) = 1.202664e+01
v(3) = 1.272388e+01
v(4) = 6.250379e+00
v(5) = 5.518861e+00
ngspice 45 ->
BJT-Regulator-B.cir
-- ready --
Quit


dc38: bjt regulator circuit
V
v(2)
12.6
12.4
12.2
12.0
11.8
11.6
11.4
15.0 16.0 17.0 18.0 19.0 20.0 21.0 22.0 23.0 24.0 25.0
v-sweep V
dc38: bjt regulator circuit
V
v(4)
v(5)
v(3)
14.0
12.0
10.0
8.0
6.0
4.0
15.0 16.0 17.0 18.0 19.0 20.0 21.0 22.0 23.0 24.0 25.0
v-sweep V
*end netlist
PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
ngspice
Windows PowerShell
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Try the new cross-platform PowerShell https://aka.ms/pscore6
Lab\Lab-2> ngspice.exe
PS C:\Users\prate\Desktop\EE230-Analog-Lab\Lab-2> ngspice.exe
PS C:\Users\prate\Desktop\EE230-Analog-Lab\Lab-2> ngspice.exe
PS C:\Users\prate\Desktop\EE230-Analog-Lab\Lab-2> ngspice.exe
PS C:\Users\prate\Desktop\EE230-Analog-Lab\Lab-2>
OUTLINE
TIMELINE
main*
Git Graph
Ln 32, Col 6
Spaces: 4
UTF-8
CRLF
SPICE
ENG
16:45
20-01-2022

4 Experiment completion status

All the sections were completed