EE230: Homework-1 Familiarization with NGSPICE Circuit Simulator and Lab Equipment

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1 Overview of the experiment

1.1 Aim of the experiment

Ngspice is a mixed-signal circuit Simulator. This experiment aims to implement some basic circuits namely :

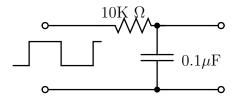
- RC Integrator
- RC Differentiator
- RC Lowpass Filter
- RC Highpass Filter
- RC Bandpass Filter
- RLC Bandpass Filter

in Ngspice and plot their characteristics.

1.2 Methods

We start by creating a netlist for each circuit, simulating on Ngspice and exporting the values to a python script to plot them using Matplotlib.

2 Design



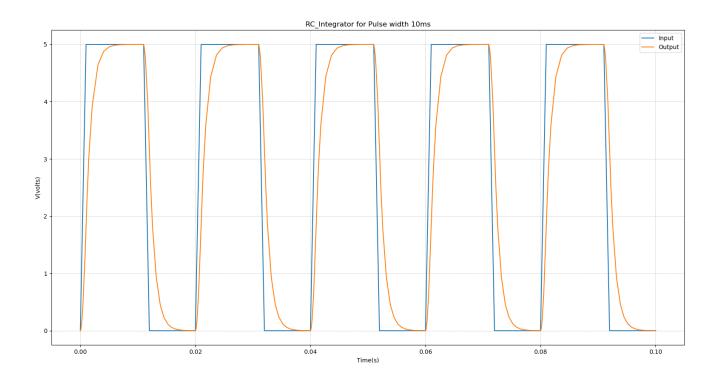
3 Simulation results

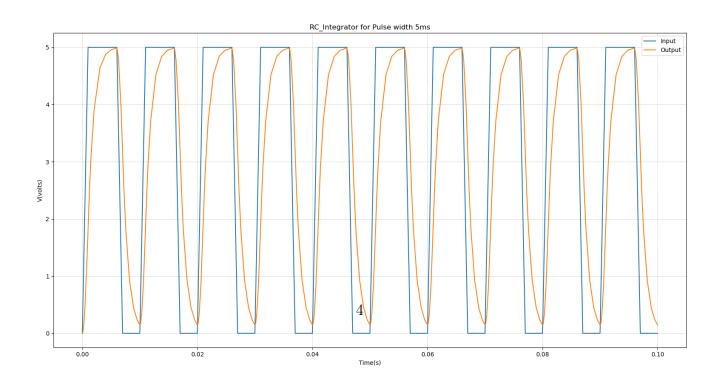
3.1 RC Integrator

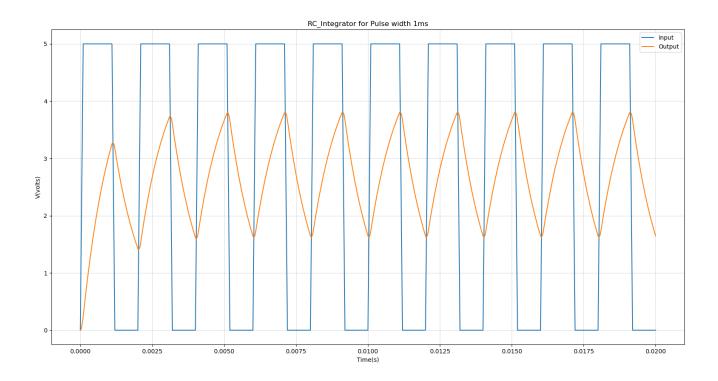
3.1.1 Code snippet

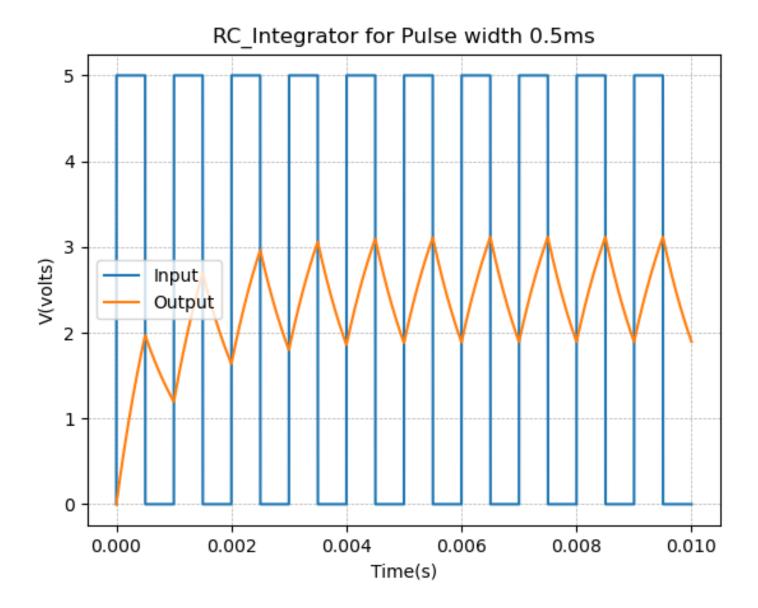
```
1 RC Integrator circuit transient analysis
2 *tau =1m #Time Period
4 *describe circuit
* <element-name> <nodes> <value/nodel>
6 r 1 2 10k
7 c 2 0 0.1u
8 *v 1 0 pulse(0 5 0 0 0 10m 20m) $10*tau
9 *v 1 0 pulse(0 5 0 0 0 10m 20m) $5*tau
*v 1 0 pulse(0 5 0 0 0 10m 20m) $1*tau
*v 1 0 pulse(0 5 0 0 0 10m 20m) $0.5*tau
*v 1 0 pulse(0 5 0 0 0 10m 20m) $0.1*tau
13 v 1 0 pulse(0 5 0 0 0 0.05m 0.1m) $0.05*tau
14 *analysis command
15 .tran 0.011m 10m
17 .control
18 run
20 *display cmd
21 plot v(1) v(2)
22 print v(1) v(2)
23 *end control mode
24 .endc
*end netlist
27 .end
```

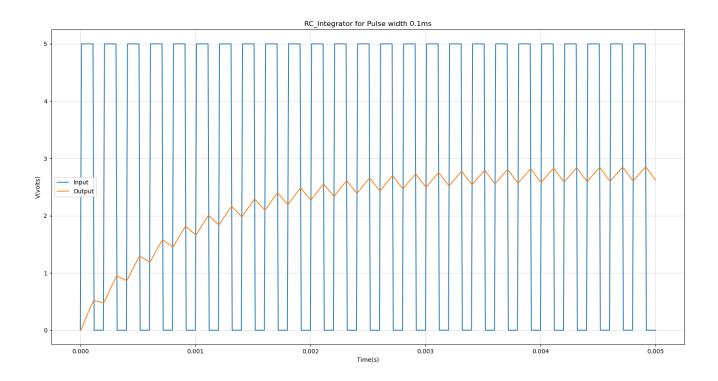
3.1.2 Simulation results

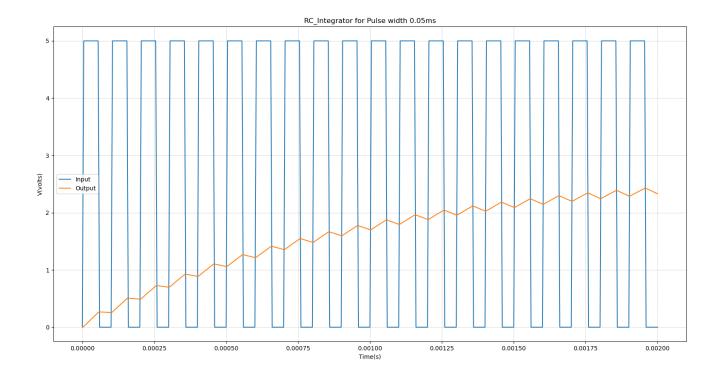












3.2 RC Differentiator

3.2.1 Code snippet

```
RC DIfferentiator circuit transient analysis

*tau =1m #Time Period

*describe circuit

* <element-name> <nodes> <value/nodel>

r 2 0 10k

c 1 2 0.1u

v 1 0 pulse(0 5 0 0 0 10m 20m) $10*tau

*v 1 0 pulse(0 5 0 0 0 10m 20m) $5*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $1*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $0.5*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $0.5*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $0.1*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $0.1*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $0.05*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $0.05*tau

v 1 0 pulse(0 5 0 0 0 10m 20m) $0.05*tau
```

```
15 .tran 0.1m 100m

16

17 .control

18 run

19

20 *display cmd

21 plot v(2) v(1)

22 print v(1) v(2)

23 *end control mode

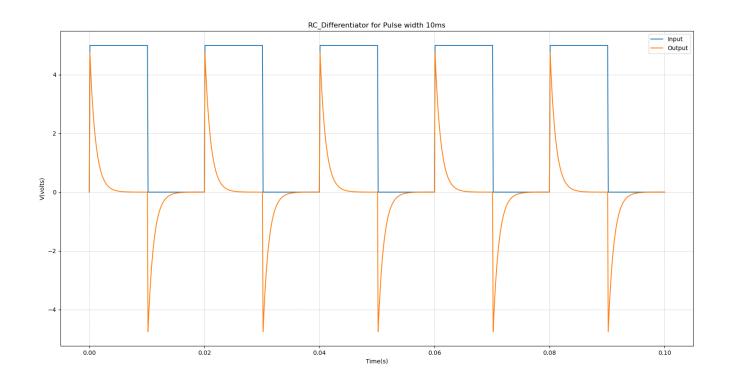
24 .endc

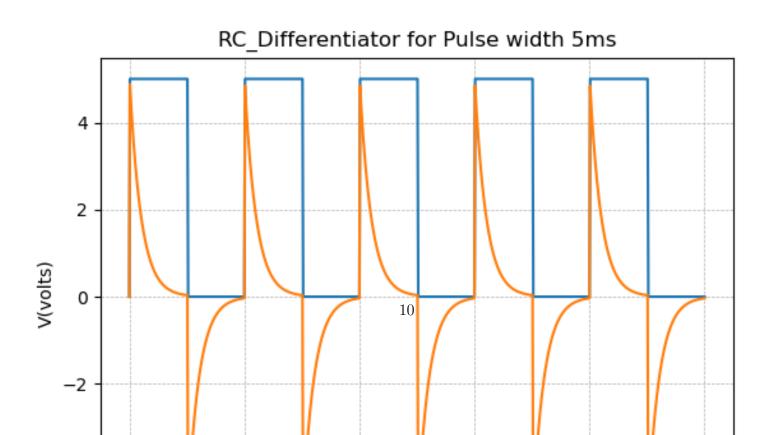
25

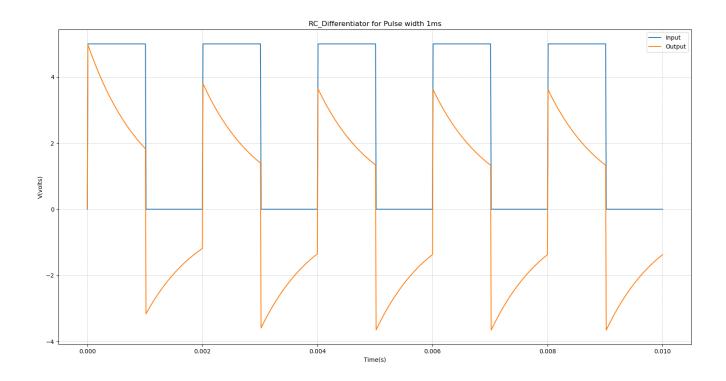
26 *end netlist

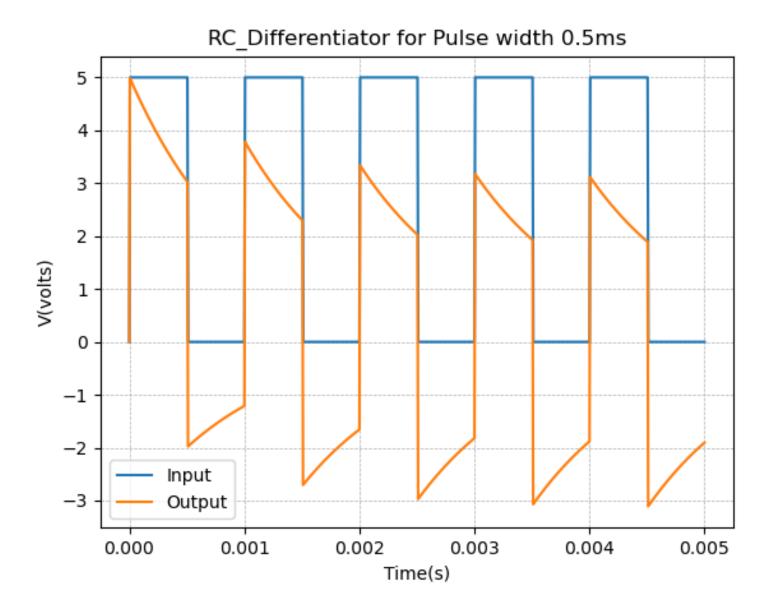
27 .end
```

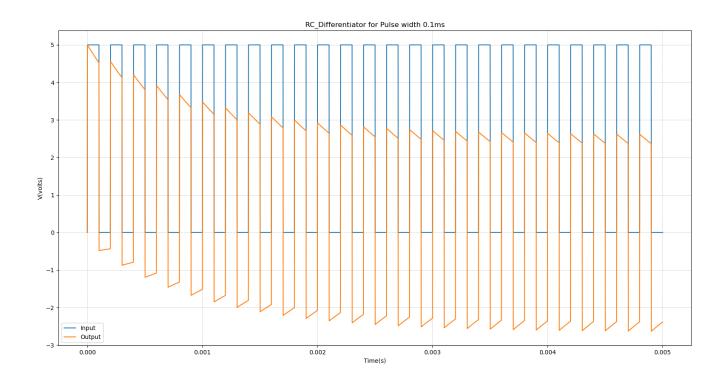
3.2.2 Simulation results

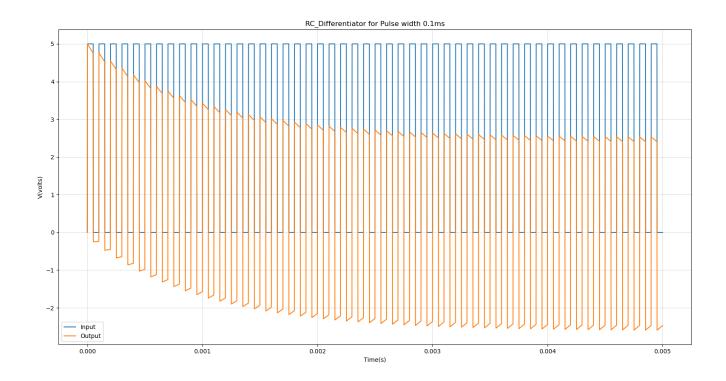












3.3 RC Lowpass Filter

3.3.1 Code snippet

```
RC Lowpass Filter

*describe circuit

* <element-name > <nodes > <value/nodel >

r 1 2 10k

c 2 0 0.1u

vin 1 0 dc 0 ac 1 $ac analysis

*analysis command

ac dec 10 1 10Meg

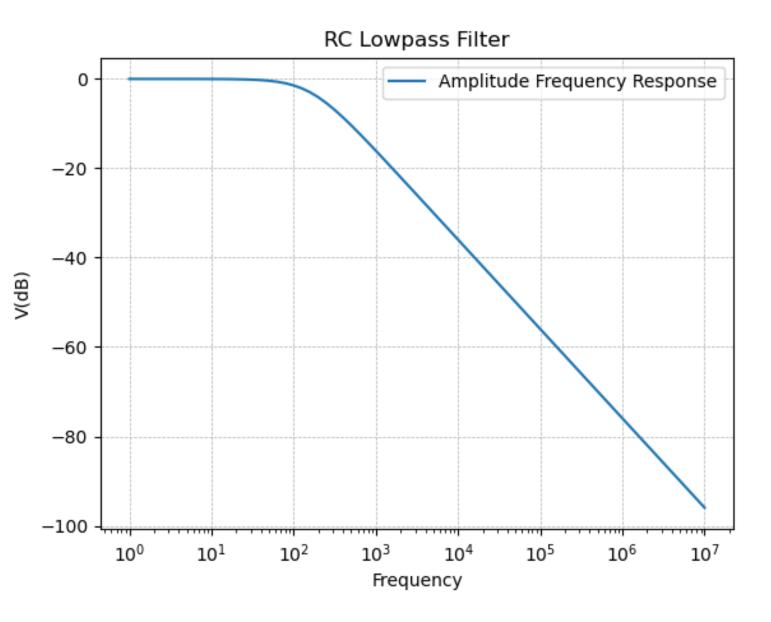
1 .control

run

1 *display cmd
```

```
plot vdb(2)
print vdb(2)
vend control mode
sendc
vend netlist
nend
```

3.3.2 Simulation results

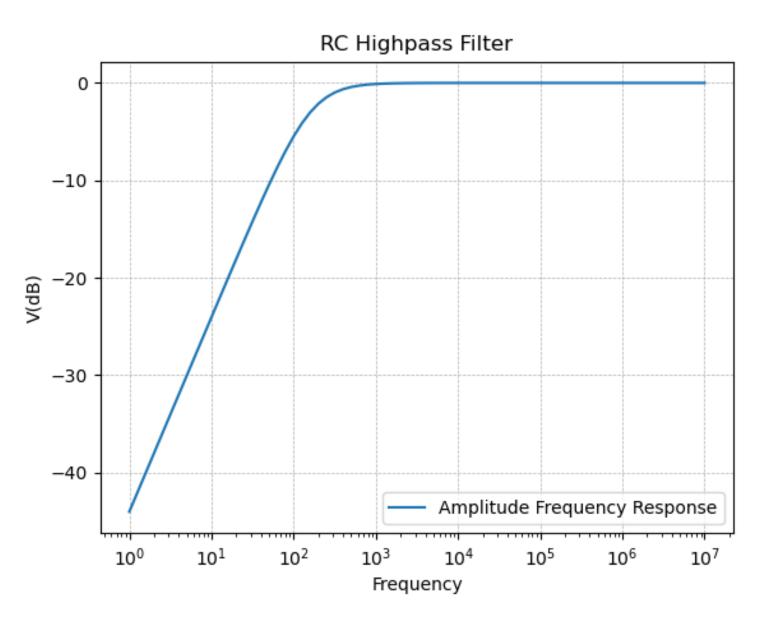


3.4 RC Highpass Filter

3.4.1 Code snippet

```
RC Highpass Filter
2 *describe circuit
3 * <element-name> <nodes> <value/nodel>
4 c 1 2 0.1u
5 r 2 0 10k
_{6} v 1 0 dc 0 ac 1 $ac analysis
7 *analysis command
_{8} .ac dec 10 1 10Meg
10 .control
11 run
**display cmd
plot vdb(2)
print vdb(2)
16 *end control mode
17 .endc
19 *end netlist
20 .end
```

3.4.2 Simulation results

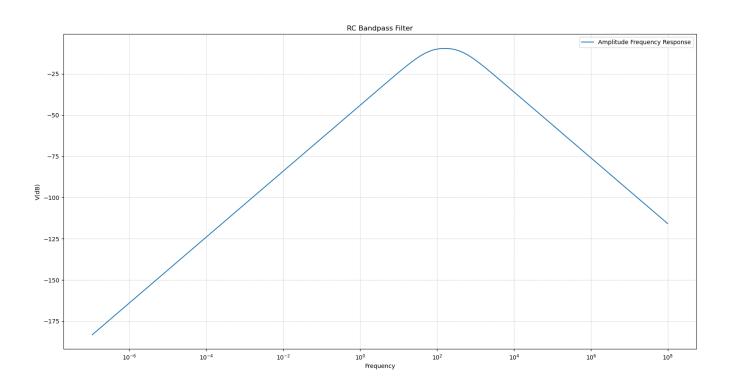


3.5 RC Bandpass Filter

3.5.1 Code snippet

```
1 RC Bandpass Filter
2 *describe circuit
3 * <element-name> <nodes> <value/nodel>
4 r1 1 2 10k
5 c1 2 3 0.1u
6 r2 3 0 10k
7 c2 3 0 0.1u
8 v 1 0 dc 0 ac 1 $ac analysis
9 *analysis command
10 .ac dec 20 0.1u 100Meg
12 .control
13 run
*display cmd
16 plot vdb(3)
*print vdb(3)
18 *end control mode
19 .endc
20
21 *end netlist
22 .end
```

3.5.2 Simulation results



3.6 RLC Bandpass Filter

3.6.1 Code snippet

```
RLC Bandpass Filter

*describe circuit

* <element-name > <nodes > <value/nodel >

1 1 2 10m

c 2 3 0.1u

r 3 0 1k

v 1 0 dc 0 ac 1 $ac analysis

*analysis command

ac dec 20 0.1u 100Meg

.control
```

```
run

*display cmd

plot vdb(3)

print vdb(3)

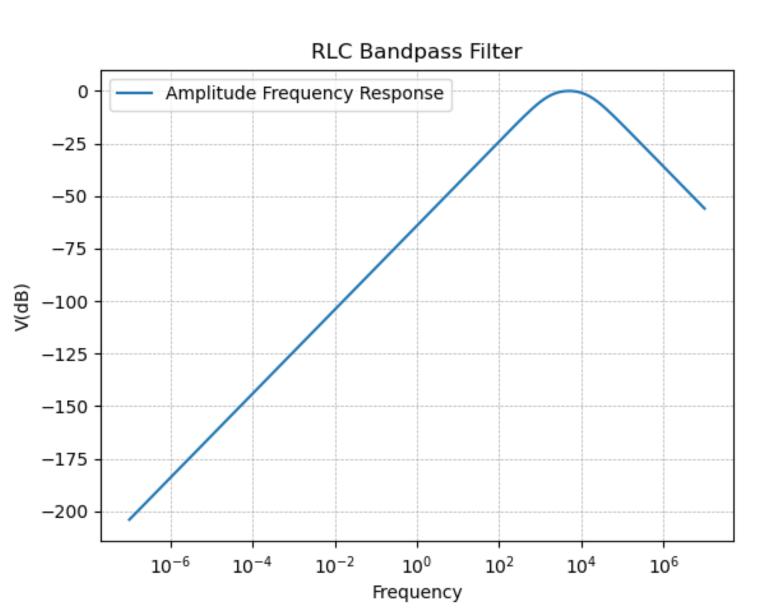
*end control mode

endc

*end netlist

end
```

3.6.2 Simulation results



4 Experimental results

- 4.1 RC Integrator
- 4.2 RC Differentiator
- 4.3 RC Lowpass Filter
- 4.4 RC Highpass Filter
- 4.5 RC Bandpass Filter
- 4.6 RLC Bandpass Filter

5 Experiment completion status

All the sections were completed