

# PRATEEK P. KULKARNI

BTech (Electronics and Communications Engineering)

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## EDUCATION

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### PES University

2022–2026 (Expected)

BTech in Electronics and Communications Engineering (VLSI)

Thesis: Photonic FPGA for Variational Quantum Algorithms

### Kendriya Vidyalaya, Hebbal

2021–2022

Grade 12

## RESEARCH INTERESTS

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Quantum Computing, Electronic Design Automation, Systems Architecture, Industry Analysis

## SELECTED COURSEWORK

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**VLSI & EDA:** Analog Circuit Design, Network Analysis and Synthesis, Computer-Aided Digital Design, Digital VLSI, Computer Organization and Design, High Performance Computing

**Quantum Track Electives:** Quantum Computing and Quantum Entanglement, Chip-Level Photonics, Quantum Transport and Logic Gates, Non-Linear Optics and Quantum Technology

## RESEARCH EXPERIENCE

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### Visiting Research Student

Feb. 2024–Present

Future Computing Systems Lab, Indian Institute of Science

Advisor: Prof. Sumit K. Mandal

Distributed Quantum Computing Architecture

### Research Assistant

Aug. 2024–Dec. 2025 (Expected)

Photonics and Quantum Tech Lab, PES University

Advisor: Prof. Kaustav Bhowmick

Quantum Machine Learning (*Undergraduate Thesis*)

## PUBLICATIONS

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### Journals:

1. Ramaseshan R, Abhishek Kumar V S, Adith Rajeev, Prathik V, Aditya Aravind, Prateek P. Kulkarni and Kaustav Bhowmick. **A Generalized Hamiltonian Approach for Designing Simple Single Photon-based Optical Quantum Devices.** *The Journal of Supercomputing, Springer*, 2025.

### Conferences:

1. Prateek Kulkarni. **RAPID: Row-Access Pattern-aware In-DRAM Prefetching.** *International Conference on Emerging Technologies for Intelligent Systems*, 2025.
2. Prateek Kulkarni. **A Low-Latency Memory Architecture using 3D XPoint and Memristor Technologies.** *5th International Conference on Communication, Computing and Industry 6.0*, 2024.

### Peer-Reviewed Posters:

1. Prateek P. Kulkarni. **DIRECT: Enabling Scalable Processing-In-Memory via DPU-to-DPU Communication.** *6th India ESD Workshop*, 2025.

### Preprints:

1. Ramaseshan R, Prateek P. Kulkarni, Sharanya Madhusudhan and Kaustav Bhowmick. **A Theoretical Treatment of Optical Metasurfaces as an Efficient Basis for Quantum Correlations.** *arXiv:2507.09517 [quant-ph]*, 2025

## TECHNICAL SKILLS

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**Programming Languages:** Python, R, Verilog, Haskell, Q#, L<sup>A</sup>T<sub>E</sub>X, SQL

**Software Tools:** Matlab, Ansys, Cadence, Vivado Suite, gem5, Qiskit, Cirq, PennyLane

## SELECTED PROJECTS

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### SQLFormer: Transformer Inference in Pure SQL (Github Repository)

- Designed and implemented a full Transformer forward pass using only standard SQL queries over relational databases, expressed matrix multiplication, multi-head attention, softmax, and layer normalization declaratively using JOINS, aggregations, and window functions.
- Authored a comprehensive paper (available on GitHub) analyzing correctness, complexity, and performance across PostgreSQL, DuckDB, and PyTorch baselines.

### PipSim: RISC-V Pipeline Simulation Framework (Github Repository)

- Developed Python-based RISC-V pipeline simulator with real-time visualization for instruction flow and hazard detection. The framework enables comprehensive performance analysis for 5-stage pipeline architectures.

- Implemented data forwarding and branch prediction mechanisms achieving educational tool adoption across multiple computer architecture courses.

#### **RegDyno.Ai: Time-Series Prediction Framework** (Patent Published, Journal No. 1/2025)

- Developed custom distribution modeling framework for satellite communication data, achieving 15%-25% improvement in prediction accuracy over state-of-the-art forecasting methods including ARIMA, LSTM, and Prophet models.
- Successfully deployed production-ready ML pipeline with automated noise reduction capabilities, resulting in patent publication for novel prediction methodology.

#### **surface2cirqit: Quantum Circuit Conversion Package** (Github Repository)

- Developed automated Surface Code to Quantum Circuit conversion pipeline with syndrome extraction protocols, achieving 20%-40% gate count reduction through circuit optimization.
- Created scalable Python package enabling seamless integration with existing quantum computing frameworks for error correction implementation.

### **AWARDS AND RECOGNITION**

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<b>Q-Pragathi funding under KITS, Govt. of KTK (INR 1,20,000)</b> IISc Quantum Technology Initiative (Metasurface-based Quantum Computing)	Sept 2024
<b>Workshop Selection</b> Present and Future Computing Systems, IISc (80 participants selected)	Jan 2024
<b>Funded Internship</b> ISFCR Long-Term Internship, PES University (10 recipients, declined)	Jan 2024
<b>National Runner-up</b> Explain The Concept, Pravega 2019 (Undergraduate Fest), IISc	Feb 2019

### **TEACHING EXPERIENCE**

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<b>Teaching Assistant:</b> Quantum Transport and Logic Gates	Spring 2025
<b>Teaching Assistant:</b> Quantum Entanglement and Quantum Computation	Fall 2025

### **PROFESSIONAL SERVICE**

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**Reviewer:** IEEE CONECCT 2025, IEEE DMC 2025, IEEE TQE, Wiley Systems Engineering

### **REFERENCES**

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**Prof. Sumit K. Mandal**  
Assistant Professor, CSA, IISc  
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**Prof. Kaustav Bhowmick**  
Associate Professor, ECE, PES University  
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