Prateek Sahu

Architecture, Computer Systems, and Embedded Systems

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Education

- Ph.D. bound at **University of Texas at Austin** in **Electrical and Computer Engineering** *(2017 - Present: 3.9 GPA)*
- Undergraduate at **Indian Institute of Technology, Kanpur** in **Electrical Engineering** *(2011 - 2015: 8.2 GPA)*

Research Statement

My research interests include understanding architectural and micro-architectural tradeoffs for the performance of systems and apply them for secure processor designs. I am also eager to learn more about how hardware and software can interact to guarantee better data privacy.

Research

- **Detection of micro-architectural attacks** *(UT Austin, Jan 2018 - present)*
  - Research and development of micro-architectural malware detector based on contention of resources by various domains.
  - We evaluate the model against cache based side and covert channels like Prime-Probe and Spectre and demonstrate the effectiveness of it against a baseline system.
- **Hardware implications of 'Serverless' application stack** *(UT Austin, Sept 2018 - present)*
  - Research around micro-benchmarking of FaaS models like those on AWS Lambda and OpenFaaS on various metrics such as network, compute and memory.
  - Goal of this research is to evaluate such services with emphasis on latencies and utilization.

Past Projects

- **Low-power real-time object recognition SoC Design** *(SoC Design Project, Dr. A. Gerstlauer)*
  FPGA design and implementation of GEMM module of YOLO model on Zedboard using Vivado HLS tools
- **Verilog System Design for 32-bit x86 ISA subset** *(MicroArchitecture Course Project, Dr. Yale Patt)*
  CPU Design of a 7-stage pipelined machine with Memory module and branch predictor for subset of x86 ISA
- **Intelligent instruction duplication for Side-Channel Defence** *(Security for HW/SW Course Project, Dr. M. Tiwari)*
  Compiler solution for duplication of instructions which work on dummy data as a defence against side-channels
- **LC-3b Processor Design in C** *(Computer Architecture Course Project, Dr. Mattan Erez)*
  State machine and pipelined cycle accurate simulator for LC-3b ISA including exception and interrupt handling
- **Operating Systems Design on NachOS** *(OS Course Project, Prof. Mainak Chaudhuri)*
  Built up NachOS with syscall implementations, thread synchronization and virtual memory.
- **Cache Block Replacement** *(Dr. Mainak Chaudhuri)*
  Replacement algorithm using age, frequency and re-use distance of a cache line.

Relevant Courses

Computer Architecture	Data Structure and Algorithms	Microarchitecture
Operating Systems	Security in HW/SW Systems	Compiler

Work

- **Graduate Research Assistantship** at University of Texas at Austin, SPARK Labs (ECE) *(Spring 2018 - Current)*
- **Teaching Assistantship** at University of Texas at Austin for Operating Systems course *(Fall Semester 2017)*
- **Member of Technical Staff** at **VMware India** Software Pvt. Ltd *(2015 - 2017)*
  - IDF for system health monitoring tool using vSphere metrics

- Public cloud cost analytics using utilization statistics
- Microservices using Docker containers and Spark cluster for OTA updates to the application suite

Skills

- Languages: C, C++, Java, Verilog, Python
- Tools and Software: gem5, qemu, Vivado HLS, Matlab
- ISA: ARM v8, x86, MIPS, 8086
- Productivity tools: git, Latex