

## Lab 2 (EE533)

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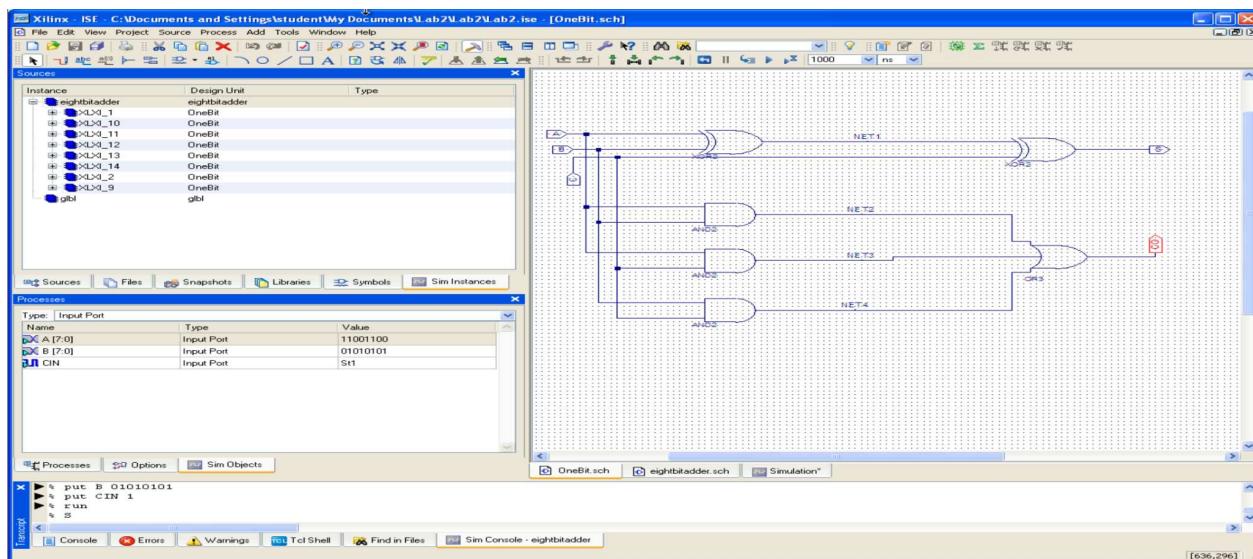
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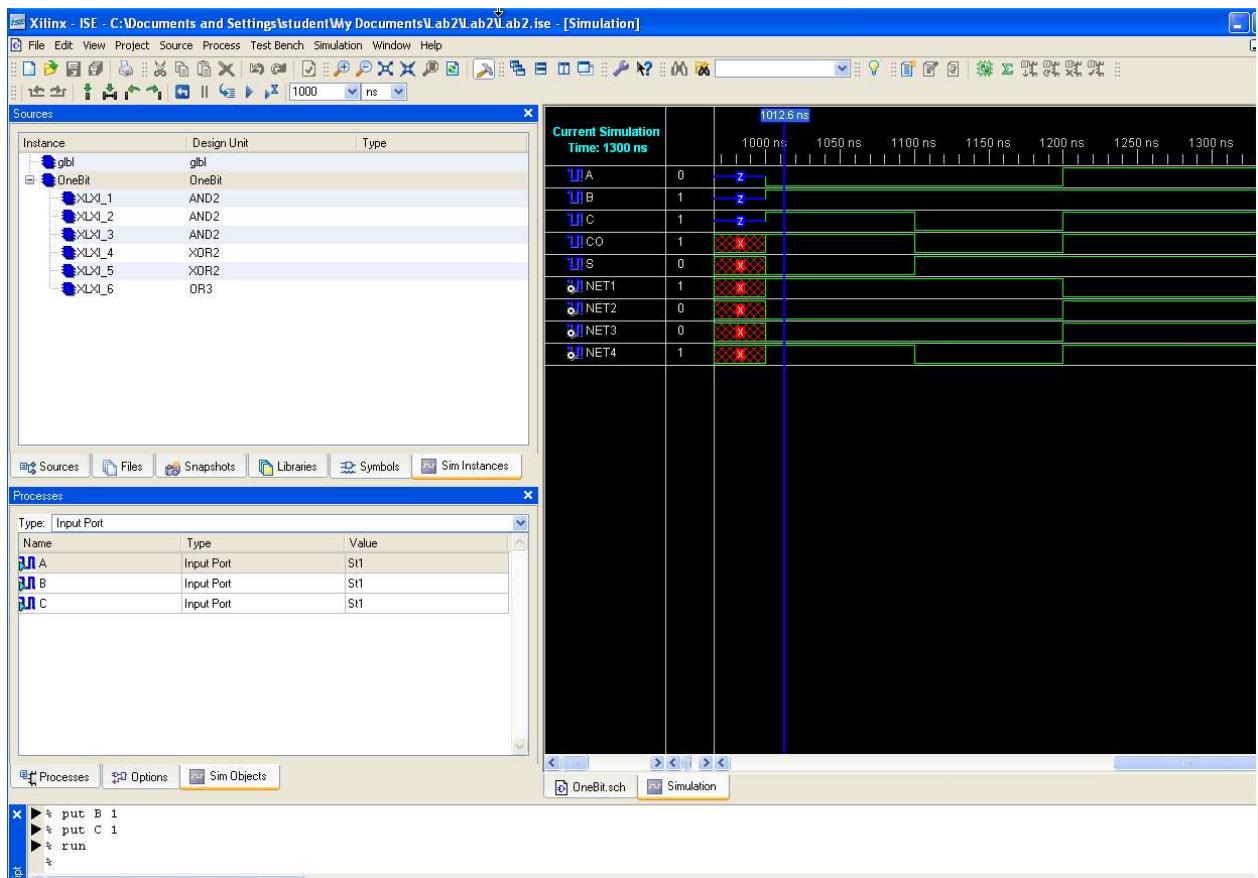
Github link : <https://github.com/prathamesh-hirekodi/EE533>

### Designing and Simulating a Synchronous 8-bit Adder

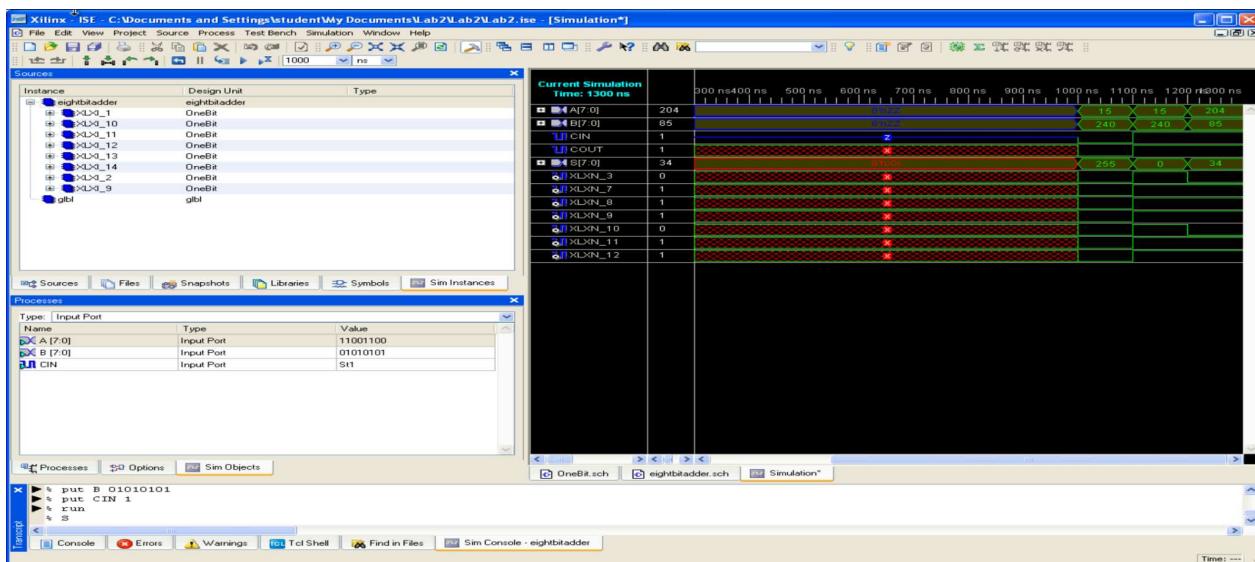
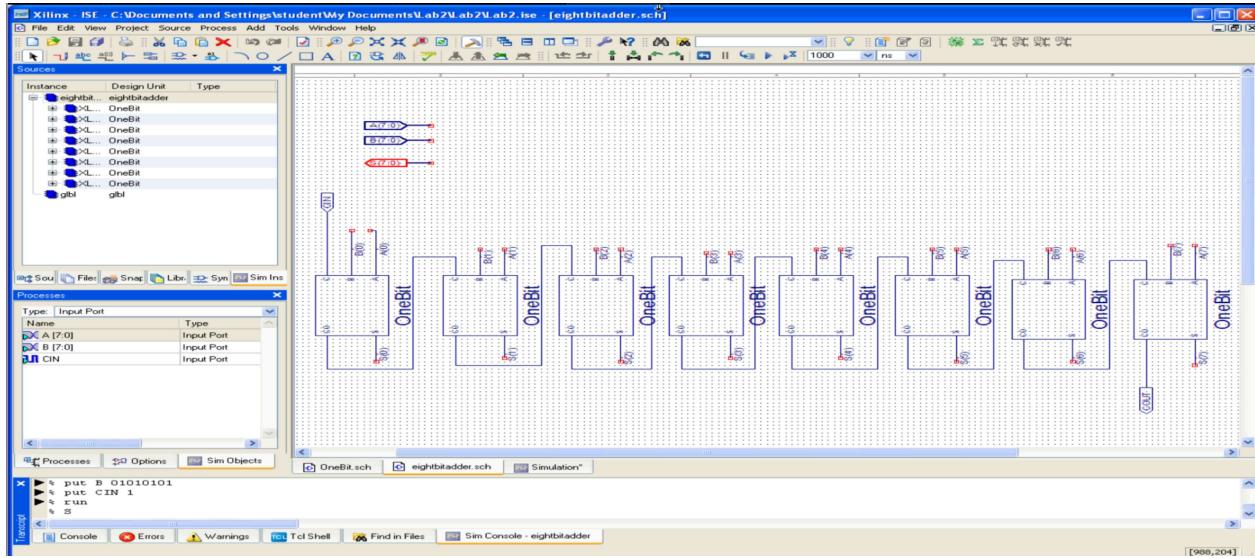
For this part, you must go through the same steps taken in the in-depth tutorial (Part 1) to build and simulate an 8-bit adder using eight 1-bit full adders and D-flip flops available (DO NOT USE THE IP CORE TO GENERATE ANY OF THE COMPONENTS) A synchronous adder has a D-flip flop before the input pins and a D-flip flop after the output pins of the adder circuit. The following must be turned in:

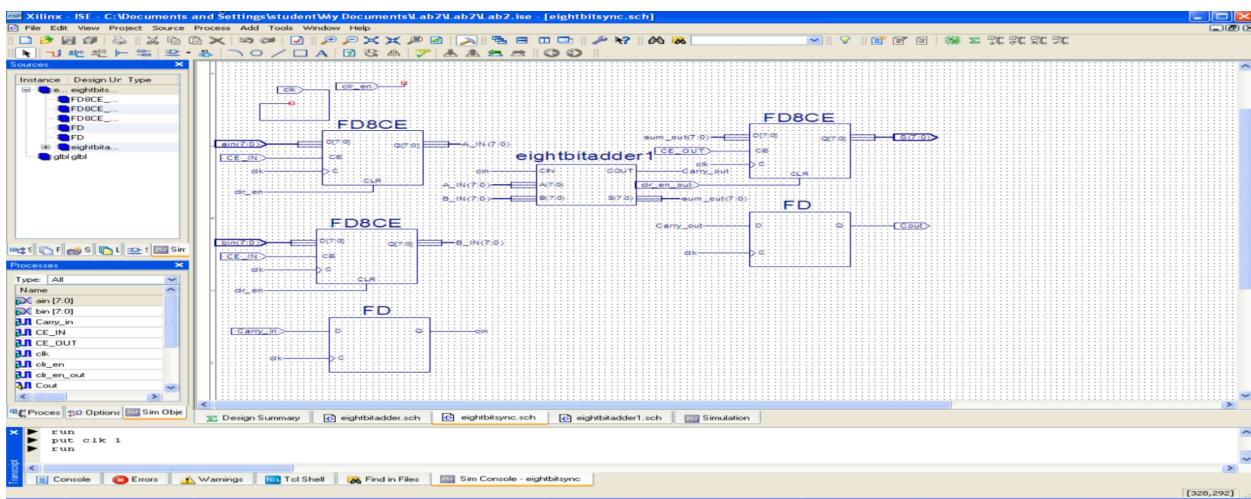
Figure 1:  
1-bit Full Adder Figure



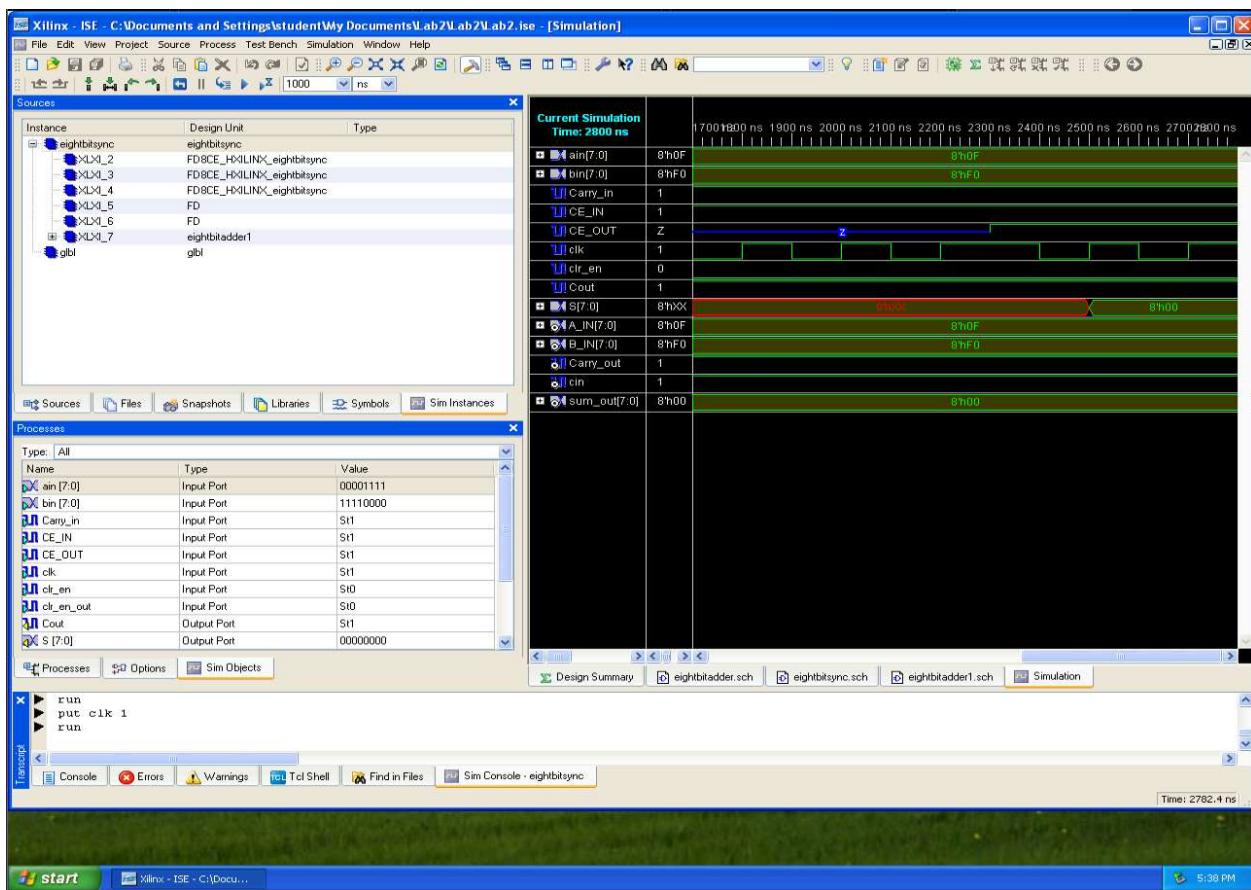


## 2: 8-bit Adder



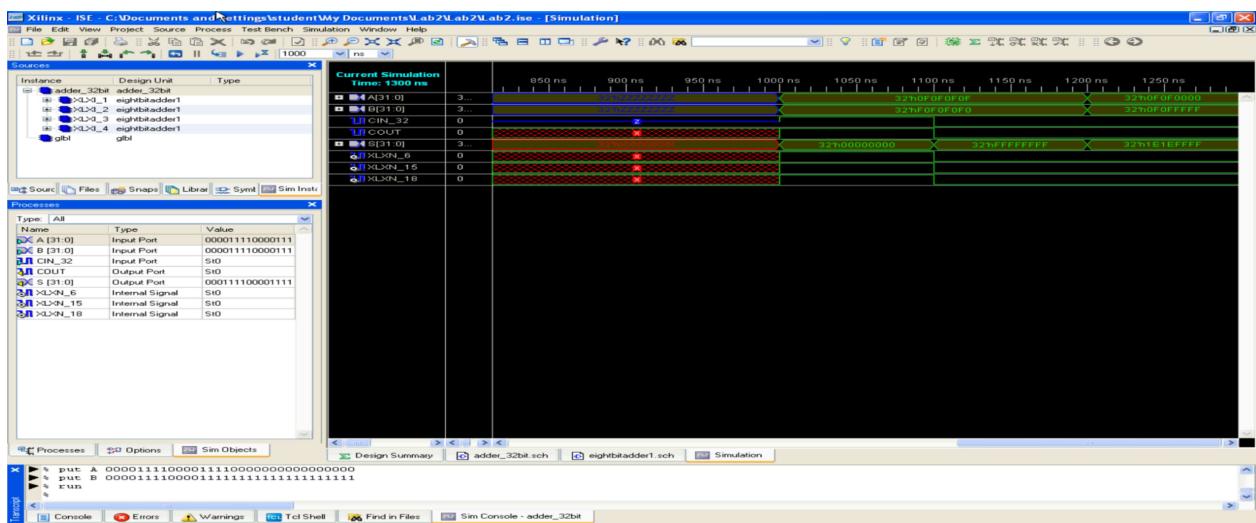
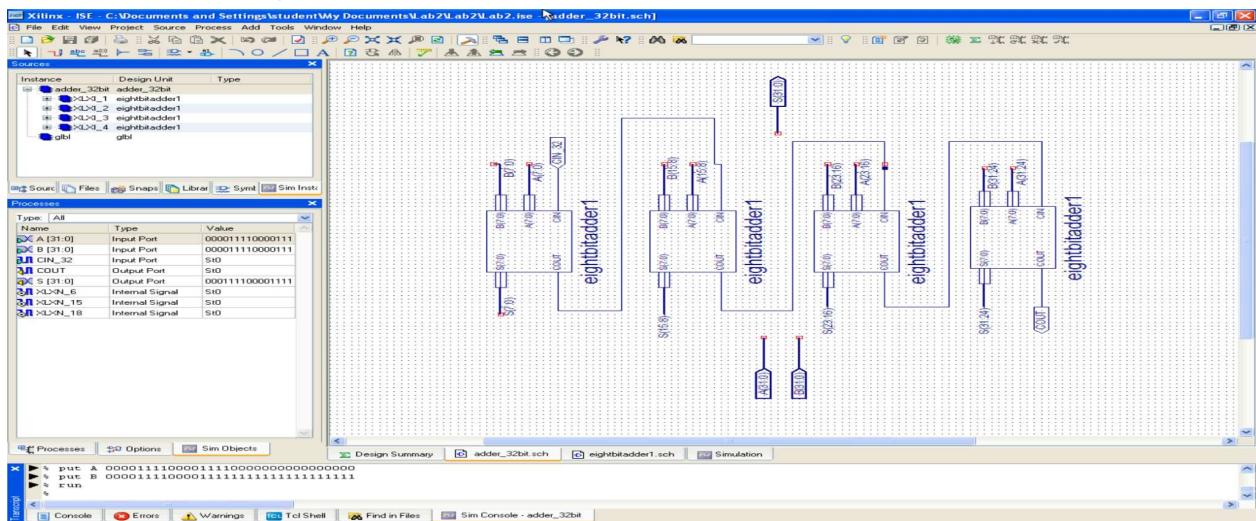


## 8 bit synchronous adder Schematic and behavioral simulation



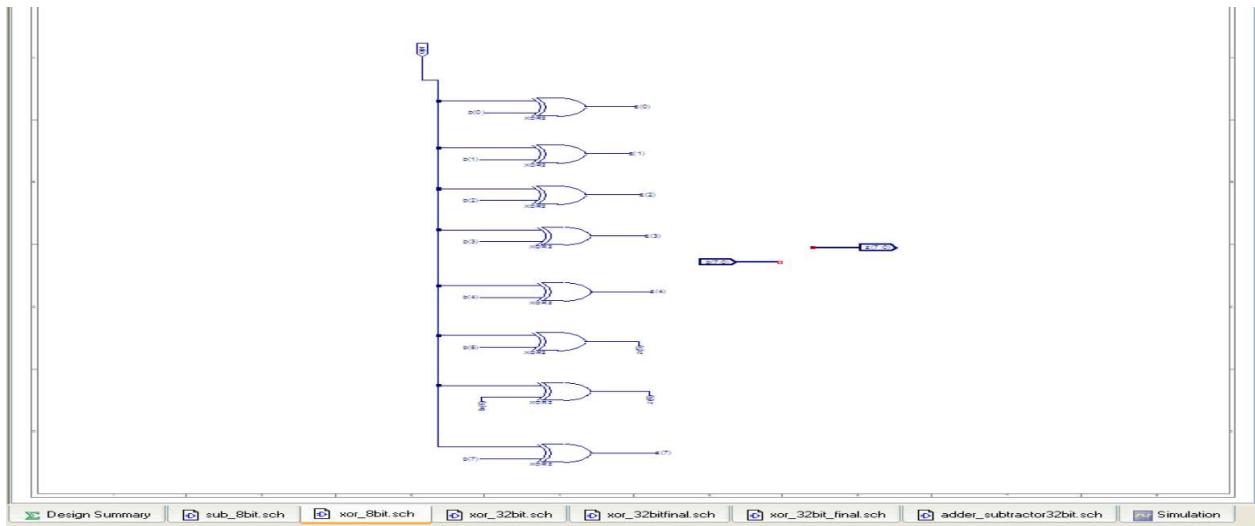
3. Extending Adder into 32-bit ALU DO NOT USE THE IP CORE A Extend the 8-bit Adder into a 32-bit Adder by instantiating and connecting 4 adders Turn in the following:

## 1. Screen capture of your schematics

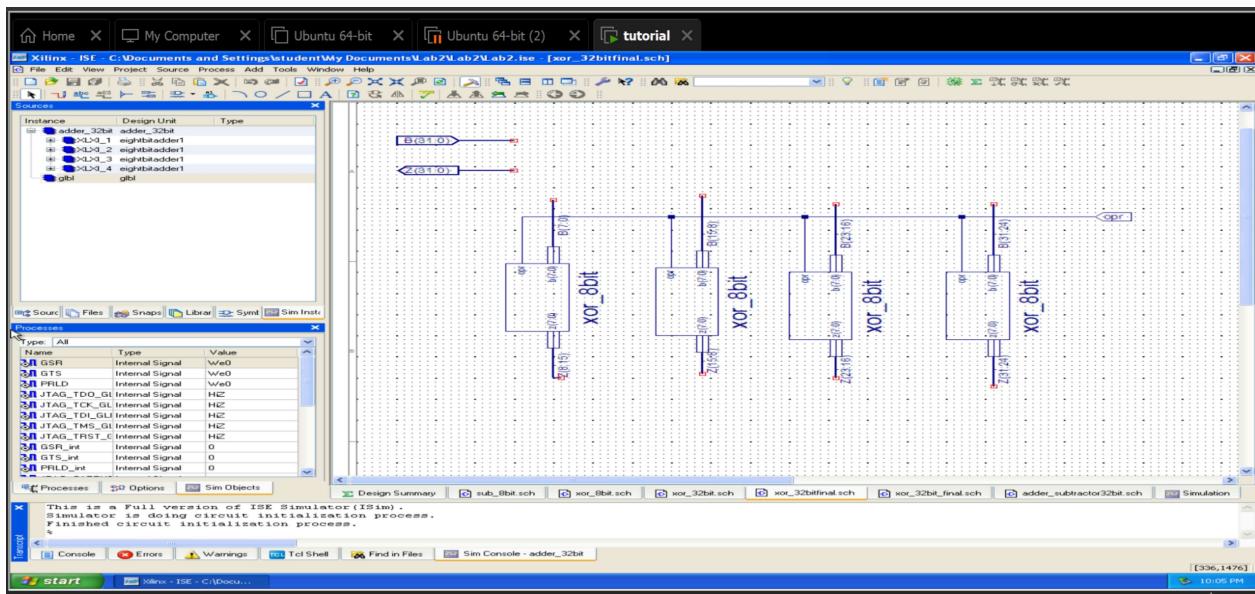


## 2. 32 bit adder\_subtractor

For this first I have created a 8 bit XOR

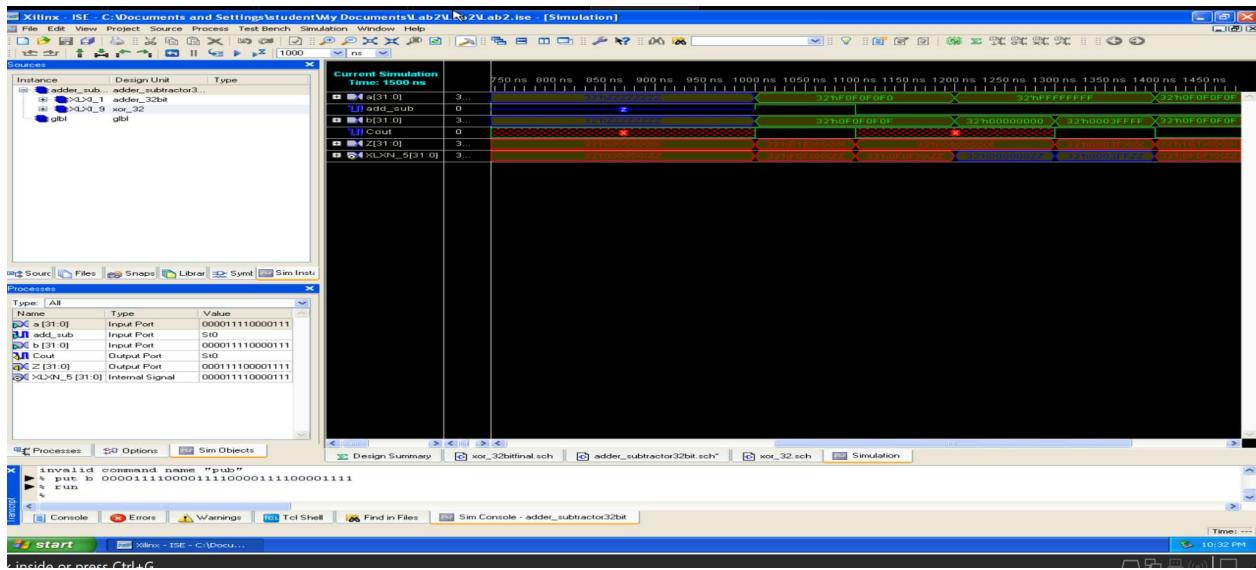
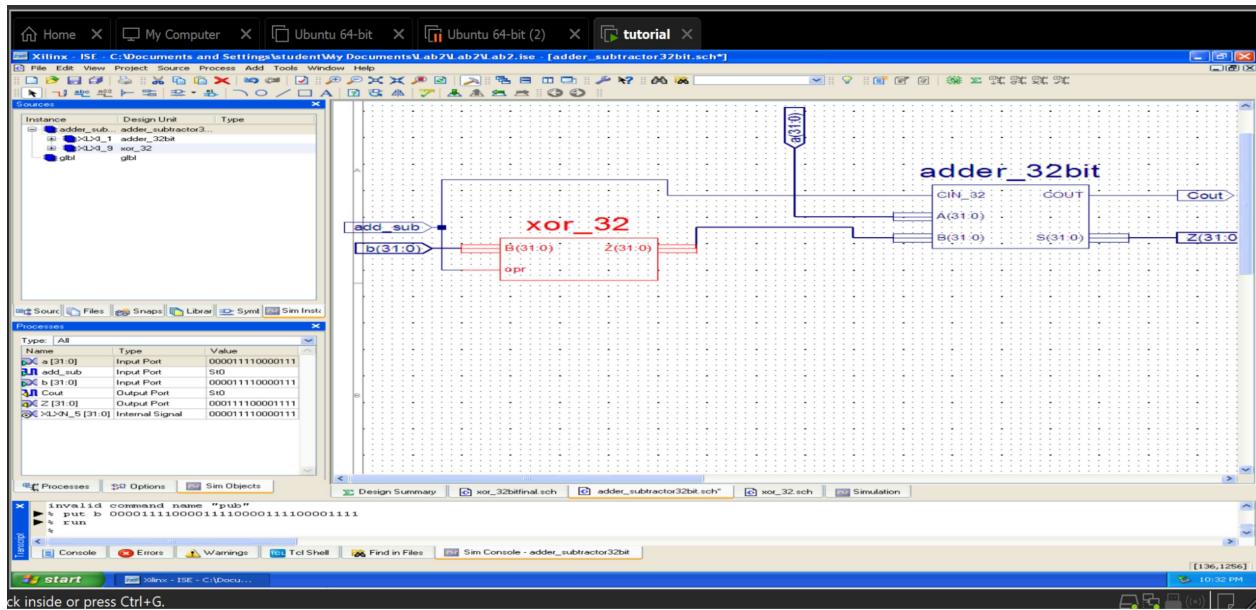


And then a 32 bit XOR

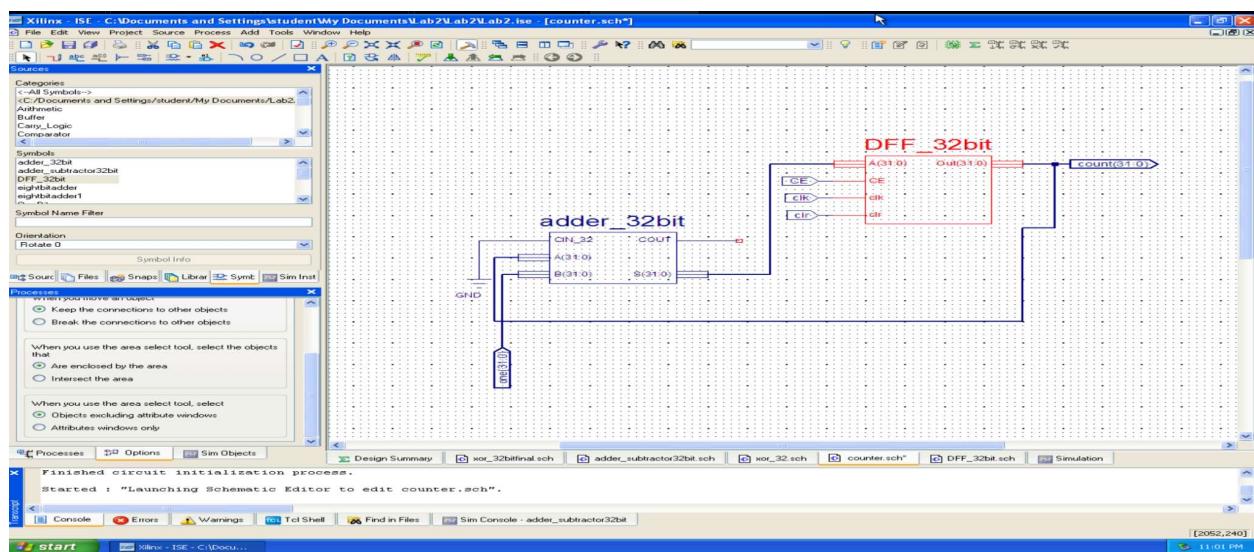


2. Screen capture of the waveforms generated by the behavioral simulation tools B Extend the 32-bit Adder to have other functions, including a subtractor, a shifter, and two other functions of your choice. Go through the mapping process of the tools to get the gate counts, such as the number of D-FF and LUTs.

### 32 bit adder\_subtractor

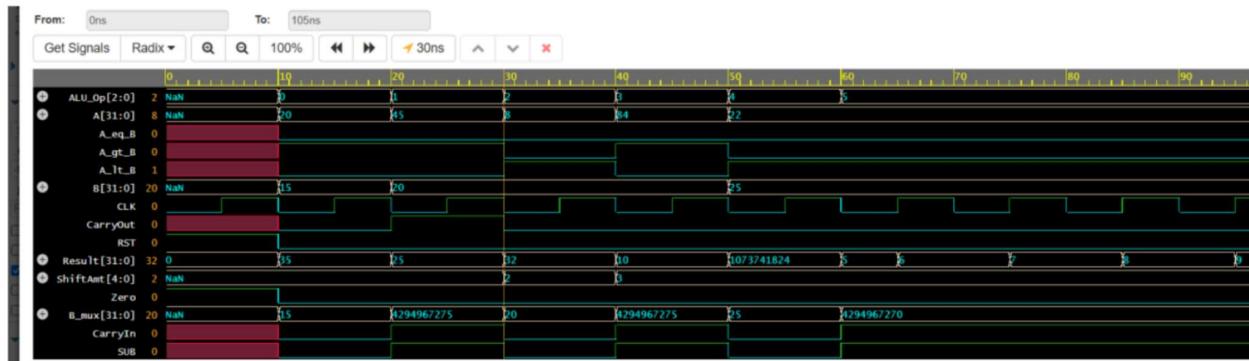


## Functions : Counter



4. Log file of the mapper C Write a Verilog equivalent of a 32-bit ALU Turn in the following:

1. Screen capture of the waveforms generated by the behavioral simulation tools



## 2. Log file of the mapper

```
Design Summary
-----
Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of 4 input LUTs:          98 out of 11,776   1%
Logic Distribution:
  Number of occupied Slices:      49 out of 5,888   1%
  Number of Slices containing only related logic: 49 out of 49 100%
  Number of Slices containing unrelated logic:    0 out of 49  0%
  *See NOTES below for an explanation of the effects of unrelated logic.
Total Number of 4 input LUTs:          98 out of 11,776   1%
Number of bonded IOBs:                101 out of 372   27%

Peak Memory Usage: 158 MB
Total REAL time to MAP completion: 6 secs
Total CPU time to MAP completion: 5 secs
```