Lab 2 (EE533)
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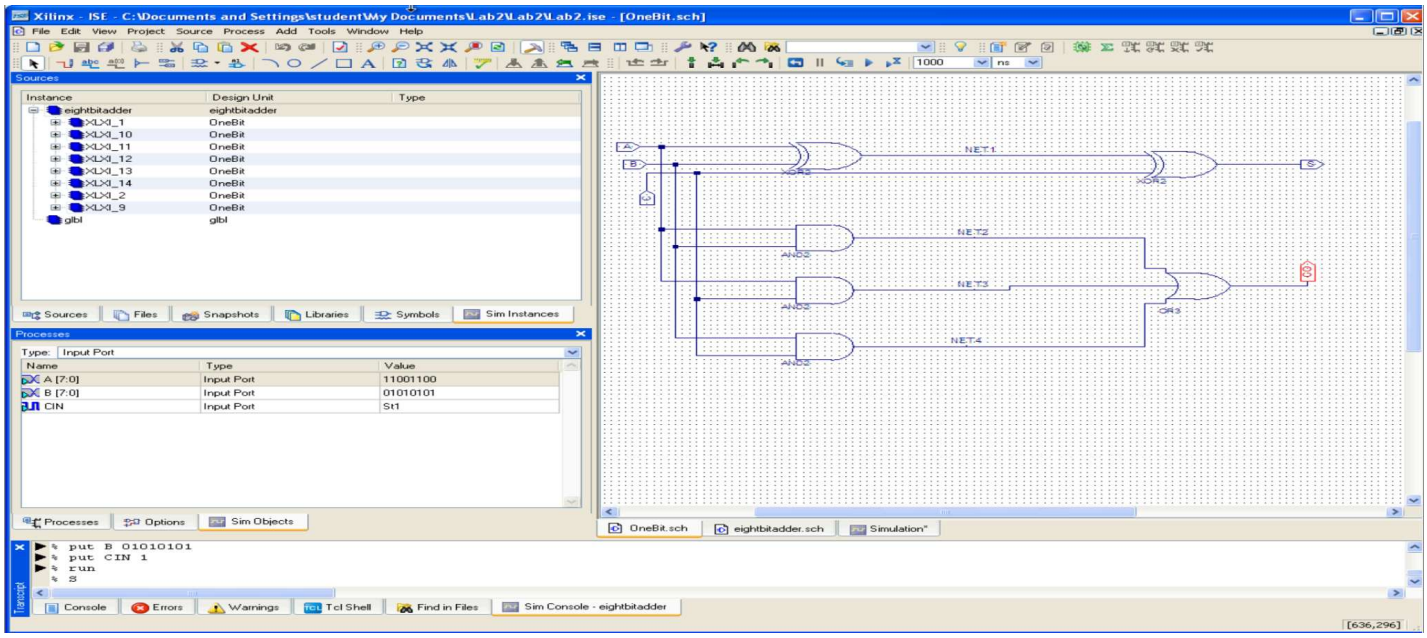
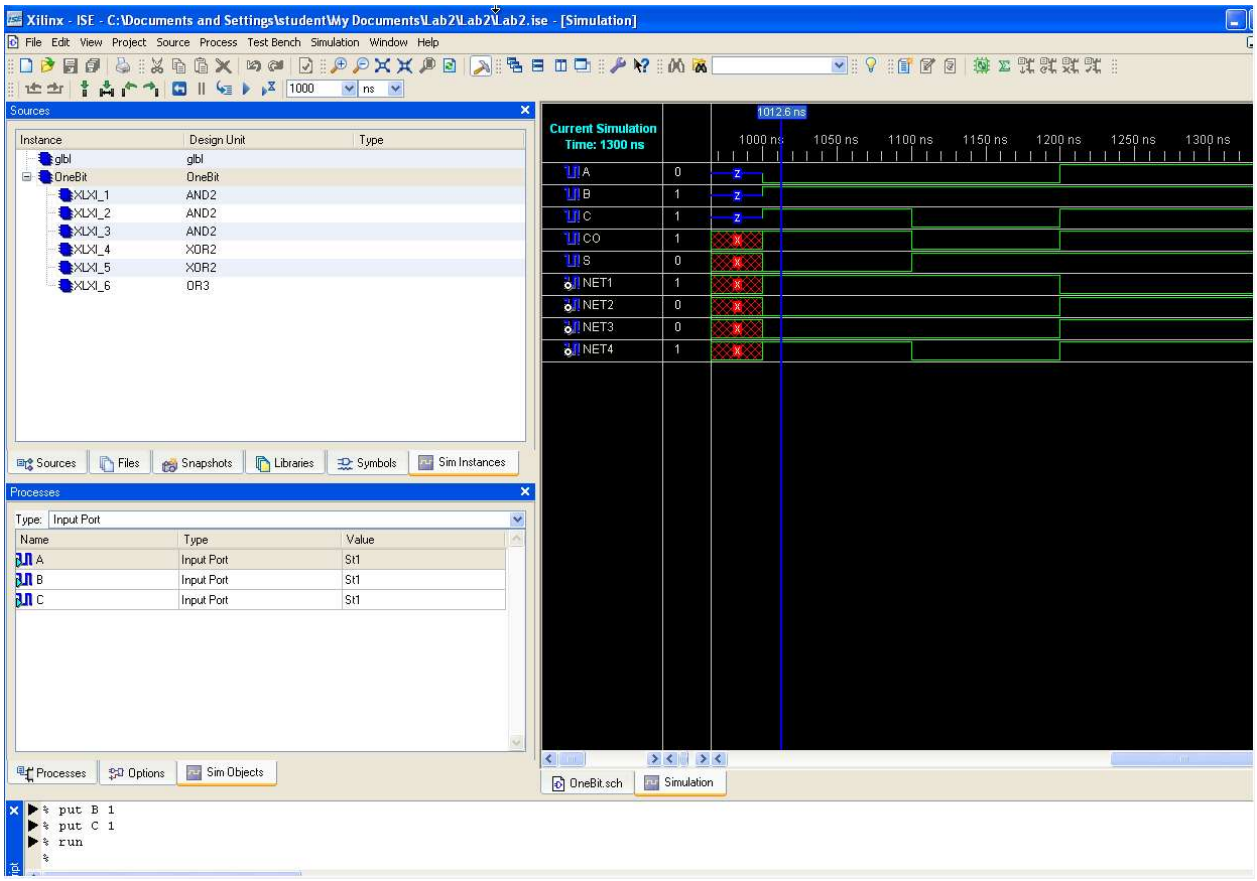
Github link : https://github.com/prathamesh-hirekodi/EE533

Designing and Simulating a Synchronous 8-bit Adder

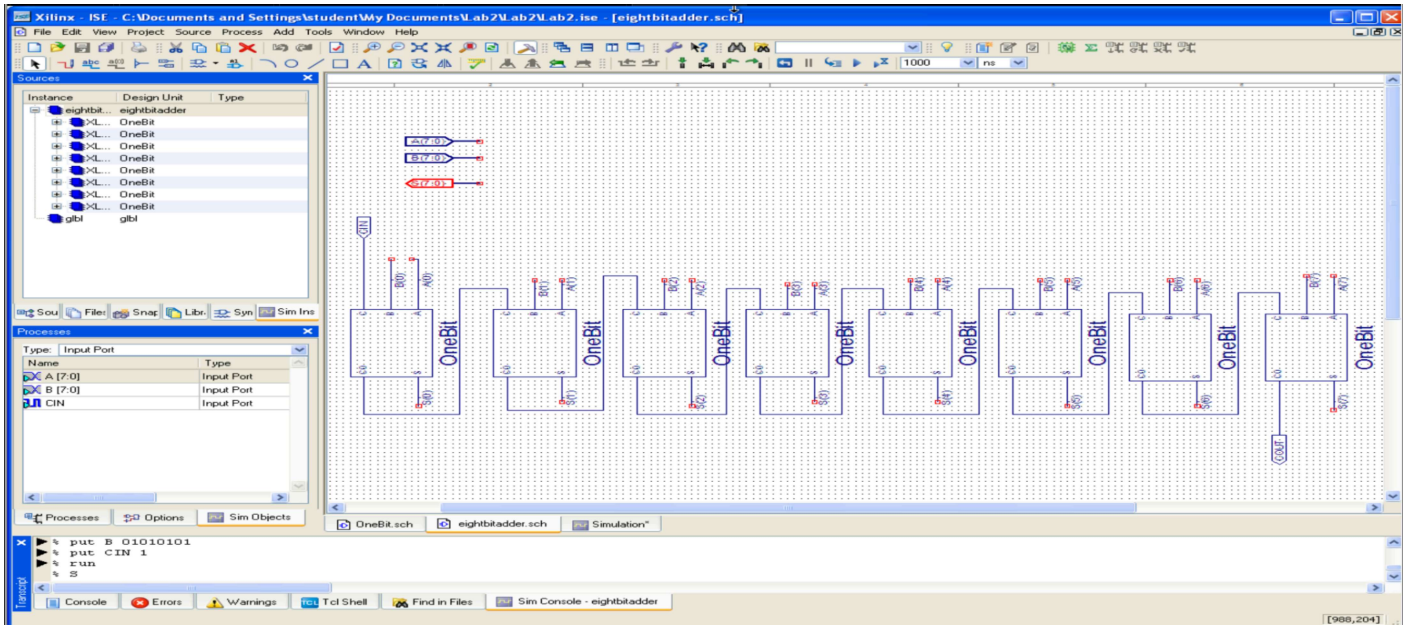
For this part, you must go through the same steps taken in the in-depth tutorial (Part 1) to build and simulate an 8-bit adder using eight 1-bit full adders and D-flip flops available (DO NOT USE THE IP CORE TO GENERATE ANY OF THE COMPONENTS) A synchronous adder has a D-flip flop before the input pins and a D-flip flop after the output pins of the adder circuit. The following must be turned in:

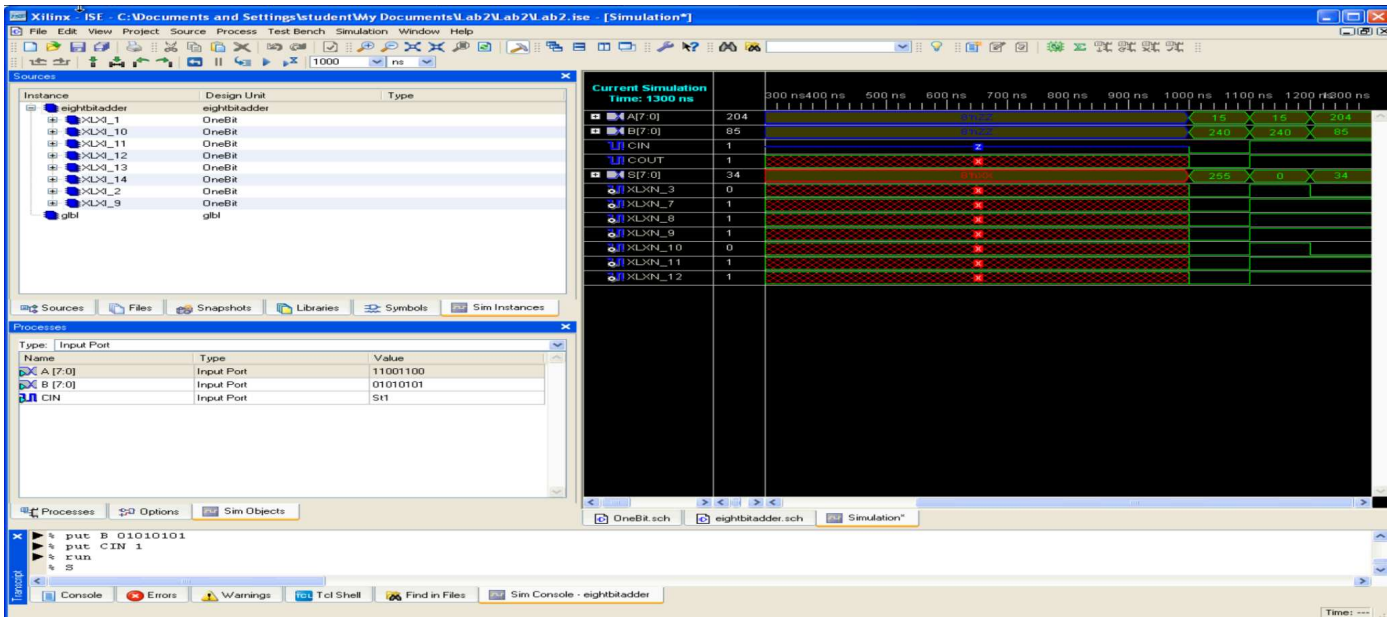
Figure 1:
1-bit Full Adder Figure

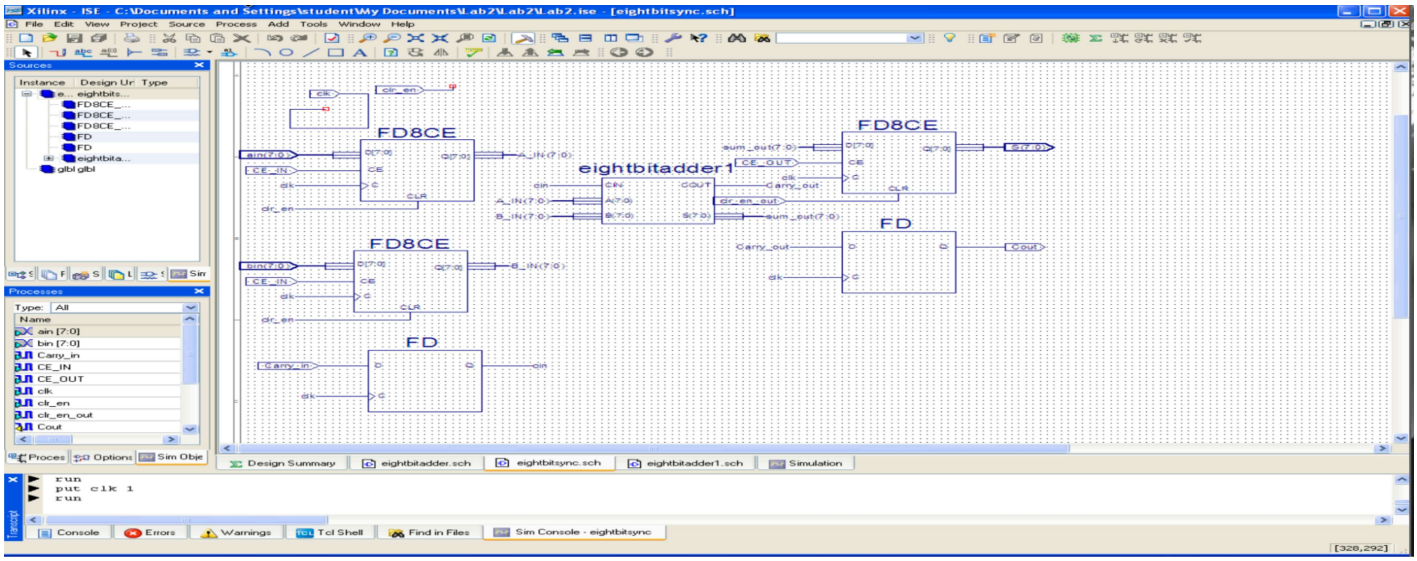



Xilinx - ISE - C:\Documents and Settings\student\My Documents\Lab2\Lab2\Lab2.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources
Instance
Design Unit
Type
glbl
OneBit
XLXI_1
XLXI_2
XLXI_3
XLXI_4
XLXI_5
XLXI_6
AND2
AND2
AND2
XOR2
XOR2
OR3
Sources
Files
Snapshots
Libraries
Symbols
Sim Instances
Processes
Type: Input Port
Name
Type
Value
A
B
C
Input Port
St1
Processes
Options
Sim Objects
Current Simulation Time: 1300 ns
1012.6 ns
1000 ns
1050 ns
1100 ns
1150 ns
1200 ns
1250 ns
1300 ns
A
B
C
CO
S
NET1
NET2
NET3
NET4
OneBit.sch
Simulation
% put B 1
% put C 1
% run
%

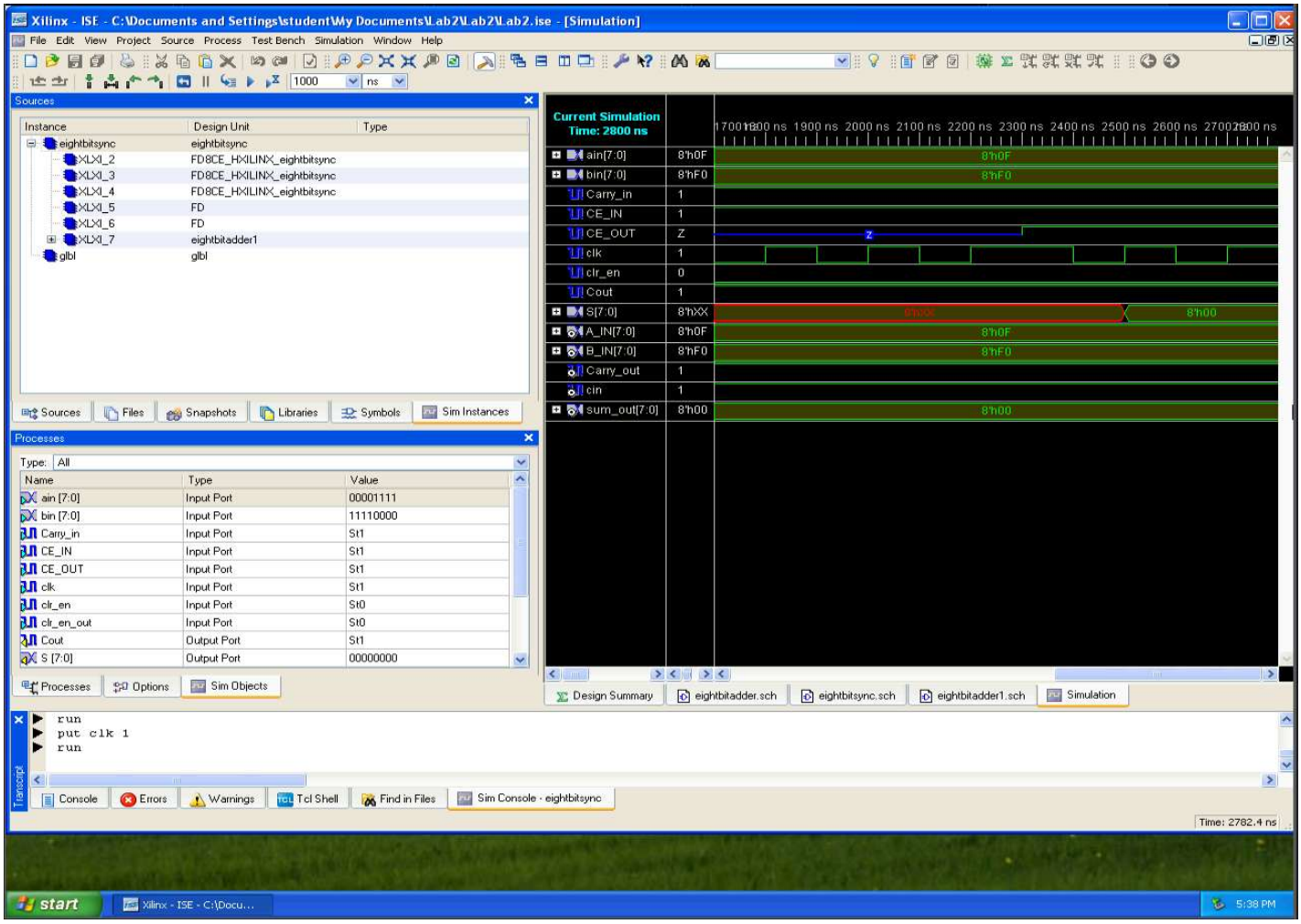
2: 8-bit Adder


Xilinx - ISE - C:\Documents and Settings\student\My Documents\Lab2\Lab2.ise - [eightbitadder.sch]
File Edit View Project Source Process Add Tools Window Help
Sources
Instance Design Unit Type
eightbit... eightbitadder
OneBit
glbl
A[7:0]
B[7:0]
S[7:0]
CIN
COUT
Processes
Type: Input Port
Name Type
A [7:0] Input Port
B [7:0] Input Port
CIN Input Port
Processes Options Sim Objects
OneBit.sch eightbitadder.sch Simulation*
put B 01010101
put CIN 1
run
S
Console Errors Warnings Tcl Shell Find in Files Sim Console - eightbitadder


Xilinx - ISE - C:\Documents and Settings\student\My Documents\Lab2\Lab2.ise - [Simulation*]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources
Instance Design Unit Type
eightbitadder eightbitadder
OneBit
glbl
Sources Files Snapshots Libraries Symbols Sim Instances
Processes
Type: Input Port
Name Type Value
A [7:0] Input Port 11001100
B [7:0] Input Port 01010101
CIN Input Port St1
Processes Options Sim Objects
Current Simulation Time: 1300 ns
300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns 1000 ns 1100 ns 1200 ns 1300 ns
A[7:0] 204
B[7:0] 85
CIN 1
COUT 1
S[7:0] 34
XLXN_3 0
XLXN_7 1
XLXN_8 1
XLXN_9 1
XLXN_10 0
XLXN_11 1
XLXN_12 1
OneBit.sch eightbitadder.sch Simulation*
put B 01010101
put CIN 1
run
S
Console Errors Warnings Tcl Shell Find in Files Sim Console - eightbitadder

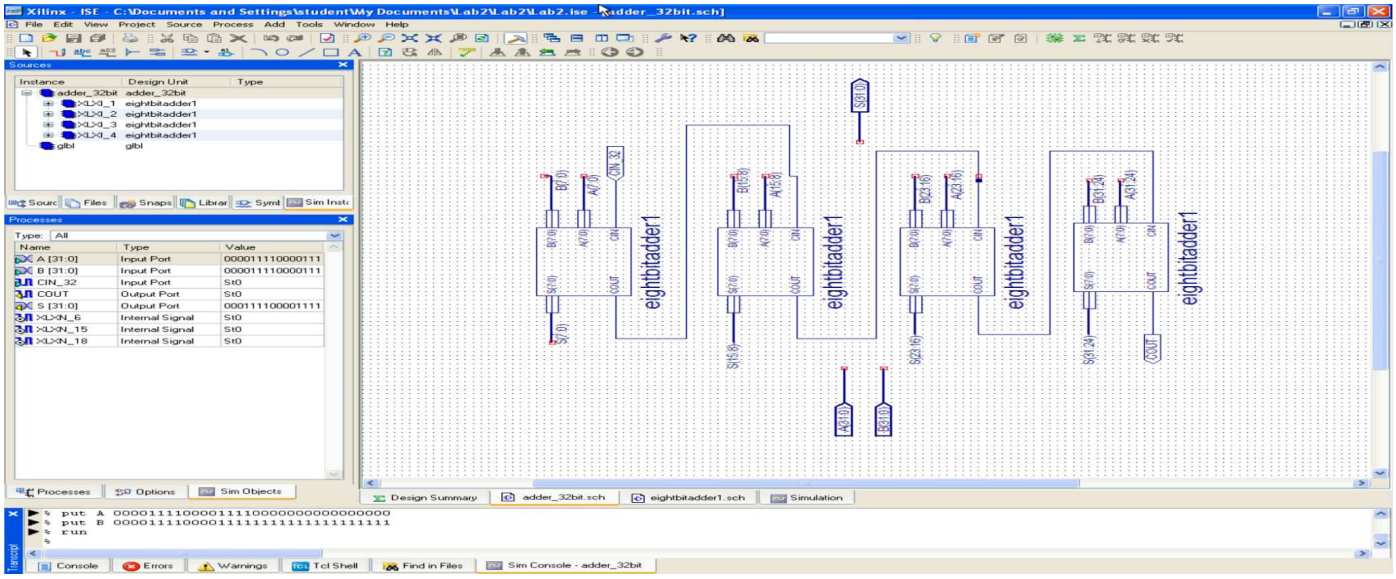


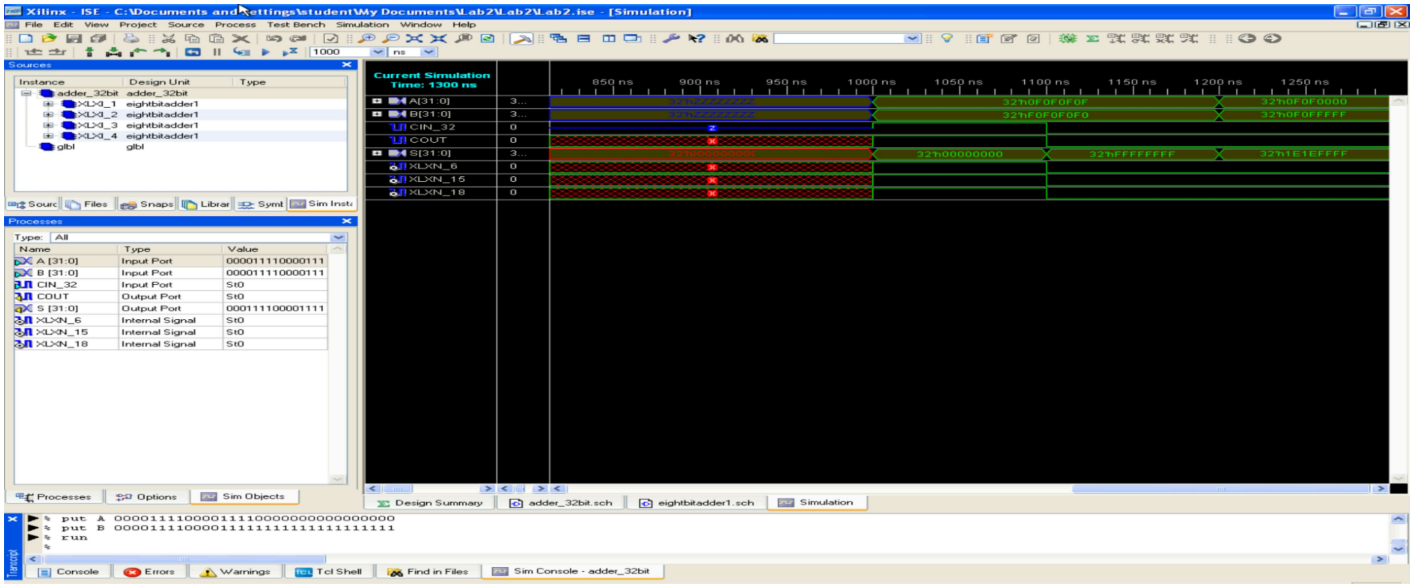
8 bit synchronous adder Schematic and behavioral simulation



3. Extending Adder into 32-bit ALU DO NOT USE THE IP CORE A Extend the 8-bit Adder into a 32-bit Adder by instantiating and connecting 4 adders Turn in the following:

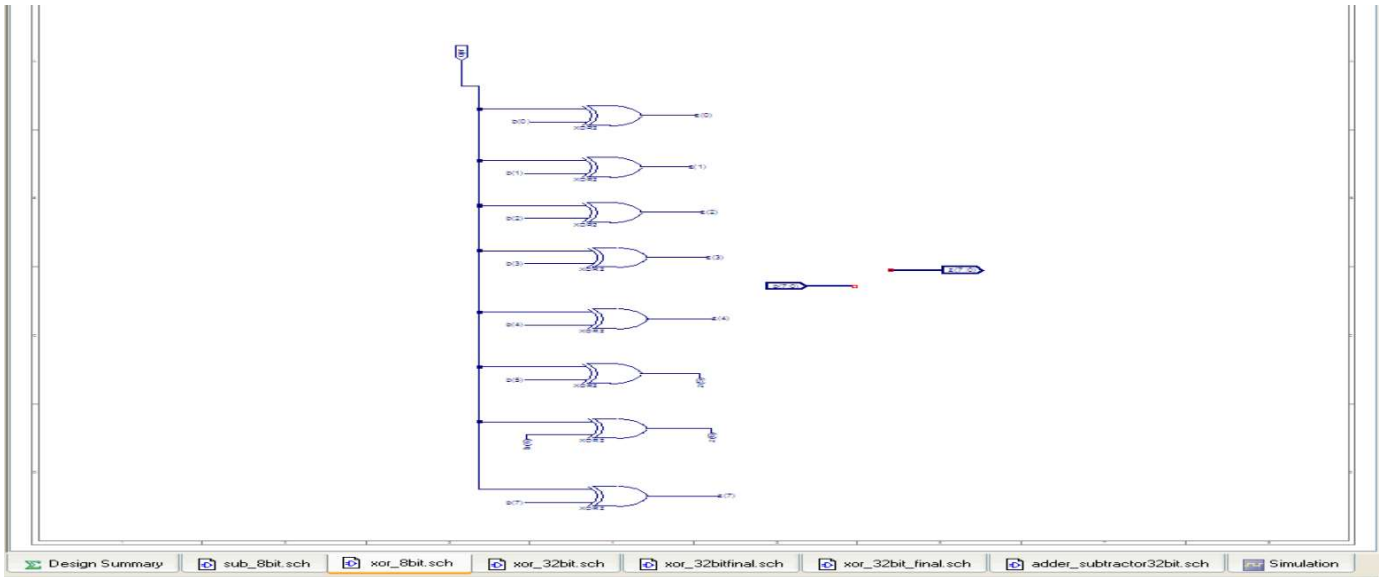
1. Screen capture of your schematics



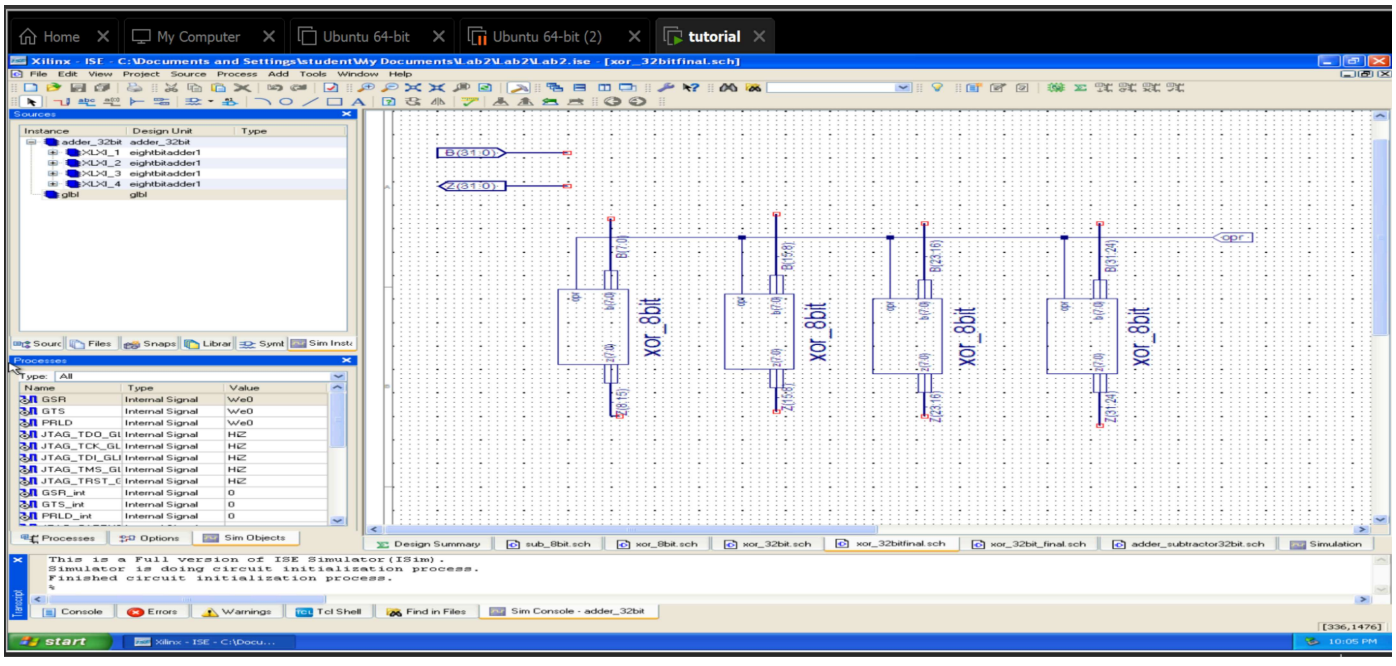


2. 32 bit adder_subtractor

For this first I have created a 8 bit XOR

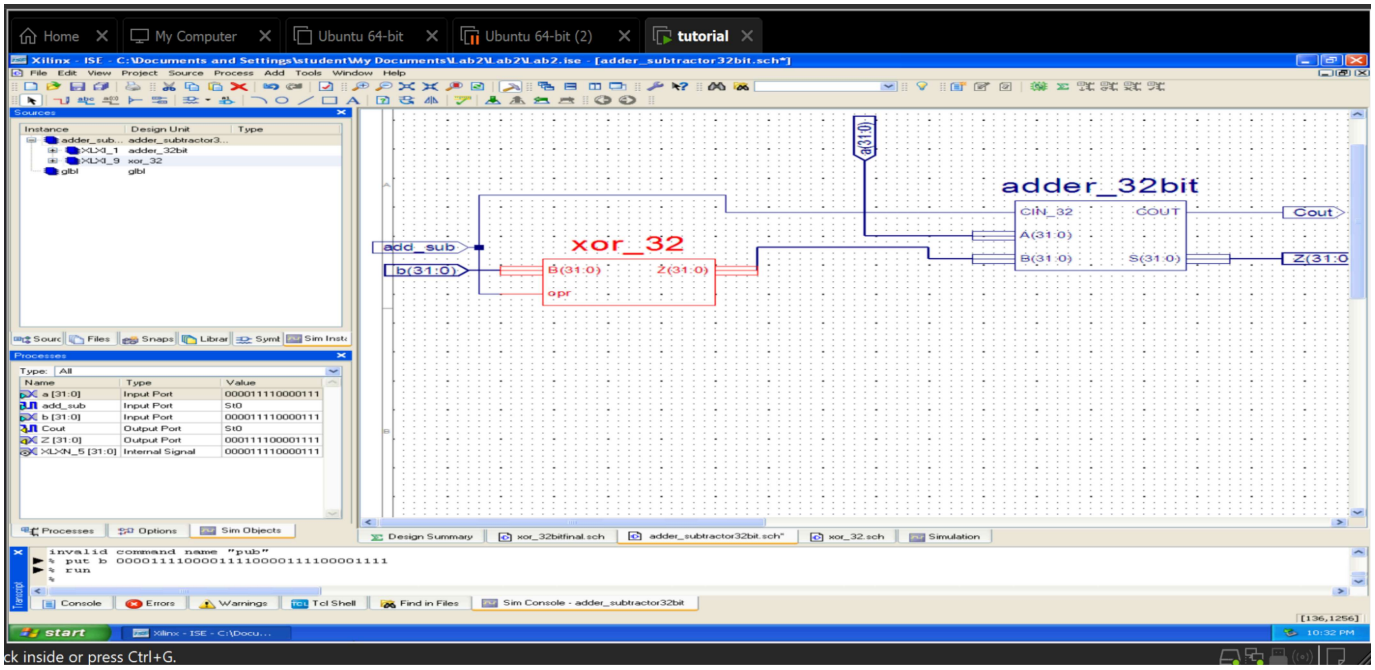


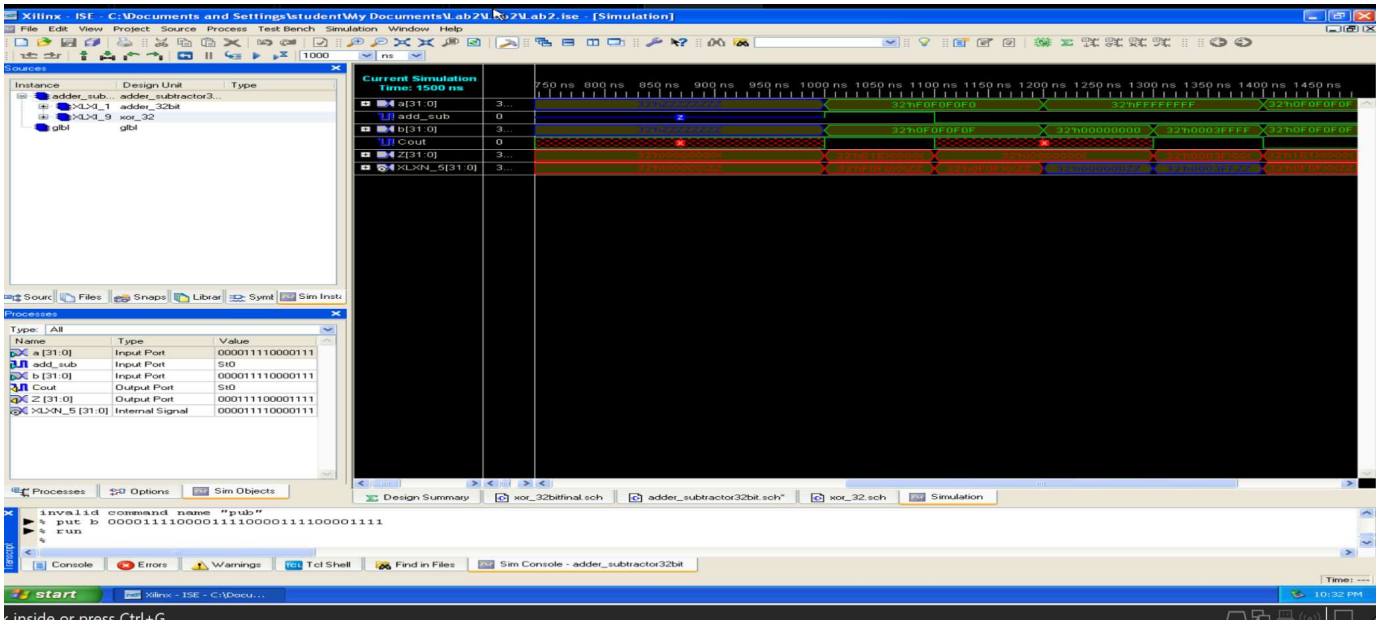
And then a 32 bit XOR



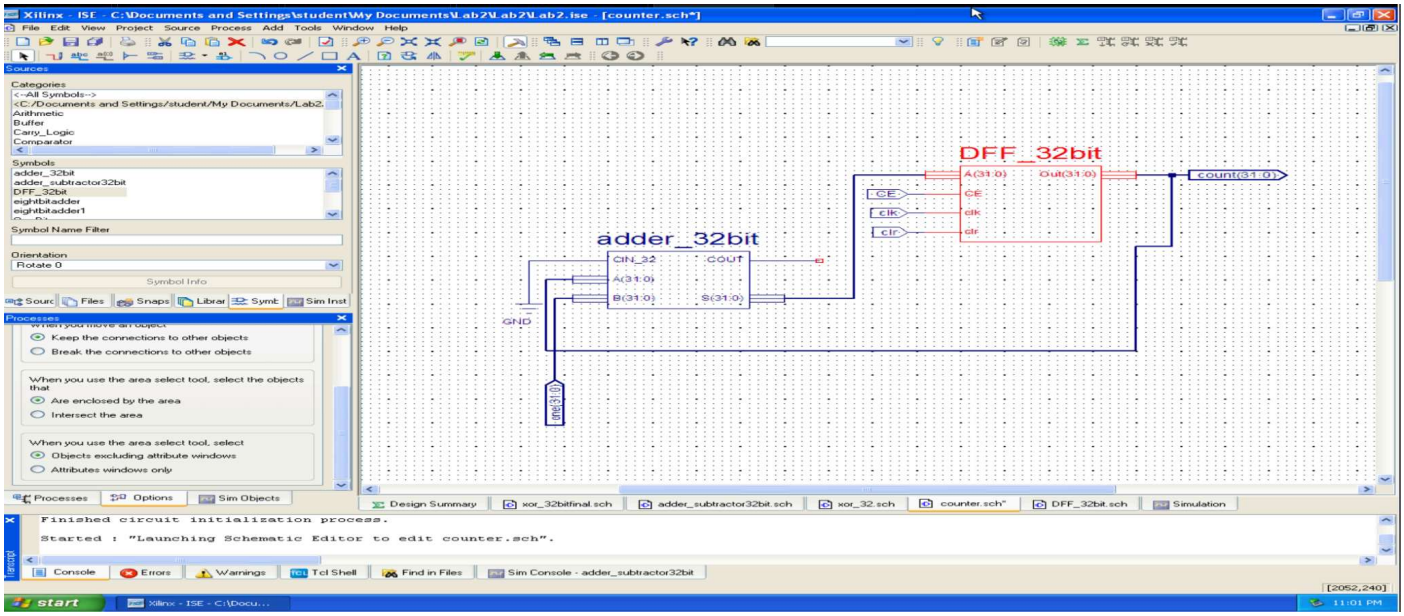
2. Screen capture of the waveforms generated by the behavioral simulation tools B Extend the 32-bit Adder to have other functions, including a subtractor, a shifter, and two other functions of your choice. Go through the mapping process of the tools to get the gate counts, such as the number of D-FF and LUTs.

32 bit adder_subtractor

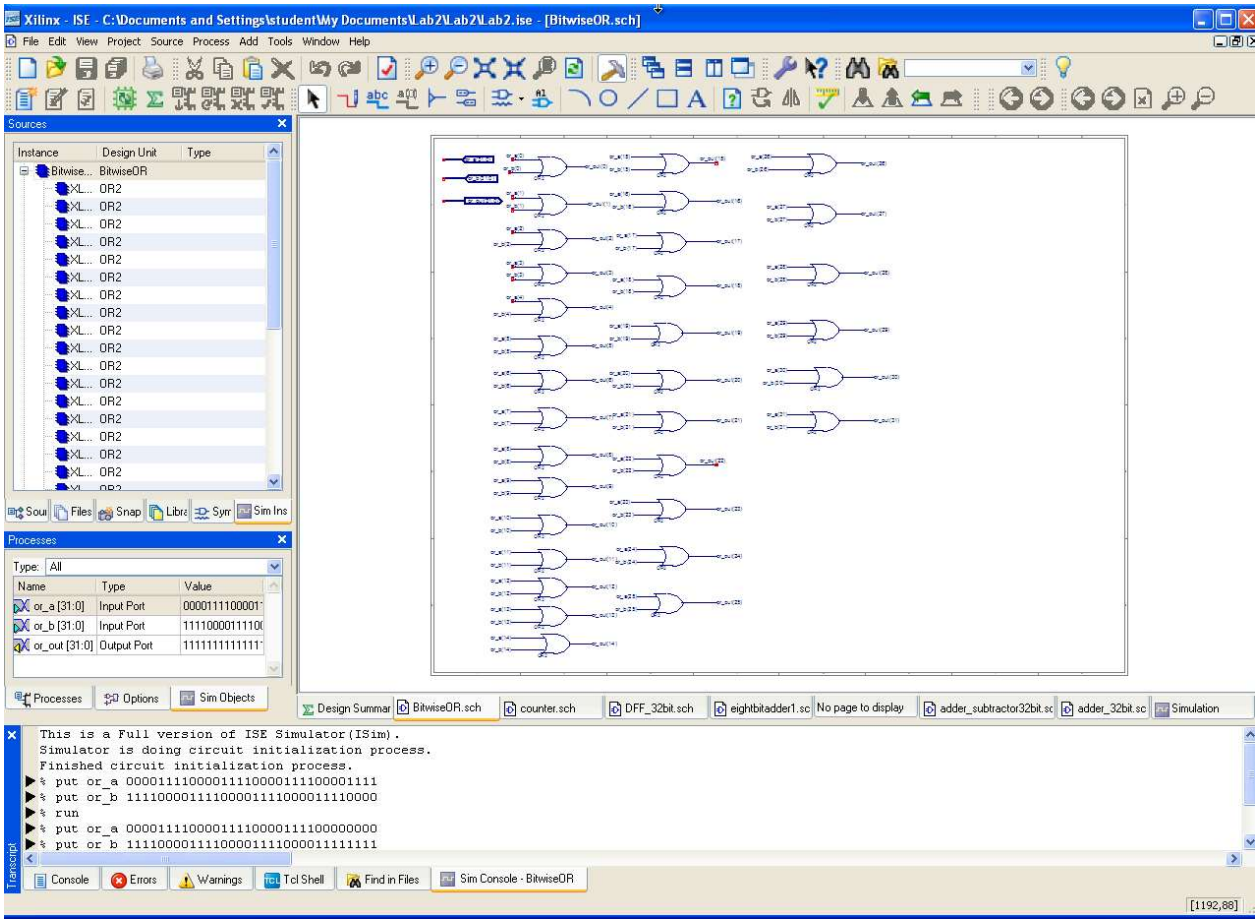




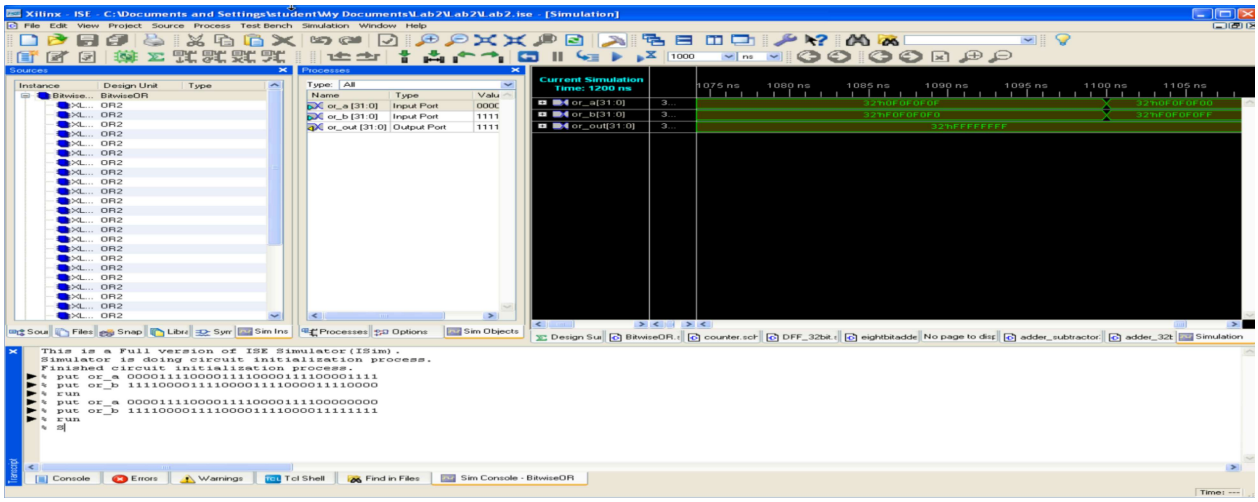
Functions : Counter



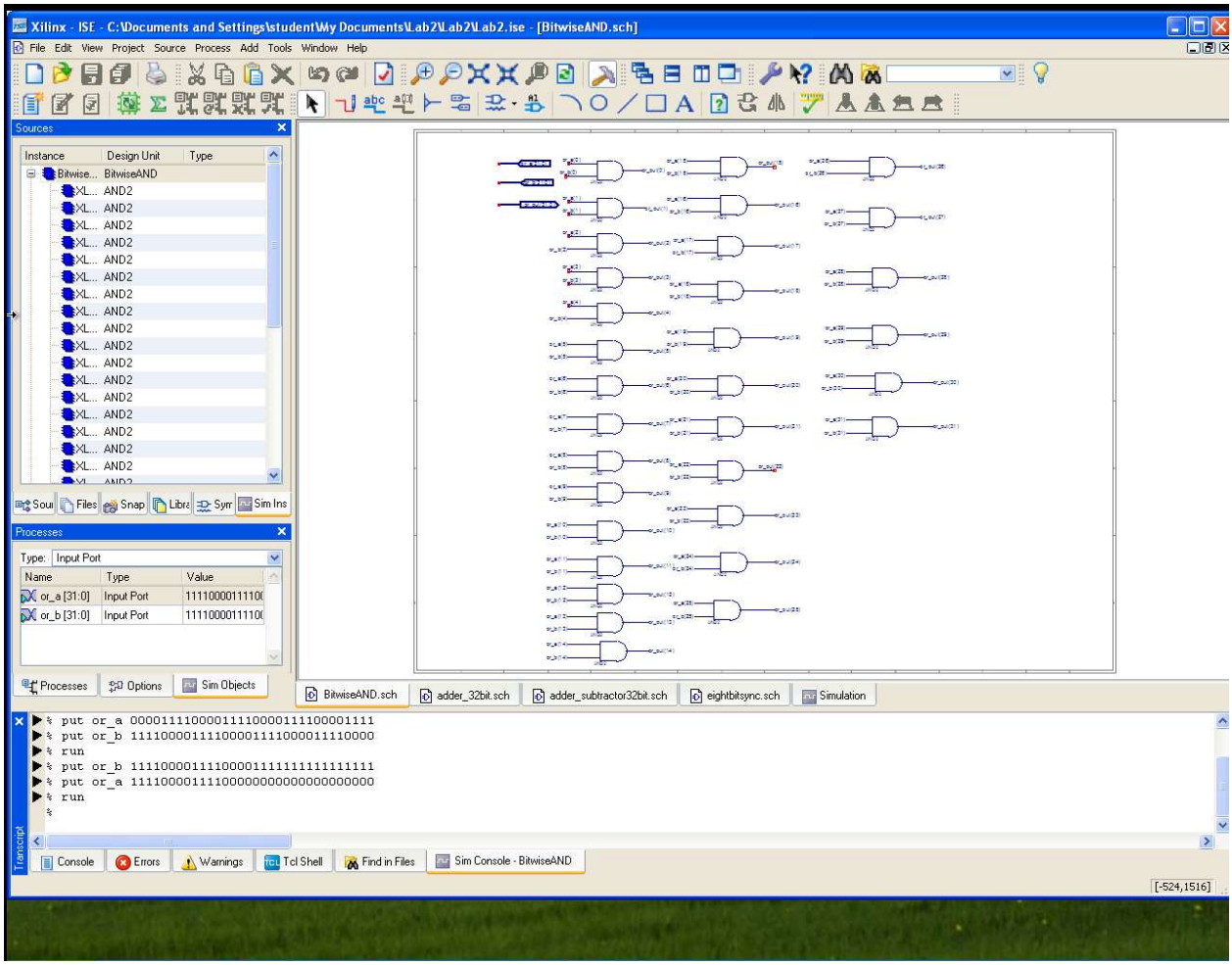
Function : 32Bitwise OR Schematic



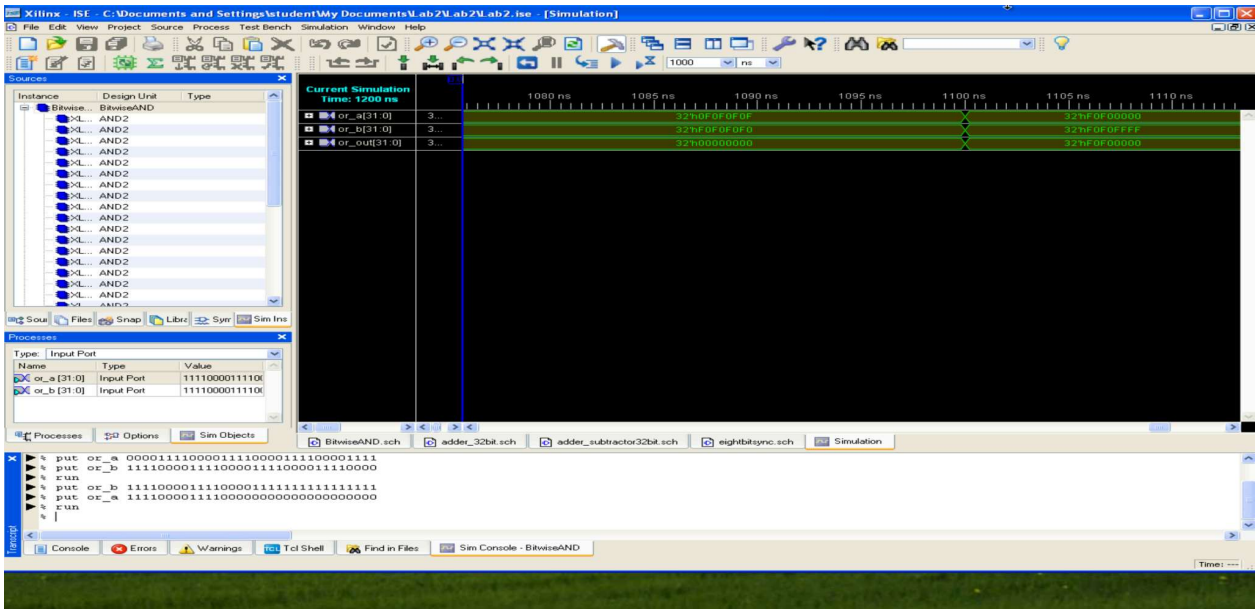
32BitWiseOR Simulation



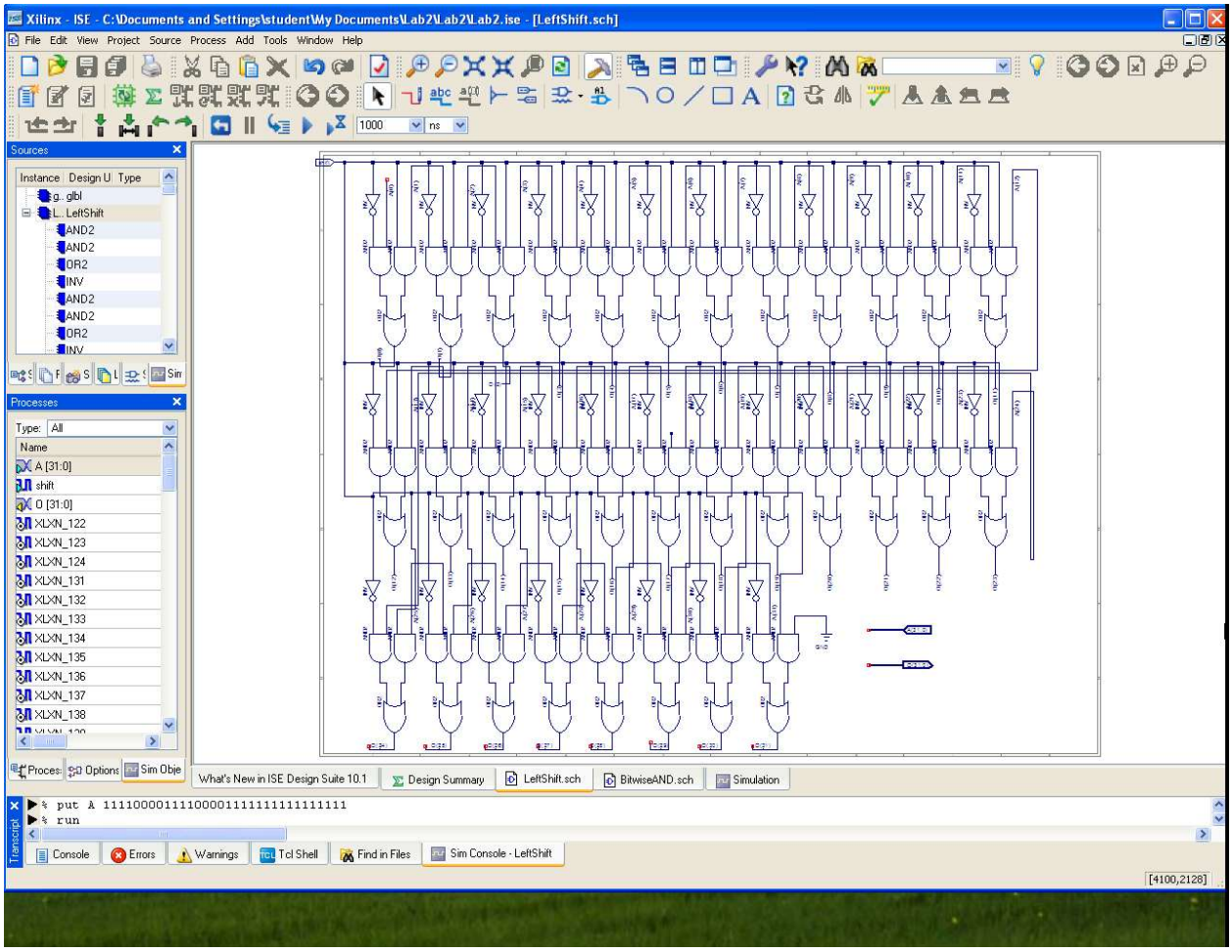
Function: 32BitwiseAND Schematic



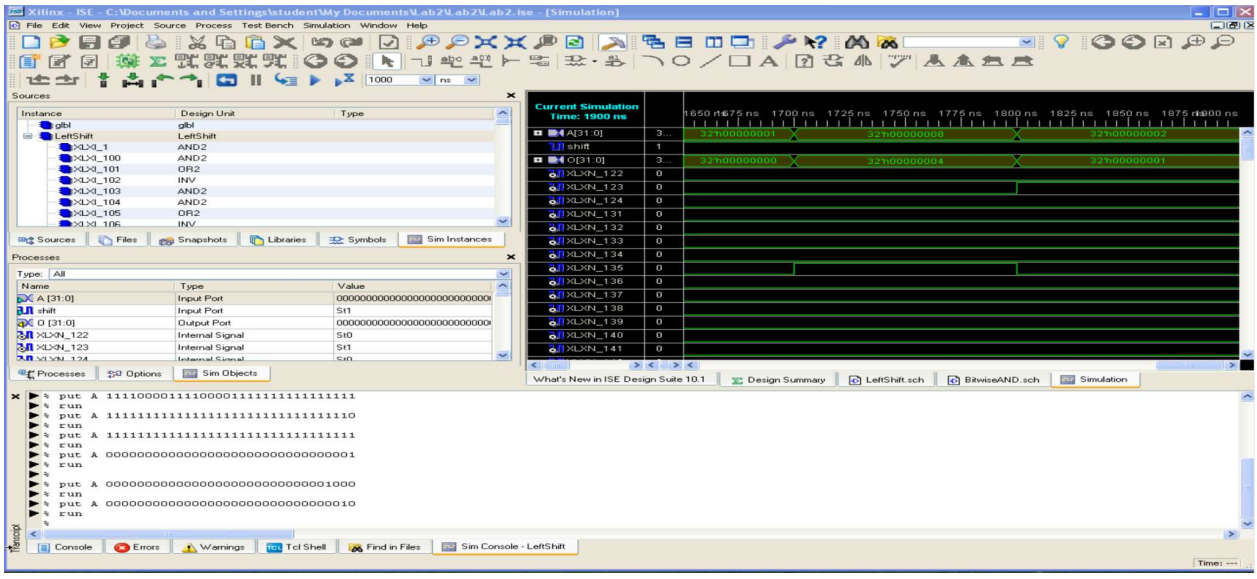
32BitwiseAND Simulation



Function : Shifter

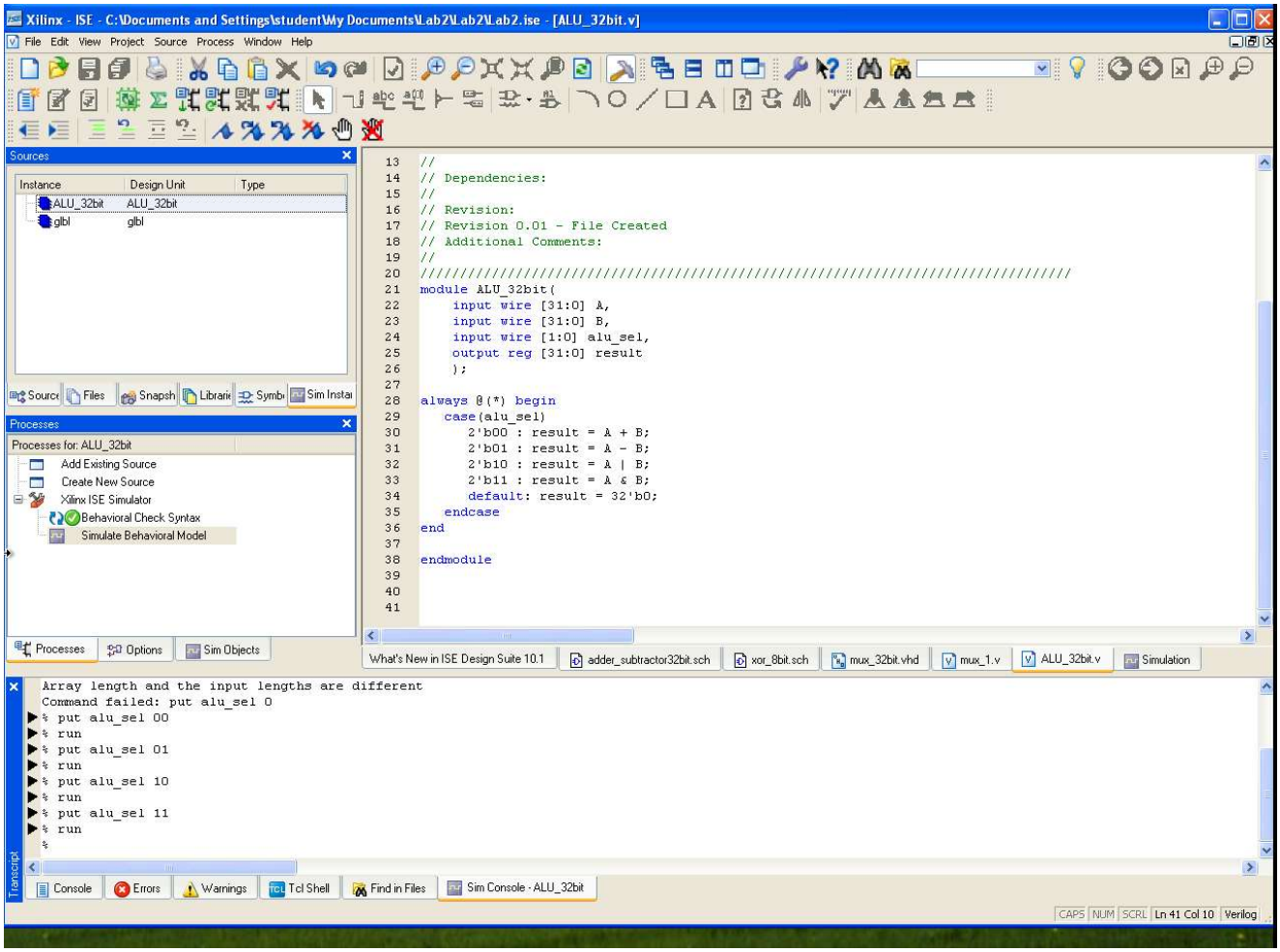


Schematic

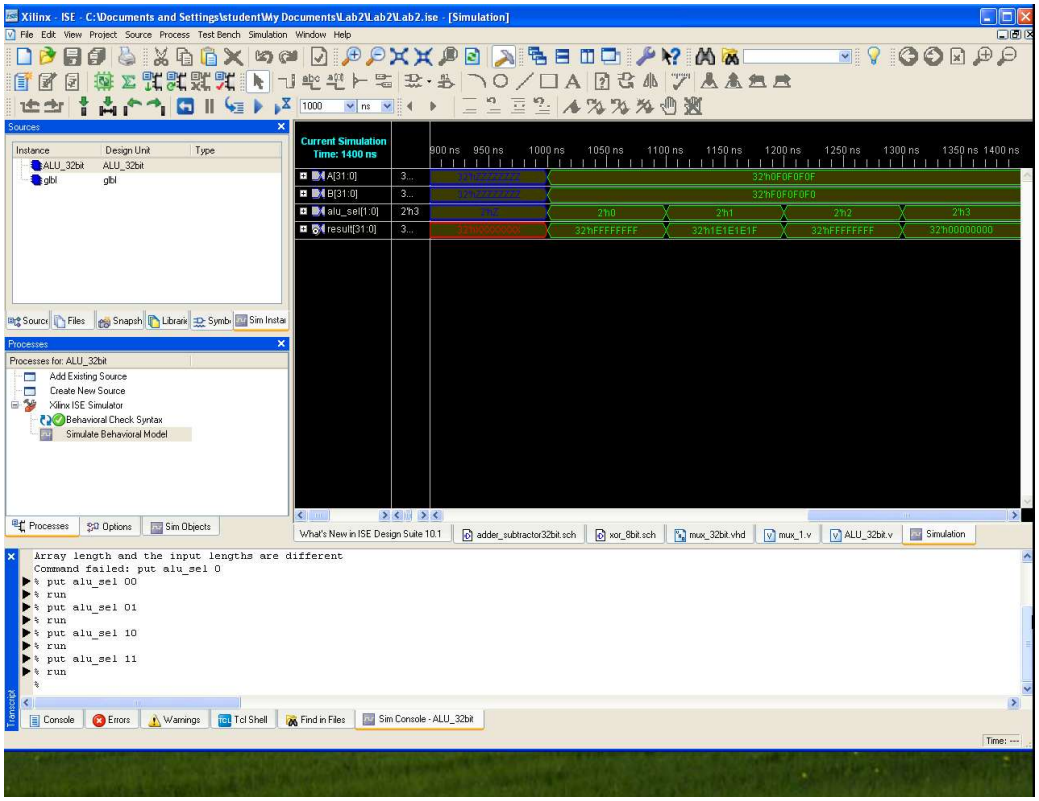


4. Log file of the mapper C Write a Verilog equivalent of a 32-bit ALU Turn in the following:

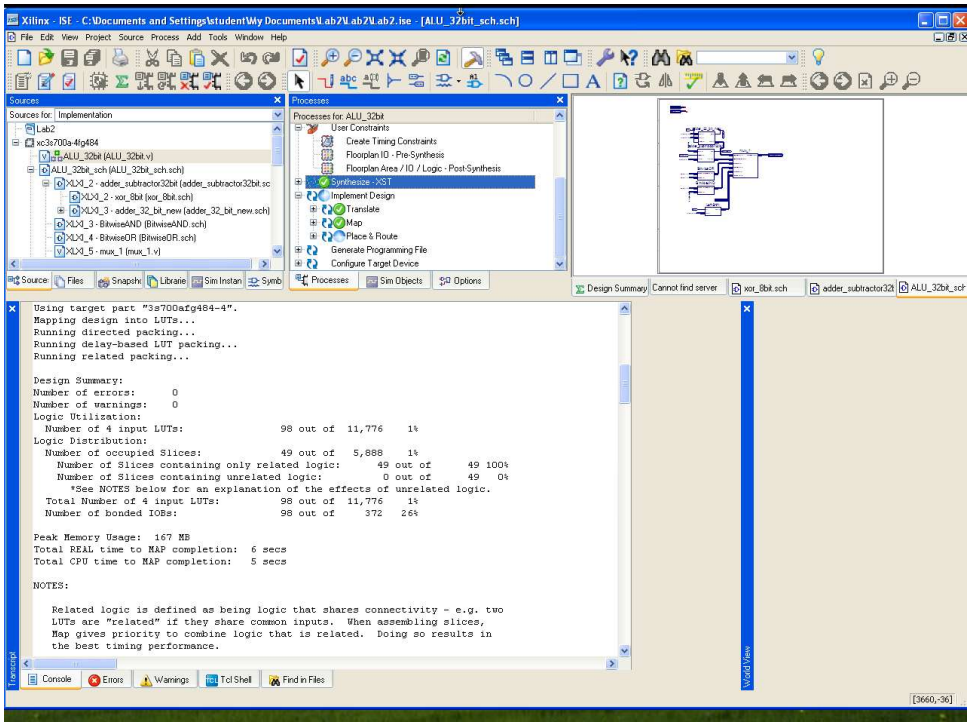
1. Screen capture of the waveforms generated by the behavioral simulation tools



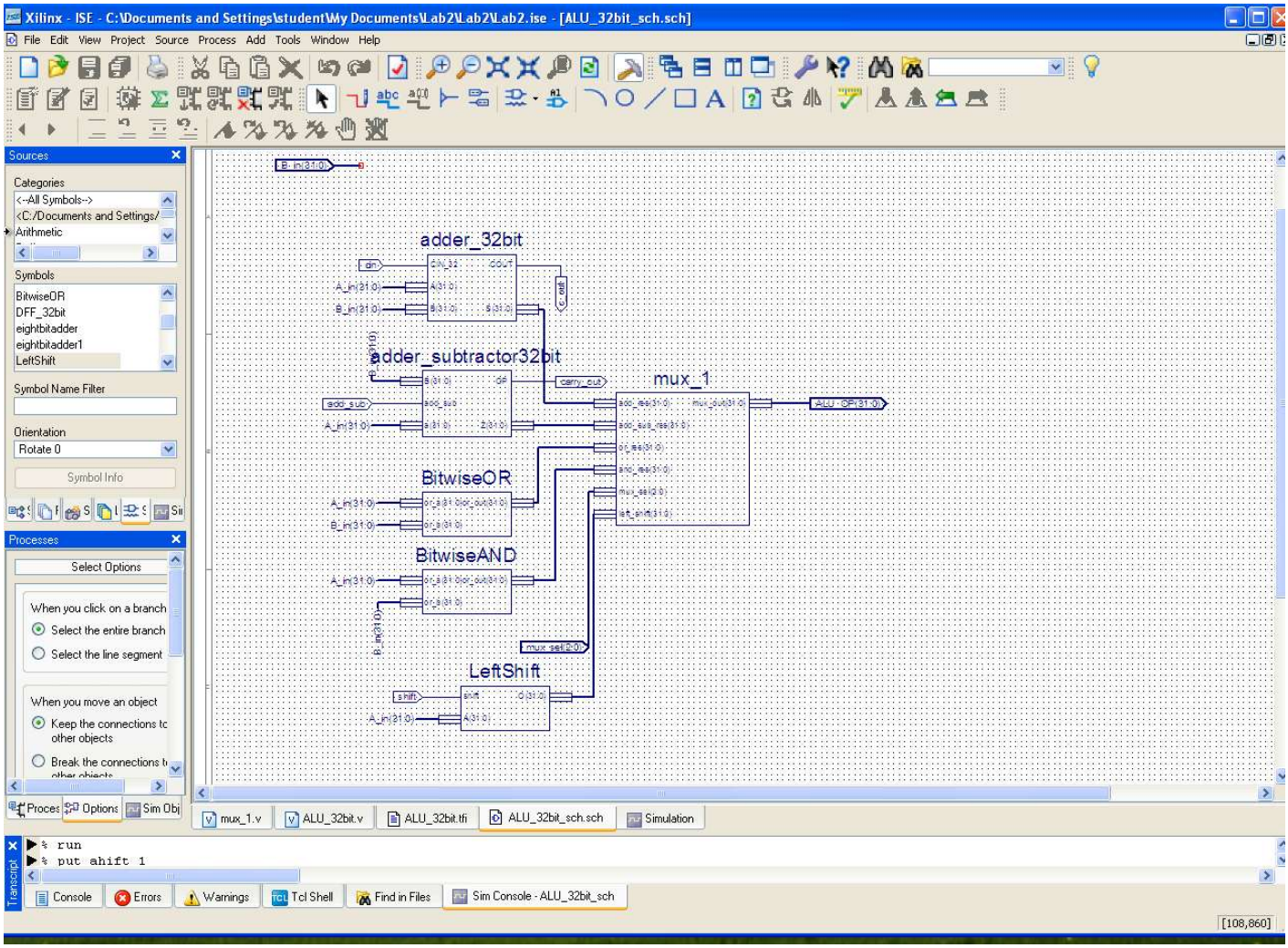
Verilog behavioral Simulation



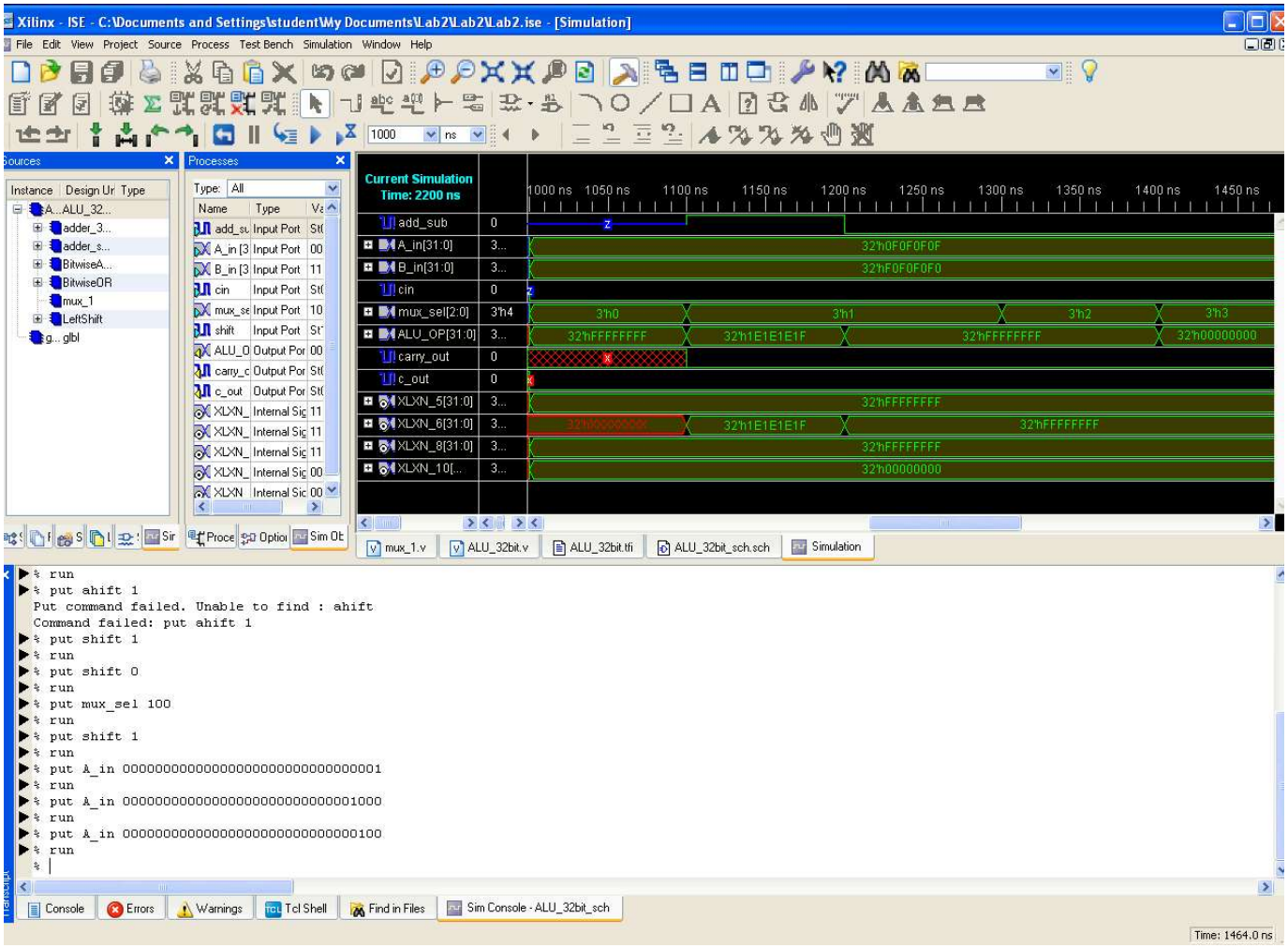
32 Bit Verilog Code - Map Report



32 Bit ALU - Schematic



32 Bit ALU schematic- behavioral Simulation



32 Bit ALU schematic - Map Report