Due Date: Sunday September 29, 11:59pm– Submit this editable **Word** document NOT pdf

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EEDG/CE 6370
Design and Analysis of Reconfigurable Systems
Homework 4 – Physical design

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Part I – Design Implementation and timing analysis

a.) Follow the instructions in the lab sheet and synthesize the design without replacing any LUT in Chip Planner. Report the logic utilization (ALMs/ALUTs), total registers, pins, block memory, DSP blocks and DLLs used using the fitter report. Include a screenshot of the report too.

Marks
2

ALMs/ALUTs	FFs	IOs	DSPs	BRAM	DLLs
49/84	77	241	0	0	0

ALMs, Registers, Pins I/Os, DLLs, BRAM, DSP:

Fitter Summary

<<Filter>>

Fitter Status	Successful - Sun Sep 29 20:17:15 2024
Quartus Prime Version	22.1std.2 Build 922 07/20/2023 SC Lite Edition
Revision Name	DE1_SoC_i2sound
Top-level Entity Name	DE1_SoC_i2sound
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	49 / 32,070 (< 1 %)
Total registers	77
Total pins	241 / 457 (53 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total RAM Blocks	0 / 397 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

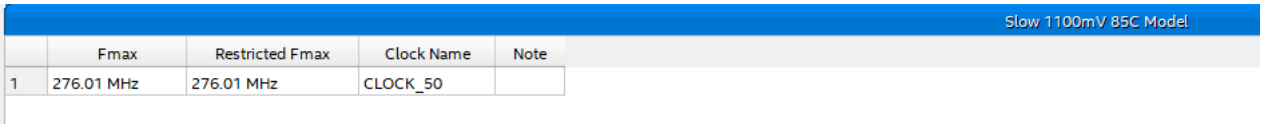
ALUTs:

▼ Combinational ALUT usage for logic	84	
-- 7 input functions	1	
-- 6 input functions	16	
-- 5 input functions	7	
-- 4 input functions	16	
-- <=3 input functions	44	
Combinational ALUT usage for route-throughs	6	

b.) Open the Timing analyzer and report the maximum frequency. Include screenshot.

Marks
2

Maximum Frequency: 276.01MHz

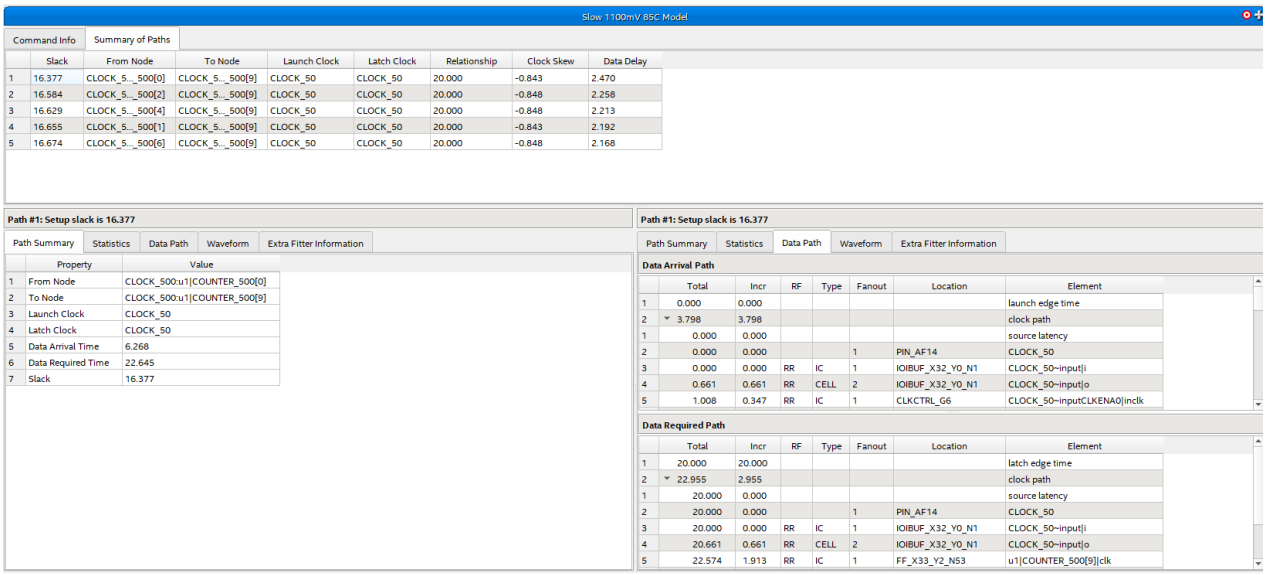


c.) Annotate here the 5 longest critical paths from Timing analyzer and annotate here their delay and slack. Include screenshot.

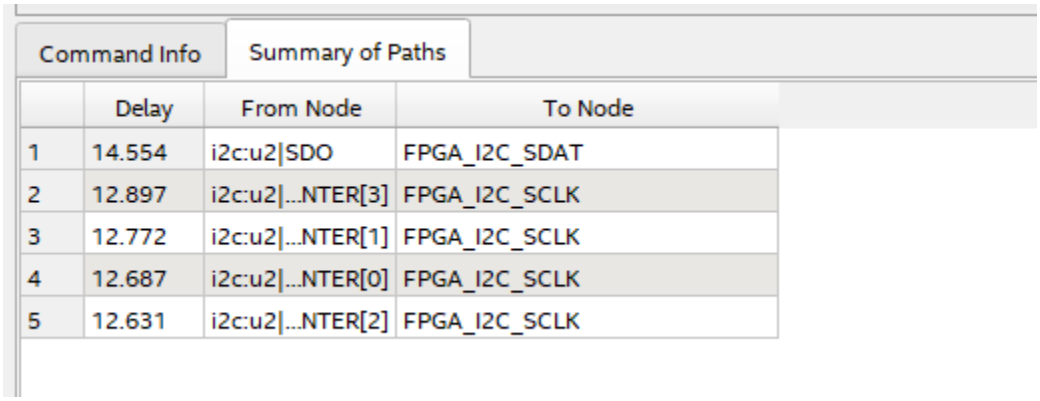
Marks
2

Critical Path	Data Delay	Delay	Slack
1	2.470	14.554	16.377
2	2.258	12.897	16.584
3	2.213	12.772	16.629
4	2.192	12.687	16.655
5	2.168	12.631	16.674

Slack:



Delay:



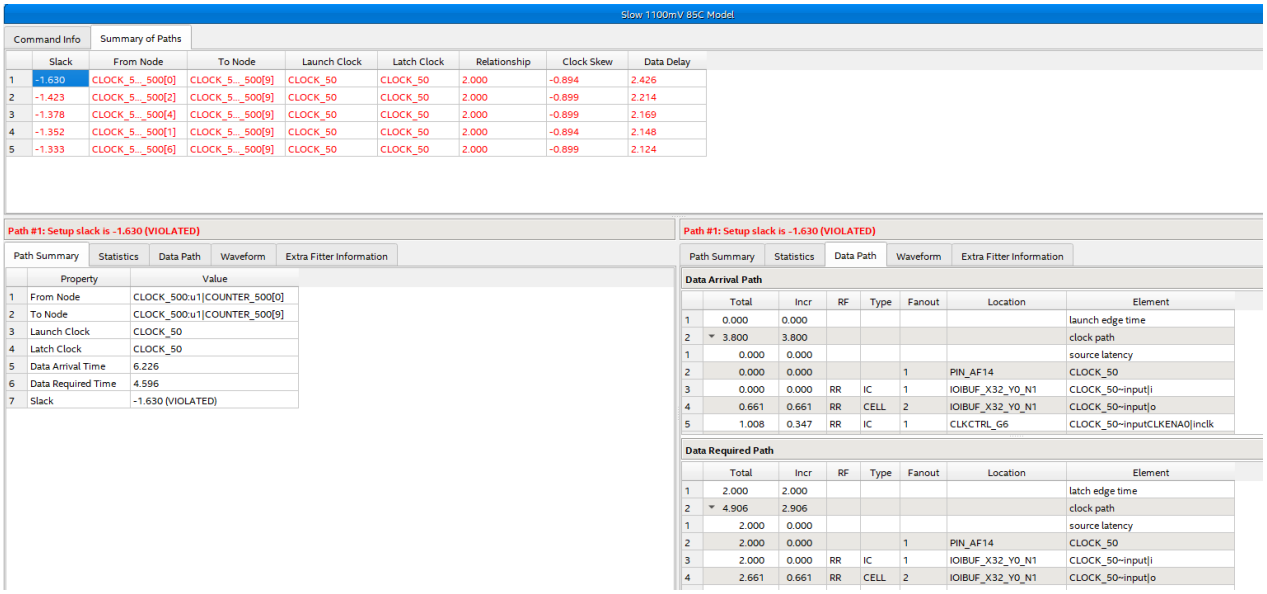
e.) Change the sdc constraint file setting the clock constraint to a period of 2ns (500Mhz) instead of 20ns (50Mhz). Reopen the Timing analyzer and report the 5 longest critical paths and their slack. Compare with the results in c). What did you notice? (include screenshot of the delays)

Marks
2

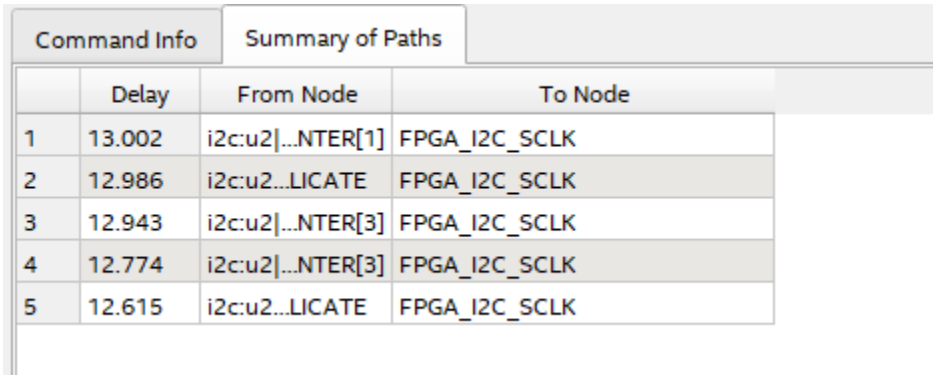
Critical Path	Delay	Slack	Data Delay
1	13.002	-1.630	2.404
2	12.986	-1.423	2.172
3	12.943	-1.378	2.127

4	12.774	-1.352	2.082
5	12.615	-1.333	2.461

Slack:



Delay:



Observation:

- Delay: for 20ns constraints the longest delay was 14.554ns whereas for 2ns it became 13.002ns.
- Slack: for 20ns constraints all slacks were positive whereas for 2ns all slacks became negative.
- Result: The negative slack indicates that the design cannot meet the new timing requirements, which means that the circuit cannot operate correctly at 500MHz.

Part II – Chip Planner

a.) Change back the sdc clock constraint to 20ns. Move the resources explained in the lab sheet (top and bottom left) using the Chip planner and re-compile the program.
Report the 5 longest critical paths from Timing Analyzer after the replacement. How did this affect the critical path? Compare the results with the original placement results. Explain why.

Marks
6

	Critical Paths Original	**Critical Paths New (moved)**
1	CLOCK_500:u1|COUNTER_500[0] to CLOCK_500:u1|COUNTER_500[9]	CLOCK_500:u1|COUNTER_500[0] to CLOCK_500:u1|COUNTER_500[9]
2	CLOCK_500:u1|COUNTER_500[2] to CLOCK_500:u1|COUNTER_500[9]	CLOCK_500:u1|COUNTER_500[9] to CLOCK_500:u1|COUNTER_500[9]
3	CLOCK_500:u1|COUNTER_500[4] to CLOCK_500:u1|COUNTER_500[9]	CLOCK_500:u1|COUNTER_500[2] to CLOCK_500:u1|COUNTER_500[9]
4	CLOCK_500:u1|COUNTER_500[1] to CLOCK_500:u1|COUNTER_500[9]	CLOCK_500:u1|COUNTER_500[1] to CLOCK_500:u1|COUNTER_500[9]
5	CLOCK_500:u1|COUNTER_500[6] to CLOCK_500:u1|COUNTER_500[9]	CLOCK_500:u1|COUNTER_500[9] to CLOCK_500:u1|COUNTER_500[10]

Critical Path Original

Command Info | Summary of Paths

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	16.377	CLOCK_5..._500[0]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	-0.843	2.470
2	16.584	CLOCK_5..._500[2]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	-0.848	2.258
3	16.629	CLOCK_5..._500[4]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	-0.848	2.213
4	16.655	CLOCK_5..._500[1]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	-0.843	2.192
5	16.674	CLOCK_5..._500[6]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	-0.848	2.168

Critical Path New

Command Info | Summary of Paths

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	12.681	CLOCK_5..._500[0]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	1.177	8.186
2	13.035	CLOCK_5..._500[9]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	-0.171	6.484
3	14.788	CLOCK_5..._500[2]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	1.131	6.033
4	14.890	CLOCK_5..._500[1]	CLOCK_5..._500[9]	CLOCK_50	CLOCK_50	20.000	1.134	5.934
5	15.012	CLOCK_5..._500[9]	CLOCK_5...500[10]	CLOCK_50	CLOCK_50	20.000	-2.307	2.371

Changes in .qsf file after placement:

```
set_location_assignment FF_X27_Y80_N28 -to
"CLOCK_500:u1|COUNTER_500[0]"
set_location_assignment LABCELL_X1_Y77_N0 -to "CLOCK_500:u1|Add2~1"
set_location_assignment LABCELL_X1_Y77_N3 -to "CLOCK_500:u1|Add2~37"
```

Observation:

- Moving the components altered the physical distance between connected elements, affecting signal propagation times.
- As the new placement forced the router to use different paths, optimizing some connections while making others longer.
- While the specific timings changed, the fundamental timing-critical section of the circuit remained similar. This suggests that the manual placement adjustments had a limited impact on the overall timing performance of the design.

These are changes that were made in Quartus prime QSF File while the cells were moved in the chip planner

set_location_assignment FF_X27_Y80_N28 -to "CLOCK_500:u1|COUNTER_500[0]"
set_location_assignment LABCELL_X1_Y77_N0 -to "CLOCK_500:u1|Add2~1"
set_location_assignment LABCELL_X1_Y77_N3 -to "CLOCK_500:u1|Add2~37"

b.) Create a YouTube video showing the working designs and showing how you measured the information reported int this homework

Marks
6

Link: https://youtu.be/z4V1cA9y1s4