EEDG/CE 6370
Design and Analysis or Reconfigurable Systems
Homework 9 – HPS+FPGA

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Student Name:

Part I –Simple HPS+FPGA System

a.) Follow the instructions in the My_First_HPW_FPGA.pdf document provided by Terasic and show that the system is working. In this example the SW running on the HPS does:

- The LED on DE1-SoC will be expected to perform 60 times of LED light shift operation, and then the program is terminated.

Deliverables:

(i) Report the number of FPGA resources used, and the maximum frequency achieved.

(ii) Report the size of the compiled SW program

(iii) A YouTube video showing that the system works.

Marks
6
0

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	2242
2		
3	Combinational ALUT usage for logic	3361
1	-- 7 input functions	29
2	-- 6 input functions	545
3	-- 5 input functions	541
4	-- 4 input functions	821
5	-- <=3 input functions	1425
4		
5	Dedicated logic registers	2945
6		
7	I/O pins	368
8	I/O registers	186
9	Total MLAB memory bits	0
10	Total block memory bits	526336
11		
12	Total DSP Blocks	0
13		
14	Total DLLs	1
15	Maximum fan-out node	CLOC...nput
16	Maximum fan-out	2414
17	Total fan-out	28855
18	Average fan-out	3.62

	Property	Value
1	From Node	soc_system:u0|soc_system_hps_0:hps_0|soc_..._0_hps_io_border:border|sdio_inst~FF_2218
2	To Node	HPS_SD_DATA[3]
3	Delay	24.633

i. FPGA resources utilized:

ALUTs – 3361

ALMs – 2242

I/O pins – 368

DLLs – 1

DSP Blocks – 0

Block Memory Bits – 526336

Maximum Delay – 24.633 ns

Maximum Frequency – 40.6 MHz

ii. Size of the Complied Program – 14.8 KB

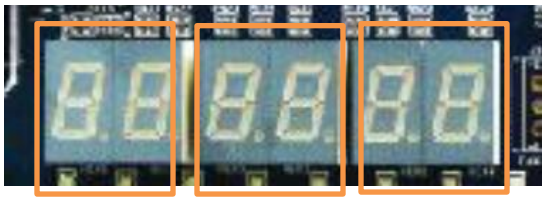
```
root@socfpga:/media/my_first_fpga# ls -al
drwxr-xr-x     3 root     root         16384 Jan  1  1970 .
drwxr-xr-x    12 root     root          4096 Sep 28 04:44 ..
drwxr-xr-x     1 root     root            56 Nov 14  2024 .dropbox.device
drwxr-xr-x     2 root     root         16384 Sep 12  2023 System Volume Information
drwxr-xr-x     1 root     root         14800 Nov 24  2024 my_first_hps-fpga
root@socfpga:/media/my_first_fpga# _
```

iii. YouTube Video: https://youtu.be/941a477GRRQ

Part II – Modifying the HPS+FPGA System

a) Modified the system so that the 7-segment displays on the board will display a running counter generated by the HPS which counts, seconds, minutes and hours. Every 1 second until 60 seconds and then wraps around incrementing the minutes, which in turn wrap around when 60 minutes is reached by incrementing the hours by one, which in turn wrap around when 24 is reached.

Marks
12
0



seconds minutes hours

Deliverables:

(i) Show that your system works by creating a small video (You do not need to wait for the hour to change).

(ii) Report the FPGA resources used, max frequency, etc.

(iii) Attach all of the project files in zipped file.

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	3153
2		
3	▼ Combinational ALUT usage for logic	4975
1	-- 7 input functions	38
2	-- 6 input functions	729
3	-- 5 input functions	795
4	-- 4 input functions	1390
5	-- <=3 input functions	2023
4		
5	Dedicated logic registers	4020
6		
7	I/O pins	368
8	I/O registers	186
9	Total MLAB memory bits	0
10	Total block memory bits	526336
11		
12	Total DSP Blocks	0
13		
14	Total DLLs	1
15	Maximum fan-out node	CLOC...nput
16	Maximum fan-out	3489
17	Total fan-out	39048
18	Average fan-out	3.67

	Property	Value
1	From Node	soc_system:u0|soc_system_hps_0:hps_0|soc_..._0_hps_io_border:border|sdio_inst~FF_2218
2	To Node	HPS_SD_DATA[3]
3	Delay	24.633

i. YouTube Video: https://youtu.be/33jeTdHJBRU

ii. FPGA resources utilized:

ALUTs – 4975

ALMs – 3153

I/O pins – 368

DLLs – 1

DSP Blocks – 0

Block Memory Bits – 526336

Maximum Delay – 24.633 ns

Maximum Frequency – 40.6 MHz

iii. Submitted a .zip folder (Homework9_part2) along with this document in eLearning.