

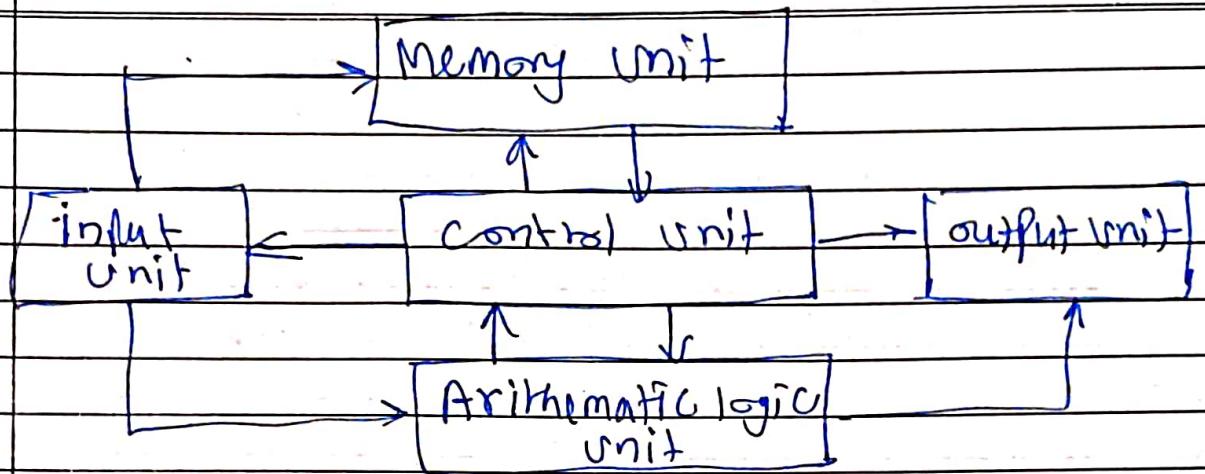
Arch.^f Computer organization UNIT I

Computer Evaluation

1 Von Neumann Architecture (First Generation)

The first electronic computer, ENIAC (Electronic Numerical Integrator and computer) was designed & constructed under the direction of Eckert & Mauchly at the Moore School of Engg. It was made up of more than 18000 vacuum tubes and 1500 relays. It was able to perform nearly 5000 additions or subtractions per second. The ENIAC was a decimal rather than a binary machine. Its data memory consisted of 20 accumulators. Each capable of storing 10 digit decimal numbers. Each digit was represented by a ring of 10 vacuum tubes and only one vacuum tube was on state to represent by a ring of 10 vacuum tube. Drawback is that it was wired in for specific computations. For modifications & replacements of programs manually setting of switches and plugging & unplugging of cables was necessary. It was time consuming process.

Von Neumann and originators of ENIAC designed the first stored program computer named EDVAC (Electronic Discrete Variable Computer). The stored program concepts in EDVAC facilitated the users to enter and alter various programs and do variety of computations. EDVAC project was further developed by Von Neumann with Institute of Advanced Studies (IAS).



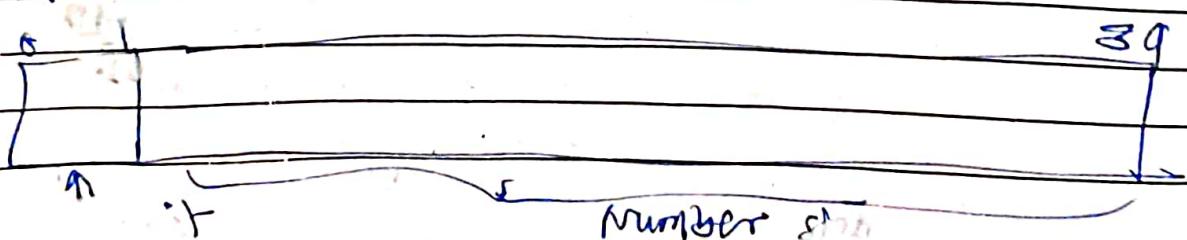
A Von Neumann Machine

Von Neumann machine general structure is shown in above fig. It consists of 5 basic units.

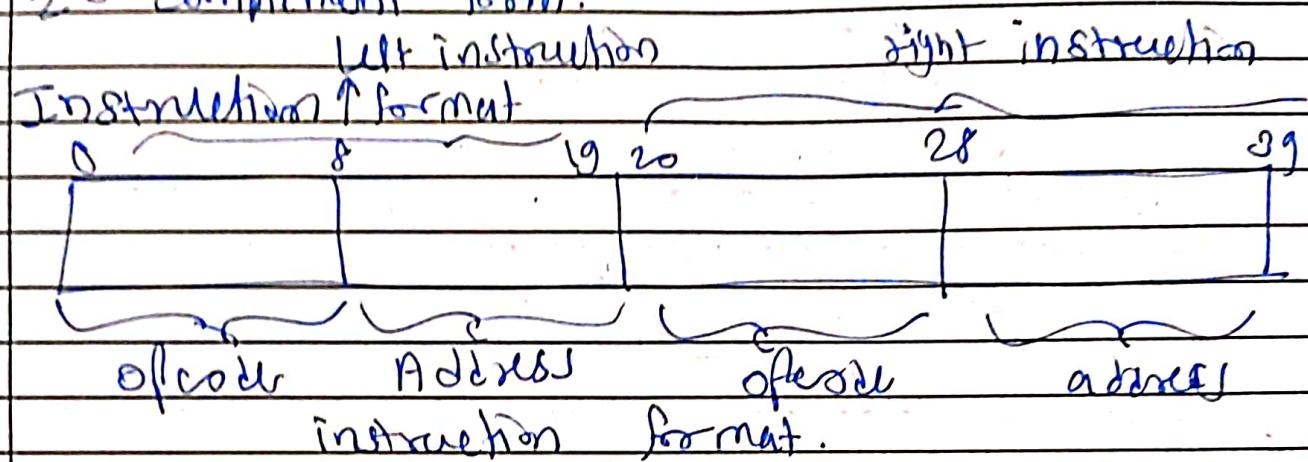
1. If unit transmits data & instructions from the outside world to machine. It is operated by control unit.
2. The memory unit stores both, data and instructions
3. The arithmetic logic unit performs arithmetic & logical operations.
4. The control unit fetches and interprets the instructions in memory and causes them to be executed.
5. The off unit transmit and interprets the instructions in memory & causes them to be executed.

The original IAS machine (Von Neumann machine) memory unit consists of 4096 storage locations of 40 bit each.

Data format



The left most bit represents the sign of the number 0 for +ve and 1 for -ve numbers, while the remaining 39 bits indicate the number's size in a 2's complement form.



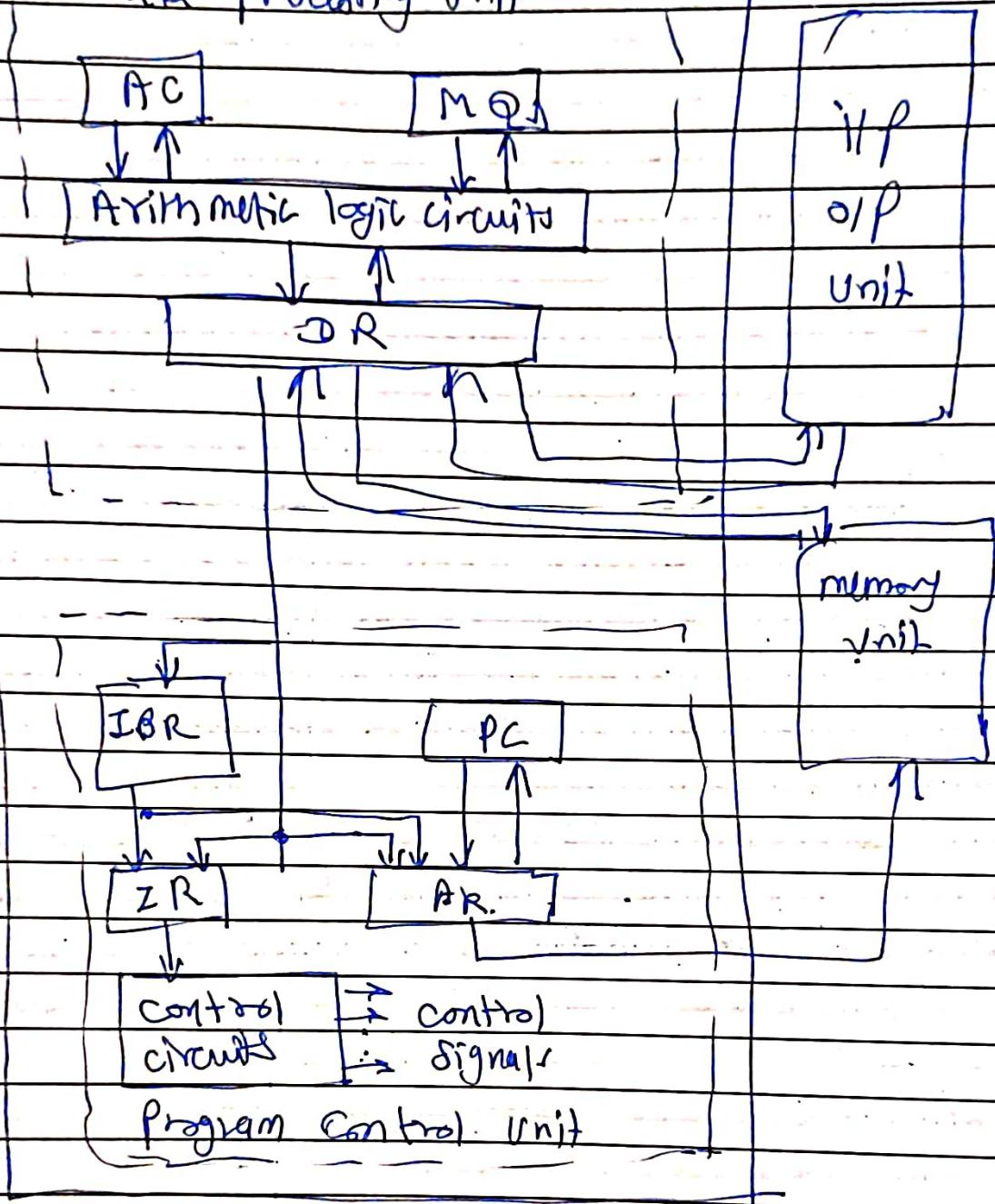
Each instruction is of 20 bits so that two instruction can be stored in each 40 bit memory location. instruction consist of 2 parts - 8 bit opcode i.e. operation code and 12 bit address. opcode defines the operation to be performed and address part identifies any of the 2^{12} memory locations that may be used to store an operand of the instruction.

institute of advanced studies

IAS / Von Neumann machine structure

Register	Abbreviation
Accumulator	AC
multiplier quotient	MQ
Data register	DR
Program counter	PC
instruction buffer Register	IBR
Address Register	AR
instruction Register	IR

Central Processing Unit Data Processing Unit



Structure of a first generation computer - IAS.

PC - Program Counter

If it is an address register. It is used to store the address of next instruction to be executed and hence also referred to as instruction address register.

IAS - Institute for advanced studies.

AR - Address Register

It is a 12 bit address register. It is used to specify the address in memory of the word to be written into or read from the DR.

DR - Data register.

It is a 40 bit register. It is used to store any 40 bit word. A word transfer can take place between the 40 bit data register DR of the CPU and any memory location. The DR may be used to store an operand during the execution of an instruction.

AC (Accumulator) & MQ (multiplier-quotient)

There are 2 40 bit registers used for the temporary storage of operands & result.

IR (instruction register) & IBR (instruction buffer register)

Program control unit fetches two instructions simultaneously from memory. The opcode of the first instruction is placed in the instruction register (IR) and the instruction that is not to be executed immediately, is placed in the instruction buffer register, (IBR).

Instructions of IAS computer - 5 groups

1 Data transfer

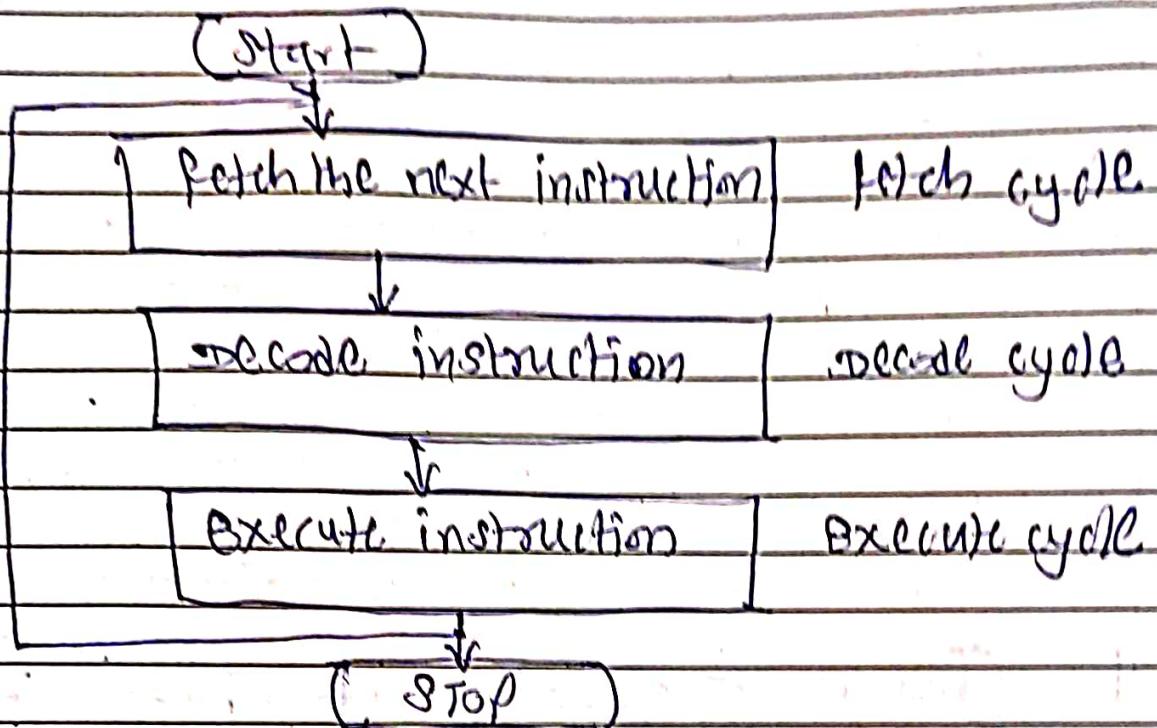
2 Unconditional branch

3 Conditional branch

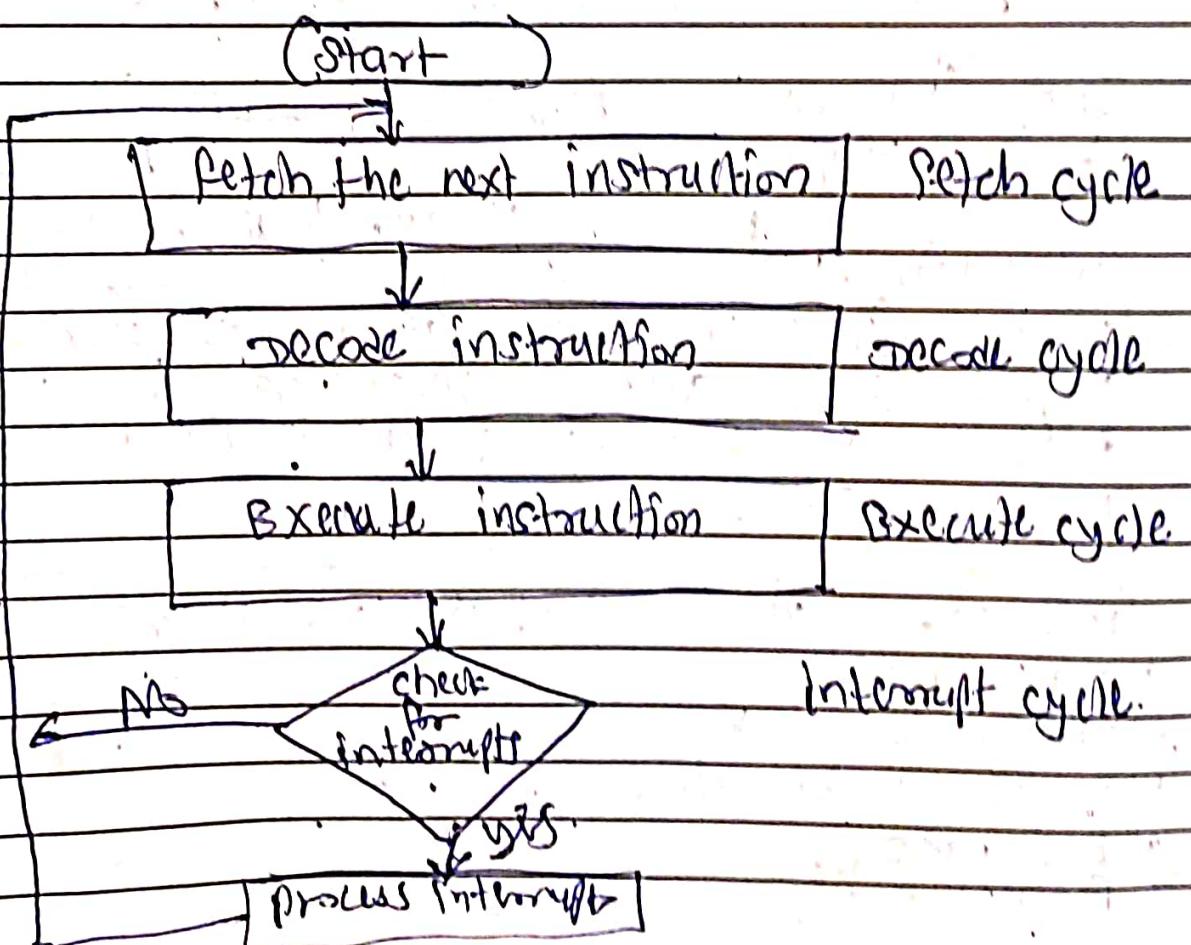
4 Arithmetic

5 Address modify

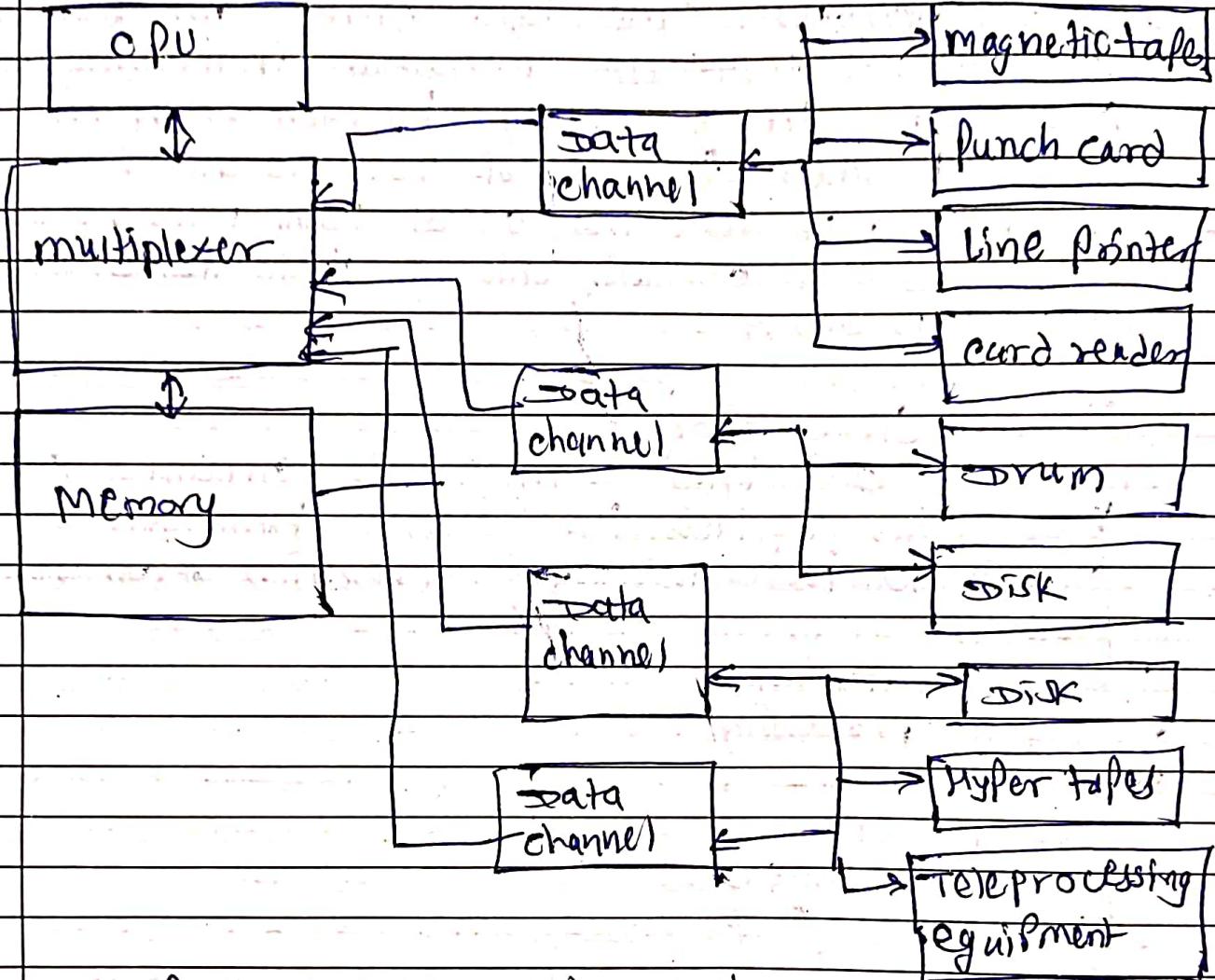
instruction cycles



Basic
instruction
cycle
with
interrupt.



2nd generation - IBM 7094 System



The first major change in the electronic computer came with the replacement of the vacuum tube by transistor. CPU can handle floating point and fixed point operations.

In 2nd generation magnetic core memory and magnetic drum storage devices were more widely used. The higher level languages such as Fortran were developed making the preparation of application programs much easier. System programs like compilers were developed to translate these high level

language programs into assembly language program.

In IBM 7094 configuration, uses of data channels. The data channel can perform sequence of instruction execution independently relieving the processing burden of the CPU.

Another feature of 7094 is use of multiplexer, it schedules access to the memory from the CPU & data channels, allowing these devices to act independently.

Third Generation

In 1960's integrated circuit (IC) began to replace the discrete transistor circuits to introduce 3rd generation of computers. It uses

- 1. multi programming
- 2. parallel processing
- 3. pipelining
- 4. multiplexing
- 5. sharing resources

Ex. IBM 360/370

Features of IBM 360/370

- 1. It uses 32 bit or 4 byte word format
- 2. It has 16 general registers & 4 double length floating point registers.
- 3. Provide extensive instruction set
- 4. Support data transfer instructions for register to register, register to memory, memory to register or memory to memory.
- 5. Memory is faster & can be extended up to 1 million words for same model.

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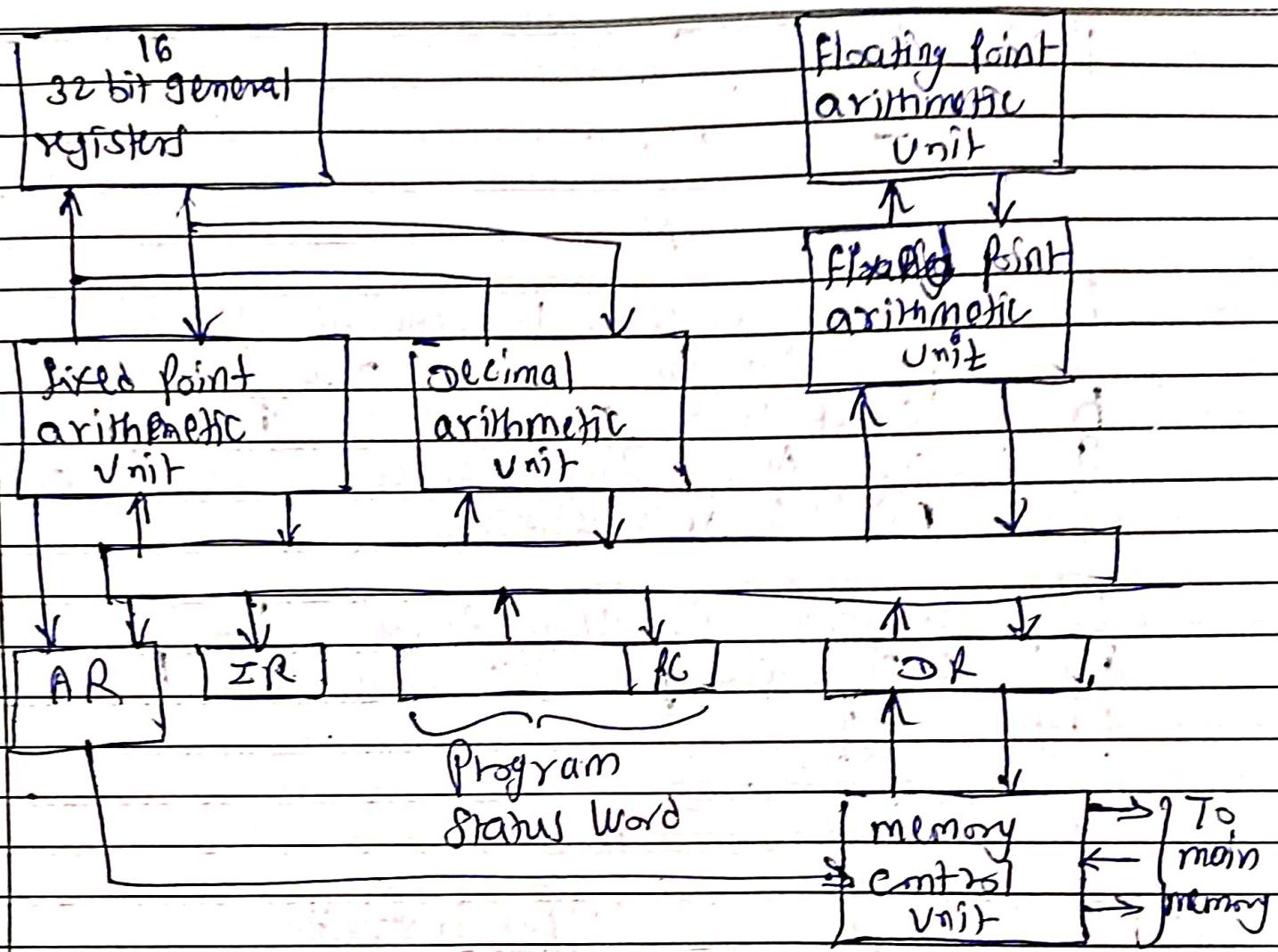
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Eg. IBM 360/370

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CPU structure of 3360-370 Series Computers.

4th generation

It is based on advanced integrated circuit technology. LSI + VLSI technology.

In 4th generation computer concurrency, pipelining, caches & virtual memory are used to produce the high performance computing system. 4th generation products are portable notebook computers, desktop computers, workstations, interconnected by local area net, WAN, & Internet.

Basic

Performance Equation

$$T = \frac{N \times S}{R} \Rightarrow \frac{10 \times 5}{3} = \frac{50}{3} = 18.8 \text{ ms}$$

N - No. of actual instructions executed by processor for execution of a program.

R - clock rate measured in cycles per second.

S - avg. No. of steps needed to execute one machine instruction.

When machine instruction execution time is measured in terms of cycles per instruction (CPI) the program execution time is

$$T = \frac{N \times CPI \times T}{R}$$

Performance parameters $P = \text{No. of processor cycle per instruction}$

$M = \text{No. of memory reference}$

$K = \text{ratio between memory cycle \& processor cycle}$

$N = \text{Machine instruction count}$.

$R = \text{clock rate}$

System attributes

- 1 instruction set architecture
- 2 compiler technology
- 3 processor implementation of control
- 4 cache \& memory hierarchy.

processor Speed

1. Branch prediction —

The processor predicts which group of instructions are likely to be processed next. If the processor guesses correct most of the times, it can prefetch those instructions and buffer them. Branch prediction increases the amount of work available for the processor to execute.

2. Data flow analysis —

Processor checks the dependency of instructions on each other. It can schedule instructions when they are ready for execution, independent of original program order. The instruction is said to be ready for execution when it is not dependent on the result of other instruction.

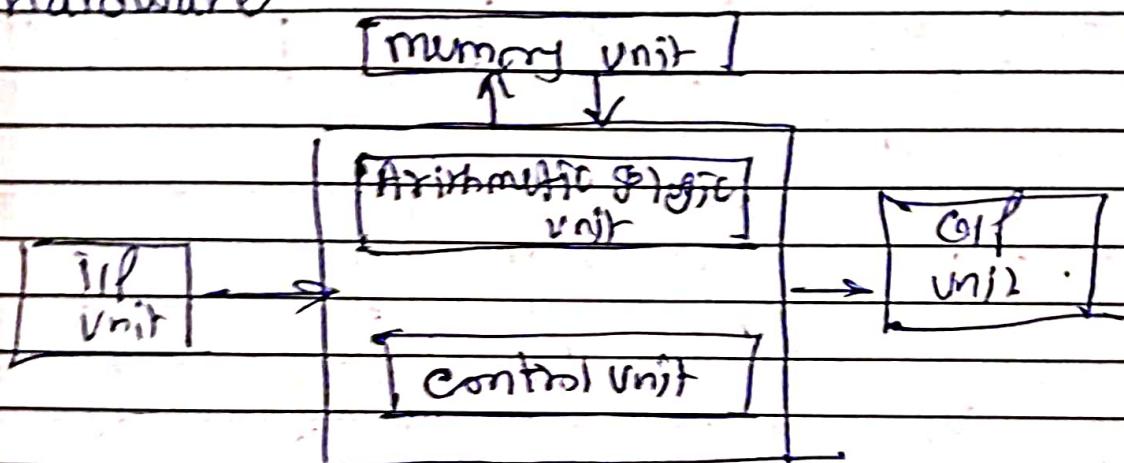
3. Speculative execution —

Using branch prediction and data flow analysis, some processors speculatively execute instructions ahead of their actual appearance in the program execution. This allows processor to keep its execution units busy and prevents unnecessary delay.

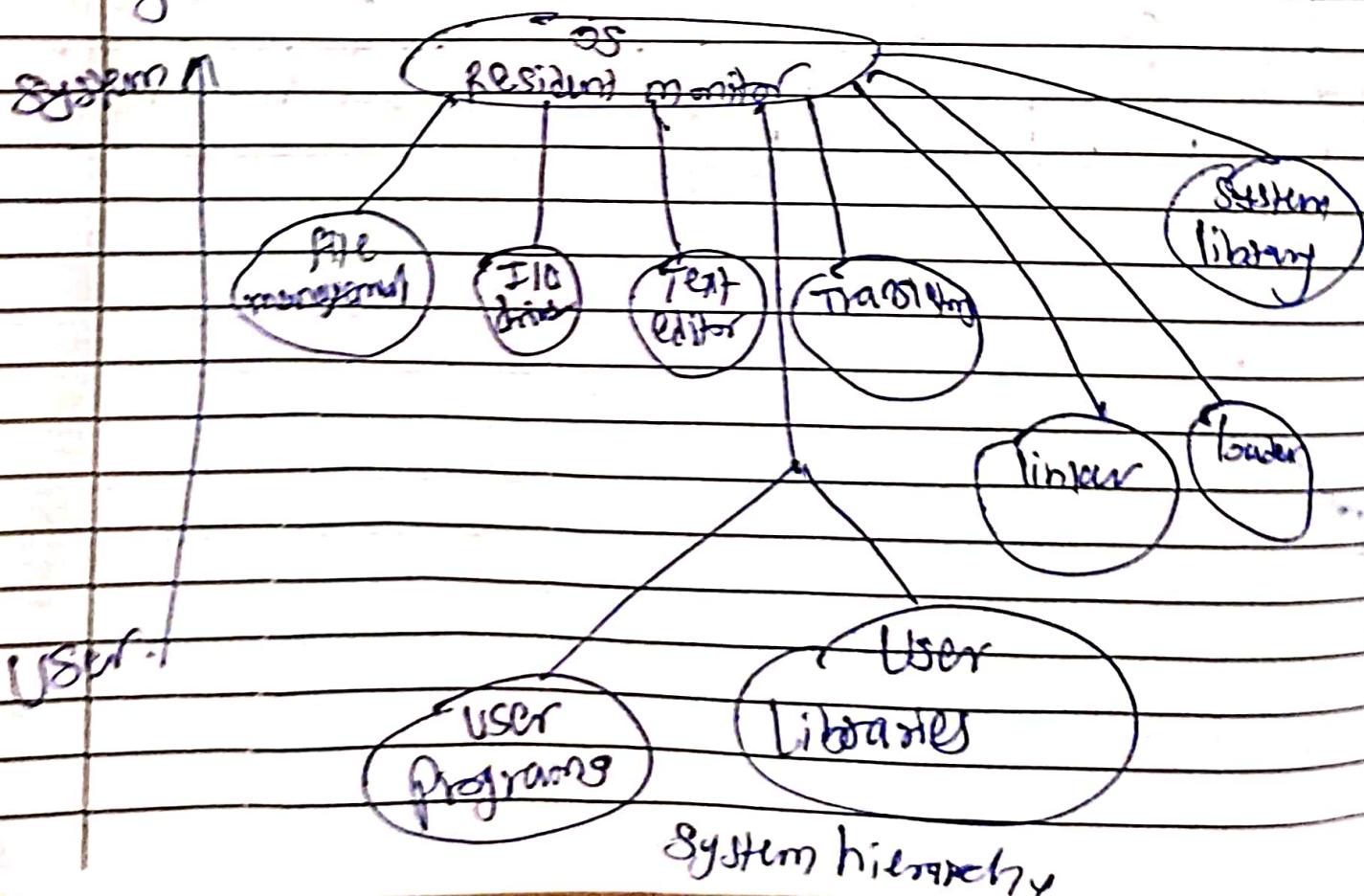
Computer components - 4

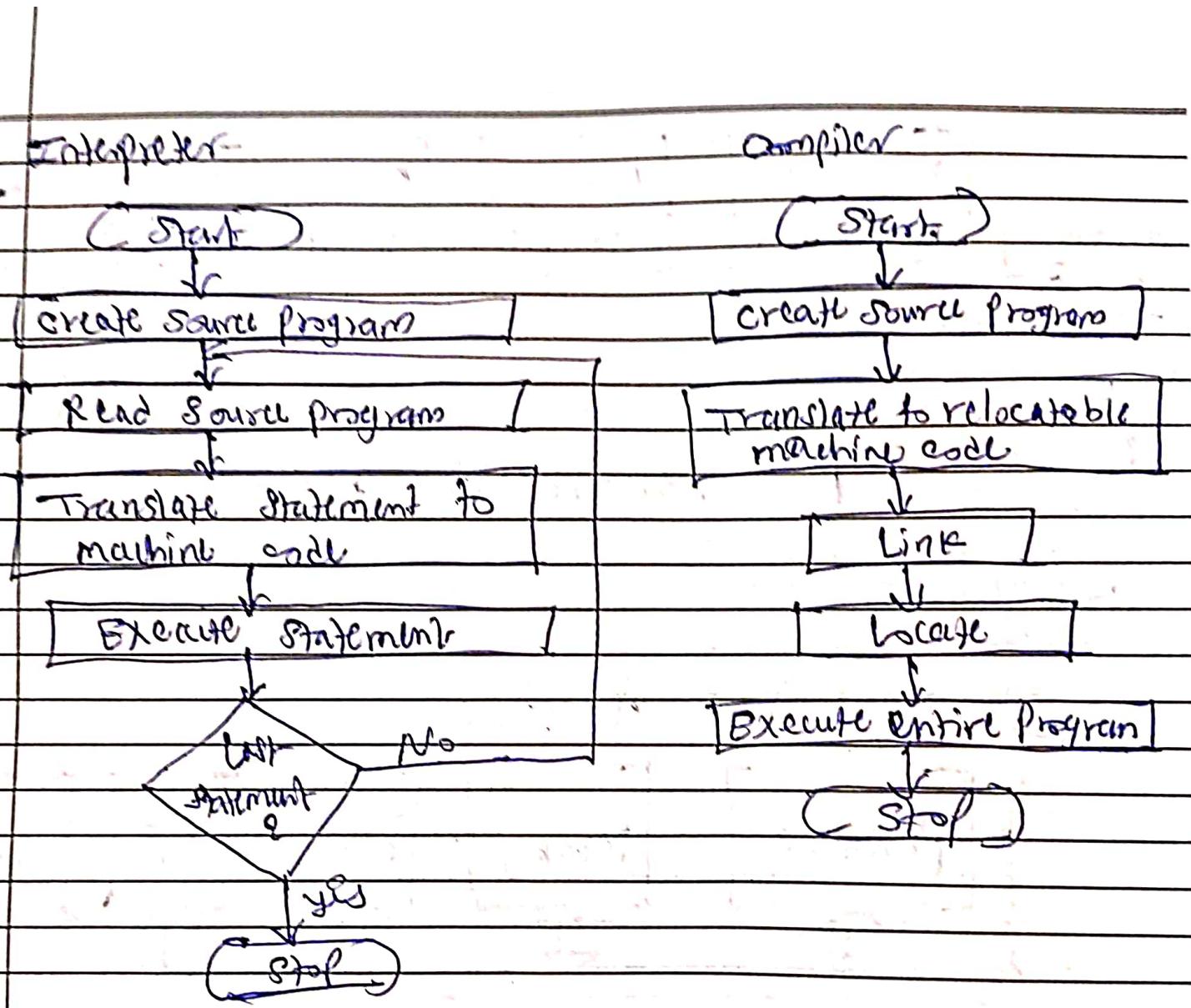
- 1 Hardware
- 2 Software
- 3 Data
- 4 Users

I Hardware



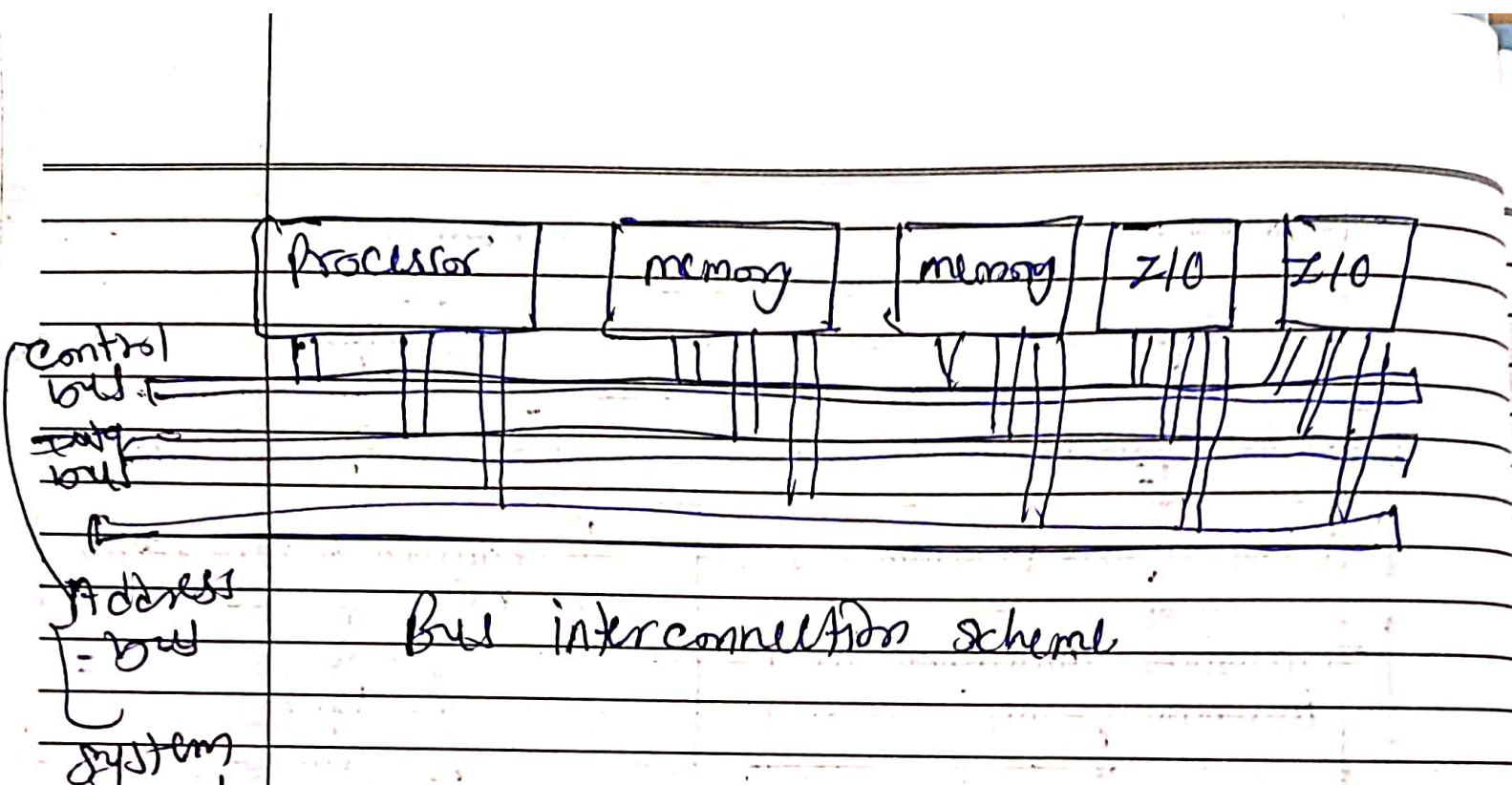
II System SW





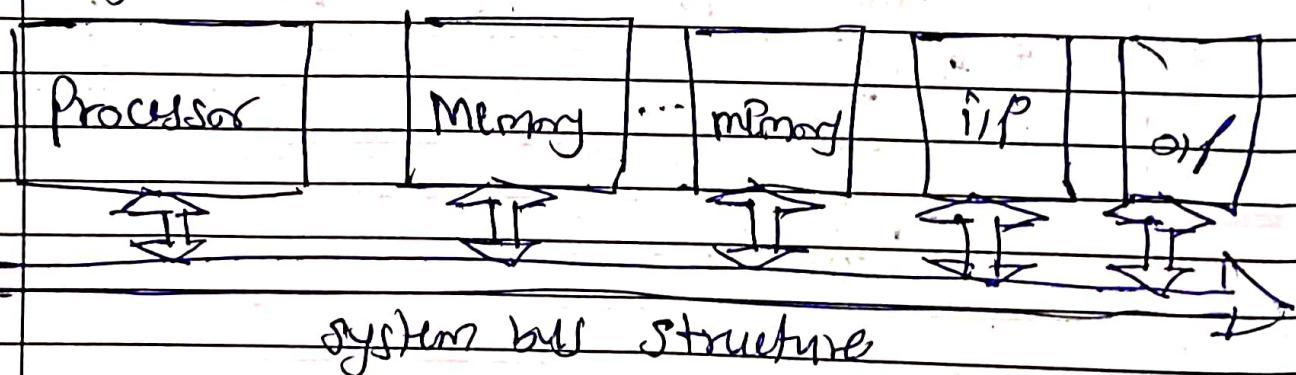
Bus interconnection

- 1 Data bus
- 2 Address bus
- 3 Control buses



Bus interconnection scheme

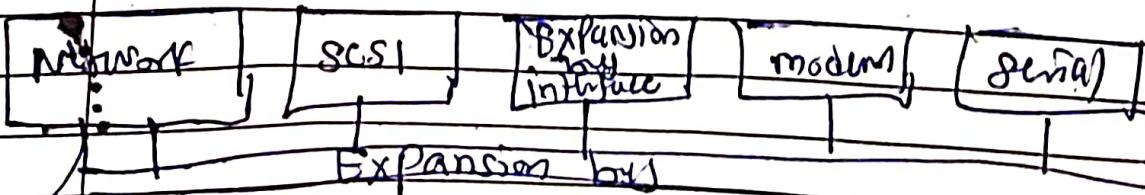
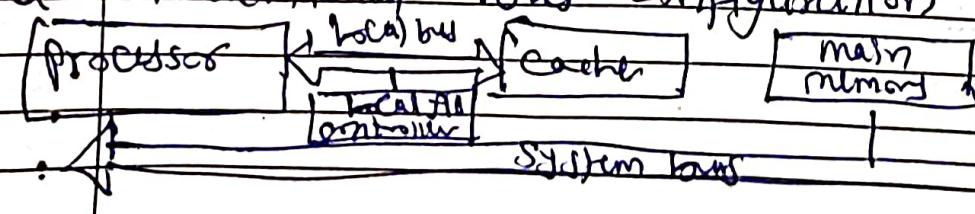
I Single bus structure



system bus structure

II multiple bus structure

a Traditional bus configuration

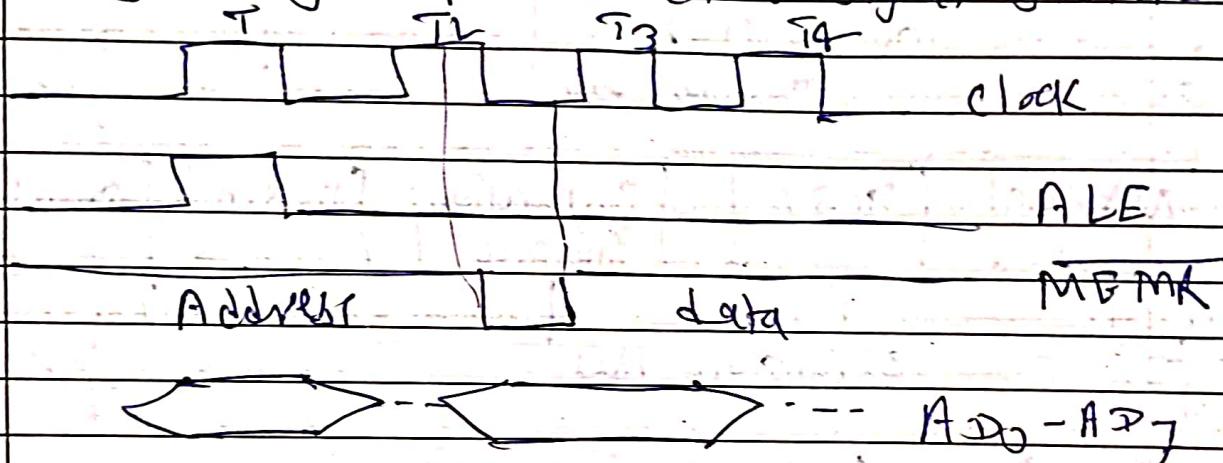


Traditional bus configuration

Bus - It is communication pathway connecting two or more devices.

I Synchronous bus

- ① All devices driving timing information from a common clock line.
- ② Timing depends on clock signal & state.

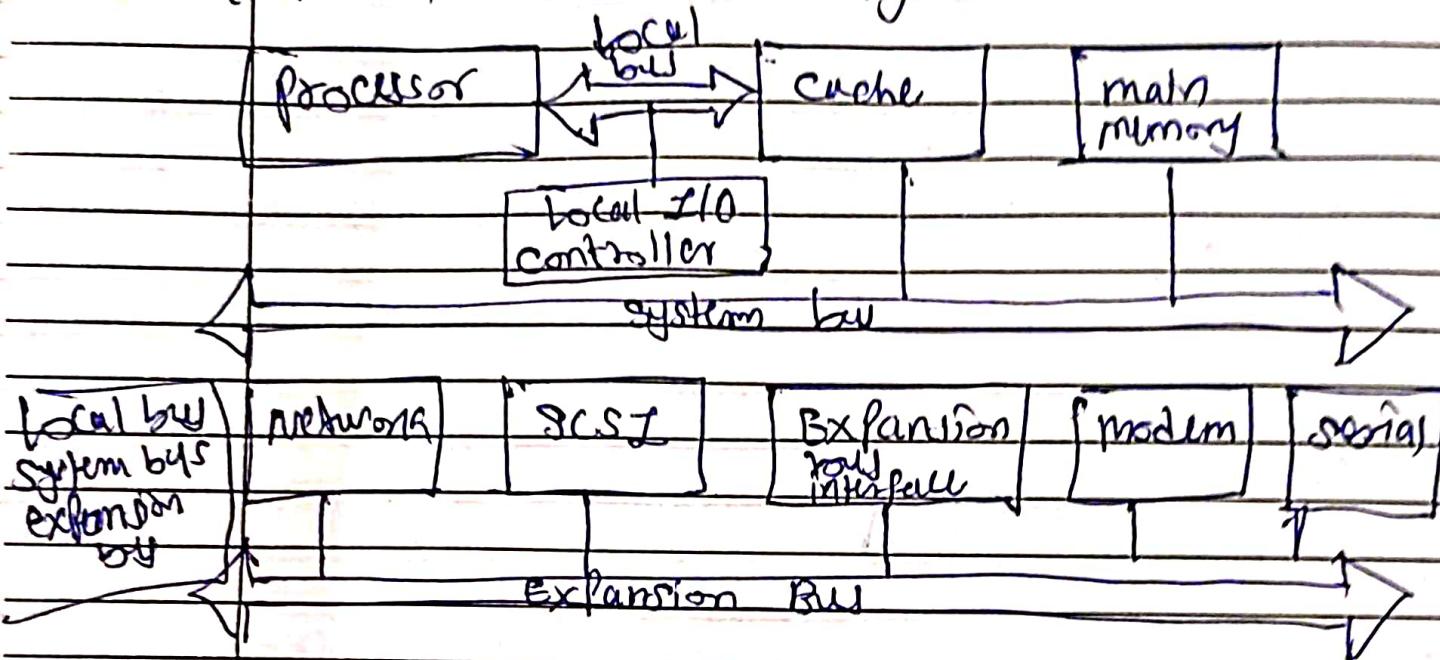


II Asynchronous bus

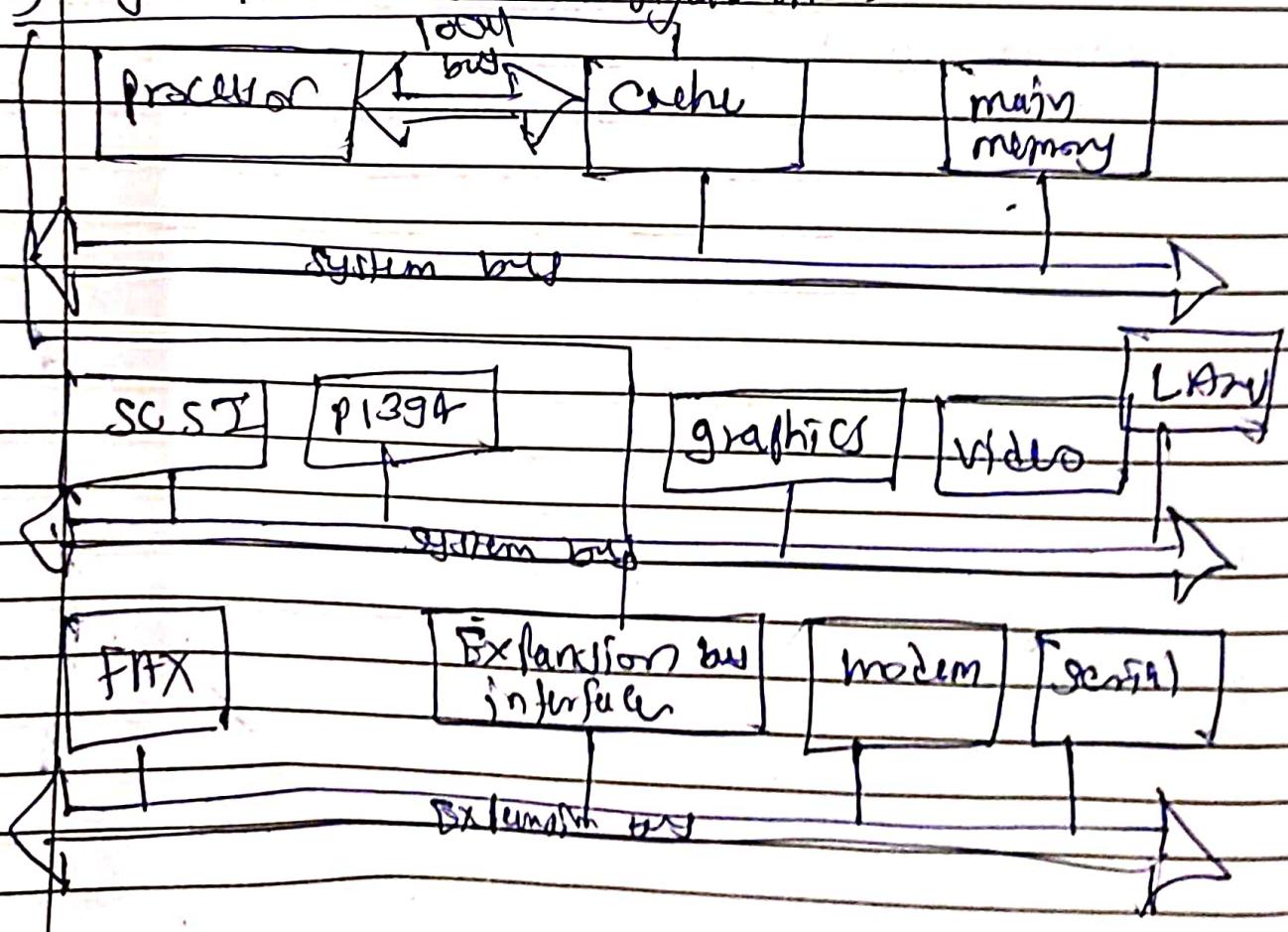
- ① use handshaking signals between processor & device
- ② No common clock

multiple bus structure

a) Traditional bus configuration



b) High speed bus configuration



Explain the bus design parameters or how to implement buses in computer system?

- 1 Types of bus - Dedicated or multiplexed.
- 2 Method of Arbitration - Centralized or distributed.
- 3 Timing - Synchronous or asynchronous
- 4 Bus width - Address or data
- 5 Data transfer type - Read write, read modify write
read after write or block.