Practical 4

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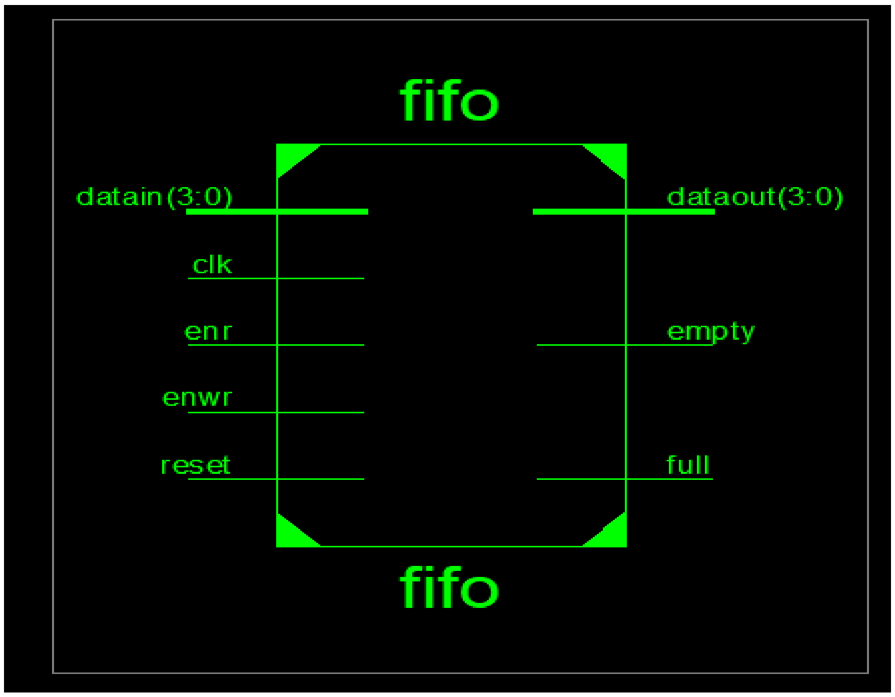
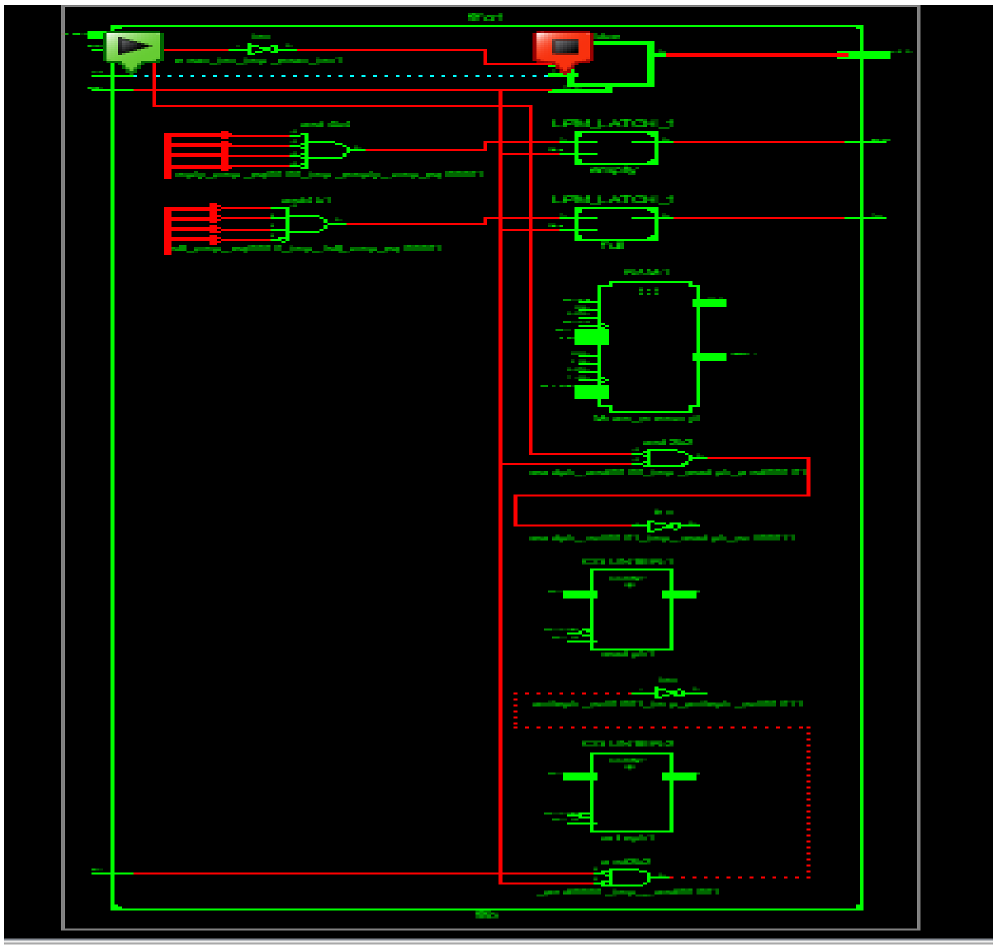
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_arith.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
entity fifo is
    Port ( enr,enwr,clk,reset : in   STD_LOGIC;
           datain : in   STD_LOGIC_VECTOR (3 downto 0);
           dataout : out   STD_LOGIC_VECTOR (3 downto 0);
           full,empty : out   STD_LOGIC);
end fifo;

architecture Behavioral of fifo is
type memory_type is array (0 to 7)of STD_LOGIC_VECTOR (3 downto 0);
signal memory: memory_type;
signal readptr,writeptr:STD_LOGIC_VECTOR (3 downto 0):="0000";
begin
process(clk,reset)
```

```
begin
if (reset='1') then dataout<="0000";
else
if (clk'event and clk='1' and enr<='0' and enwr<='1') then
memory(conv_integer(writeptr))<=datain;
writeptr<=writeptr+'1';
end if;
if (clk'event and clk='1' and enr<='1' and enwr<='0') then
dataout<=memory(conv_integer(readptr));
readptr<=readptr+'1';
end if;
if readptr="0000" then
empty<='1';
else empty<='0';
end if;
if writeptr="0111" then
full<='1';
else full<='0';
end if;
end if;
end process;
end Behavioral;
```


fifo
datain(3:0)
clk
enr
enwr
reset
dataout(3:0)
empty
full
fifo

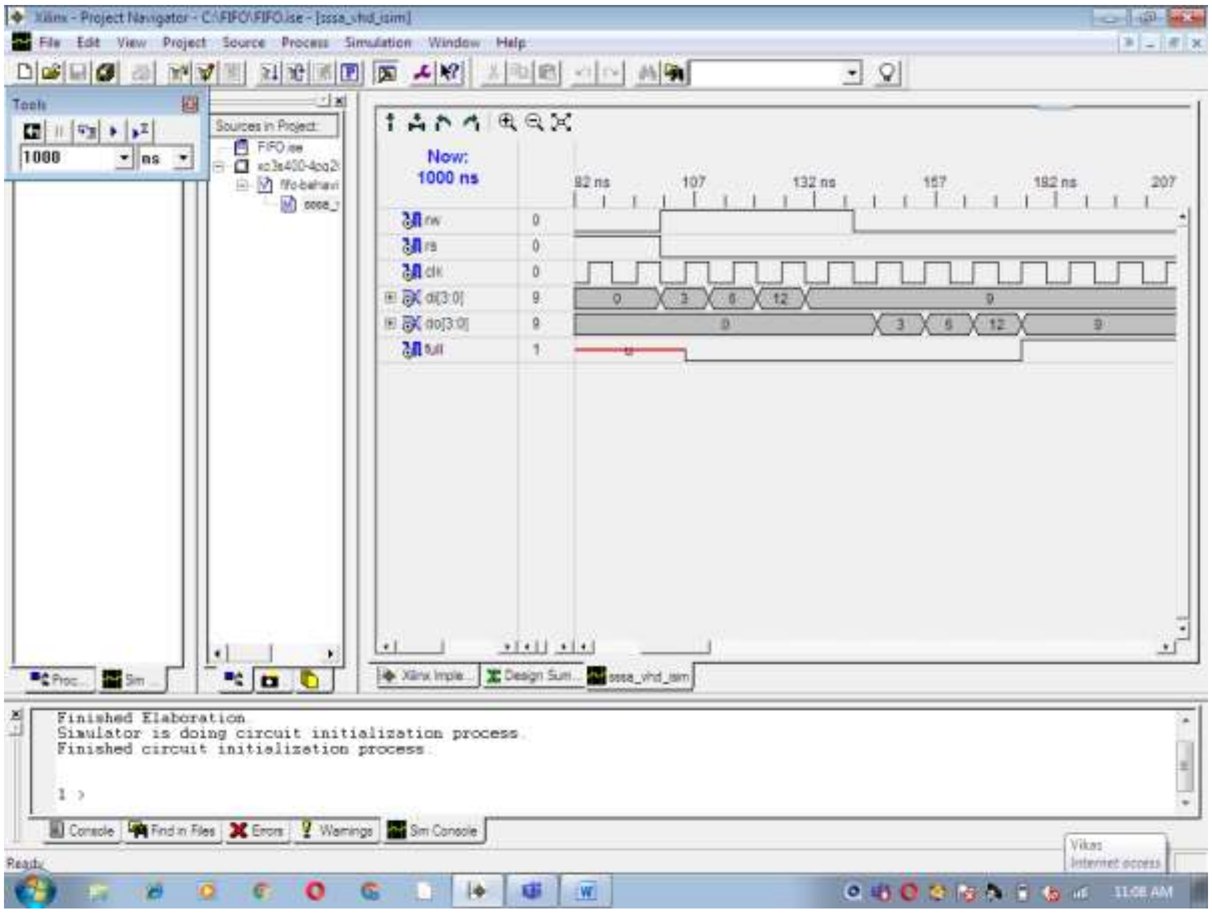

LPM_LATCH_1
LPM_LATCH_1
RAM_1
COUNTER_1
COUNTER_2

testbench

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;


ENTITY sss IS
END sss;


ARCHITECTURE behavior OF sss IS


    -- Component Declaration for the Unit Under Test (UUT)


    COMPONENT fifo
    PORT(
         enr : IN   std_logic;
         enwr : IN   std_logic;
         clk : IN   std_logic;
         reset : IN   std_logic;
         datain : IN   std_logic_vector(3 downto 0);
         dataout : OUT   std_logic_vector(3 downto 0);
         full : OUT   std_logic;
         empty : OUT   std_logic
        );
    END COMPONENT
   --Inputs
```

```
    signal enr : std_logic := '0';
    signal enwr : std_logic := '0';
    signal clk : std_logic := '0';
    signal reset : std_logic := '0';
    signal datain : std_logic_vector(3 downto 0) := (others => '0');

        --Outputs
    signal dataout : std_logic_vector(3 downto 0);
    signal full : std_logic;
    signal empty : std_logic;

    -- Clock period definitions
    constant clk_period : time := 10 ns;
BEGIN
        -- Instantiate the Unit Under Test (UUT)
    uut: fifo PORT MAP (
            enr => enr,
            enwr => enwr,
            clk => clk,
            reset => reset,
            datain => datain,
            dataout => dataout,
            full => full,
            empty => empty
         );
    -- Clock process definitions
    clk_process :process
    begin
               clk <= '0';
               wait for clk_period/2;
               clk <= '1';
               wait for clk_period/2;
    end process;
    -- Stimulus process
    stim_proc: process
    begin
enwr<='1'; enr<='0';
datain<="0001"     ;
        -- hold reset state for 100 ns.
        wait for 10 ns;
datain<="0010";
        -- hold reset state for 100 ns.
        wait for 10 ns;
datain<="0100"     ;
        -- hold reset state for 100 ns.
        wait for 10 ns;
```

```
                datain<="1000";
        -- hold reset state for 100 ns.
        wait for 10 ns;
                datain<="0011"    ;
        -- hold reset state for 100 ns.
        wait for 10 ns;
datain<="0111";
        -- hold reset state for 100 ns.
        wait for 10 ns;
                datain<="1111";
        -- hold reset state for 100 ns.
        wait for 10 ns;
                datain<="1001";
        -- hold reset state for 100 ns.
        wait for 10 ns;
enwr<='0'; enr<='1';
 wait for 80 ns;
        wait for clk_period*10;
        -- insert stimulus here
        wait;
    end process;
END
```



```
Finished Elaboration
Simulator is doing circuit initialization process.
Finished circuit initialization process.

1 >
```

CLOCK DIVISION

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_arith.ALL;

use IEEE.STD_LOGIC_unsigned.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;


-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fifo is
    Port ( enr,enwr,clk,reset : in   STD_LOGIC;
           datain : in   STD_LOGIC_VECTOR (3 downto 0);
           dataout : out   STD_LOGIC_VECTOR (3 downto 0);
           full,empty : out   STD_LOGIC);
end fifo;

architecture Behavioral of fifo is
type memory_type is array (0 to 7)of STD_LOGIC_VECTOR (3 downto 0);
signal memory: memory_type;
signal clk1: std_logic;
signal count : std_logic_vector(20 downto 0);
signal readptr,writeptr:STD_LOGIC_VECTOR (3 downto 0):="0000";
begin
process(clk)
begin
if(clk'event and clk='1') then
count<=count+1;
end if;
```

```
clk1<=count(20);
end process;
process(clk1)
begin
--if (reset='1') then dataout<="0000";
--else
if (clk1'event and clk1='1' and enr<='0' and enwr<='1') then
memory(conv_integer(writeptr))<=datain;
writeptr<=writeptr+'1';
end if;

if (clk1'event and clk1='1' and enr<='1' and enwr<='0') then
dataout<=memory(conv_integer(readptr));
readptr<=readptr+'1';
end if;

if readptr="0000" then
empty<='1';
else empty<='0';
end if;

if writeptr="0111" then
full<='1';
```

```
else full<='0';

end if;

--end if;

end process;


end Behavioral;
```

UCF FILE

```
net clk loc=p183;

net reset loc=p102;

net enr loc=p101;

net enwr loc=p87;

net datain(0) loc=p80;

net datain(1) loc=p78;

net datain(2) loc=p77;

net datain(3) loc=p74;

net dataout(0) loc=p168;

net dataout(1) loc=p171;

net dataout(2) loc=p172;

net dataout(3) loc=p175;

net full loc=p154;

net empty loc=p161;
```