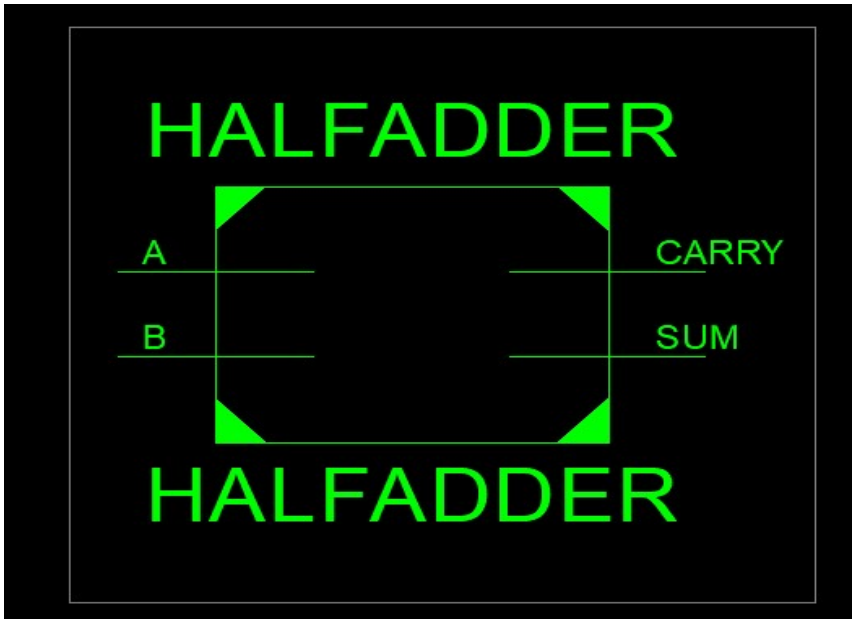
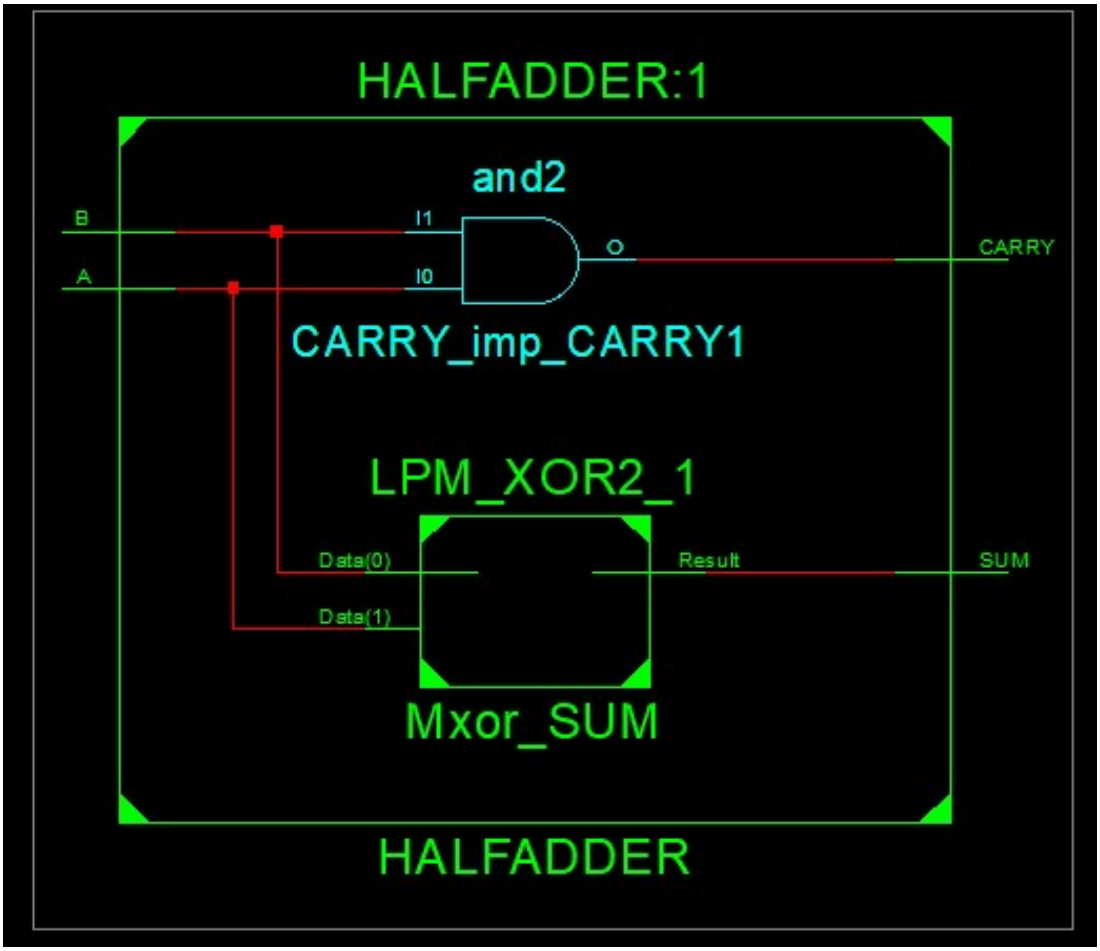
Practical No -: 10

HALF ADDER -:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity HALFADDER is
        Port ( A : in STD_LOGIC;
                    B : in STD_LOGIC;
                    SUM : out STD_LOGIC;
                    CARRY : out STD_LOGIC);
end HALFADDER;
architecture Behavioral of HALFADDER is
begin
SUM<=A XOR B;
CARRY<= A AND B;
end Behavioral;
```



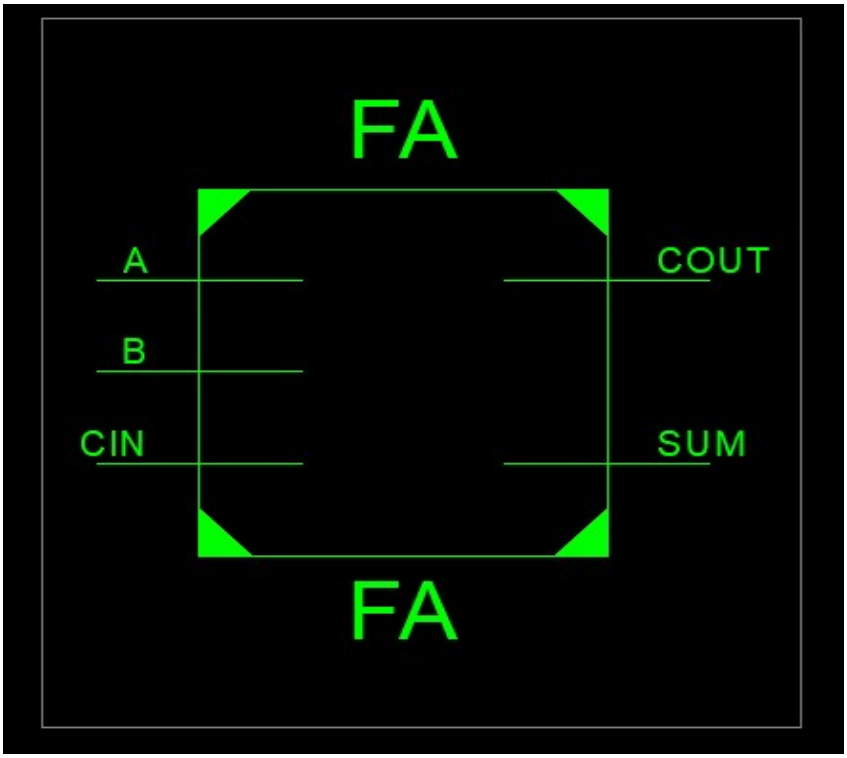


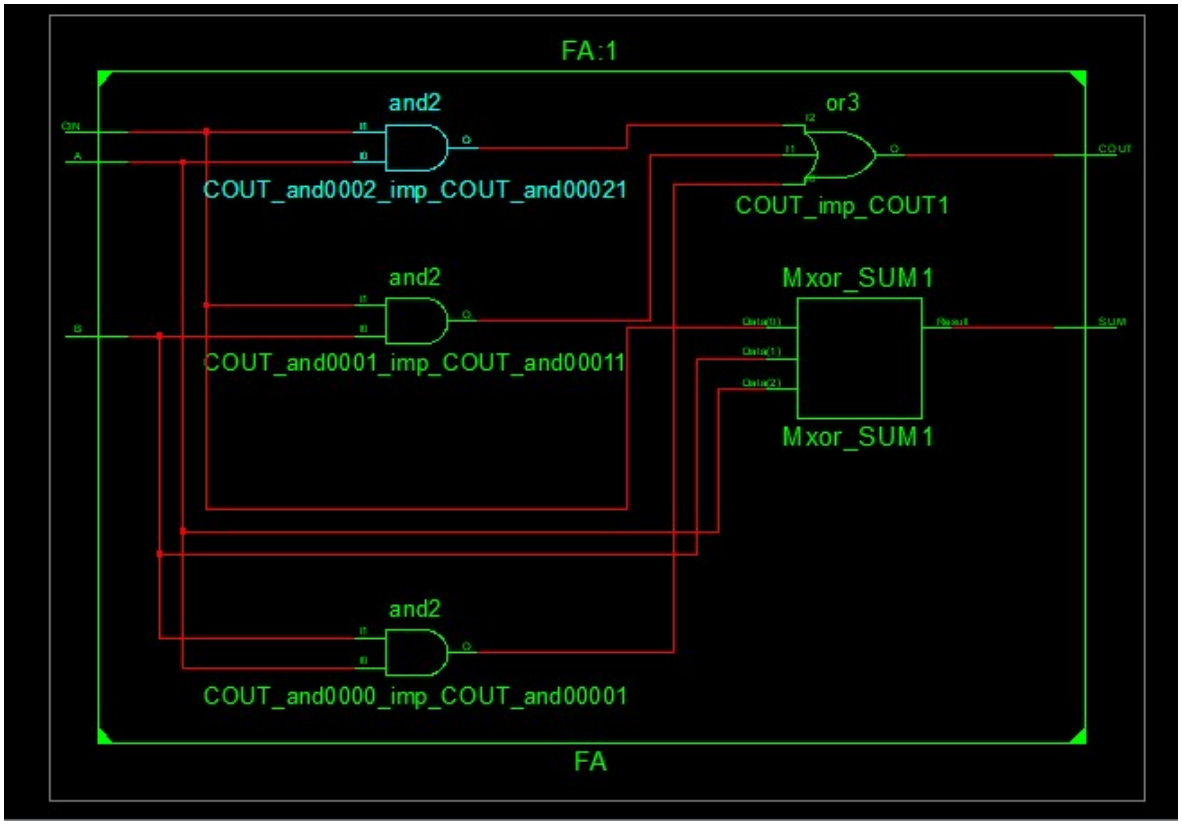
FULL ADDER -:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity FULLADDER is
        Port ( A : in     STD_LOGIC;
                    B : in     STD_LOGIC;
                    CIN : in     STD_LOGIC;
                    SUM : out     STD_LOGIC;
                    COUT : out     STD_LOGIC);
end FULLADDER;
```

```
architecture Behavioral of FULLADDER is
begin
component HALFADDER
port( A : in     STD_LOGIC;
                 B : in     STD_LOGIC;
                 SUM : out     STD_LOGIC;
                 CARRY : out     STD_LOGIC);
end component;
signal S1,C1,C2:STD_LOGIC;
begin
ha1:HALFADDER port map (A,B,S1,C1);
ha2:HALFADDER port map (S1,CIN,SUM,C2);
COUT<=C1 OR C2;
end Behavioral;
```





TESTBENCH -:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY FAA IS
END FAA;

ARCHITECTURE behavior OF FAA IS
    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT FA
    PORT(
        A : IN     std_logic;
        B : IN     std_logic;
        CIN : IN     std_logic;
```

```
            SUM : OUT      std_logic;
            COUT : OUT     std_logic
          );
    END COMPONENT;

    --Inputs
    signal A : std_logic := '0';
    signal B : std_logic := '0';
    signal CIN : std_logic := '0';
      --Outputs
    signal SUM : std_logic;
    signal COUT : std_logic;
BEGIN
      -- Instantiate the Unit Under Test (UUT)
    uut: FA PORT MAP (
            A => A,
            B => B,
            CIN => CIN,
            SUM => SUM,
            COUT => COUT );
    -- Stimulus process
    stim_proc: process
    begin
       -- hold reset state for 100 ns.
A<='0'; B<='0'; CIN<='0';
wait for 100 ns;
A<='0'; B<='0'; CIN<='1';
```

```
wait for 100 ns;
A<='0'; B<='1'; CIN<='0';
wait for 100 ns;
A<='0'; B<='1'; CIN<='1';
wait for 100 ns;
A<='1'; B<='0'; CIN<='0';
wait for 100 ns;
A<='1'; B<='0'; CIN<='1';
wait for 100 ns;
A<='1'; B<='1'; CIN<='0';
wait for 100 ns;
A<='1'; B<='1'; CIN<='1';
wait for 100 ns;
wait;
end process;
```