

# Design and realization of low dropout voltage regulators in PMIC for portable applications

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**Design and Realization of Low DropOut Voltage Regulators in  
PMIC for Portable Applications**

**LI KAN**

**School of Electrical and Electronic engineering**

A thesis submitted to the Nanyang Technological University  
in partial fulfilment of the requirement for the degree of  
Doctor of Philosophy

**2020**

## **Statement of Originality**

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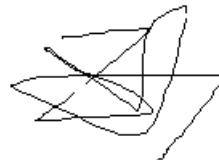
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## **Supervisor Declaration Statement**

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## **Authorship Attribution Statement**

This thesis contains material from 2 papers published in the following peer-reviewed journals / from 1 paper accepted at conferences in which I am listed as the first author.

Chapter 3 is published as "A transient-enhanced low dropout regulator with rail-to-rail dynamic impedance attenuation buffer suitable for commercial design." *Microelectronics Journal*, 63 (2017): 27-34.

The contributions of the co-authors are as follows:

- A/Prof Zheng Yuanjin provided the initial project direction and edited the manuscript drafts.
- I wrote the drafts of the manuscript. The manuscript was revised together with A/Prof Siek Liter.
- I performed all the silicon design, verification, data collection, and conducted data evaluation.

Chapter 4 is published as "A 600-mA, Fast-Transient Low-Dropout Regulator With Pseudo-ESR Technique in 0.18- $\mu$ m CMOS Process," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, pp. 1–11, 2019, doi: 10.1109/TVLSI.2019.2947534.

The contributions of the co-authors are as follows:

- I prepared the manuscript drafts. The manuscript was revised by A/Prof Zheng Yuanjin and Prof Jin Xiangliang
- I performed all the silicon design, verification, data collection, and conducted data evaluation.
- Mr. Xiaoxiao conducted the circuit simulations and layout for silicon experiment.

Chapter 5 is published as "A Multi-Loop Slew-Rate-Enhanced NMOS LDO Handling 1-A-Load-Current Step With Fast Transient for 5G Applications," in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2020.3005789.

It is also published as "A multi-loop slew-rate enhanced NMOS LDO handling 1A load current step with fast transient" IEEE, International Symposium on Circuits and Systems (ISCAS), Seville, Spain, May 17-20 2020.

The contributions of the co-authors are as follows:

- I prepared the manuscript drafts. The manuscript was revised by A/Prof Zheng Yuanjin
- I performed all the circuit design, verification, data collection, and conducted data evaluation.
- Mr. Yang ChuanShi and Dr. Guo Ting conducted the circuit simulations and layout for silicon experiment.



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## **Abstract**

Power Management Integrated Circuit (PMIC) is becoming increasingly important in modern mobile applications because high-quality power supply is increasingly demanded by mobile electronics such as System-on-Chips (SoCs), Mobile Station Modem (MSM), camera image sensor, etc. Low DropOut linear regulators (LDOs) is one of the most critical modules in PMIC that ascertain the quality of the power supply of the said mobile electronic. Note that PMIC first steps down the battery voltage to a lower regulated voltage by high efficiency but noisy switching regulators. Thereafter, LDO follows the switching regulators to filter out the switching component of the output of the switching regulator to generate a low-noise, high quality supply voltage.

Amongst all the design metrics of LDO, a fast load transient response with small overshoot/undershoot is arguably the most important yet challenging specification for LDO to achieve. This is mainly due to two reasons. Firstly, modern mobile SoC is becoming more and more complex with higher computational capability. This leads to a large current consumption and fast switching activity, which demands LDO to handle large load step/attack (e.g.,  $1A/1\mu s$ ). Secondly, mobile electronics are exploiting the advanced semiconductor fabrication process where the supply voltage is small and less tolerable to supply spike/noise.

This Ph.D work pertains to the investigation and study of various design techniques for high performance LDO achieving superior load transient response that is suitable for modern mobile application. Specifically, three fast transient LDO designs embodying three novel design techniques are developed and

proposed:

1. The first proposed LDO achieves fast transient response by using a high swing dynamic biasing impedance-attenuation buffer. The impedance-attenuation buffer helps the loop stability and improves the transient response. The buffer's feature of rail-to-rail swing makes the LDO's power FET size smaller than traditional buffer design for the same current deliverability. This thesis also analyzes its design robustness in terms of stability and offset. A low-cost trim method is also introduced to achieve a high yield for potential production. This LDO with high swing dynamic biasing impedance-attenuation buffer has been fabricated in 0.18- $\mu$ m HV CMOS process. The silicon size of the LDO is 137000  $\mu$ m<sup>2</sup>. The LDO's quiescent current is 15 $\mu$ A and can deliver up to 600mA loading current. The maximum transient output voltage variation is 1.5% with a load step of 500mA/100ns.
2. The second proposed LDO is a dual-loop compensated, fast-transient LDO. It is successfully implemented in a 0.18- $\mu$ m CMOS process with a total silicon area of 210  $\mu$ m  $\times$  593  $\mu$ m. The proposed LDO is composed of two feedback loops. The fast feedback loop (FFL) employs direct output voltage spike detection through the capacitive coupling, resulting in significantly improved, large-signal transient response and loop bandwidth at the same time. Its voltage spike is 15 mV for a load step of 600 mA. The proposed LDO has a loop bandwidth of 2.3 MHz at a load current of 600 mA with a 30  $\mu$ A quiescent current. A power transistor with the pseudo-equivalent series resistance (ESR) technique is proposed

for loop stability improvement. It enables the usage of the low-cost, multilayer ceramic capacitors in mobile applications. The constant biased voltage feedback loop (VFL) has a loop gain larger than 60 dB under all load conditions, which enables a good line and load regulation.

3. The third proposed LDO is a high current NMOS LDO with superior transient response. It is realized in 0.13 $\mu$ m SOI CMOS process featuring a 10mV undershoot and overshoot with 1A/100ns load current. The superior transient performance is achieved by a new multi-loop feedback scheme. The presented LDO also embodies a new frequency compensation scheme, which enables a stable 60dB DC loop gain despite 1A load current variation. This contributes to a small load regulation of 0.6 $\mu$ V/A and line regulation of 0.23mV/V. The LDO consumes 35 $\mu$ A quiescent current. The silicon size of the LDO is 325 $\mu$ m  $\times$  106 $\mu$ m.

All the proposed designs in this thesis achieve decent performance metrics, while consuming reasonable quiescent currents when they are compared with the representative prior-art works.

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# Table of Contents

Statement of Originality.....	ii
Supervisor Declaration Statement .....	iii
Authorship Attribution Statement .....	iv
Abstract.....	vi
Acknowledgement.....	ix
List of Figures .....	xiv
List of Tables.....	xix
Chapter 1 Introduction.....	1
1.1.    Background and motivation.....	1
1.2.    Objectives .....	5
1.3.    Contributions.....	5
1.4.    Organization of the thesis .....	6
Chapter 2 Literature review .....	9
2.1.    Review of low-dropout voltage regulator principle and topologies	9
2.2.    Review of the performance parameter metrics of an LDO.....	14
2.2.1.  DC and transient line/load regulation.....	16
2.2.2.  Regulator's input and output impedance .....	18
2.2.3.  Power supply rejection .....	19
2.2.4.  Other design parameters .....	20
2.3.    Types of error amplifier for LDO design .....	21

2.4.	Design consideration of the power transistor in LDO.....	22
2.5.	Review of the frequency compensation techniques for LDO regulator .....	24
2.5.1.	Review of the second order system.....	25
2.5.2.	Two-stage amplifier with Miller or Ahuja compensation .....	27
2.5.3.	Multi-stage nested Miller compensation .....	33
2.5.4.	Multi-stage feed forward compensation .....	37
2.5.5.	Internal zero compensation .....	39
2.6.	Review of prior-art transient response enhancing techniques .....	42
2.6.1.	The LDO with a super buffer stage for slew rate enhancement ...	43
2.6.2.	LDO with PID control: .....	44
2.7.	Summary.....	47
Chapter 3	A Low dropout regulator with rail-to-rail dynamic impedance attenuation buffer .....	49
3.1.	Design of the proposed LDO .....	49
3.2.	Circuit implementation and analysis of the proposed LDO design .. .....	55
3.2.1.	Loop analysis of Miller and Ahuja compensation techniques .....	57
3.2.2.	Offset analysis and the proposed solution for commercial design	64
3.3.	Hardware measurements of the proposed LDO.....	67
3.4.	Conclusions.....	69

Chapter 4 A 600mA fast-transient PMOS low-dropout regulator with pseudo-ESR technique .....	71
4.1.    Introduction.....	72
4.2.    The proposed LDO architecture.....	74
4.2.1.    Conceptual stability analysis for dual loop compensation .....	76
4.2.2.    Large-signal behavior of the fast feedback loop .....	78
4.2.3.    The pseudo-ESR technique.....	81
4.3.    Circuit implementation and stability analysis.....	84
4.3.1.    Circuit implementation .....	84
4.3.2.    Small signal analysis .....	86
4.4.    Experimental results .....	93
4.5.    Conclusions.....	100
Chapter 5 A multi-loop slew-rate enhanced NMOS LDO handling 1A load current transient.....	101
5.1.    The proposed LDO architecture.....	102
5.1.1.    Conceptual stability analysis of multi-loop compensation .....	103
5.1.2.    Large-signal behavior of the fast feedback loop .....	105
5.2.    Circuit implementation and stability analysis.....	106
5.2.1.    The adaptive buffer with the fast current feedback loop .....	108
5.2.2.    The auto-self-voltage-shift circuit network (ASVS).....	109
5.3.    Experimental results .....	116
5.4.    Conclusions.....	123

Chapter 6 Conclusions and future works.....	125
6.1.        Conclusions.....	125
6.2.        Future works .....	127
Author's publications .....	131
Journal publications .....	131
Conference publications.....	131
References.....	133

## List of Figures

Figure 1.1 Market research done by NPD [1].....	1
Figure 1.2 Typical power management integrated circuit for SOC .....	2
Figure 1.3 Typical voltage supply regulator module in PMIC [8].....	3
Figure 1.4 The two-steps approach in PMIC design [2].....	4
Figure 2.1 Generic low-dropout linear regulator. ....	10
Figure 2.2 Regulator efficiency versus biasing current [16].....	11
Figure 2.3 The block diagram of an (a) PMOS LDO, and a (b) NMOS LDO. .	12
Figure 2.4 Plot of the DC line/load regulations. ....	17
Figure 2.5 Typical transient response to positive and negative load jumps [8], [9]. .....	17
Figure 2.6 Typical regulator input/output impedance. ....	18
Figure 2.7 The types of amplifiers (a) Type A, (b) Type B.....	21
Figure 2.8 The operation regions of the LDO power transistor.....	23
Figure 2.9 LDO $I_{LOAD}$ versus minimum headroom. ....	23
Figure 2.10 Typical second order system. ....	25
Figure 2.11 Transient step response of second order system [44]. ....	26
Figure 2.12 Two stage amplifier with Miller compensation.....	27
Figure 2.13 Signal flow for RHP zero analysis.....	29
Figure 2.14 Signal flow for RHP zero cancelling nulling resistor analysis. ....	30
Figure 2.15 Miller compensation with nulling resistor. ....	31
Figure 2.16 Typical amplifier structure with Ahuja compensation [48]. ....	32
Figure 2.17 Simulated gain/phase plots for the Ahuja compensation circuit. ...	33
Figure 2.18 Structure of a three-stage NMC amplifier with the nested Miller compensation [49]. .....	34

Figure 2.19 Bode plot of the nested Miller compensation loop.....	36
Figure 2.20 Basic structure of AFFC amplifier [56].....	37
Figure 2.21 A circuit diagram of multi-stage feedforward compensation [57].	38
Figure 2.22 AC gain bode plot of feedforward compensated amplifier [57]....	39
Figure 2.23 The structure of the LDO with internal zero compensation [3]. ....	40
Figure 2.24 Different Bode diagrams. (a) $\omega_z$ is constant. (b) $\omega_z$ varies [3].....	41
Figure 2.25 The circuit implementation of $R_c$ . .....	42
Figure 2.26 Slew rate enhancement circuitry [70]. .....	44
Figure 2.27 A block diagram of a PID controller in a feedback loop. .....	45
Figure 2.28 schematic of tri-loop FVF based LDO [5].....	45
Figure 2.29 The diagram of LDO with derivative (D) control [72]. .....	46
Figure 2.30 An implementation example of LDO with derivative (D) control [72]. .....	46
Figure 3.1 LDO with intermediate dynamically biased buffer [22].....	50
Figure 3.2 LDO with proposed high swing super source follower buffer with dynamic biasing.....	51
Figure 3.3 (a) The rail-to-rail high swing super source follower buffer (RRHS- SSF); (b) Local super source follower loop analysis; (c) Gate pole analysis. ....	53
Figure 3.4 Schematic of the proposed LDO design. .....	56
Figure 3.5 AC small signal model for open loop circuitry. .....	58
Figure 3.6 Plot of the LDO loop gain and the power supply rejection (PSR). ..	61
Figure 3.7 AC simulation results of the LDO loop response with different loading condition. .....	64
Figure 3.8 LDO offset Monte Carlo simulation results. ....	65
Figure 3.9 Block diagram of the offset trim scheme. ....	66

Figure 3.10 The die photo of the proposed LDO.....	68
Figure 3.11 Measured load transient response of the proposed LDO( load step between 1mA and 600mA). .....	69
Figure 3.12 Measured PSR performance with 300mA load.....	69
Figure 4.1 System architecture of the proposed LDO.....	75
Figure 4.2 (a) Conceptual diagram of the dual loop compensation. (b) Bode plot sketch of the dual loop compensation.....	77
Figure 4.3 (a) Large signal transient response of the LDO with a step-up load transient. (b) Large signal transient response of the LDO with a step-down load transient.....	80
Figure 4.4 The relationship between the conventional ESR technique and the pseudo-ESR technique (AC small signal).....	82
Figure 4.5 Schematic of the proposed LDO design. ....	83
Figure 4.6 Small-signal model of voltage spike detector. ....	85
Figure 4.7 Small-signal model of the proposed LDO. ....	86
Figure 4.8 Loop frequency response of the proposed LDO at medium to heavy load conditions (simulation).....	89
Figure 4.9 (a) Simulation results of loop gain/phase of the proposed LDO with load current at 300mA, 10mA, 100 $\mu$ A, and 10 $\mu$ A. (b) Loop stability versus process corner/temperature. (c) Monte Carlo simulation result of loop stability of the proposed LDO. ....	93
Figure 4.10 Chip micrograph and layout. ....	94
Figure 4.11 Testing setup for the proposed PMOS LDO. ....	95

Figure 4.12 Measured output transient response of 600mA load step. (a) The transient response of the load current steps of 600mA in 100ns. (b) The transient response of the load current steps of 600mA in 1μs. ....	96
Figure 4.13 Measured PSR versus frequency for $I_{Load}=10\text{mA}$ and $I_{Load}=300\text{mA}$ when $V_{out}=1.8\text{V}$ , $V_{in}=2\text{V}$ , and $CL=1\mu\text{F}$ .....	97
Figure 4.14 Measured line transient response at the load current of 300mA. ...	97
Figure 5.1 System architecture of the proposed LDO. ....	103
Figure 5.2 (a) Conceptual diagram of the multi-loop compensation. (b) Bode plot sketch of the multi-loop compensation.....	104
Figure 5.3 (a) Large signal transient response of LDO for load step-up. (b) Large signal transient response of LDO for load step-down. ....	105
Figure 5.4 Schematic of the proposed NMOS LDO design. ....	107
Figure 5.5 Small-signal model of the voltage spike detector.....	108
Figure 5.6 Small-signal model of the proposed LDO. ....	110
Figure 5.7 Loop frequency response (simulation) of the proposed LDO at medium to heavy load conditions.....	114
Figure 5.8 Simulation results of loop gain/phase of the proposed LDO with load current of $10\mu\text{A}$ , $50\mu\text{A}$ , $500\mu\text{A}$ , $1\text{mA}$ , $5\text{mA}$ , $10\text{mA}$ , $50\text{mA}$ , $500\text{mA}$ . ....	116
Figure 5.9 Chip micrograph and layout. ....	117
Figure 5.10 Measured output transient response of 1000mA load step. (a) The transient response of the load current steps of 1000mA in 100ns. (b) The transient response of the load current steps of 1000mA in 1μs. ....	119
Figure 5.11 (a) Measured PSR versus frequency for $I_{Load}=500\text{mA}$ when $V_{out}=1.8\text{V}$ , $V_{in}=2\text{V}$ , and $CL=1\mu\text{F}$ . (b) Measured load regulation when $V_{out}=1.8\text{V}$ , $V_{in}=2\text{V}$ . ....	120

Figure 6.1 The typical circuit diagram of the low noise LDO design ..... 127

Figure 6.2 The system solution of the extremely low noise LDO design. ..... 128

## **List of Tables**

Table 4.1 List of loop poles and zeros of the proposed PMOS LDO.....	88
Table 4.2 Performance summary of the proposed PMOS LDO. ....	99
Table 5.1 List of loop poles and zeros of the proposed NMOS LDO. ....	112
Table 5.2 Performance summary of the proposed NMOS LDO.....	122



# Chapter 1

## Introduction

### 1.1. Background and motivation

The consumer electronics industry has expanded rapidly in recent years. The demand for the battery-powered electronic device is growing exponentially. The user's requirement of longer battery life and smaller size drives the engineers to come up with more and more advanced techniques for improving circuit power efficiency with minimum cost. According to the market research from NPD [1], the total smartphone annual shipments increase every year as shown in Figure 1.1. And the demand will continue to grow.

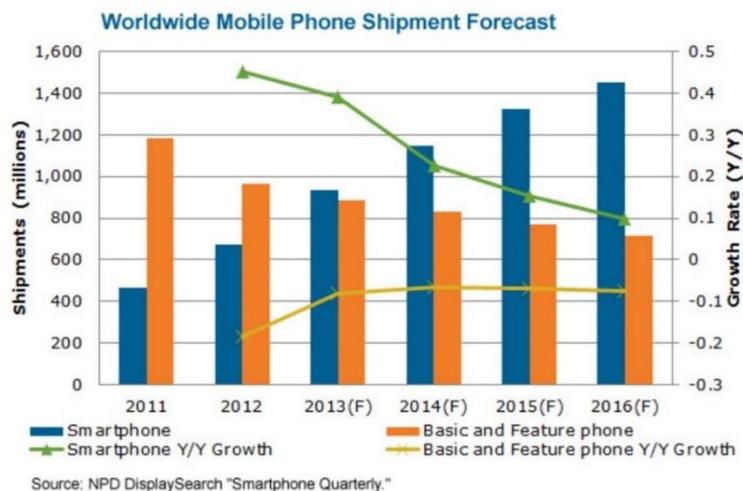


Figure 1.1 Market research done by NPD [1].

To achieve lower standby current consumption and high power conversion efficiency at the same time, power management integrated circuit (PMIC) is playing a very critical role in the battery-powered devices, such as smartphones

and tablets, etc. Generally, power management includes managing the power supply to be used, conserved or distributed, and controlling the different power supply level generation. A typical PMIC for SOC is shown in Figure 1.2 [2], [3]. It integrates not only regulators, but also battery charger, fuel gauge, and high accuracy crystal clock reference for the RF circuits and microprocessors. Different types of regulators are used to provide the voltage or current sources to the loads through the printed circuit board (PCB) traces or Flat Flex Cables [3], [4], [5], [6], [7]. The power up sequencing controller and supervisor are also included in PMIC.

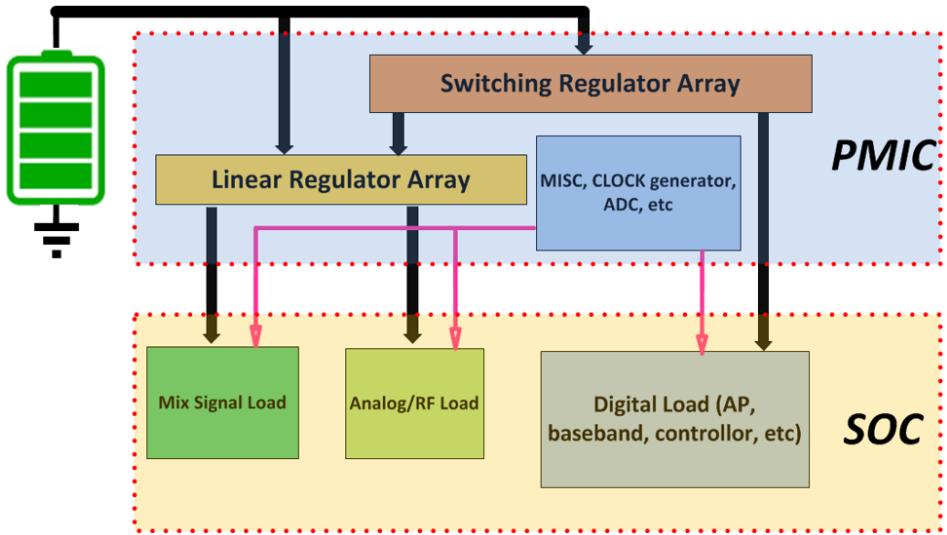
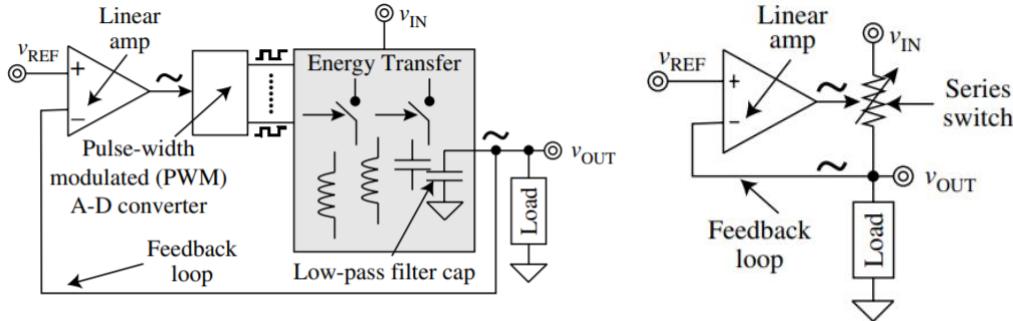


Figure 1.2 Typical power management integrated circuit for SOC.

There are typically two types of power regulators in PMIC design: switching mode power supply (SMPS) regulator (including switching inductor based regulator and switching capacitor based regulator) and linear regulator, as shown in Figure 1.3. Both regulators can produce the almost load-independent fixed voltage power supply out of a variable energy source. SMPS regulator can step up/down the voltage for different applications with high power efficiency. Although linear regulator is not power efficient and only support voltage step-

down, one of the important advantages is low noise output voltage, which is highly important for some special circuit modules, such as RF, ADC, etc.



### Switching Regulator

- Efficiency, step up, down or both
- Commonly referred as SMPS

### Linear Regulator

- Inefficiency, only step down
- Commonly referred as LDO

Figure 1.3 Typical voltage supply regulator module in PMIC [8].

The LDO is one of the most critical modules in power management system as it is used to regulate the rippled supply to provide a “clean” voltage source for all kind of noise-sensitive or level-sensitive analog/RF/digital modules [9], [10], [11], [12], [13]. For commercial products, it becomes very challenging to design an LDO with high stability, low voltage dropout, fast transient, and a small area, and accurate output voltage under process-voltage-temperature (PVT) variations.

Firstly, large power FET is needed, as while delivering high loading current, it requires a very low voltage drop across the power FET to achieve high power efficiency. Secondly, to avoid device being turned off or getting reset abnormally, fast transient response with smaller voltage variation at load-switching is essentially important for portable applications. Thirdly, a reasonable power supply rejection and output voltage accuracy are required for LDO that supplies sensitive loading. In short, LDO requires careful design by balancing circuit topology, amplifier gain, and quiescent current, etc. [9], [10].

Instead of using regulators under the battery to directly supply each module, a

two-step approach is widely used nowadays in PMIC design, as shown in Figure 1.4. The primary regulators, which can handle large load current, are used to generate shared power supply. The primary regulators (i.e., switching regulators) are commonly used to provide a wide range of output voltages. The output voltage can be either higher or lower than the battery supply voltage with different regulator design topologies. Switching regulator works as an energy transporter by moving small chunks of energy, bit by bit, from the battery to the output. The energy losses involved in such energy-transportation are relatively small. Since the energy transportation in the switching regulator is running in a non-continuous way, there are always voltage ripples appeared at regulator output, which is normally not acceptable for noise-sensitive circuits.

Then, an array of secondary regulators are LDOs that operate under the shared power supply are built to supply individual modules. They generate multiple voltage output independently for the system. As compared to switching regulator, LDO has better transient response, lower noise and better power supply isolation, but its efficiency is low. As a result, a switching regulator followed by a linear regulator topology could be a good solution for both performance and efficiency.

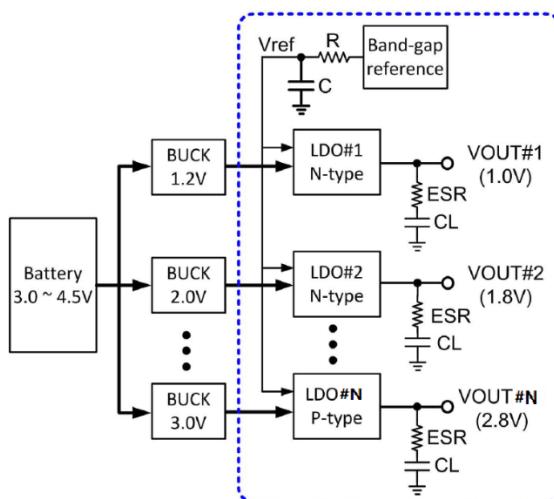


Figure 1.4 The two-steps approach in PMIC design [2].

## **1.2. Objectives**

The thesis objectives are listed below:

- (i) To investigate and understand the design challenges of high-performance LDO designs. To conduct a comprehensive literature review on performance metrics, frequency compensation schemes and transient response enhancement techniques.
- (ii) To explore techniques that could advance the LDO design for battery-powered portable devices, with better transient response, smaller area and lower quiescent current. This work pertains to the design and realization of the fast transient LDOs for battery-powered portable applications.

## **1.3. Contributions**

The contributions of this thesis are the design and monolithic realization and testing characterization of three high-performance analog linear voltage regulators (LDOs) in the CMOS process.

The specific contributions to the LDOs are:

- (1) An LDO with a rail-to-rail swing dynamic biasing impedance-attenuation buffer has been fabricated in a  $0.18\text{-}\mu\text{m}$  HV CMOS process. The buffer's featured rail-to-rail swing allows a smaller power FET to be used compared with traditional buffer design. This design also improves robustness in terms of stability and offset. A low-cost trim method is also introduced to achieve a potential high yield in production.

- (2) A dual-loop compensated, fast-transient PMOS LDO is successfully implemented in a  $0.18\text{-}\mu\text{m}$  CMOS process with a total silicon area of  $210\text{ }\mu\text{m} \times 593\text{ }\mu\text{m}$ . The proposed LDO is composed of two feedback loops. The fast feedback loop (FFL) employs direct output voltage spike detection through capacitive coupling, resulting in significantly improved large-signal transient response and loop bandwidth. A power transistor with the pseudo-equivalent series resistance (ESR) technique is proposed for loop stability improvement. It enables the usage of the low-cost, multilayer ceramic capacitors in mobile applications. The constant biased voltage feedback loop (VFL) has a loop gain larger than  $60\text{ dB}$  under all loading conditions, enabling a good line and load regulation.
- (3) A high current with superior transient response NMOS LDO is realized in  $0.13\mu\text{m}$  SOI CMOS process featuring a  $10\text{mV}$  undershoot and overshoot with a  $1\text{A}/100\text{ns}$  load current. The superior transient performance is achieved by a new multi-loop feedback scheme. The proposed LDO also employs a new frequency compensation scheme, enabling a stable  $60\text{dB}$  DC loop gain despite a  $1\text{A}$  load current variation.

All the proposed designs in this thesis achieve decent performance metrics while consuming reasonable quiescent currents when compared with prior-art.

## 1.4. Organization of the thesis

The remainder of this thesis is organized as follows.

Chapter 2 reviews the low-dropout linear regulator. Firstly, the performance metrics are presented. It mainly focuses on line/load regulation, power supply

ripple rejection, and accuracy. Secondly, both frequency compensation techniques and the prior-art transient response enhancing techniques are reviewed. Analysis on different types of regulator design is also discussed.

In Chapter 3, design details on an LDO with a high swing dynamic biasing impedance-attenuation buffer is discussed. The buffer's rail-to-rail swing makes the LDO's power FET size smaller than traditional buffer design for the same current capability. This chapter also analyses its design robustness in terms of stability and offset. A low-cost trim method is also introduced.

Chapter 4 presents a dual loop-compensated, fast-transient LDO for battery-powered applications. The proposed LDO is composed of two feedback loops. The fast feedback loop (FFL) employs direct output voltage spike detection through the capacitive coupling, resulting in significantly improved large-signal transient response and loop bandwidth at the same time. A power transistor with the pseudo-equivalent series resistance (ESR) technique is proposed for loop stability improvement. It enables the usage of the low-cost, multilayer ceramic capacitors in mobile applications. The constant biased voltage feedback loop (VFL) enables a good line and load regulation.

In Chapter 5, a high current with superior transient response NMOS LDO is proposed. The superior transient performance is achieved by a new multi-loop feedback scheme.

Conclusions of this thesis are drawn in Chapter 6. Future research recommendations are also presented.



# **Chapter 2**

## **Literature review**

In this chapter, we will first review the principle and topologies of the low-dropout voltage regulator. Then, key performance parameters are discussed in details, followed by the power FET design considerations. This thesis emphasizes on frequency compensation and fast load transient response techniques. Therefore, various frequency compensation techniques are discussed, including (a) Miller or Ahuja Compensation; (b) Multi-Stage Nested Miller Compensation; (c) Multi-Stage Feed Forward Compensation; (d) Internal zero compensation; etc. Subsequently, a few prior-art transient response enhancing techniques are reviewed in details.

### **2.1. Review of low-dropout voltage regulator principle and topologies**

LDO design is quite mature nowadays, and some of the earliest designs can be traced back to the early 1970s [14], [15]. The primary function of the LDO is to provide a clean and stable voltage source for the loadings. The output voltage should be insensitive to supply voltage and load current variations.

Figure 2.1 shows the generic LDO circuit structure. The design consists of an error amplifier (EA), a buffer stage, a power transistor, a feedback network and an accurate voltage reference. A large power FET is needed for high current delivery capability. A buffer stage is usually introduced to improve the transient response. The quiescent current ( $I_Q$ ) is the difference between LDO's input

current and load current, which is the total current of the error amplifier and buffer stage.  $V_{Drop}$  is the voltage dropout across the power transistor when the regulator is in operation. Based on the analysis of this circuit model, the regulator's power efficiency can be expressed by Equation (2.1).

$$\eta = \frac{V_{out} * I_{Load}}{(V_{out} + V_{Drop}) * (I_Q + I_{Load})} \quad (2.1)$$

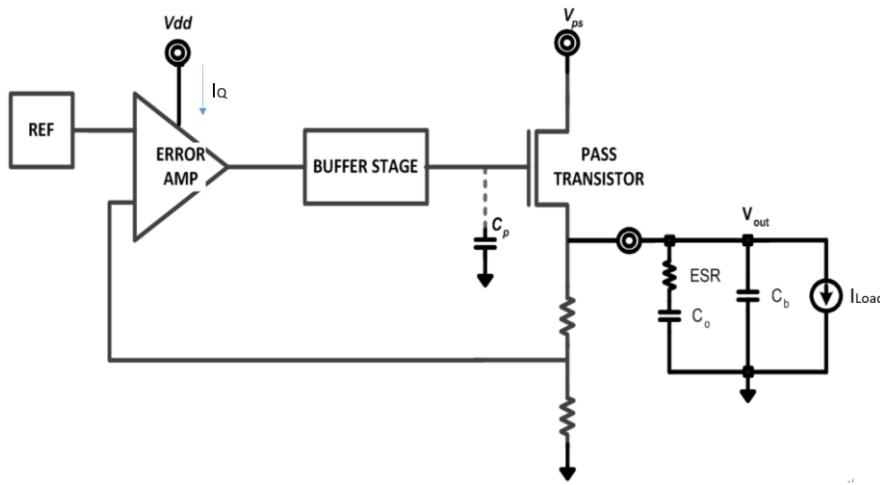


Figure 2.1 Generic low-dropout linear regulator.

The power efficiency is a function of voltage drop ( $V_{Drop}$ ) and quiescent current ( $I_Q$ ). The regulator's overall power efficiency can be improved by reducing the  $V_{Drop}$  and  $I_Q$ . Figure 2.2 shows the plot of regulator power efficiency versus load current under a particular output voltage and dropout voltage condition across different regulator's quiescent current [16]. The power efficiency of regulator in light-load condition is a critical parameter for a battery-powered system, since the standby mode or light-load condition is the dominated condition for most applications. Hence, it is extremely important to reduce the regulator's quiescent current. As shown in Figure 2.2, an improvement of quiescent current from  $10\mu A$

to  $1\mu\text{A}$  can greatly improve the power efficiency from 45% to 82%. Also, the reduction of the dropout voltage across the power transistor will improve power efficiency as well. However, reduction of quiescent current and dropout voltage degrades the LDO's transient performance including slewing and ripples. In many reports [9], [10], [17], [18], [19], the LDOs have to consume large quiescent current to meet transient performance specification. To address the dilemma of efficiency degradation and poor transient response, a slew-rate enhancement circuitry is introduced to speed up the regulator's transient response without the penalty of the huge quiescent current [20], [21]. Besides the power efficiency, the DC and AC performances (line regulation, load regulation, output voltage accuracy, power supply rejection etc.) are also essential for an LDO.

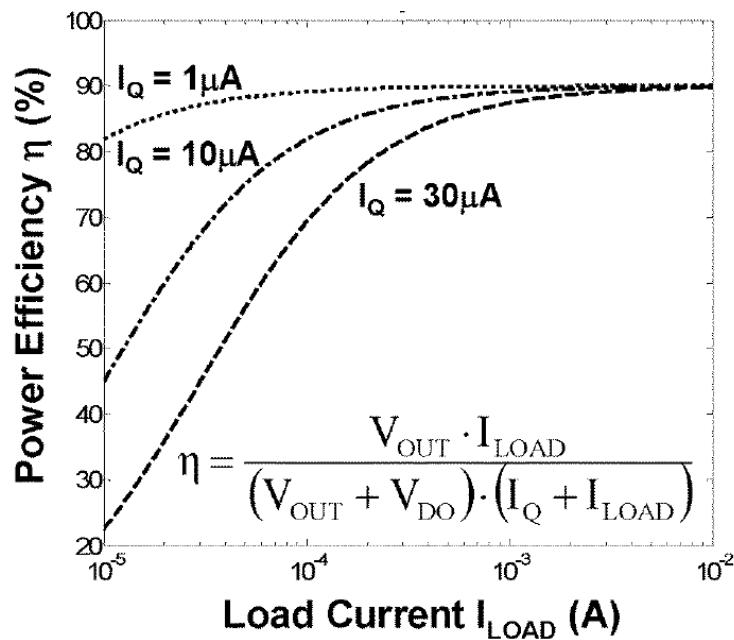


Figure 2.2 Regulator efficiency versus biasing current [16].

In view of analog LDO designs, there are many reported LDO topologies, each with its specific advantages and limitations. Choosing the appropriate LDO topology is always critical for the specific application. Here, several representative analog LDO design topologies are reviewed.

Generally, there are mainly two ways to categorize the different analog LDO topologies. Firstly, The LDOs can be categorized into PMOS LDO [22], [23], [24] and NMOS LDO [25], [2], [26] based on the type of the power transistor in the LDO design. Secondly, the LDOs can be also categorized into cap-LDO and capless-LDO based on the size of the output capacitor.

(1) Using the first categorization method, the simplified block diagram of PMOS LDO and NMOS LDO are depicted in Figure 2.3 (a) and (b) respectively. Basically, from a block-level or system-level point of view, an LDO is just a two-stage amplifier in a negative feedback control loop. This amplifier consists of an error amplifier stage and the output stage. However, LDO design is unique and different from just a classic amplifier design. LDO is expected to handle a very wide range of load current, which can be from zero current up to Ampere range.

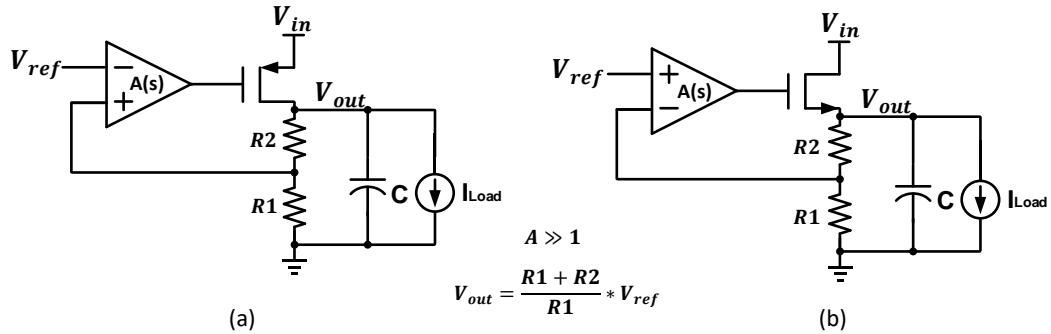


Figure 2.3 The block diagram of an (a) PMOS LDO, and a (b) NMOS LDO.

For the PMOS LDO, a PMOS power FET is used in the output stage, which can be treated as a class-A common source amplifier. Given the load variation and load profile difference, the overall loop gain varies, and loop poles and zeros move all over the place, which makes the design very challenging.

For the NMOS LDO, an NMOS power FET is used in the output stage, which is a source follower. Recent studies have shown that NMOS LDO is advantageous over PMOS LDO from both DC and transient perspectives [2], [27], [26]. The power stage of NMOS LDO is a source follower featuring low output impedance. Therefore, the DC loop gain is relatively insensitive to load conditions leading to good line regulation and load regulation over a wide load current range. Moreover, the low output impedance also contributes to a small overshoot/undershoot during a load transient. Lastly, the NMOS LDO is more area efficient than PMOS LDO.

Specifically, in the PMOS LDO design, the error amplifier and the PMOS power FET can share the same input supply, while in the NMOS LDO, it requires a higher supply voltage for the error amplifier to achieve a low dropout voltage [27], [2], [28]. The requirement of higher separate power supply increases the design complexity of the NMOS LDO. In the battery-powered PMIC, this can be easily achieved by powering the error amplifier directly from the battery [2], [3].

(2) With the second categorization method, the type of LDO is defined based on the presence of the output capacitor (in the range of a few  $\mu\text{F}$ ) [14], [29], [30], [31], [32], [3], [33]. The LDO requiring an off-chip capacitor is defined as the cap-LDO. The LDO without an off-chip capacitor is defined as capless-LDO. It is attractive to have the capless-LDO in the system for the reduction of the printed circuit board (PCB) area and Bill-of-Materials (BOM) costs. However, the performance of the capless-LDO is compromised, with limited supported load current range, poor load transient response and poor PSR at high frequencies. Both academics and industry have tried many capless-LDO voltage regulator

designs, but many of the architectures have been prevented from practical use due to the performance limitation. Most of the reported capless-LDOs only improve specific performance parameters such as load regulation, line regulation, or fast settling time. And the LDO supports very limited range of load capacitor due to stability concern. The maximum supported load current is usually less than 100mA [26], [34], [35], [36]. They also suffer significant losses in terms of dynamic performance and PSR effectiveness. On the contrary, the cap-LDO voltage regulator uses the  $\mu$ F-range off-chip output capacitor, which contributes to a good power-supply noise rejection and superior line/load transient response performance. With the same dynamic performance and PSR specification, cap-LDO compares favorably with capless-LDO on power consumption, as the passive component serves as a charger and can provide instantaneous current during load changes. Therefore, cap-LDOs are much preferred in many applications. Because there is always a visible pole at the output of cap-LDO due to the larger size off-chip capacitor, capacitor non-idealities such as ESR/ESL must be carefully considered in the cap-LDO design [37]. A careless selection of the type or size of the off-chip capacitor could lead to stability or dynamic performance problems.

## 2.2. Review of the performance parameter metrics of an LDO

Before getting into the regulator performance metrics, it is worthwhile to discuss the different types of load in the VLSI systems, as power regulator may behave differently with different type of load. The type of load refers to not only the voltage-current characteristics of the load, but also how the load current varies with time.

The first type of load is DC constant load. Taking a class-A amplifier as an example, the total current, looking from its supply, is always equal to the total bias current. That total current is not a function of supply unless we purposely design so for certain performance reason. This is typically true in most analog circuits with the fixed bias current. Therefore, it is also called an analog load.

The second type is the resistive load, which is also a DC load. As the name suggests, the value of the resistive load current is directly proportional to the supply.

Although they are both DC loads, the way that they impact the system is fundamentally different. The small-signal impedance of the analog load is decoupled from the DC impedance of the load. Even at full-load condition, the impedance of an analog load as if there is no-load, while for resistive load, that is not the case. This must be taken into consideration in the regulator design. Otherwise, the regulator can be easily unstable. For DC load, although decoupling is not necessary, it may still require a capacitor for other purpose, such as noise and load/line transient response.

The third type of load is the switching load, which is usually the digital load. Typical digital load current has a high peak-to-average ratio. The peak spike current can be high but only lasts for a very short period of time (i.e., in the range of pico-seconds). Typically, the loop of regulator is not able to respond to such fast current spikes. Hence, to handle the switching load, it always requires a large decoupling capacitor.

After introducing the types of load, we can now dive into the performance metrics. Generally, the LDO's performance parameters fall into the following categories:

- (1) DC parameters: quiescent current, Dropout voltage, DC load/line regulation, efficiency, and temperature characteristics, etc.
- (2) Dynamic parameters: transient load/line response, start-up time, shutdown time, etc.
- (3) AC parameters: loop stability, power supply rejection, noise, etc.
- (4) Other parameters: silicon area, ESR, capacitive range, etc.

Here are some key performance parameters to be described in detail.

### **2.2.1. DC and transient line/load regulation**

The DC line regulation refers to the DC change in the output voltage as the function of the DC change in the regulator input voltage. The DC load regulation refers to the DC change in the output voltage as the function of the DC change in the load current. DC line and load regulation can be expressed in (2.3) and (2.4) [8]. The detailed output-input characteristic curve are shown in Figure 2.4. For a finite DC loop gain, the DC load regulation is not perfect. The load regulation error  $\Delta V_{LD}$  is

$$\Delta V_{LD} = \Delta I_{Load} R_{CL} = \Delta I_{Load} \left( \frac{R_{OL}}{1 + A_{OL}} \right) \quad (2.2)$$

Where  $R_{CL}$  is the close-loop output impedance.  $R_{OL}$  is the open-loop output impedance.  $A_{OL}$  is the DC gain across the feedback loop [8].

$$V_{Line} = \frac{V_{o\_max} - V_{o\_min}}{V_{o\_nom}} * 100 \% . \quad (2.3)$$

$$V_{Load} = \frac{V_{o\_max} - V_{o\_min}}{V_{o\_nom}} * 100 \% . \quad (2.4)$$

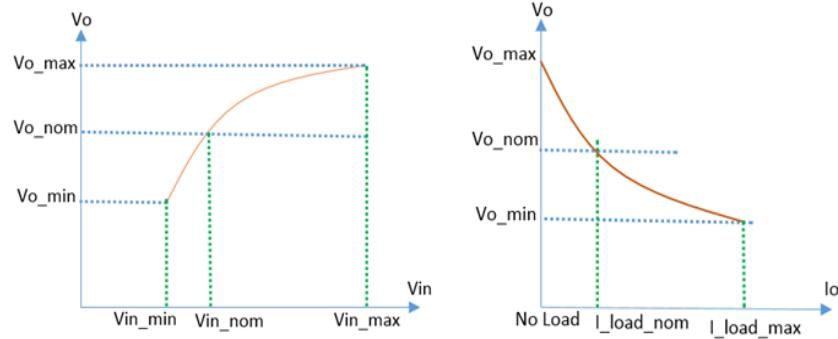


Figure 2.4 Plot of the DC line/load regulations.

The transient line/load regulation refers to the transient change in the output voltage due to a transient change in the regulator input voltage/ load (Figure 2.5). The undershoot and overshoot are the response of the step of the input voltage or load current. Similar as the DC line/load regulation, they are defined in terms of accuracy normalized to a nominal output voltage.

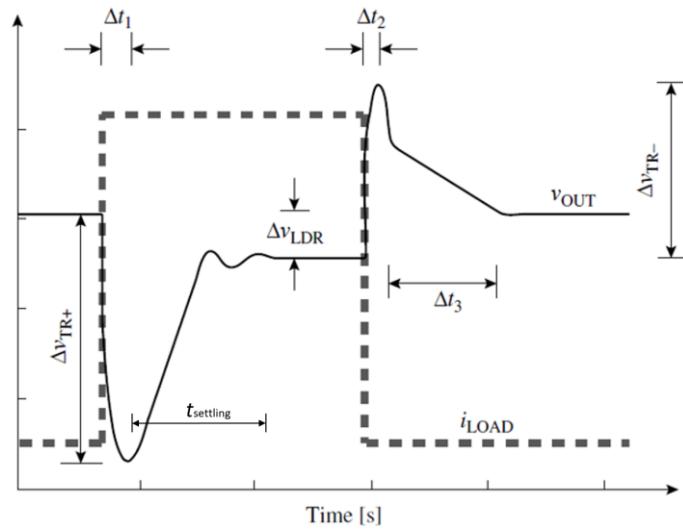


Figure 2.5 Typical transient response to positive and negative load jumps [8], [9].

The response time  $\Delta t_1$  can be expressed as the below equation.

$$\Delta t_1 = \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par} \frac{\Delta V}{I_{sr}} \quad (2.5)$$

It is the function of the regulator closed-loop bandwidth ( $BW_{cl}$ ) and error amplifier's slew rate, which is associated with the power FET's parasitic capacitance ( $C_{par}$ ) and tail current bias ( $I_{sr}$ ). To reduce  $\Delta t_1$ , the dynamic biased error amplifier and power FET drive buffer are proposed in some research papers. [22], [38], [39], [40].

### 2.2.2. Regulator's input and output impedance

The regulator output impedance is used to define how one load disturbance affects the other load circuit if they are sharing the same regulator output as the power supply source. The output impedance determines whether different loads can be shared on the same regulator. The regulator input impedance defines the ability of the regulator to suppress variation in the input voltage. Figure 2.6 shows the typical regulator's output/input impedance versus frequency. It is a strong function of regulator loop bandwidth and output de-coupling capacitance, etc. Designing a regulator with high loop bandwidth and smaller de-coupling capacitance for a given current consumption budget is always a challenging job.

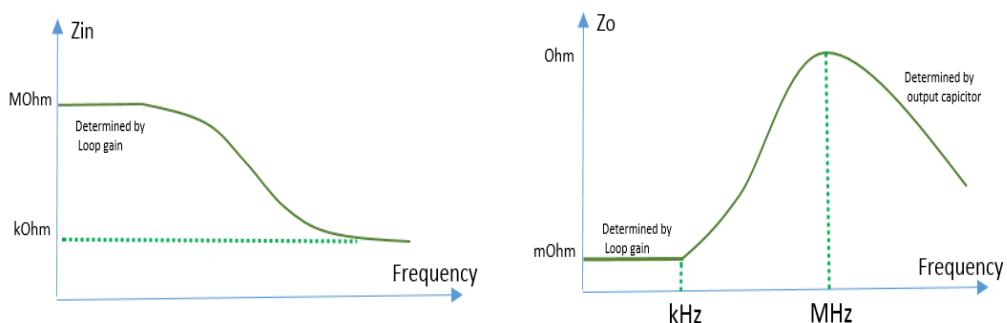


Figure 2.6 Typical regulator input/output impedance.

### 2.2.3. Power supply rejection

The ideal regulator can maintain the output when the supply noise is injected. It cannot be realized in the real world. Power supply rejection (PSR) is used to describe how well the actual devices can reject the voltage ripple coming from the device's power supply across various frequencies as shown in Equation (2.6). In LDO case, PSR is defined as the output ripple over the input supply ripple in our interested frequency range as shown in Equation (2.7).

$$PSR = 20 \log \frac{Ripple_{output}(s)}{Ripple_{input}(s)} \quad (2.6)$$

Specifically, for an LDO design, it can be written as

$$PSR = 20 \log \frac{A_{vo}(s)}{A_v(s)} \quad (2.7)$$

Here,  $A_v$  is the open-loop gain of the whole regulator's negative feedback loop and  $A_{vo}$  is the loop gain defined when the regulator loop is broken. From the equation, the power supply rejection can be intuitively improved by increasing the regulator's loop gain and bandwidth and enhance the open-loop isolation between the input power supply and regulator output. For a typical regulator design,  $A_{vo}$  is normally in a range of -5dB to 15dB, which is limited by the regulator's current rating and transistor parasites related to process nodes. As shown in the equation, the regulator loop gain and unity-gain bandwidth are the dominant factors for the power supply ripple rejection in our interested frequency range. The overall PSR is dominated by the error amplifier for the low-frequency range. The bandwidth of PSR is dominated by the error amplifier. When the

frequency is higher than the loop bandwidth, the PSR is determined by the output capacitance [23], [27], [41], [42].

#### **2.2.4. Other design parameters**

Output noise voltage is one of the important design parameters for the LDOs, which can be the supply of the noise-sensitive circuitry such as RF and sensor node. The specification of the noise voltage is defined as the RMS noise voltage over a specified range of frequency with the condition of constant input and output. The main contributors to the regulator noise voltage are the voltage reference noise and regulator noise itself. The voltage reference is normally generated from an on-chip bandgap reference and an off-chip decoupling capacitance is widely used for the reduction of noise in many commercial products [3]. Most of the noise in the regulator come from the error amplifier, including thermal and flicker 1/f noise. It is always a design challenge on the trade-off between noise and power consumption to meet certain system performance requirements. For most regulators used for sensitive loading, an off-chip bypass capacitor is normally required at the output node for further noise reduction and high PSR.

Another important parameter in LDO design is the output voltage accuracy. The overall accuracy can be defined as below equation.

$$Accuracy \approx \frac{|\Delta V_{Line}| + |\Delta V_{Load}| + \sqrt{\Delta V_{o,ref}^2 + \Delta V_{o,amp}^2 + \Delta V_{o,r}^2 + \Delta V_{o,TC}^2}}{V_{out}} \quad (2.8)$$

Here,  $\Delta V_{Line}$  and  $\Delta V_{Load}$  are the line and load regulation, respectively. Other contribution factors include reference voltage drift ( $\Delta V_{o,ref}$ ), sampling resistor tolerance ( $\Delta V_{o,r}$ ), error amplifier's offset and drift ( $V_{o,amp}$  and  $\Delta V_{o,TC}$ ) [8].

### 2.3. Types of error amplifier for LDO design

As shown in Figure 2.7, the single-ended output error amplifier in LDO is usually realized with a differential input pair and the diode-connected MOSFET for differential-to-single-end conversion [43]. Based on the type of diode-connected MOSFET used, it can be divided into two types. Type A (a) has PMOS current mirror at the supply side, while Type B (b) has NMOS current mirror at the bottom.

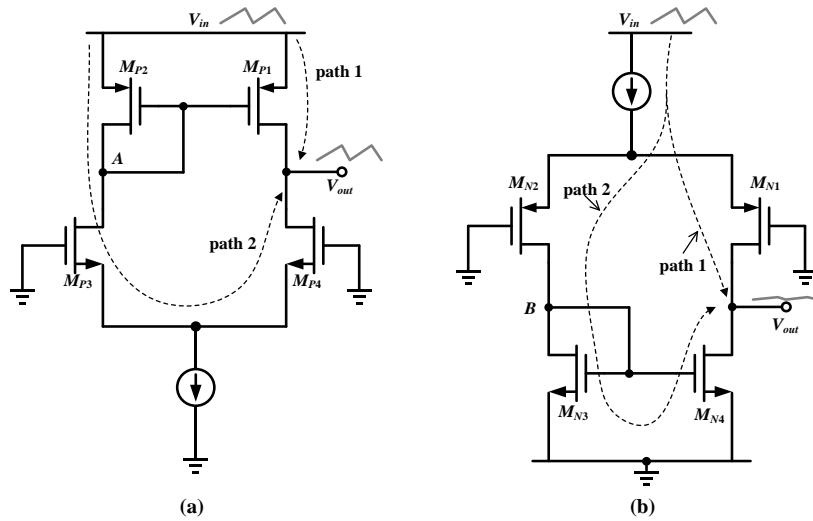


Figure 2.7 The types of amplifiers (a) Type A, (b) Type B.

To determine which type is better for error amplifier in LDO, PSR analysis are done on both types.

For Type A amplifier, as the circuit is symmetric, the voltage at the output node ( $V_{out}$ ) is essentially equal to the voltage at the PMOS current mirror gate (node A). The voltage at this node A depends on the current flowing in the bridge and

the supply ( $V_{in}$ ). With a fixed bias current,  $V_{gs}$  of  $M_{P2}$  remain unchanged. Therefore, node A voltage tracks  $V_{in}$ .

Similarly for Type B amplifier shown in Figure 2.7 (b), the amplifier's output ( $V_{out}$ ) follows the gate voltage of the NMOS current mirror (node B). The voltage level is well determined by  $V_{gs}$  of  $M_{N3}$ , which tracks the ground, instead of  $V_{in}$ . Therefore, this amplifier's PSR is high, given that the bias current and  $V_{gs}$  of  $M_{N3}$  do not change when the supply varies.

As shown in Figure 2.3, the error amplifier's output is connected to the gate of power FET. For PMOS LDO, the power FET works as a current source. Therefore, Type A amplifier is preferred for PMOS LDO. For NMOS LDO, the power FET works as the source follower. Therefore, Type B amplifier is better for NMOS LDO.

## 2.4. Design consideration of the power transistor in LDO

To realize an LDO with good regulations, fast transient response and high PSR, a high loop gain is needed. The power transistor is part of the LDO control loop, thus its transconductance ( $gm$ ) and transistor output impedance ( $rds$ ) directly impact the loop gain and consequently the LDO performance.

Figure 2.8 illustrates  $I_{DS}$  (the load current) versus  $V_{DS}$  (headroom) of the power transistor [43]. To achieve high  $gm$  and  $rds$  at a given load current, the headroom across the power transistor should be high enough to operate the FET in the saturation region. Given that  $rds = dV_{ds}/dI_{ds} = 1/\text{slope of the curve}$ ,  $rds$  is high where the curve is flat. If the headroom is lowered that the device enters the “gray” zone, the LDO performance starts to degrade, particularly PSR. The LDO may

still be able to regulate the output voltage but performance may not be up to the specification.

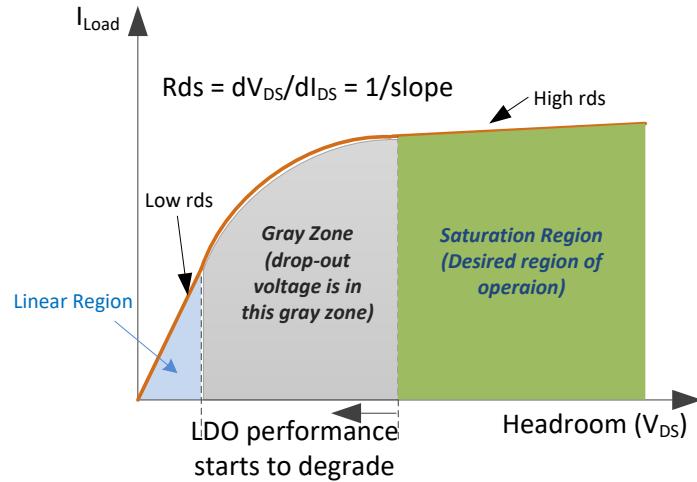


Figure 2.8 The operation regions of the LDO power transistor.

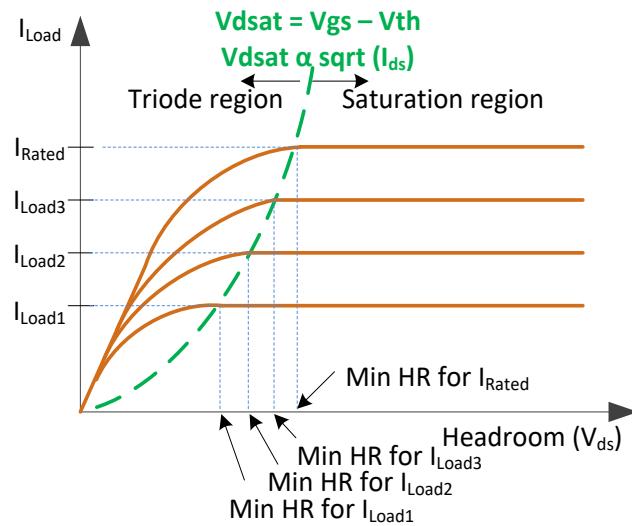


Figure 2.9 LDO  $I_{LOAD}$  versus minimum headroom.

Figure 2.9 further illustrates the minimum headroom required across the power transistor at different load currents to keep the FET in saturation. The headroom at which the FET enters saturation is defined as  $V_{DSAT} = V_{GS} - V_{TH} \propto \sqrt{I_{LOAD}}$  and illustrated in the figure by the dotted green line. If we define the LDO's

designed headroom at the rated load current, the acceptable operational headroom is defined by Equation (2.9), which can be smaller when the load current decreases.

$$\text{HeadRoom} = \text{Designed HeadRoom} \times \sqrt{\frac{I_{\text{Load}}}{I_{\text{Rated}}}} \quad (2.9)$$

## 2.5. Review of the frequency compensation techniques for LDO regulator

Basically, all linear regulator design can be treated as a multi-stage amplifier design with closed-loop configuration. As shown in Figure 2.3, normally the power transistor is designed with a big size in order to achieve low dropout voltage and deliver high current. The large parasitic capacitance of the power transistor could harm the loop stability. In the linear regulator design, the pole of power FET gate is normally pushed to high frequency by introducing a buffer with the penalty of extra current consumption. Nowadays, frequency compensation for an LDO loop is realized by pole splitting technique, the pole and zero cancellation technique or multi-loop compensation (also known as PID control method). In this section, we first review the second-order system in terms of AC analysis and the corresponding transient behavior. Then, the two-stage amplifier designs with Mirror and Ahuja compensation techniques are discussed. And to achieve high loop gain and wide bandwidth, design techniques on multi-stage amplifier are reviewed. Lastly, pole-zero cancellation technique is introduced in brief.

### 2.5.1. Review of the second order system

Most of the stable systems are second-order systems or can be simplified as second-order systems. Studying the behavior of a second-order system can give an insight of the relationship between circuit response and pole locations, so that the simple rules and design guide can be derived for stability.

Firstly, the typical second-order system related to the regulator design is shown in Figure 2.10. Based on the diagram, the transfer function between  $V_{in}$  and  $V_{out}$  can be obtained with the following derivation.

$$\left(V_{in} - \frac{V_{out}}{k}\right) \frac{\omega_u}{s} \frac{1}{1 + \frac{s}{P_2}} = V_{out} \quad (2.10)$$

$$V_{in} = V_{out} \frac{s}{\omega_u} \left(1 + \frac{s}{P_2}\right) + \frac{V_{out}}{k} \quad (2.11)$$

$$\frac{V_{out}}{V_{in}} = \frac{k}{1 + \frac{s * k}{\omega_u} + \frac{s^2 * k}{\omega_u P_2}} \quad (2.12)$$

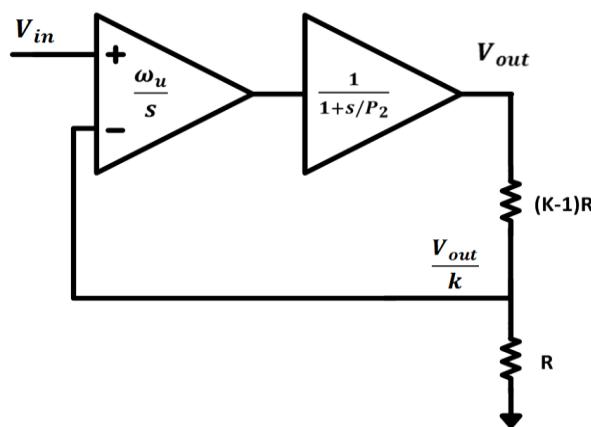


Figure 2.10 Typical second order system.

This second-order system can be characterized by its natural frequency and damping factor.

Here, the natural frequency:

$$\omega_n = \sqrt{\frac{\omega_u P_2}{k}} \quad (2.13)$$

The damping factor:

$$\xi = \frac{1}{2} \sqrt{\frac{k * P_2}{\omega_u}} \quad (2.14)$$

The corresponding transient step response is plotted in Figure 2.11 with different damping factors. It is defined as critical damping when  $\xi = 1$ ; under-damping when  $\xi < 1$ ; over-damping when  $\xi > 1$ . Considering the trade-off between response time and overshoot, a critical or slightly under-damping is always desired in design.

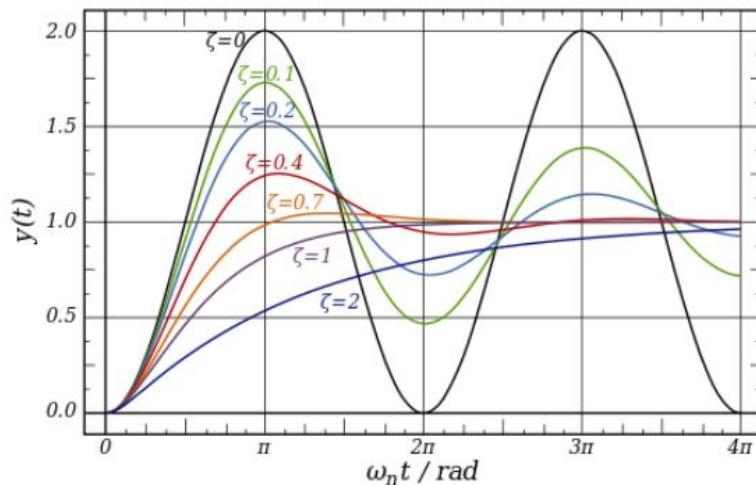


Figure 2.11 Transient step response of second order system [44].

### 2.5.2. Two-stage amplifier with Miller or Ahuja compensation

#### (1) Two-stage amplifier with Miller compensation

Miller compensation for a two-stage system is well known in amplifier design.

The Miller effect is utilized to reduce the total compensation capacitor size, thus the final amplifier silicon area can be reduced. To illustrate this compensation scheme, the simplified circuitry model for a Miller compensated two-stage amplifier is shown in Figure 2.12. The second stage can be treated as the current-controlled voltage source.

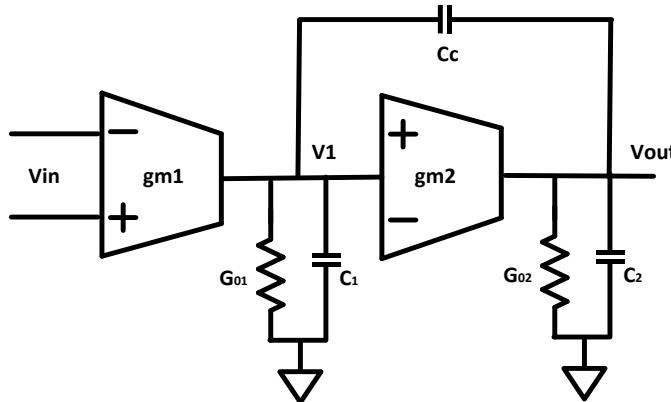


Figure 2.12 Two stage amplifier with Miller compensation.

The above circuitry has only two state variables. This is a second-order system with two poles. The KCL equation can be expressed as below.

$$\begin{bmatrix} s(C_1 + C_c) + G_{o1} & -sC_c \\ gm_2 - SC_c & s(C_2 + C_c) + G_{o2} \end{bmatrix} \begin{bmatrix} V1 \\ Vout \end{bmatrix} = \begin{bmatrix} -gm_1 * Vin \\ 0 \end{bmatrix} \quad (2.15)$$

After simplification, the  $V_{in}$  and  $V_{out}$  can be expressed as

$$\frac{V_{out}}{Vin} = \frac{gm_1(gm_2 - SC_c)}{s^2(C_1C_c + C_2C_c + C_1C_2) + s(C_c(gm_2 + G_{o1} + G_{o2}) + C_1G_{o2} + C_2G_{o1}) + G_{o1}G_{o2}} \quad (2.16)$$

The denominator is the second-order equation. System poles can be obtained by solving the roots. With the assumption that the two roots are far from each other, the transfer function is given in Equation (2.17).

$$\frac{V_{out}}{Vin} = \frac{A_0(1 - \frac{s}{Z_1})}{\left(1 + \frac{s}{-P_1}\right)\left(1 + \frac{s}{-P_2}\right)} \quad (2.17)$$

Here are two poles and one right-half-plane zero. The corresponding parameters are calculated as the following:

DC gain:

$$A_0 = \frac{gm_1}{G_{o1}} \frac{gm_2}{G_{o2}} \quad (2.18)$$

The first pole:

$$P_1 = -\frac{\frac{G_{o1}}{C_c\left(\frac{gm_2}{G_{o2}}+1\right)+C_1}}{C_2 + \frac{C_c C_1}{C_c + C_1}} \quad (2.19)$$

The second pole:

$$P_2 = -\frac{\frac{gm_2 \frac{C_c}{C_c+C_1} + G_{o2}}{C_2 + \frac{C_c C_1}{C_c + C_1}}}{C_2 + \frac{C_c C_1}{C_c + C_1}} \quad (2.20)$$

The right-hand plane zero:

$$Z_1 = +\frac{gm_2}{C_c} \quad (2.21)$$

Intuitively,  $P_1$  and  $P_2$  can be understood easily. Due to the Miller effort, the effective capacitance at V1 node is much larger than that of  $C_c$ . The total capacitor associated with  $V_{out}$  node is  $C_2 + \frac{C_c C_1}{C_c + C_1}$  and the effective impedance of

$V_{out}$  is  $1/(gm_2 \frac{C_c}{C_c + C_1} + G_{o2})$ . Based on the above equations, by comparing the results with and without  $C_C$ , it is evident that the Miller compensation capacitor  $C_C$  moves the original first stage pole to a much lower frequency while moving the second stage pole to a much higher frequency. Hence, this compensation scheme can be categorized into the pole splitting compensation.

From the above equation, a right-half-plane (RHP) zero is introduced, which harms the system stability. To understand how the RHP zero is generated, a simplified second stage with the compensation capacitor is drawn in Figure 2.13.

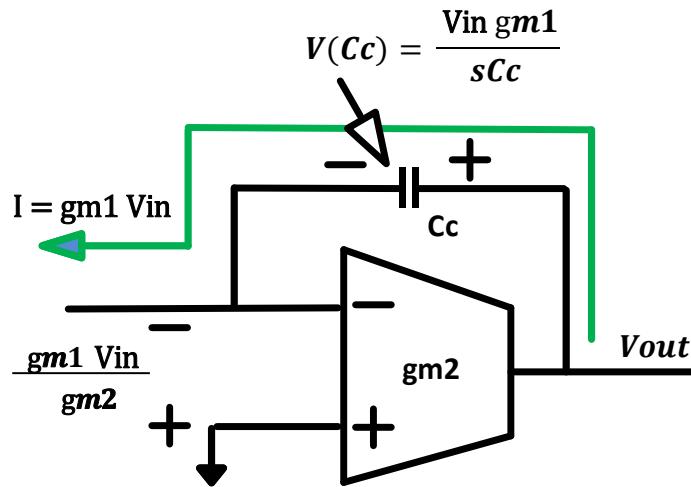


Figure 2.13 Signal flow for RHP zero analysis.

To simplify the analysis, the DC impedance is ignored. We assume the input current of this second stage is  $gm_1 V_{in}$ . For this current-controlled voltage source (transconductance amplifier), the ideal output voltage supposedly is  $gm_1 V_{in} / sCc$ . However, it is not the voltage that appeared at  $V_{out}$  since  $gm_2$  is infinite. Since all the current across  $C_C$  is also from this second stage transconductance ( $gm_2$ ), then the circuit output voltage is expressed as:

$$V_{out} = -\frac{gm_1 V_{in}}{gm_2} + \frac{gm_1 V_{in}}{sC_c} = gm_1 V_{in} \left( \frac{1}{sC_c} - \frac{1}{gm_2} \right) \quad (2.22)$$

From this equation and above circuit, it is obvious that an RHP zero appears. As shown in Figure 2.14, we can add an extra series resistor with the value of  $1/gm_2$ . The voltage across this series resistor cancels the input voltage of the second stage. And now  $V_{out}$  is the ideal voltage we expected, and the value is  $gm_1 V_{in}/sC_c$ . In this way, the RHP zero is removed. And the added resistor is called the nulling resistor. Also note that when the nulling resistor value is chosen to be larger than  $1/gm_2$ , the RHP zero is moved to LHP, which can be useful for the system stability. Figure 2.15 shows the traditional two-stage Miller-compensated amplifier with a nulling resistor.

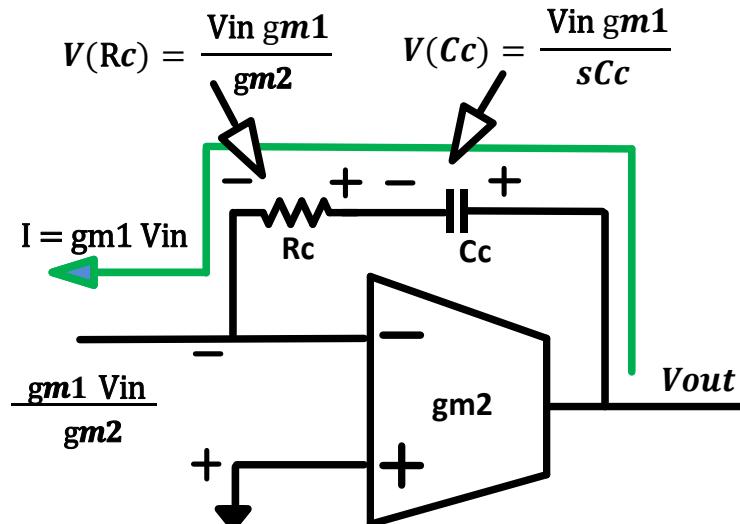


Figure 2.14 Signal flow for RHP zero cancelling nulling resistor analysis.

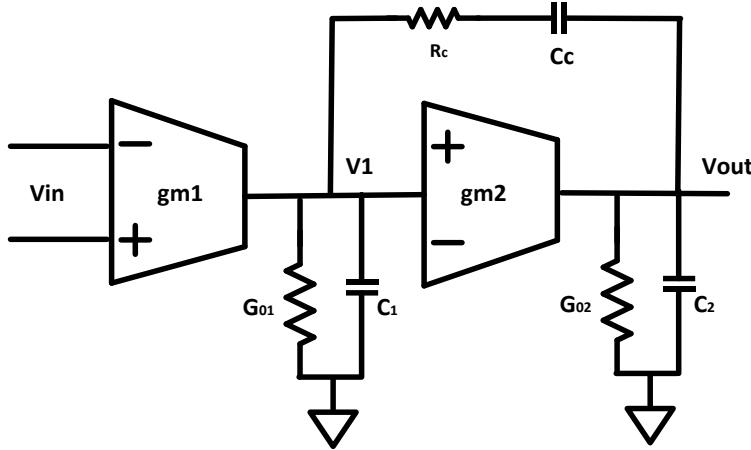


Figure 2.15 Miller compensation with nulling resistor.

However, adding the nulling resistor also introduces an extra pole, whose value is given by:

$$P_3 = -\frac{1}{R_c} \left( \frac{1}{C_c} + \frac{1}{C_1} + \frac{1}{C_2} \right) \quad (2.23)$$

Although adding nulling resistor with a value larger than  $1/gm2$  can move the RHP zero to LHP, the introduced extra pole also starts to come in and harms the system phase margin. The extreme case is that the nulling resistor is infinite so that the feedback path is “open”. There would be no more Miller effect for pole-splitting and all poles remain at the original location, making the system unstable.

## (2) Two-stage amplifier with Ahuja compensation

As shown in the above RHP zero analysis, the feed-forward path creates an RHP zero and introduces phase delay. If the feedback path can be kept while eliminating the feed-forward path, it would get the full benefit from Miller compensation. Therefore, Ahuja compensation is introduced with a better closed-loop power supply rejection and a higher unity-gain bandwidth [45], [46]. At the same time, it is suitable to drive heavy capacitive or resistive load [47], [48]. A

popular version of the Ahuja compensation circuitry is shown in Figure 2.16.

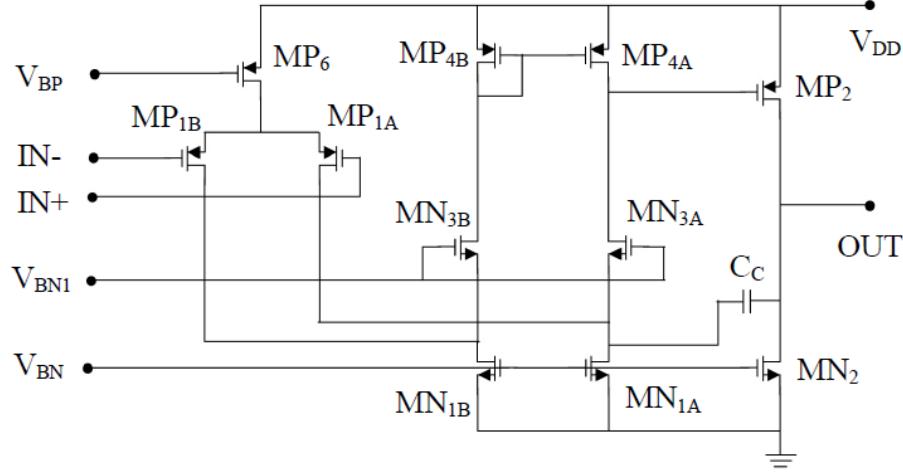


Figure 2.16 Typical amplifier structure with Ahuja compensation [48].

Since the compensation capacitor is connected to the source of MN<sub>3A</sub> in Ahuja compensation, we can see that the feed-forward path signal is heavily attenuated as compared to Miller compensation. Ahuja-compensated regulator also produces better performance of PSR than that of Miller-compensated regulator in high frequency range. For Miller compensation, C<sub>c</sub> creates a “short” from output to N1 in high frequency range, resulting in an AC “diode-connected” power FET driving the load, which causes PSR degradation. However, for Ahuja compensation, C<sub>c</sub> helps to improve regulator PSR by degrading PSR at N1 node.

The loop transfer function based on Figure 2.16 can be expressed as (2.24).

$$A(s) = \frac{A_0(1 + \frac{s}{Z_1})}{\left(1 + \frac{s}{P_1}\right)\left(\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n}s + 1\right)} \quad (2.24)$$

$$A_0 = g_{m1}g_{m2}r_1r_2; P_1 = -\frac{g_{m1}}{A_0 C_c}; Z_1 = -\frac{g_{m3}}{\sigma C_c} \quad (2.25)$$

$$\omega_n = \sqrt{\frac{g_{m2}g_{m3}}{\rho C_1 C_2}} ; \quad \xi = \frac{1}{2} \sqrt{\frac{C_1 g_{m3}}{\rho C_2 g_{m2}}} \left(1 + \frac{C_2}{C_c}\right) \quad (2.26)$$

Here

$$\sigma = 1 + \frac{C_3}{C_c} ; \quad \rho = 1 + \frac{C_3}{C_c} + \frac{C_3}{C_2} ; \quad \omega_o = \frac{g_{m1}}{C_c} \quad (2.27)$$

As compared to the Miller compensation loop, the Ahuja compensation loop itself is a second-order closed-loop system. As discussed, the closed-loop second-order system has very different behaviors with different design parameters, which could also affect the overall loop stability. For Ahuja compensation, the higher the  $gm_3$  value, the better the overall loop stability. The Figure 2.17 plots the AC loop analysis of Ahuja-compensated amplifier with the different  $gm_3$  values.

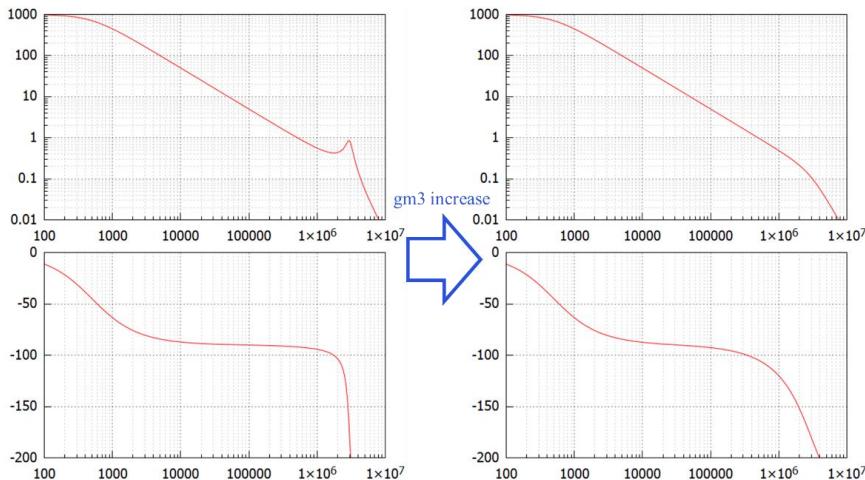


Figure 2.17 Simulated gain/phase plots for the Ahuja compensation circuit.

### 2.5.3. Multi-stage nested Miller compensation

Normally the error amplifier needs a high DC gain for good regulator line and load DC regulation. The high gain performance can be obtained by using three or more gain stage amplifier topology. However, an amplifier with three or more

stages cannot be easily compensated with traditional methods. The nested Miller compensation (NMC) is a straightforward and well-known technique for multistage high gain amplifier compensation, as shown in Figure 2.18 (take a 3-stage amplifier as the example) [49], [50], [51], [52]. There is a Miller capacitor across the final stage, and an additional Miller capacitor added for every added gain stage in the amplifier.

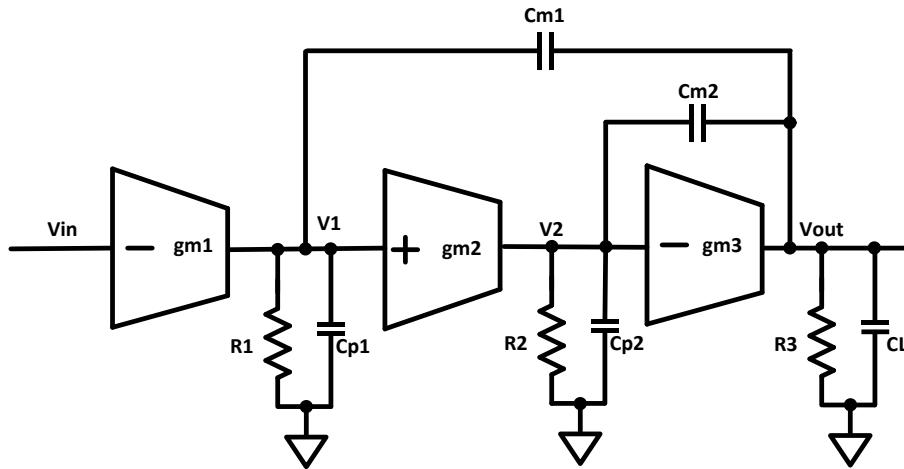


Figure 2.18 Structure of a three-stage NMC amplifier with the nested Miller compensation [49].

The overall small-signal transfer function can be derived with the following assumptions:

- (1)  $C_{m1}$ ,  $C_{m2}$ , and  $C_L$  are much larger than  $C_{p1}$  and  $C_{p2}$ .
- (2)  $gm_3 \gg gm_1$  and  $gm_2$ .

Ignoring the two zeros, the simplified transfer function is given by:

$$A_{v(NMC)}(s) = A_1(s) * A_2(s) = \frac{A_{dc}}{\left(1 + \frac{s}{p_{-3dB}}\right)} * \frac{1}{\left(1 + s \frac{C_{m2}}{gm_2} + \frac{s^2 C_L C_{m2}}{gm_2 gm_3}\right)} \quad (2.28)$$

where the overall DC gain and dominant pole are:

$$A_{dc} = g_{m1}g_{m2}g_{m3}R1R2R3 \quad (2.29)$$

$$P_{-3dB} = (C_{m1}g_{m2}g_{m3}R1R2R3)^{-1} \quad (2.30)$$

Re-writing the second-order expression at the denominator of  $A_2(s)$  with the standard form we have:

$$1 + 2\zeta \frac{s}{\omega_n} + \left(\frac{s}{\omega_n}\right)^2, \quad \omega_n = \sqrt{\frac{g_{m2}g_{m3}}{C_{m2}C_L}}, \quad \zeta = \frac{1}{2} \sqrt{\frac{g_{m3}C_{m2}}{g_{m2}C_L}} \quad (2.31)$$

The natural frequency of the second-order equation is between the second and third stage's unity-gain frequency. While the damping factor is decided by the ratio of the third and second stage's unity-gain frequency.

With the above well-known sub-system, we can get the bode-plot of the overall transfer-functions as shown in Figure 2.19.

From the plot, we can easily determine the stability requirement for NMC compensation based on the relationship between  $\omega_n$  and first stage unity-gain frequency  $\omega_o$ :

(a)  $\omega_n \ll \omega_o$ , there are two poles within the overall loop unity gain frequency and the system will not be stable. A dedicated zero is needed to be inserted and in most cases, the damping factor control design can also be adopted.

(b)  $\omega_n \sim \omega_o$ , with the natural frequency close to the overall loop unity-gain frequency, the overall stability is determined by the damping factor of this

second-order system. Typically,  $\zeta = \frac{1}{2} \sqrt{\frac{g_{m3}C_{m2}}{g_{m2}C_L}} \sim 0.7$ , with  $g_{m3}/C_L$  being two times of  $g_{m2}/C_{m2}$ .

(c)  $\omega_n \gg \omega_o$ , the system can be simplified to first-order single pole system.

Generally, the MNC will require:

$$\frac{g_{m3}}{C_L} > \frac{g_{m2}}{C_{m2}} > \frac{g_{m1}}{C_{m1}} \quad (2.32)$$

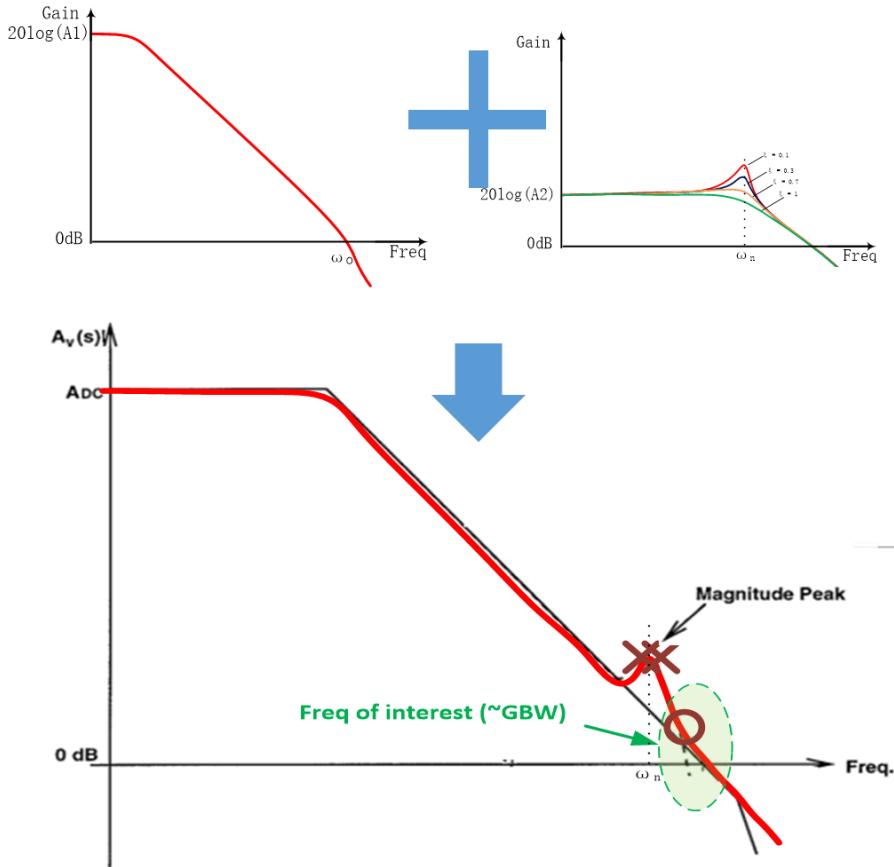


Figure 2.19 Bode plot of the nested Miller compensation loop.

This means that the unity gain frequency of the amplifier stage from right to left will decrease accordingly. The NMC compensated amplifier suffers from the bandwidth reduction and compensation capacitor area increase. There are many reported nested Miller compensation based topologies, such as MNMC [49],

NGCC [53]. Other reported papers [52], [54], [55] are also based on NMC topology with nulling resistor introduced. As analyzed above, adding a feedforward zero could be a good way of improving the bandwidth while still maintaining high DC gain. Figure 2.20 shows one example of an NMC with a feedforward compensation scheme called AFFC [56].

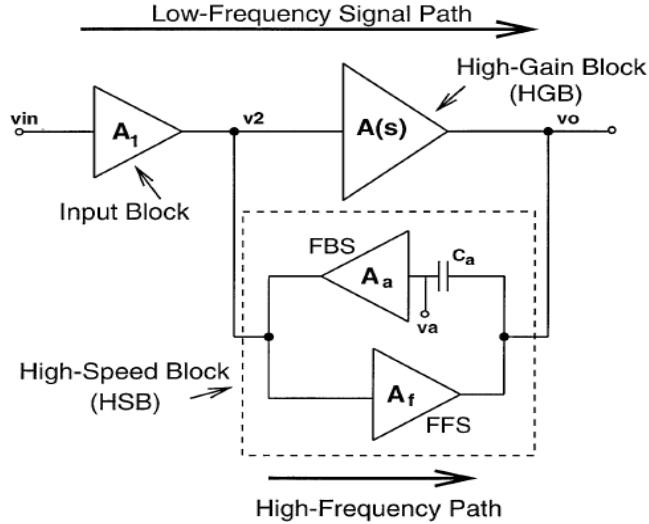


Figure 2.20 Basic structure of AFFC amplifier [56].

Here, the design consists of two paths: one is a high gain path (HGB) and another is a high-speed path (HSB). One can treat  $C_a$  and FBS as active feedback Miller compensation for NMC so that the RHP zero will be removed as compared to normal Miller compensation. The gain of FBS ( $A_a$ ) helps to reduce the capacitor size. The FFS helps to improve the bandwidth.

#### 2.5.4. Multi-stage feed forward compensation

The main drawback of NMC is the enormous current consumed to achieve the required bandwidth. And many capacitors used for NMC take large silicon area. The alternative way of achieving high DC or low-frequency gain is active

feedforward compensation. The simplified conceptual diagram is shown in Figure 2.21.

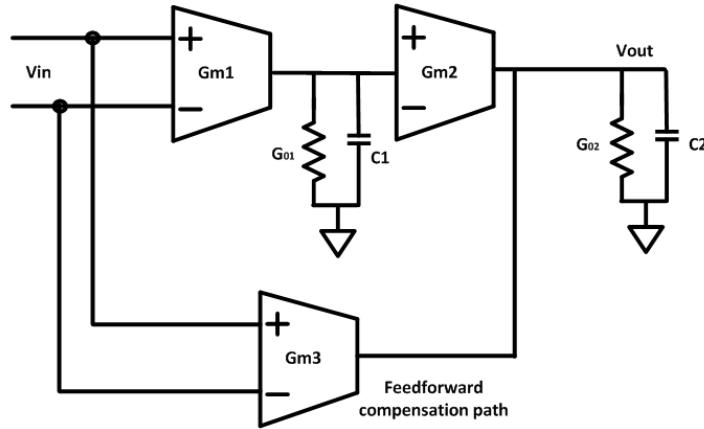


Figure 2.21 A circuit diagram of multi-stage feedforward compensation [57].

Here the overall DC gain is

$$A_0 = \frac{gm_3}{G_{02}} + \frac{gm_1 gm_2}{G_{01} G_{02}} \quad (2.33)$$

The overall transfer function is

$$\frac{V_{out}}{Vin} = \left( gm_3 + \frac{gm_1 gm_2}{G_{01} + sC_1} \right) \frac{1}{G_{02} + sC_2} \quad (2.34)$$

Define

$$\frac{V_{out}}{Vin} = \frac{A_0(1 - \frac{s}{Z_1})}{\left(1 - \frac{s}{P_1}\right)\left(1 - \frac{s}{P_2}\right)} \quad (2.35)$$

The corresponding pole and zero are:

$$P_1 = -\frac{G_{01}}{C_1}; P_2 = -\frac{G_{02}}{C_2}; \quad (2.36)$$

$$Z_1 = -\frac{gm_3 G_{01} + gm_1 gm_2}{gm_3 C_1} \approx -\frac{gm_1 gm_2}{gm_3 C_1}$$

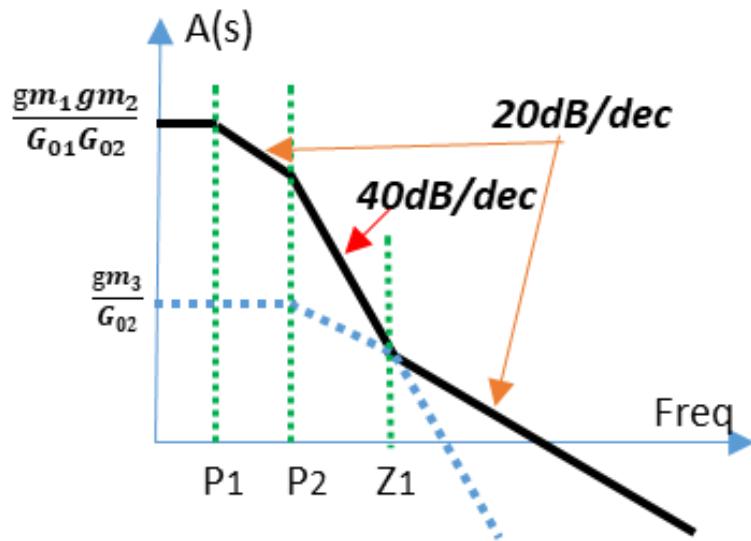


Figure 2.22 AC gain bode plot of feedforward compensated amplifier [57].

Figure 2.22 shows the AC gain plot of the feedforward compensated amplifier. From the above analysis, the DC gain and amplifier unity gain frequency are decoupled. The  $gm_3$  determines the “AC” response while the  $gm_1$  and  $gm_2$  decide the overall gain. They can be designed with low power consumption circuitry since they are supposed to be designed as “slow” as possible.

### 2.5.5. Internal zero compensation

The concept of internal zero compensation is by adding a zero inside the loop to cancel the load pole. The added zero tracks the circuit’s output stage pole, known as pole-zero tracking. The illustration of the idea is shown in Figure 2.23 [3], [58].

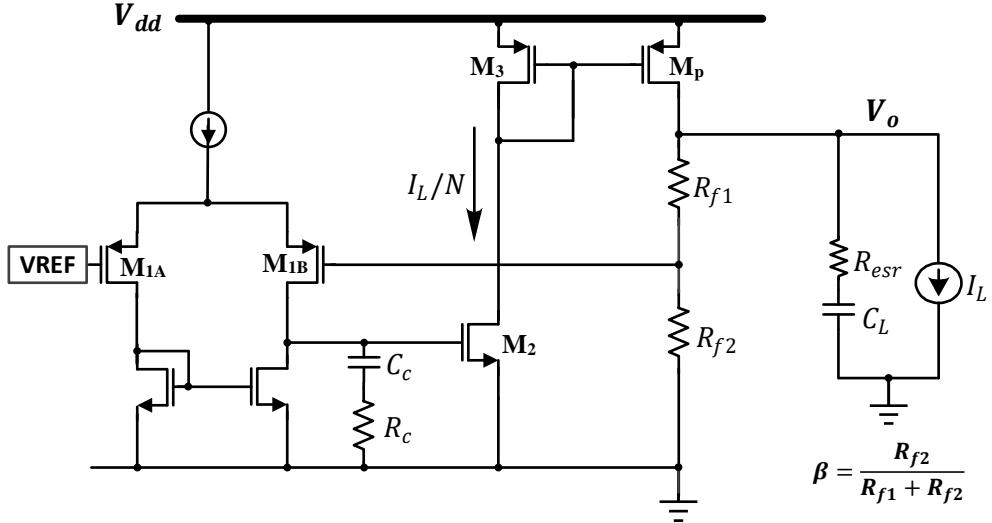


Figure 2.23 The structure of the LDO with internal zero compensation [3].

It is a three-stage amplifier design with three poles in the loop. Since the magnitude of the output pole is proportional to the load current, this inserted zero should track the load current. And it should be located between the second pole and the third pole. Otherwise, the loop cannot be stable over the entire loading range. In this example, the pole associated with the second stage ( $p_2$ ) is designed to be higher than the loop Unity Gain Frequency (UGF), and it tracks the load current since  $gm_3$  (the transconductance of  $M_3$ ) is proportional to  $\sqrt{I_L}$ .

$$\omega(p2) \approx \frac{gm_3}{C_p} \propto \sqrt{I_L} \quad (2.37)$$

The loop can be stable so long as the slope of the loop gain at the UGF is at 20dB per-Decade in the Bode plot, as shown in Figure 2.24.

From the bode plot, it is obvious that the loop unity gain frequency (UGF) is a function of transconductances of the error amplifier and power FET ( $gm_1$  and  $gm_p$ ), the gain of the second stage gain ( $A_{2nd} = gm_2 / gm_3$ ) and the feedback factor ( $\beta$ ).

$$\omega_o \approx \frac{\beta A_{2nd} g m_1 g m_p R_C}{C_L} \quad (2.38)$$

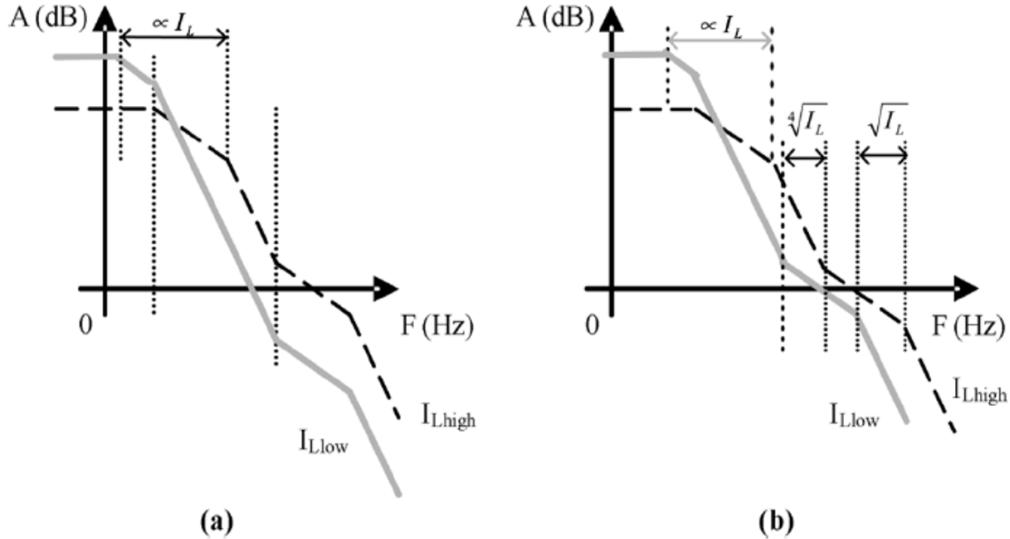


Figure 2.24 Different Bode diagrams. (a)  $\omega(z)$  is constant. (b)  $\omega(z)$  varies [3].

To have enough phase margin, the frequency of zero is typically designed to be 3 times lower than the UGF ( $\omega_o$ ).

$$\omega_z = \frac{\omega_o}{3} \quad (2.39)$$

This gives:

$$R_C = \sqrt[4]{\frac{3C_L}{C_C} \frac{\beta A_{2nd}}{g m_1 g m_p}} \propto \sqrt[4]{I_L} \quad (2.40)$$

It shows that the  $R_C$  needs to be a variable resistor with the resistance proportional to  $\sqrt[4]{I_L}$ . In practice, this can be implemented as depicted in Figure 2.25 for simplicity.

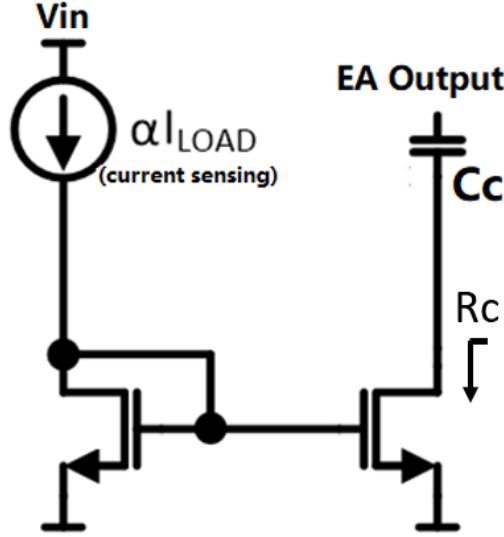


Figure 2.25 The circuit implementation of  $R_c$ .

## 2.6. Review of prior-art transient response enhancing techniques

The state-of-the-art LDOs with low quiescent current and fast transient performance can be found in recent publications [22], [3], [59], [60], [61], [62], [63], [16], [64], [38]. However, many of them find limitations in system-on-chip (SoC) battery-powered portable commercial applications, where the output load current can be 1 A or more with very stringent requirements on DC voltage variation and transient load current variations. Obviously, these LDOs usually show a poor transient line/load regulation performance with big undershoot and overshoot due to the lack of off-chip capacitor [65], [66], [67], [26]. In this thesis, we focus on the design of transient response enhanced LDO with the off-chip capacitor involved. This section reviews the transient performance enhancement techniques, which include (a) the adaptive biased super buffer design for LDO slew rate enhancement; (b) LDO design with PI/PID control technique for both frequency compensation and transient enhancement.

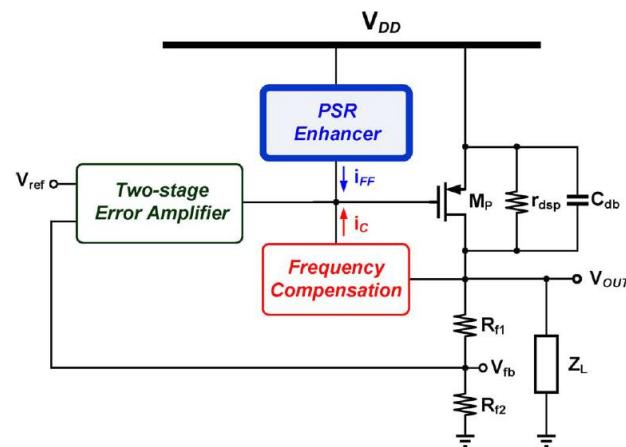
### 2.6.1. The LDO with a super buffer stage for slew rate enhancement

For an LDO design, the dynamic transient response not only relies on the output capacitor, but also depends on the loop bandwidth and the slew rate of the error amplifier.

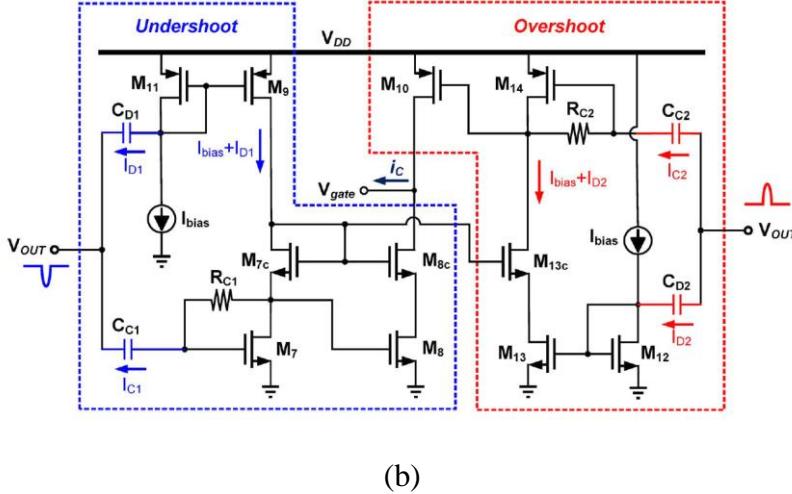
$$\Delta t = \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par} \frac{\Delta V}{I_{sr}} \quad (2.41)$$

$C_{par}$  is the LDO power transistor's gate capacitance. For high current rating LDOs, large power FET gate capacitance is always a concern, as it affects loop stability and slew rate. A buffer is widely used in LDO design to improve loop stability, slew rate and transient response [22].

The buffer's current bias tracks the output loading current with a wide loading dynamic range and enhances the slewing during high loading transients. Besides the slew rate, the undershoot and overshoot of LDO can also be improved by adding extra output voltage undershoot and overshoot detection circuit as shown below [31], [32], [68], [69], [70].



(a)



(b)

Figure 2.26 Slew rate enhancement circuitry [70].

The main idea is to directly sense the output voltage glitch before the loop responses and immediately apply the bias changes to the power transistor's gate.

### 2.6.2. LDO with PID control:

As shown in Equation (2.44), other than fast slew rate, a higher loop bandwidth is also required for LDOs to achieve fast transient response with small voltage glitch at loading current changes. To achieve a balanced speed (requires high bandwidth) and accuracy (requires a high DC loop gain), the multi-loop compensation scheme is used in many reported designs, which is also called PID control. In those design, a slow (I) voltage loop is dedicated for loop gain requirement, which contributes a main low-frequency pole. A fast response (P) loop is a wideband path with an equivalent zero that helps to extend the loop bandwidth. The D control is always together with the P loop to form a “bandpass” transfer function. It only senses the slope information of the LDO for loop AC response improvement. A block diagram of a PID controller in a feedback loop is shown in Figure 2.27.

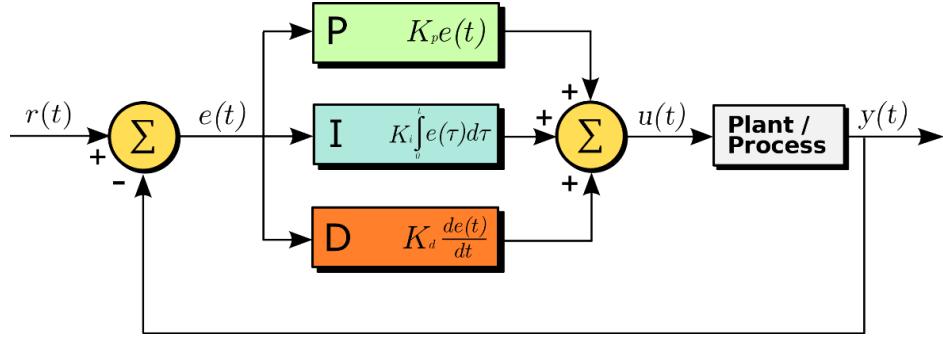


Figure 2.27 A block diagram of a PID controller in a feedback loop.

### 2.6.2.1. LDO with PI control:

Flip voltage follower (FVF) based LDO design is one of the design examples with PI control [67], [5], [71]. Figure 2.28 is a cap-less LDO (fully integrated) design based on FVF with full-spectrum power supply rejection.

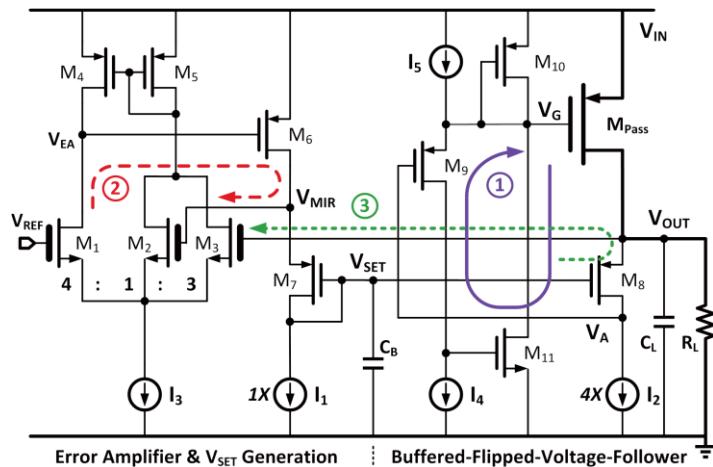


Figure 2.28 schematic of tri-loop FVF based LDO [5].

There are a total of 3 loops in this design, which serve different performance enhancement purposes. Loop 1 is an ultra-fast low gain loop with a very high bandwidth due to the introduced super source follower buffer. Loop 2 is designed to be a slow loop, which generates the  $V_{MIR}$  and  $V_{SET}$  voltage. Loop 3 is the overall voltage loop to improve DC accuracy.

### 2.6.2.2. LDO with derivative (D) control

As shown in Figure 2.27, a derivative path is a high-pass path, which contributes a zero in the overall transfer function. The high-pass path is sensitive to the high-frequency component of the feedback signal. An LDO with derivative (D) control is shown in Figure 2.29. The implementation example is shown in Figure 2.30.

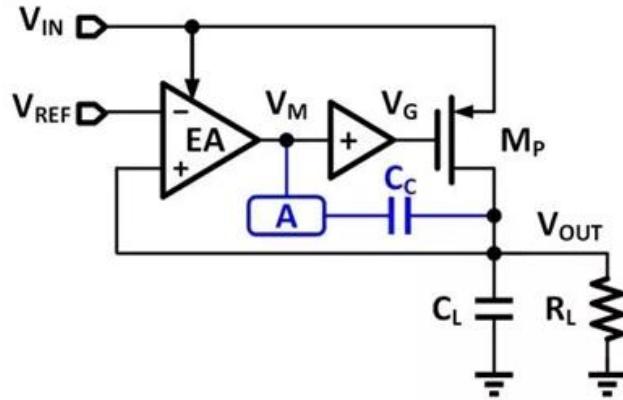


Figure 2.29 The diagram of LDO with derivative (D) control [72].

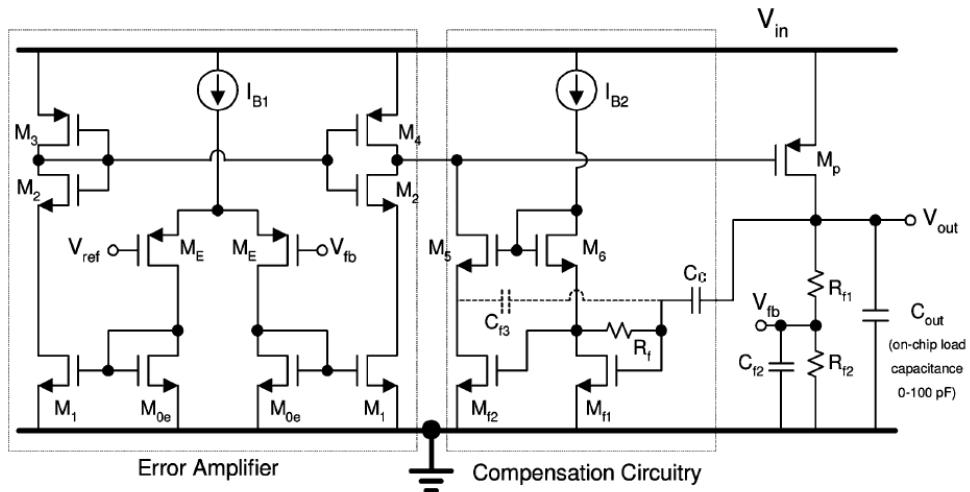


Figure 2.30 An implementation example of LDO with derivative (D) control [72].

A high-pass derivative (D) path obtains the slope information of the signal, and it represents a zero in the frequency domain. In other words, a high-pass

derivative (D) path responds only to fast-changing signals. A coupling capacitor  $C_c$  is a high-pass sensing capacitor.

It is important to note that the high-pass derivative (D) path is sensitive to high-frequency signals including noises. To reduce the influence of high-frequency noise on the loop, one or two high-frequency poles are always placed in the real LDO design. As a result, the high-pass has a band-pass transfer function.

The Miller capacitor has the effect of D-control as well. In fact, Miller compensation pushing the second-pole to higher frequency is the result of its high-pass nature. However, the gain of simple Miller compensation is small. Therefore, the effect of the D-control is not obvious.

## 2.7. Summary

In this chapter, we have reviewed key design parameters for LDO, including line/load regulation, power supply ripple rejection, and accuracy. Comprehensive analysis has been conducted to the loop compensation techniques. Since fast transient is becoming increasingly important for future LDOs and the design of fast transient LDO is challenging, we have reviewed state-of-the-art fast transient LDO embodying advanced fast transient techniques. A brief discussion of the pros and cons of the said techniques has also been presented.



## **Chapter 3**

### **A Low dropout regulator with rail-to-rail dynamic impedance attenuation buffer**

A large portion of this Chapter has been published in Microelectronics Journal [73].

In this chapter, a rail-to-rail high swing super source follower buffer (RRHS-SF) is proposed with the optimized minimum power FET size. To achieve a higher yield and more predictable performance, an accurate current sensing circuit is presented to generate the buffer's dynamic biasing. The designed LDO can deliver current from up to 600mA. In addition, a trim scheme with minor engineering cost is introduced to minimize input-referred DC offset.

This chapter is organized as follows. Section 3.1 presents the design of our proposed LDO and the design considerations. Section 3.2 presents the key contribution of the proposed LDO. The detailed circuit implementations and the loop analysis are described in Section 3.3. In the end, Section 3.4 draws the conclusions.

#### **3.1. Design of the proposed LDO**

A large power FET is needed for high current delivery capability. To avoid the low frequency pole formed by the power FET parasitic capacitor and the high impedance of the error amplifier output, a buffer stage is usually introduced. The most commonly used buffer is the single-stage source follower, which provides low impedance ( $1/g_m$ ) at the PMOS power FET gate with a pole of  $g_m/C_p$  (here

$C_p$  is the parasitic capacitance of the power FET). To push this pole to a frequency much higher than the LDO loop unity-gain frequency, the W/L ratio of the PMOS transistor and the DC biasing current have to increase.

A dynamic biased super source follower (DB-SSF) is introduced in [22] to act as a buffer to drive the PMOS FET as shown in Figure 3.1. The buffer current biasing will track the output loading current in a wide dynamic range and enhance the slewing during transient between the different loadings.

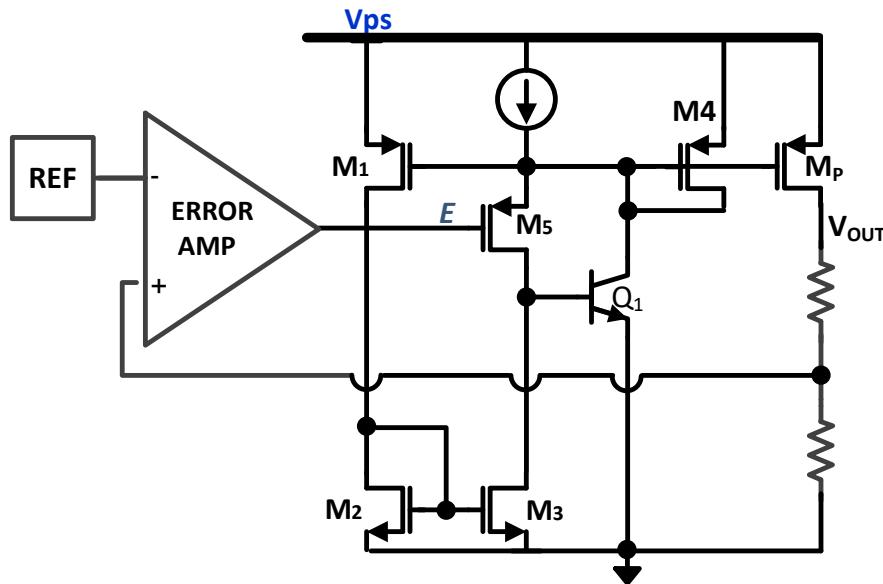


Figure 3.1 LDO with intermediate dynamically biased buffer [22].

However, DB-SSF might have some limitations during mass production. First of all, since the buffer is designed using PMOS source follower, the lowest buffer output voltage is around  $[V_{gs} + V_{dsat}]$ , which limits the overdrive of the power FET and does not utilize its maximum driving capability. Therefore, a larger PMOS power FET is necessary to deliver high current. This shows that the PMOS type buffer is not an optimized design for high current rating LDOs. The NMOS type buffer can maximize overdrive voltage for power FET, so that it is a better choice

where silicon area is a concern. A buffer with rail-to-rail swing can minimize the PMOS power transistor size.

Figure 3.2 shows the proposed high swing dynamic biasing super source follower buffer design with new current sensing circuit architecture. The bipolar Q1 (CMOS technology compatible, vertical NPN bipolar transistor) is designed as a feedback device connected in parallel with the buffer's output transistor. The buffer's impedance is reduced by  $(1 + \beta)$  times due to the shunt feedback ( $\beta$  is the current gain of the bipolar transistor Q1, it is around 15 in CMOS process). Hence, to achieve the required low impedance ( $R_o$ ), the DC biasing current can be  $(1 + \beta)$  time smaller than the normal source follower buffer and the size of the PMOS buffer can also be further reduced. Theoretically, the Q1 can be replaced by an NMOS transistor [5].

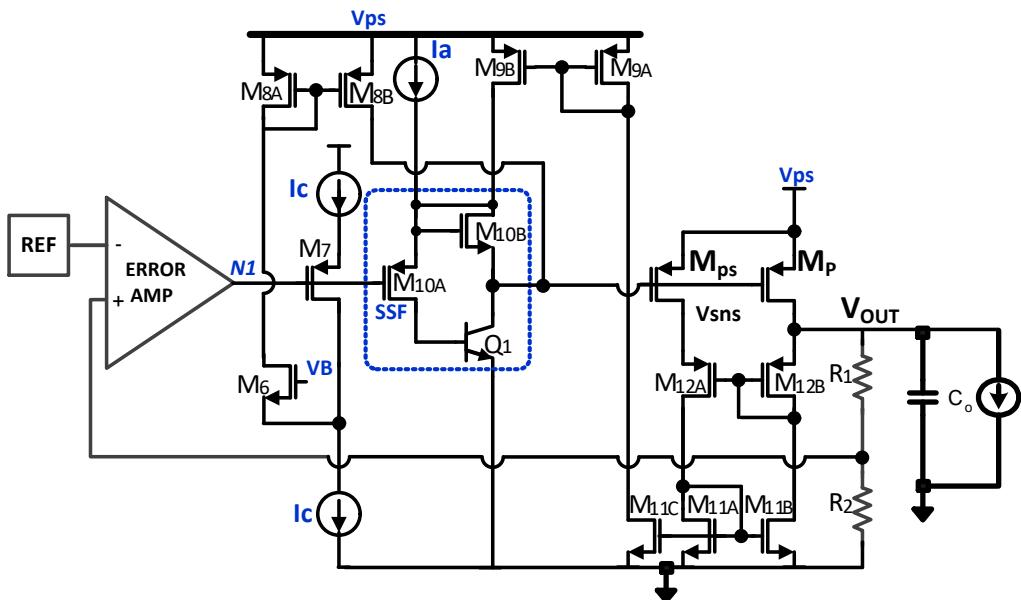


Figure 3.2 LDO with proposed high swing super source follower buffer with dynamic biasing.

The buffer drives the power FET from rail-to-rail with a variable biasing

according to LDO loading. As compared to the traditional PMOS super source follower, a new native NMOS device  $M_{10B}$  is inserted between buffer output and PMOS source, whose  $V_{gs}$  varies according to the LDO output load current. When the LDO is loaded with high current,  $M_{10B}$  will act as a DC level shifter and the buffer will drive the power FET gate with the voltage as low as 100mV, which gain extra  $\sim 600$ mV for power FET  $V_{gs}$  over-drive voltage as compared to the design with the normal p-type super source follower reported in [22]. Therefore, the PMOS power FET size is minimized. When the LDO's loading is small, the buffer biasing current will decrease. The  $V_{ds}$  of native NMOS devices  $M_{10B}$  will be close to zero, allowing the buffer's output voltage to rise close to the power rail. Here the load sensing circuit consists of  $M_{11A}$ ,  $M_{11B}$ ,  $M_{12A}$ ,  $M_{12B}$ ,  $M_p$ , and  $M_{ps}$ . The device  $M_{ps}$  is the main sensing FET, which is matched with the power FET ( $M_p$ ).

In this design,  $M_{11A}$  and  $M_{11B}$ ;  $M_{12A}$  and  $M_{12B}$  are designed with the same size.  $V_{sns}$  will be the same as  $V_{out}$ , such that current sensing accuracy is not affected by the transistor channel length modulation effect. In addition, the sensing clamping circuit only consists of a current mirror, as a result, a faster clamping response and smaller die area will be achieved as compared to the opamp based sensing clamping scheme. The RRHS-SSF is biased by the load sensing circuitry. The total current of the RRHS-SSF varies from  $6\mu A$  to  $600\mu A$  when the LDO's load current varies from 0 to  $600mA$ . Figure 3.3 shows the simulation results of RRHS-SSF local loop stability analysis. The local loop can be treated as a single-pole loop since NPN's base impedance is low. A minimum loop phase margin of  $68deg$  is achieved across all the bias conditions. With the total RRHS-SSF current varying from  $6\mu A$  to  $600\mu A$ , the loop's unity gain frequency varies from  $6MHz$

to 150MHz, which is much higher than the LDO loop unity gain frequency. The gate pole of LDO's power transistor will not affect LDO loop stability.

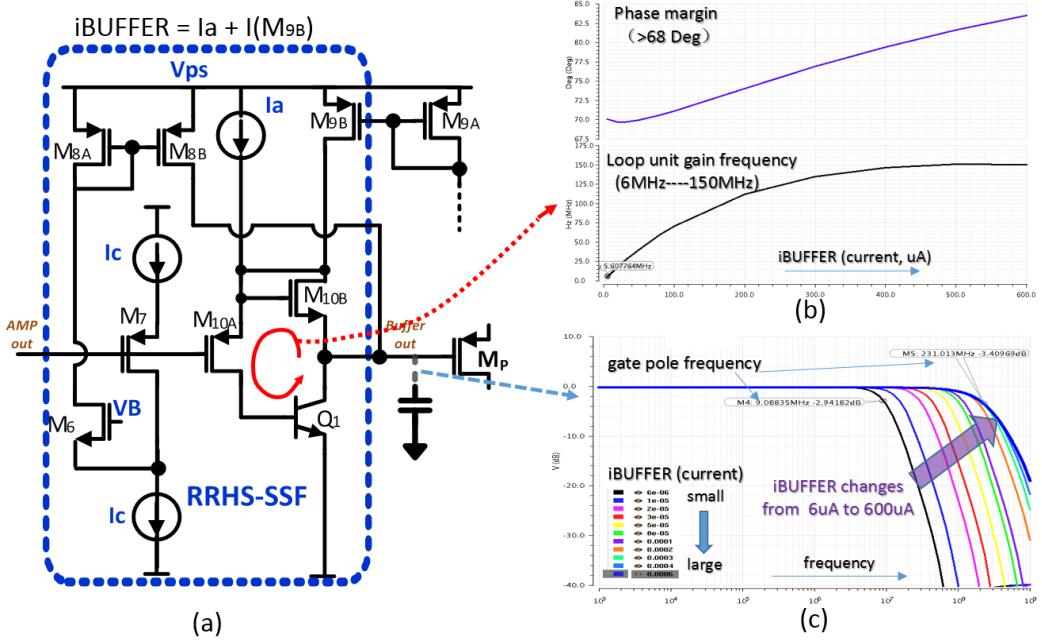


Figure 3.3 (a) The rail-to-rail high swing super source follower buffer (RRHS-SSF); (b) Local super source follower loop analysis; (c) Gate pole analysis.

Another concern for the LDO design is the leakage current which becomes more serious at high temperatures and at light load conditions. It is the source-drain current when PMOS is not properly turned off. For the high current rating LDO, the size of power FET is large so that its leakage current increases rapidly at fast process corners and at high temperature conditions. If the leakage is larger than the load current, the LDO will lose regulation and the output voltage will increase without loop control, which may cause the reliability issue of the load circuitry due to voltage stress. Considering that the power FET leakage current is a strong function of its source-gate voltage bias ( $V_{sg}$ ), to reduce the leakage,  $V_{sg}$  has to be close to zero or even negative for light load or no-load case.

Under light or no-load condition, the buffer should be designed to allow the

output voltage to reach the power rail for leakage reduction. In Figure 3.1, current sensing does not work in light or no-load condition. Although the M1 can sense the power FET leakage current, it is applied to M5's drain instead of its source. It will be much more difficult to get the buffer output voltage reaching the rail voltage ( $V_{ps}$ ). The  $I_a$  shown in Figure 3.3 (value:  $6\mu A$ ) should be designed high enough to pull up the buffer output voltage. At light load condition,  $M_{ps}$  still works as the current sensing for  $M_p$ , and the leakage current will still pass through  $M_{11A}$  to  $M_{9A}$  and mirror to  $M_{9B}$  to pull up the buffer output voltage. A simple circuit which consists of  $M_6$ ,  $M_7$ ,  $M_8$  will sense the light loading condition and help to pull the buffer output further closer to the power rail. In this way,  $I_a$  can be set small without losing the sensing accuracy even at the LDO light load condition. The proposed LDO design can turn off the power FET at no-load condition, enabling it to achieve a good load regulation specification over a wider range of process and temperature variations.

In short, the proposed buffer provides a low impedance node for the PMOS FET gate, so that its pole is located at sufficiently high frequency for all loading conditions. Considering that the biasing circuit is dynamic and works by sensing the load condition, the LDO current at light load condition is small so that good power efficiency is achieved. In addition, the proposed buffer with rail-to-rail swing also reduces the PMOS FET size and leakage.

### **3.2. Circuit implementation and analysis of the proposed LDO design**

As shown in Figure 3.4, the proposed super source follower buffer (RRHS-SSF) is inserted between these two stages to push the non-dominated pole introduced by the power FET to a frequency higher than the loop unity-gain bandwidth. A compensation scheme is designed to accommodate two major poles located at the error amplifier's output node N1 and the LDO output for stability consideration. The single-stage folded-cascode error amplifier ( $M_1—M_5$ ) in this design provides enough DC gain to meet the power supply rejection and the line regulation specification. It also provides enough output voltage swing for the dynamic requirements at high load condition. The second stage is the power PMOS FET in common-source configuration, whose gain varies with the LDO load condition. The single-stage folded-cascode structure error amplifier ( $M_1—M_5$ ) is shown in Figure 3.4, which provides enough DC gain for the whole loop. The off-chip loading capacitor used is in the micro-farad range.

In this design, the Ahuja (cascode-Miller) compensation is adopted for robustness concern. The Ahuja compensation capacitor splits the poles at both the error amplifier's output N1 and LDO output  $V_{out}$ . It also avoids the right-half-plane zero by removing the feed-forward path while keeping the feedback path, which is in favour as compared to the traditional Miller compensation [45]. The loop stability is thus achieved over the entire load range.

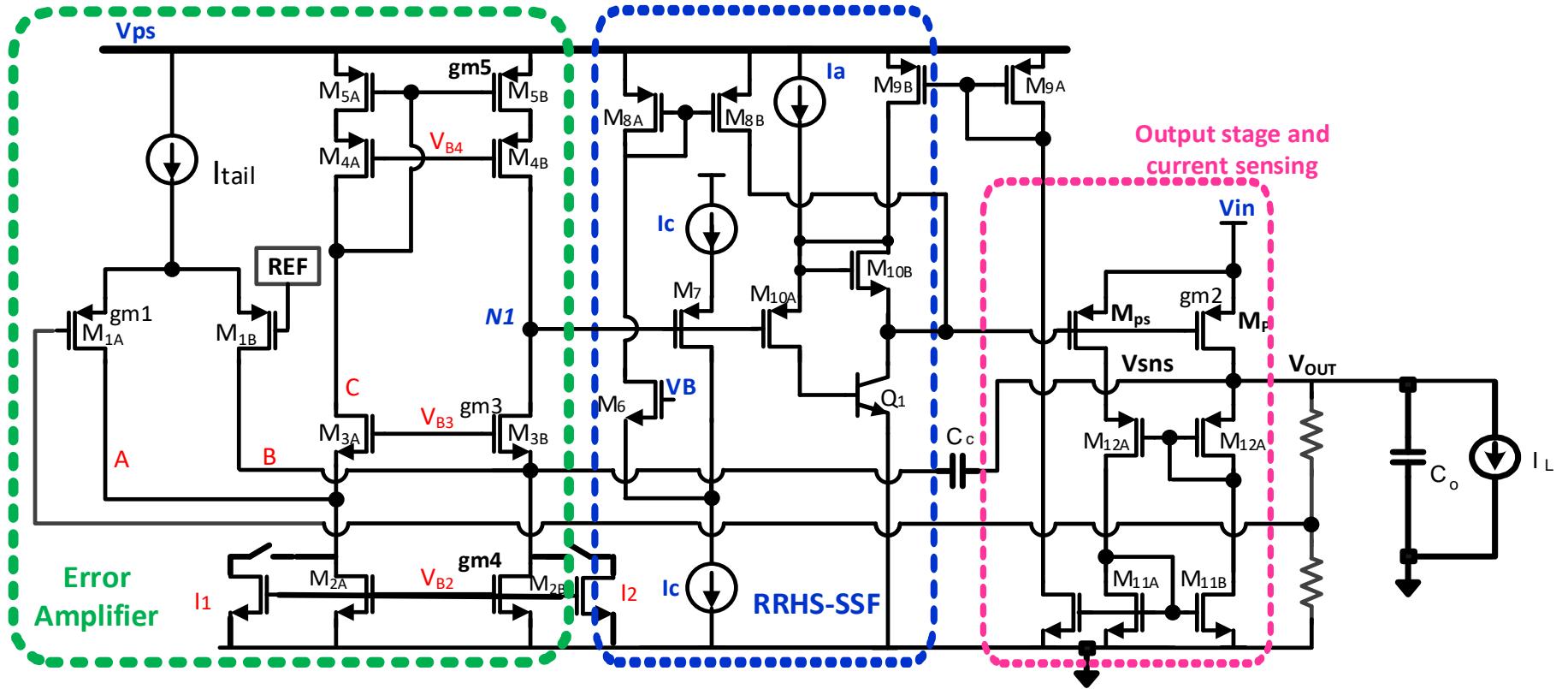
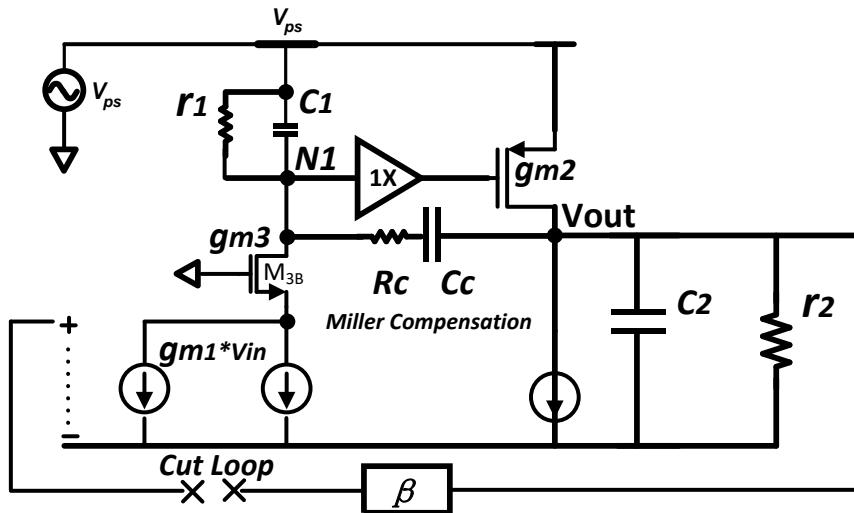


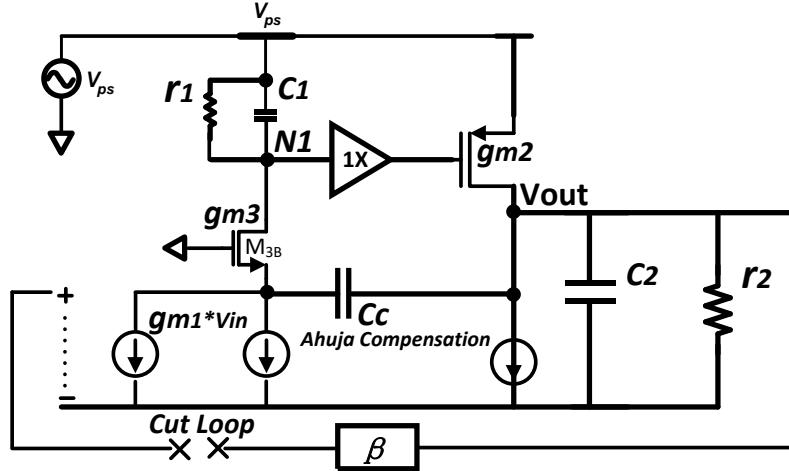
Figure 3.4 Schematic of the proposed LDO design.

### 3.2.1. Loop analysis of Miller and Ahuja compensation techniques

Figure 3.5 shows the simplified AC small-signal model of the LDO circuitry with both the Miller compensation scheme and the Ahuja compensation scheme. Here  $gm_1$ ,  $gm_2$ , and  $gm_3$  represent the transconductances of the input pair, the power FET and the cascode device  $M_{3B}$  respectively. The super source follower buffer pushes the pole introduced by the power FET gate to a higher frequency, and thus can be ignored for the simplicity of the loop analysis. We can understand the compensation scheme from both physics point of view and the mathematical derivation of the AC small-signal model. Both analysis can converge to the same conclusion.



(a) Miller compensation.



(b) Ahuja compensation.

Figure 3.5 AC small signal model for open loop circuitry.

The voltage swing at  $N1$  and  $M_{3B}$ 's source are  $V(N1) = gm_1 r_{out} V_{in}$  and  $V(M_{3B}) = gm_1/gm_3 V_{in}$  respectively. Since the impedance at node  $N1$  has:  $r_1 \gg 1/gm_3$ , it is obvious that voltage swing  $V(M_{3B})$  is much less than the voltage swing at node  $N1$ . Since the compensation capacitor is connected to  $V(M_{3B})$  for Ahuja compensation, it is clear that the feed-forward path signal is heavily attenuated by Ahuja compensation as compared to the normal Miller compensation. Ideally, if  $gm_3 \gg gm_1$ , there will be almost no signal directly passing through  $C_c$  to the output so that no right-hand plane zero appears. However, large  $gm_3$  required by Ahuja compensation will create the DC offset issue. It can be visualized intuitively that the Ahuja compensated regulator has better power supply rejection in the middle and high-frequency region as compared to the Miller compensated regulator. Power supply ripple rejection at low frequency is determined by the DC loop gain. Both Miller and Ahuja will show similar PSR provided DC loop gain is the same. At the middle or high frequency, for Miller compensation,  $C_c$  will create a “short” from output to  $N1$ , and an AC “diode-

connected” power FET will drive the load, both leading to PSR degradation. However, in the Ahuja compensation,  $C_c$  can help improve regulator PSR by degrading N1’s PSR. To have a better understanding of the above analysis, a mathematical model is derived below for both Miller and Ahuja compensation and a design guide is thus provided.

The loop transfer function and closed-loop power supply rejection for both the Miller compensated loop and the Ahuja compensated loop are derived. A comparison of these two loops is also shown. For mathematical derivation, symbols and assumptions are listed below.

(1)  $C_2 \gg C_c \gg C_1$

(2) Loop DC gain is  $A_0 = g_{m1}g_{m2}r_1r_2\beta$ , and  $\beta$  is the loop feedback factor.

(3)  $A_1(s)$  and  $A_2(s)$  are the open-loop transfer function of the Miller compensated loop and the Ahuja compensated loop respectively;  $A_{1ps}(s)$  and  $A_{2ps}(s)$  are their open-loop supply to the output transfer functions. Close loop power supply rejections are represented by  $PSR_1$  and  $PSR_2$ .

$$\begin{aligned}
 A_1(s) &= \frac{V_{out}(s)\beta}{V_{in}(s)} \\
 &= \frac{-\beta g_{m1}g_{m2}r_1r_2[s(R_c - \frac{1}{g_{m2}})C_c + 1]}{s^3C_1C_2C_cr_1r_2R_c + s^2C_2C_cr_1r_2\left(1 + \frac{C_1}{C_2} + \frac{C_1}{C_c}\right) + sg_{m2}r_1r_2C_c + 1} \\
 &\approx \frac{-A_0[s(R_c - \frac{1}{g_{m2}})C_c + 1]}{\left(s\frac{A_0C_c}{g_{m1}} + 1\right)\left(s\frac{C_2}{g_{m2}} + 1\right)\left(s\frac{C_1}{g_{m2}} + 1\right)} \quad (3.1)
 \end{aligned}$$

$$A_{1ps}(s) = \frac{V_{out}(s)}{V_{ps}(s)}$$

$$= \frac{s^2 C_1 C_2 r_1 r_2 + s g_{m2} r_1 r_2 C_c + 1}{s^3 C_1 C_2 C_c r_1 r_2 R_c + s^2 C_2 C_c r_1 r_2 \left(1 + \frac{C_1}{C_2} + \frac{C_1}{C_c}\right) + s g_{m2} r_1 r_2 C_c + 1} \quad (3.2)$$

$$PSR_1(s) = \frac{A_{1ps}(s)}{A_1(s)} = \frac{s^2 C_1 C_2 r_1 r_2 + s g_{m2} r_1 r_2 C_c + 1}{A_0 [s(R_c - \frac{1}{g_{m2}})C_c + 1]}$$

$$\approx \frac{\left(s \frac{A_0 C_c}{g_{m1}} + 1\right) \left(s \frac{C_1}{g_{m2}} + 1\right)}{A_0} \quad (3.3)$$

Here (3.1) is the open-loop transfer function of the Miller compensated loop, where the open-loop dominant pole is located at  $\frac{g_{m1}}{A_0 C_c}$ .  $R_c$  has to be carefully designed to track with power FET transconductance  $g_{m2}$  and move the RHP zero to LHP. For an LDO with a wide range of load conditions, a variable  $R_c$  is needed, as the second pole varies with  $g_{m2}$  due to the load variation. To avoid the third pole affecting the loop phase margin, the parasitic capacitor  $C_1$  at N1 should be designed as small as possible. The smaller the buffer size, the easier the loop stability design. The open-loop transfer-function of  $V_{out}(s)$  vs  $V_{ps}(s)$  is shown in (3.2). The LDO's PSR can be obtained by evaluating  $\frac{A_{1ps}(s)}{A_1(s)}$  (3.3) and it is plotted with a dash line in Figure 3.6. At frequencies below the open-loop dominant pole, the PSR is determined by loop DC gain. When frequency goes high, the PSR will degrade at the rate of 20dB/Dec. A lower frequency dominant pole helps to maintain loop stability while the PSR at the middle or high

frequency becomes worse. The trade-off between loop stability and PSR makes the Miller compensation scheme not as good a solution for the regulator design.

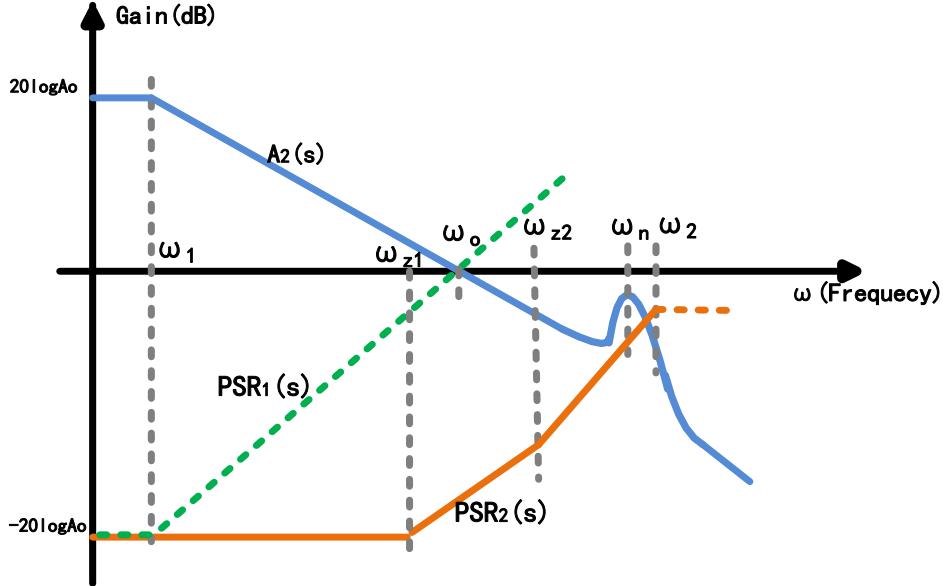


Figure 3.6 Plot of the LDO loop gain and the power supply rejection (PSR).

For the Ahuja compensated loop, the open-loop transfer function and PSR are derived.

$$\begin{aligned}
 A_2(s) &= \frac{V_{out}(s)*\beta}{V_{in}(s)} \\
 &= \frac{-\beta g_{m1}g_{m2}r_1r_2 \left( s^2 \frac{c_1 c_c}{g_{m2} g_{m3}} + s \frac{c_c}{g_{m2} g_{m3} r_1} - 1 \right)}{s^3 \frac{c_1 c_2 c_c r_1 r_2}{g_{m3}} + s^2 C_1 C_c r_1 r_2 \left( 1 + \frac{c_2}{c_c} \right) + s g_{m2} r_1 r_2 c_c + 1} \\
 &= \frac{-A_0 \left( s \sqrt{\frac{c_1 c_c}{g_{m2} g_{m3}}} + 1 \right) \left( s \sqrt{\frac{c_1 c_c}{g_{m2} g_{m3}}} - 1 \right)}{\left( s \frac{A_0 c_c}{g_{m1}} + 1 \right) \left( \frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n} s + 1 \right)} \quad (3.4)
 \end{aligned}$$

Where the natural frequency and damping factor are calculated as:

$$\omega_n = \sqrt{\frac{g_{m3}g_{m2}}{C_1C_2}}; \xi = \frac{1}{2}\sqrt{\frac{C_1g_{m3}}{C_2g_{m2}}}\left(1 + \frac{C_2}{C_c}\right) \quad (3.5)$$

$$A_{2ps}(s) = \frac{V_{out}(s)}{V_{ps}(s)}$$

$$= \frac{\left(s\frac{C_c}{g_{m3}} + 1\right)(sC_1r_1 + 1)}{s^3\frac{C_1C_2C_cr_1r_2}{g_{m3}} + s^2C_1C_cr_1r_2\left(1 + \frac{C_2}{C_c}\right) + sg_{m2}r_1r_2C_c + 1} \quad (3.6)$$

$$PSR_2(s) = \frac{A_{2ps}(s)}{A_2(s)} \approx \frac{\left(s\frac{C_c}{g_{m3}} + 1\right)(sC_1r_1 + 1)}{A_0\left(s\sqrt{\frac{C_1C_c}{g_{m2}g_{m3}}} + 1\right)\left(s\sqrt{\frac{C_1C_c}{g_{m2}g_{m3}}} - 1\right)} \quad (3.7)$$

Hence the poles of  $A_2(s)$  and  $PSR_2(s)$  are

$$\omega_o = \frac{g_{m1}}{C_c}; \omega_1 = \frac{g_{m1}}{A_0C_c}; \omega_2 = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_c}} \quad (3.8)$$

The zeros of  $A_2(s)$  and  $PSR_2(s)$  are:

$$\omega_{z1} = \frac{1}{r_1C_1}; \omega_{z2} = \frac{g_{m3}}{C_c} \quad (3.9)$$

Based on Figure 3.6, it is better to have [74]:

$$\omega_2 > \omega_n > \omega_{z1} > \omega_o > \omega_1 \quad (3.10)$$

From (3.4), it can be treated as a system consisting of a 1st order non-ideal

integrator (with exact transfer function from  $V_{in}$  to N1) in series with the Ahuja loop (the second-order term shown in the denominator). This Ahuja loop will create two conjugate poles above unity gain frequency, which creates a peaking of the loop gain amplitude at the natural frequency  $\omega_n$  as shown in Figure 3.6. The gain amplitude peaking is a function of the damping factor  $\xi$ . With proper design, a big damping factor can be achieved with a reasonable peaking without affecting loop stability. Based on the locations of the poles and zeros, the loop gain and power supply rejection (PSR) are plotted. It is obvious that the Ahuja compensated LDO has a better power supply rejection than the Miller compensated LDO since we can design to make  $\omega_{z1} > \omega_1$ .

It is clear to see that a smaller  $C_1$  helps to improve the LDO PSR performance. The proposed super source follower will not only push the power FET pole to a high frequency but also reduce  $C_1$  to achieve a better power supply rejection. Since the second-order effect is determined by the damping factor and the natural frequency, a higher  $\omega_n$  and  $\xi$  are required for a better loop phase margin. With  $\omega_n \gg \omega_o$  and  $\xi \approx 1$ , it has:

$$\sqrt{\frac{g_{m3}g_{m2}}{C_1C_2}} \gg \frac{g_{m1}}{C_c} \quad (3.11)$$

$$\xi \approx \frac{1}{2} \sqrt{\frac{C_1g_{m3}}{C_2g_{m2}}} \frac{C_2}{C_c} \approx 1 \quad (3.12)$$

Combining (3.11) and (3.12), we have:

$$\sqrt{\frac{g_{m3}g_{m2}}{C_1C_2}} \gg 2g_{m1} \sqrt{\frac{g_{m2}}{C_1C_2g_{m3}}} \quad (3.13)$$

Therefore,  $g_{m3} \gg g_{m1}$  is desired

A high quiescent current biased cascode branch is needed for the Ahuja compensation loop to achieve better loop stability. Since the LDO load current can vary from zero to 600mA,  $g_{m3} \sim 10 g_{m1}$  is chosen to meet the stability requirement across process corners and temperature variation. The current bias of the cascode branch is much higher than the input pair biasing. With this DC biasing condition, there is a risk of DC offset issue, which is also applicable to all the Ahuja related compensation schemes. Figure 3.7 shows the designed loop AC analysis plot for LDO light/full load conditions. The simulation condition is that the input voltage ( $V_{in}$ ) equals to 2V and the output voltage ( $V_{out}$ ) equals to 1.8V.

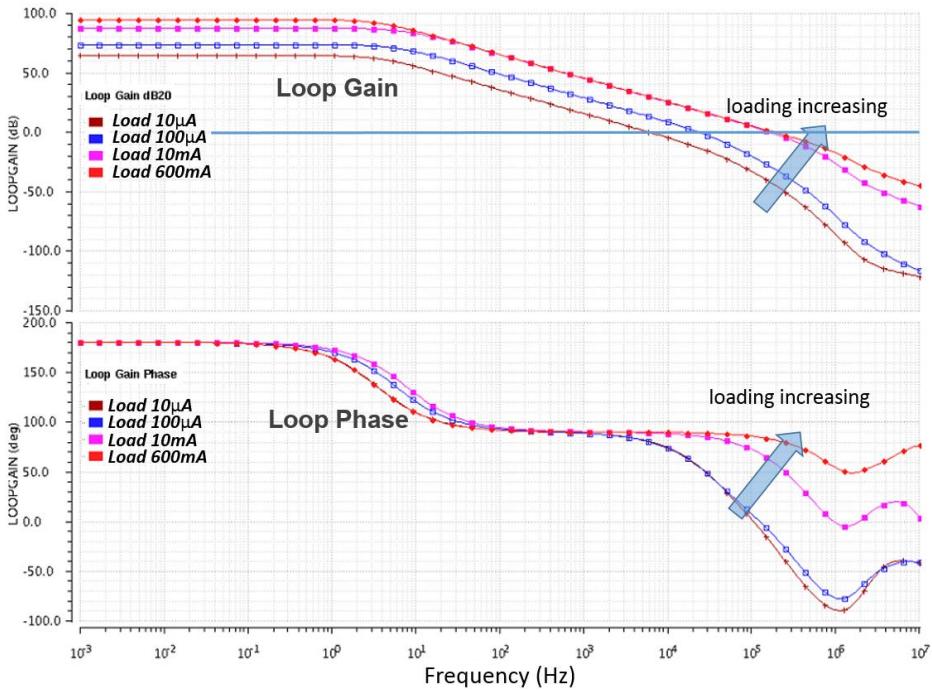


Figure 3.7 AC simulation results of the LDO loop response with different loading condition.

### 3.2.2. Offset analysis and the proposed solution for commercial design

Accuracy is another critical specification for the commercial LDO design, where the absolute output voltage accuracy, load and line regulation variation [9], [10]

are important. The absolute output voltage accuracy is determined by the error of reference voltage and the DC offset of the error amplifier in the LDO. The input-referred offset voltage can be shown by the formula below:

$$V_{os}(in) = \sqrt{(Vos_1)^2 + (Vos_2 * \frac{g_{m4}}{g_{m1}})^2 + (Vos_5 * \frac{g_{m5}}{g_{m1}})^2} \quad (3.14)$$

Here,  $Vos_1, Vos_2, Vos_5$  are the offset voltage of the input pair, the current mirror  $M_{2A}, M_{2B}$  and  $M_{5A}, M_{5B}$  respectively.

The Monte Carlo simulation was conducted and the offset distribution for the LDO is shown in Figure 3.8. The LDO output voltage can vary from 1.77V to 1.83V without trim.

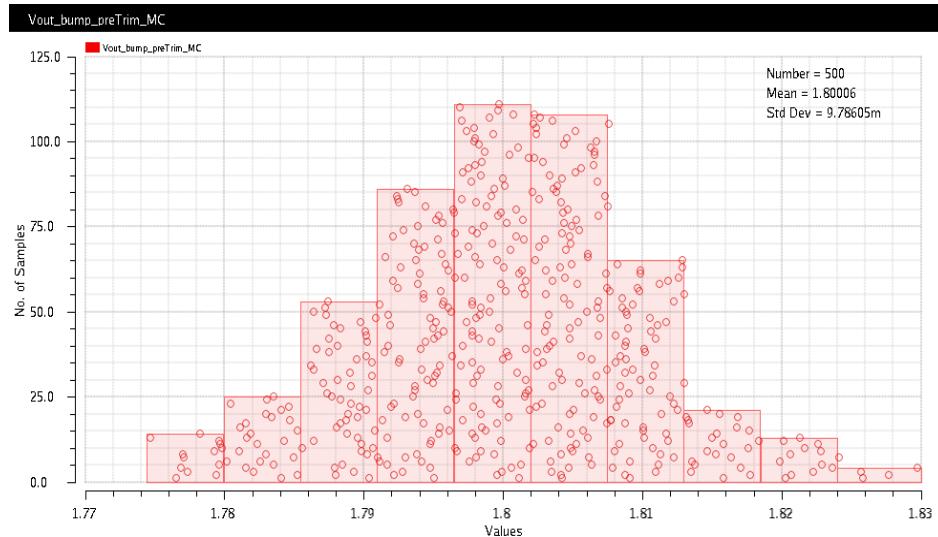


Figure 3.8 LDO offset Monte Carlo simulation results.

An LDO with smaller offset normally can be easily trimmed. However, if the LDO's offset is too large, the LDO may potentially run into a real risk: when  $I_{tail} <$  the mismatched current of the cascode branch, the LDO will lose regulation, which is considered a yield loss in commercial design. Normally there are many

LDOs integrated into a single chip if any of the LDO runs into such condition, the whole chip will be screened out in the production test stage. Even if it does not totally lose regulation, the performance is heavily affected since the overall DC gain drops, which causes line/load regulation issues. Unfortunately, this cannot be detected by production testing and the performance degradation can only be verified in the lab bench. Hence, a trimming scheme is proposed to overcome such an issue.

Figure 3.9 shows the diagram of the proposed trim scheme. Since one commercial chip would integrate many LDOs, the cost of test time will also be taken into consideration. From the previous analysis, when the Ahuja compensation is applied to such a wide load range LDO design, the added two small DACs play critical roles in the production.

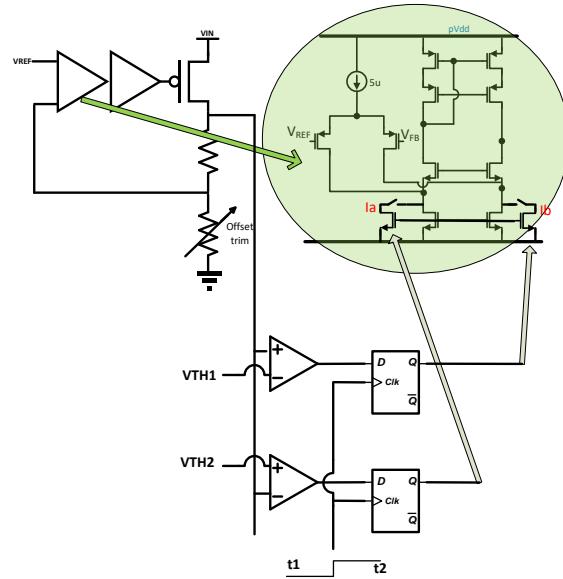


Figure 3.9 Block diagram of the offset trim scheme.

As shown in Figure 3.9 and Figure 3.4, two NMOS current sinks  $I_1$  and  $I_2$  are introduced for offset compensation. Their on or off states are determined by the LDO output offset sign and value, which is detected by the trim engine. The

input-referred compensated DC offset voltage from the current sink is  $I_2/g_{m1}$ , ( $I_1/g_{m1}$ ).  $I_1$  and  $I_2$  can be designed with the multi-bit DAC for a wider trim range. Considering the trade-off between the silicon performance and the production trim cost, one-bit offset DAC design might be a better choice, which will be woken up only when the LDO's offset voltage is larger than a certain threshold. As long as the LDO's intrinsic offset is smaller than the threshold, the LDO accuracy can be achieved by the feedback resistor trim. If we design the threshold such that 90% of the LDO's intrinsic offset is smaller than the threshold, then the total extra trim cost could only be only ~1% more as compared to resistor ladder trim alone. There is a trade-off between the trim coverage and the trim time as well. As shown in Figure 3.9, only when any of the LDOs in the chip has an offset bigger than the threshold, the DAC is wakened, and the trim will add extra adjusting steps. If all the LDOs are within the offset threshold, no extra trim steps will be introduced. Therefore, the overall trim cost is still acceptable.

### 3.3. Hardware measurements of the proposed LDO

The proposed design is fabricated in the 0.18- $\mu\text{m}$  HVCmos process. Figure 3.10 shows the die photo of the proposed LDO with the rated output current of 600mA. The LDO is designed with features such as short to ground protection, overcurrent protection, and soft slow start, etc. The die area of this LDO is 0.137 mm<sup>2</sup> (excluding PAD and ESD). The LDO's minimum input voltage is 2.2V and the maximum output voltage is 2V. The output voltage can be programmed down to 0.7V with a programmable step size. An on-chip bandgap is used as its reference input, and the output of the LDO voltage is adjusted by the feedback resistor, which is designed to cover the LDO output voltage programmable range

and offset trim range as well.



Figure 3.10 The die photo of the proposed LDO.

In worse case condition when the input voltage ( $V_{in}$ ) is 2.2V and the output voltage ( $V_{out}$ ) is 2V, the LDO should still deliver 600mA load current for all the corners, where the LDO dropout voltage is 200mV and the output capacitor is 1 $\mu$ F. Figure 3.11 shows the measured quiescent current for different loading conditions. The quiescent current is 40 $\mu$ A, while in full load condition (600mA), the LDO current reaches 900 $\mu$ A. The increased current is used to lower down the buffer impedance for the intermediate stage buffer dynamic biasing. The corresponding worst-case current efficiency of the LDO is 99.9%. The typical and worst-case line regulation is  $+/-0.07\% / V$  and  $+/-0.2\% / V$  respectively. The load regulation specification is  $+/-1\%$  referring to the mid-point load. With this dynamic biasing buffer technique, the simple Ahuja compensation scheme is used for better stability, which gives the well-behaved transient response as shown in Figure 3.11. When the LDO is tested with a step from light load to full load condition and from full load to light load condition, it has a 60mV (overshoot) / 55mV (undershoot) output voltage variation, which includes the load regulation error of 35mV. The 60mV is translated to 3% of the output voltage as the

overshoot/undershoot specification. The load regulation is also reflected in Figure 3.11. Loading change of 600mA causes 35mV output voltage shift, which translates to a 2% load regulation error.

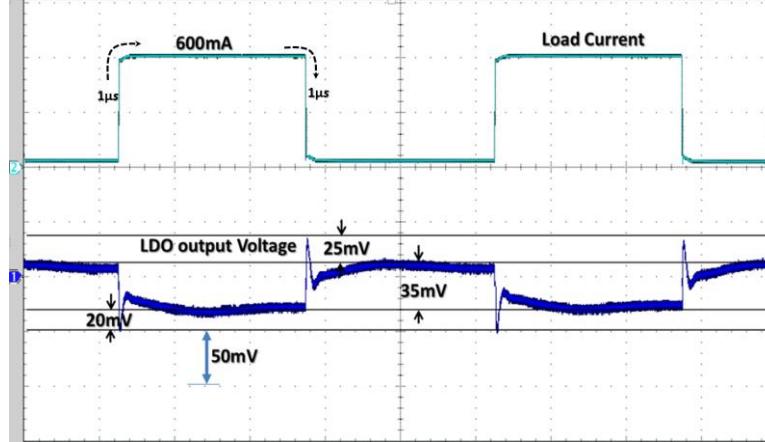


Figure 3.11 Measured load transient response of the proposed LDO( load step between 1mA and 600mA).

Figure 3.12 shows the measured power-rejection-ratio (PSR). The proposed LDO regulator can achieve a PSR of -35dB at 100 kHz with a loading of 300mA.

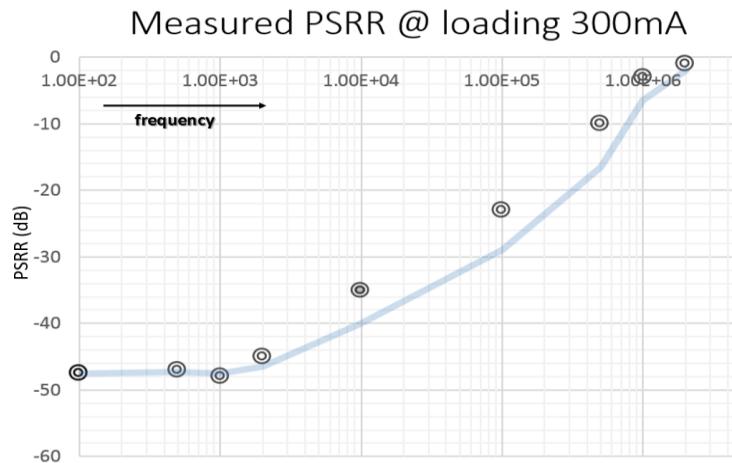


Figure 3.12 Measured PSR performance with 300mA load.

### 3.4. Conclusions

In this chapter, an LDO for portable applications with a dynamic biasing full swing impedance-attenuation buffer has been presented. The introduced DC

offset trimming method could increase the production yield with negligible cost.

With this dynamic biasing impedance-attenuation buffer and the Ahuja compensation scheme, the loop is stable over the entire load range from zero to 600mA with good transient response. The LDO can deliver as high as 600mA with a 200mV dropout voltage.

## **Chapter 4**

### **A 600mA fast-transient PMOS low-dropout regulator with pseudo-ESR technique**

A large portion of this chapter has been published in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems [75].

A dual-loop compensated fast-transient LDO has been proposed for battery-powered applications. It is successfully implemented in 0.18  $\mu\text{m}$  CMOS process with a total silicon area of  $210\mu\text{m} \times 593\mu\text{m}$ . The proposed LDO is composed of two feedback loops. The fast feedback loop (FFL) employs a direct output voltage spike detection through a capacitive coupling resulting in a significantly improved large-signal transient response and loop bandwidth at the same time. Its voltage spike is 15mV at a load step of 600mA. The proposed LDO has a  $30\mu\text{A}$  quiescent current and a loop bandwidth of 2.3MHz at a load current of 600mA. A power transistor with the pseudo equivalent series resistor (ESR) technique is proposed for loop stability improvement. It enables the usage of the low-cost multi-layer ceramic capacitor in mobile applications. The constant biased voltage feedback loop (VFL) has a loop gain of more than 60dB over all load conditions, which enables a good line and load regulation.

This chapter is organized as follows: Section 4.1 is the introduction. Section 4.2 describes the concept and working principle of the proposed LDO. The detailed circuit implementations and the loop stability analysis are described in Section 4.3. Section 4.4 discusses the experiment results and key parameter comparison. In the end, the conclusions are drawn in Section 4.5.

## 4.1. Introduction

The capacitor-based LDO is indispensable for various noise-sensitive or supply level-sensitive modules (e.g. camera, Double DataRate (DDR) memory, etc.) in mobile devices [2], [3], [27]. These modules are becoming increasingly power-hungry and their dynamic current profile often contains a fast-transient component because the modern mobile emphasizes large scale integration of multi-function and fast operation speed. The LDO for these modules needs to provide a well-regulated supply voltage with small output variation, small overshoot and undershoot despite the heavy load current and fast load transients. For example, DDR memory can draw a few hundreds of mA load current with a load transient of 300mA/100ns and it requires a robust power supply voltage with less than 1% variation.

The design of LDO for large load current dynamic is challenging for the following primary reasons.

1. The overshoot and undershoot of the LDO output may be unacceptably high during fast load transients. A preliminary analysis is as follows [9]:

$$\Delta V_o = \frac{\Delta I_L T_r}{C_L} + R_{esr} \Delta I_L \quad (4.1)$$

$$T_r \approx \frac{1}{BW_{cl}} + \frac{C_{par} \Delta V_g}{I_{sr}} \quad (4.2)$$

where  $\Delta V_g$  is the voltage variation across the pass transistor's gate parasitic capacitor,  $I_{sr}$  is the slewing current charging and discharging the gate parasitic capacitor ( $C_{par}$ ), and  $BW_{cl}$  is the close loop unity-gain bandwidth

of the LDO. From (1), the LDO output overshoot or undershoot  $\Delta V_o$  is largely proportional to  $\Delta I_L$ . In order to achieve a small  $\Delta V_o$ , the LDO needs to be designed with small  $T_r$  and/or large  $C_L$ , [9], [38], [76], [77]. However, these two solutions are arguably impractical for modern mobiles because the former typically relies on the large power dissipation of the LDO, and the latter causes undesirable increase in device form factor [77], [78], [22], [21].

2. Both low-frequency poles at the error amplifier's output and the LDO's output degrade the loop stability. The equivalent series resistance (ESR) compensation technique is used to stabilize the regulation loop [76], [79], [80]. It is worth noting that the stability issue is further exacerbated due to the utilization of the low-cost Multi-Layer Ceramic Capacitor (MLCC) output capacitor in mobile applications. The ESR of MLCC is generally small. Consequently, the intrinsic zero of the output capacitor (typically facilitates loop stability) is at high frequency. Therefore, the conventional output capacitor ESR zero compensation technique would not be appropriate for LDO with MLCC.
3. Load regulation and line regulation are deteriorated in heavy load conditions. This is largely due to the substantially reduced loop gain under a heavy load condition, particularly when the error amplifier is biased adaptively.
4. The circuit complexity is typically adversely increased. Complex auxiliary circuit blocks are often augmented to accommodate the wide load current range and fast load transients. The circuit complexity is a practical design consideration for real production [3]. For example, a parallel-connected

circuit at error amplifier output for transient performance enhancement will potentially increase the LDO input-referred offset, which may involve extra trim cost in real production.

## 4.2. The proposed LDO architecture

To improve the transient response, the dynamic/adaptive biasing and multi-loop schemes are employed in recent LDO designs to achieve a better transient response performance without sacrificing the overall power efficiency [22], [39], [81], [82], [83]. For the adaptive biasing scheme, the DC loop gain drops when the load current increases. A single-stage error amplifier may not be able to meet the DC loop gain requirement at a heavy load current condition. The multistage amplifier is used for the gain enhancement, which complicates the design of the compensation circuit for loop stability. The proposed new LDO design uses the dynamic biasing scheme as shown in Figure 4.1.  $C_f$  senses the LDO's output current and adjusts the error amplifier's biasing current dynamically. Both slew rate and loop bandwidth are enhanced, and the DC loop gain is not affected. The output voltage spike detection can be internal or external. The direct detection at the output node will be faster due to less propagation delay [82], [84], [85]. The architecture is based on the Dual Loop Compensation technique (DLC). It includes two feedback loops: one is outer slow response Voltage Feedback Loop (VFL), which consists of a resistive voltage divider composed of  $R_{f1}$  and  $R_{f2}$ , an error amplifier, a voltage buffer and a power pass transistor. Another is the inner Fast-response Feedback Loop (FFL), which consists of a differentiator based output voltage spike detector, a voltage buffer and a power pass transistor. The capacitor coupling based output voltage spike detector injects an output-

dependent current to the error amplifier's output for slew rate enhancement and loop bandwidth extension.

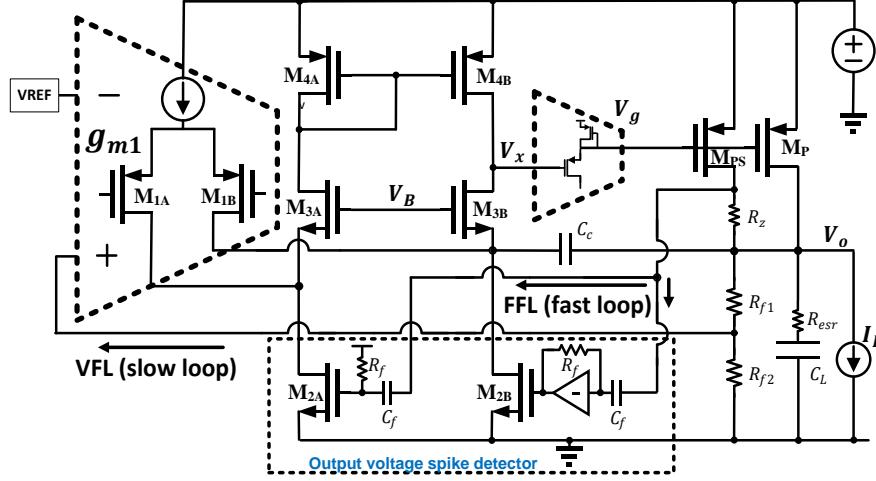


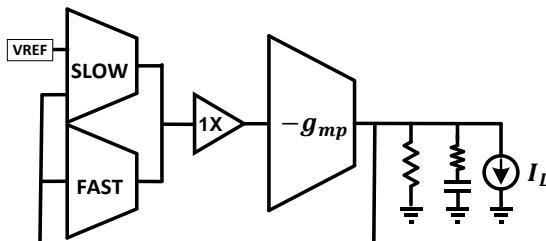
Figure 4.1 System architecture of the proposed LDO.

The capacitor coupling technique has been used for various purposes [61], [86]. In [61], the capacitor coupler senses the error amplifier's output (equivalent to  $V_x$  node in Figure 4.1) to expedite the transient. However, the long delay of the error amplifier may limit the effectiveness of this technique. In [86], capacitor couplings are implemented in both the input reference voltage node and the output node to facilitate the dynamic voltage scaling tracking. A separate push-pull transient enhancement loop is utilized for transient performance improvement. In this work, we propose an approach that compensates loop stability and improves transient response concurrently. We reuse the error amplifier's biasing circuit as the signal feedback path. Hence, the DC bias of the error amplifier does not drop when the load current increases compared to those adaptive biased error amplifiers. This makes the LDO loop gain high even when LDO is in heavy load condition. The high DC gain of the error amplifier enables better line regulation and load regulation even when the pass power transistor

works in the linear region for smaller dropout voltage, which results in a smaller silicon area [19], [87]. Additionally, since the DC bias of the error amplifier is consistent, the LDO's input-referred offset is not impacted by the load current neither. The Miller capacitor is connected between the output of the LDO and the output of the error amplifier. The capacitor value is chosen such that the bandwidth of VFL is much smaller than the bandwidth of FFL, and its value can be designed smaller than that in the conventional Miller or cascode compensated LDO. A voltage buffer inserted between the error amplifier and pass power transistor is designed with low output impedance. The voltage buffer is a PMOS super source follower, which is the same design as [22]. Hence, the frequency of the pole at the pass transistor's gate is much higher than Unity-Gain Frequency (UGF).

#### 4.2.1. Conceptual stability analysis for dual loop compensation

With the pole-splitting compensation technique, the pole at the LDO output node is usually a non-dominant pole, which is in the order of  $g_{mp}/C_L$  [45], [17]. The UGF will be decided by  $g_{m1}/C_c$  typically, and it should be designed to be smaller than  $g_{mp}/C_L$  for stability concerns. This limits the transient response performance. Hence, the DLC is adopted in this design for bandwidth extension and transient response improvement.



(a)

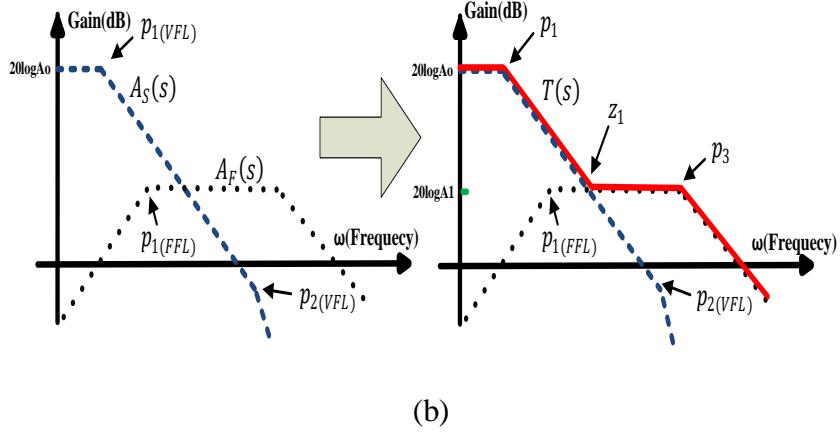


Figure 4.2 (a) Conceptual diagram of the dual loop compensation. (b) Bode plot sketch of the dual loop compensation.

The DLC can be conceptually described in Figure 4.2(a). The proposed design has two loops: the VFL provides a high-precision regulation for the LDO and the fast response FFL provides the fast response to the load changes. At light load conditions, both the VFL and FFL will determine the overall loop stability. At medium to heavy loads, the loop stability is determined by the FFL only, and the VFL has little impact on loop stability. In Figure 4.2(b),  $A_S(s)$  is the loop transfer function of the VFL, which is similar to the loop transfer function of the conventional cascode compensated LDO [22]. The dominant pole ( $p_1$ ) is located at low frequency due to the Miller effect. The inner FFL's transfer function is denoted as  $A_F(s)$ , which is a bandpass function. It determines the overall loop stability and the UGF of the LDO. Since the VFL and the FFL sum at the error amplifier output in parallel, the overall loop transfer function  $T(s)$  can be obtained as shown in Figure 4.2(b). A zero  $z_1$  is located at the frequency where the VFL gain is equal to the FFL gain in magnitude since the two loops are summed together in parallel. At a frequency higher than  $z_1$ , the FFL gain is higher than the VFL gain, thus the FFL is the dominant loop at high frequency and

determines the overall loop stability. As long as  $z_1$  is designed to be lower than the frequency of the FFL loop's dominant pole ( $p_3$ ), the loop bandwidth extension is achieved. Since the two loops are summing together in parallel instead of in series, the VFL will have less impact on the overall loop stability as compared to [83]. If the compensation capacitor  $C_c$  is chosen such that  $z_1 \ll p_2$ , the size of  $C_c$  would have minimum impact on the overall loop stability. Thus, a smaller  $C_c$  can be used for this dual loop design with less impact on the slew rate. In this design, the loop gain at  $z_1$  is around 20dB, and  $C_c$  is 5pF. Note that  $C_c$  would be 15pF if in the single loop conventional pole-splitting compensation is used. In view of this, the UGF is extended by the proposed technique.

#### 4.2.2. Large-signal behavior of the fast feedback loop

For a large load step, the undershoot and overshoot of the LDO output voltage are mainly decided by the slew rate of the voltage changes across the compensation capacitors, if the voltage buffer is fast enough. The Equation (4.1) and (4.2) can be revised to (4.3) and (4.4):

$$T_r \approx C_c \frac{\Delta V_g}{I_{sr}} \quad (4.3)$$

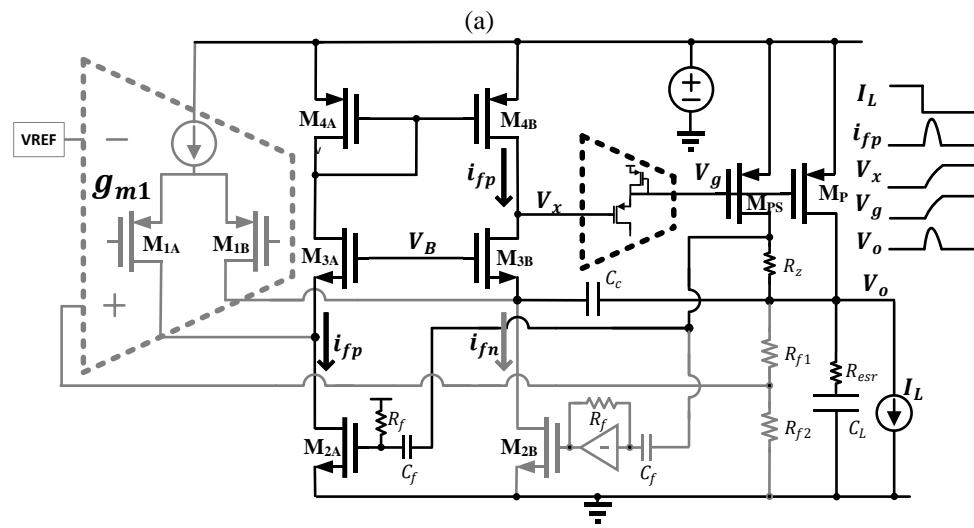
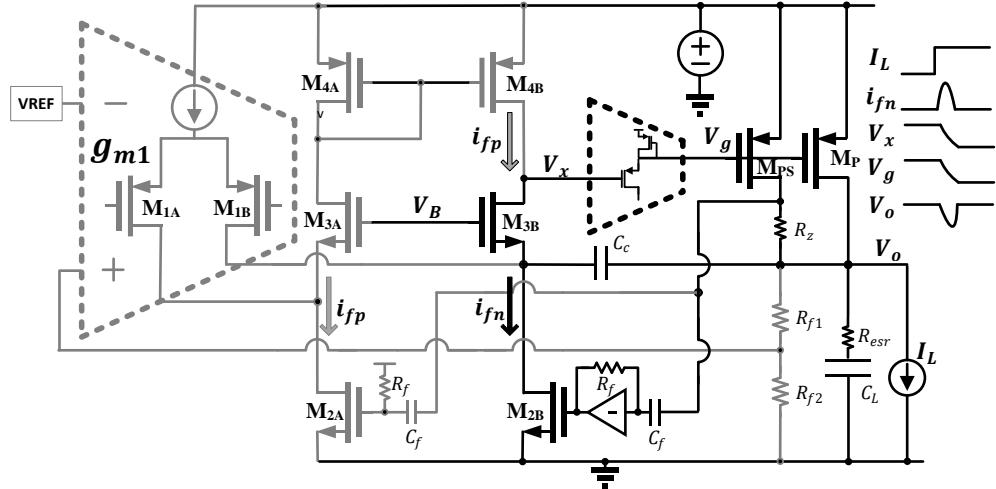
$$\Delta V_o \approx \frac{\Delta I_L C_c \Delta V_g}{I_{sr} C_L} \quad (4.4)$$

A smaller  $C_c$  and a higher slewing current alleviate the LDO output voltage spike. Figure 4.3(a) and Figure 4.3(b) depict the mechanism of the load step response enhancement. The output voltage spike detector has an unique feature of efficiently providing significant dynamic current for fast charging and discharging the  $C_c$  in response to the load steps. When the load current steps up

(from light load to heavy load), the current sensing capacitor ( $C_f$ ) converts the output voltage spike to a current that passes through the TIA resistor ( $R_f$ ) to raise the M<sub>2B</sub>'s gate voltage. In this design, M<sub>2A</sub> and M<sub>2B</sub> are biased in the subthreshold region for optimal bandwidth and slew rate. The  $i_{fn}$  is the corresponding slewing current. It can be expressed as:

$$i_{fn} = I_{so} \frac{W}{L} e^{\frac{V_{g2}}{nV_T}} \left( 1 - e^{\frac{V_{ds2}}{V_T}} \right) \cdot (1 + \lambda_{sub} V_{ds2}) \quad (4.5)$$

where  $V_{g2}$  is the gate voltage of M<sub>2B</sub>, and  $I_{so}$ ,  $n$ ,  $\lambda_{sub}$  are the process-related parameters [88].  $V_{g2}$  changes when there is an output voltage spike. As  $V_{g2}$  changes,  $i_{sn}$  changes to charge the  $C_c$  and discharge the error amplifier output node  $V_x$  respectively, which allows an undershoot reduction. When the load current steps down (from a heavy load to a light load), M<sub>2A</sub>'s gate voltage will directly follow the output voltage overshoot spike. M<sub>2A</sub> conducts an increasing slewing current ( $i_{fp}$ ) to charge the error amplifier output node  $V_x$  and discharge the compensation capacitor  $C_c$ . Since  $i_{fn} \gg i_{fp}$  for load stepping up and  $i_{fp} \gg i_{fn}$  for load stepping down, the slewing paths can be simplified as shown in Figure 4.3(a) and Figure 4.3(b).



(b)

Figure 4.3 (a) Large signal transient response of the LDO with a step-up load transient. (b) Large signal transient response of the LDO with a step-down load transient.

The design guideline for the slewing current can be expressed with given undershoot or overshoot specifications:

$$\text{Minimum}(i_{fn}, i_{fp}) > \frac{\Delta V_g C_c \Delta I_L}{\Delta V_o C_L} \quad (4.6)$$

The properly biased  $M_{2A}$  and  $M_{2B}$  are required to meet the above equation.

#### 4.2.3. The pseudo-ESR technique

As mentioned earlier in the first section, the small value of the ESR of the ceramic capacitors will make it impractical to have a useful ESR zero for the loop stability improvement. A unique feature of the DLC is that the signal feedback points for the two loops can be different. The loop stability is mainly dominated by the fast loop. Thus, the ESR zero is only necessary to be added in the fast feedback loop. In this design, a power transistor with the pseudo-ESR technique is introduced to generate a functional equivalent ESR zero, which only exists inside the FFL. As shown in Figure 4.1, the FFL starts from the  $M_{PS}$ 's drain instead of the LDO's output node. The added  $R_Z$  can emulate the off-chip capacitor's ESR and it can be well controlled by design. Figure 4.4 shows the relationship between the conventional ESR technique and the pseudo-ESR technique. The power transistor ( $M_P$ ) and the output current sensing transistor ( $M_{PS}$ ) have a ratio of  $K:1$ , where  $K$  is much larger than one. These two transistors are driven with the same gate voltage. With the assumption that the voltage across  $R_{esr}$  is much smaller than the  $V_{ds}$  of  $M_P$ , the drain current and the transconductance of the  $M_{PS}$  are proportional to the output current with a coefficient of  $1/K$ . The transfer function from  $V_g$  to  $V_f$  node can be expressed as:

$$\frac{V_f}{V_g} \approx \frac{g_{mp} \left( 1 + \frac{sR_z C_L}{K} \right)}{sC_L} \quad (4.7)$$

$$\frac{V_o}{V_g} \approx \frac{g_{mp} (1 + sR_{esr} C_L)}{sC_L} \quad (4.8)$$

As shown in Equation (4.7) and (4.8),  $R_z/K$  has the same effect as  $R_{esr}$ , which means that an internal resistor  $R_z$  can be used to replace the external off-chip

capacitor's ESR resistor. Therefore, it is an ESR compensation with a controllable equivalent ESR resistor of  $R_Z/K$ . The small size multilayer ceramic capacitors with small ESR can be used in this proposed LDO regulator with a properly designed internal resistor  $R_Z$  and current sensing ratio,  $K$ .

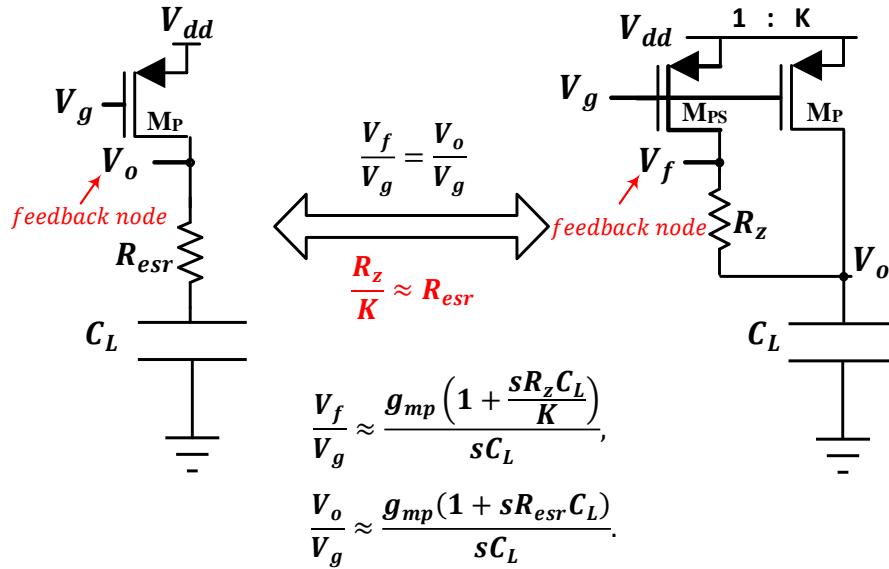


Figure 4.4 The relationship between the conventional ESR technique and the pseudo-ESR technique (AC small signal).

In the LDO design, a large ESR degrades the load transient performance. The pseudo-ESR also degrades the load transient performance, since it is fundamentally the same as the real ESR. The pseudo-ESR resistance value can be optimized based on the trade-off between load transient performance and loop stability. It benefits the transient performance by using the low ESR ceramic capacitors. And it also helps improve the loop stability with its extended loop bandwidth, especially for a fast transient LDO

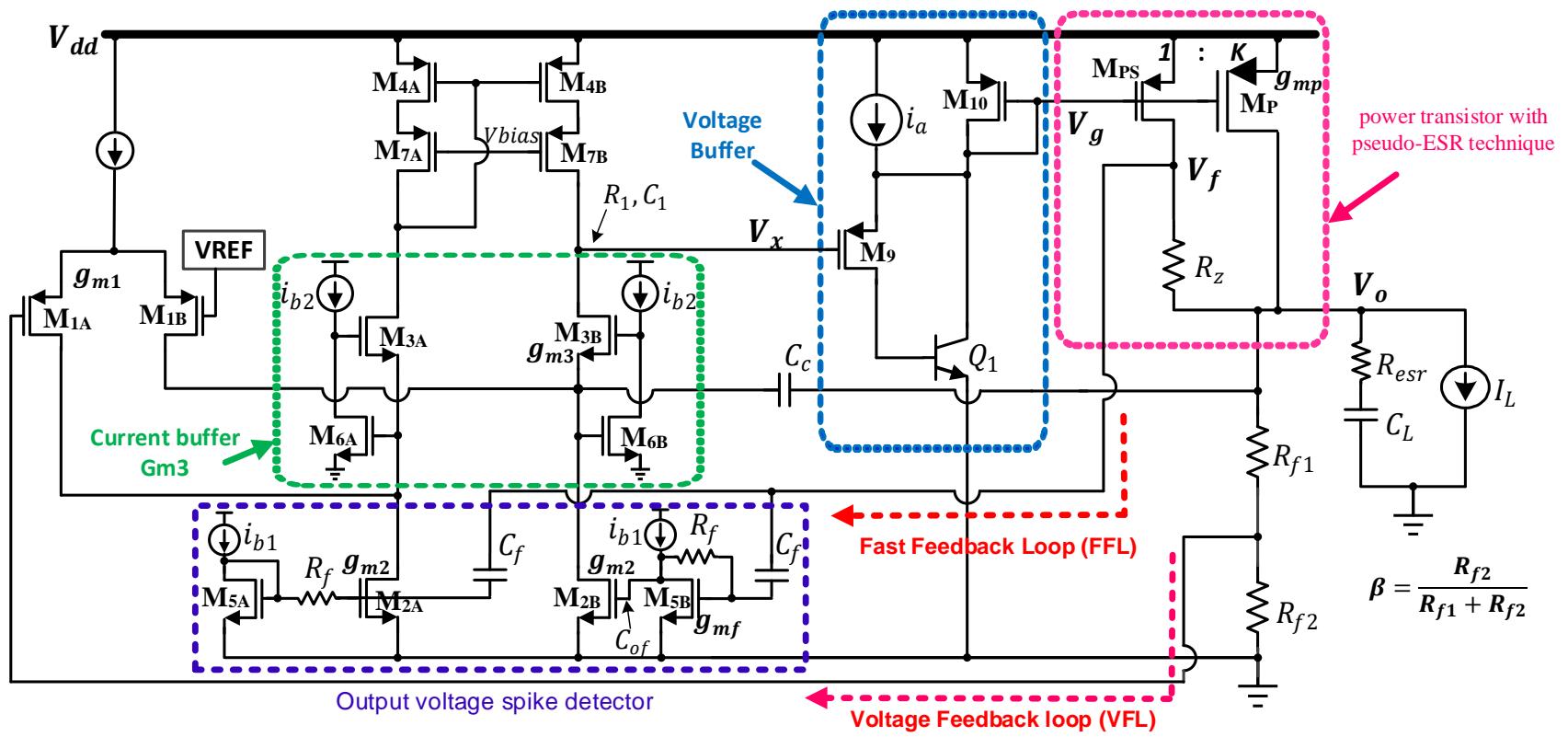


Figure 4.5 Schematic of the proposed LDO design.

## 4.3. Circuit implementation and stability analysis

### 4.3.1. Circuit implementation

Figure 4.5 depicts the transistor level implementation of the proposed LDO. The error amplifier is a folded cascode structure with a PMOS input pair ( $M_{1A}$  and  $M_{1B}$ ). The feedback path from output voltage through the resistive divider to  $M_{1A}$  forms the VFL. A transconductance and impedance boosting circuit ( $M_{3A}$ ,  $M_{3B}$ , and  $M_{6A}$ ,  $M_{6B}$ ) are embedded inside the error amplifier for further performance enhancement. The dynamic biased super source follower (DB-SSF), which consists of  $M_9$ ,  $M_{10}$ , and a bipolar transistor  $Q_1$ , serves as a voltage buffer to drive the pass transistor  $M_P$  [22], [89]. This voltage buffer pushes the pass transistor gate pole to a frequency that is much greater than the UGF. Hence, this pole can be ignored in the following loop stability analysis. A pseudo-ESR technique is introduced for loop stability improvement. The FFL consists of the pseudo-ESR resistor ( $R_Z$ ), the output voltage spike detector, the DB-SSF, and the power transistor. In the diagram,  $C_L$  is the off-chip capacitor,  $R_{esr}$  is the total ESR of the off-chip capacitor.

A larger  $g_{m3}$  is desired to reduce the Q factor of the complex poles in the VFL [45]. Increasing  $g_{m3}$  by increasing the bias current will not only consume a considerable current but also decrease the gain of the error amplifier. The self-regulated loop formed by  $M_{3B}$  and  $M_{6B}$  boosts the transconductance  $gm_3$  and the output impedance of the error amplifier. This boosted VFL gain will further enhance the LDO's line regulation and load regulation performance.

As shown in Figure 4.5, the FFL starts from the  $M_{PS}$ 's drain instead of the LDO's output node. The output voltage spike detector consists of  $M_{5A}$ ,  $M_{5B}$ ,  $M_{2A}$ ,  $M_{2B}$ ,  $C_f$ , and  $R_f$ . Any output voltage spike can be detected by the capacitor  $C_f$  directly. The significant dynamic current from this voltage spike detector can quickly charge and discharge  $V_x$  for slew rate enhancement. The capacitor type of sensing scheme naturally lets the fast feedback loop behave similarly as a high pass or bandpass filter, which does not affect the overall DC performance as compared to the adaptive biased LDO design.

Figure 4.6 shows the small-signal model of the voltage spike detector, where the transconductance of  $M_{2A}$ ,  $M_{2B}$ , and  $M_{4B}$  are denoted as  $g_{m2}$  and  $g_{mf}$ . The transfer function of the voltage spike detector is derived as:

$$\frac{i_f(s)}{v_{fb}(s)} = \frac{2g_{m2}R_fC_f s(\frac{R_f C_f}{2}s + 1)(\frac{C_{of}}{g_{mf}}s + 1)}{(R_f C_f s + 1)(\frac{R_f C_f C_{of}}{g_{mf}}s^2 + \frac{C_f}{g_{mf}}s + 1)} \quad (4.9)$$

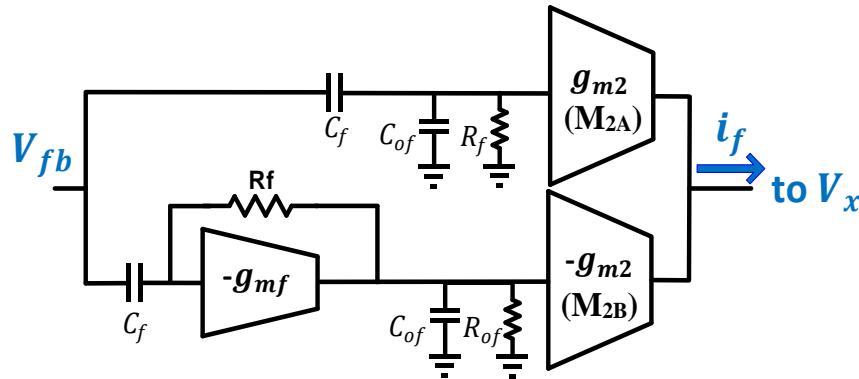


Figure 4.6 Small-signal model of voltage spike detector.

The equivalent transconductance ( $i_f(s)/v_{fb}(s)$ ) of the voltage spike detector is a band-pass function with its transconductance larger than  $g_{m2}$  after its first pole frequency ( $1/R_f C_f$ ). For the folded-cascode amplifier, the transconductance of  $M_{2A}$  and  $M_{2B}$  ( $g_{m2}$ ) is much larger than the transconductance of the amplifier

input pair ( $g_{m1}$ ). From (4.9) and Figure 4.2, it is obvious that the overall loop bandwidth is extended.

#### 4.3.2. Small signal analysis

The complete equivalent small-signal model of the proposed LDO is depicted in Figure 4.7.  $g_{m1}$  models the transconductance of the error amplifier input pair, while the error amplifier's output impedance and parasitic capacitance are denoted as  $C_1$  and  $R_1$  respectively. The effective transconductance of cascode compensation current buffer is represented by  $G_{m3}$ .  $g_{mp}$  represents the transconductance of the pass transistor. For analysis, the loop is broken at the common path of the VFL and the FFL. The transfer function of the output voltage spike detector can be replaced by the transfer function (4.9). Note that the capacitor  $C_f$  is in the order of pF range, which is considerably smaller than the off-chip capacitor. The loading effect of the voltage spike detector can be ignored in the following analysis. In this design, the current through the resistor divider is only  $2 \mu\text{A}$ , which is absorbed into the load current, such that the resistor divider ( $R_{f1}$  and  $R_{f2}$ ) can be modeled as the scaling factor  $\beta$  alone.

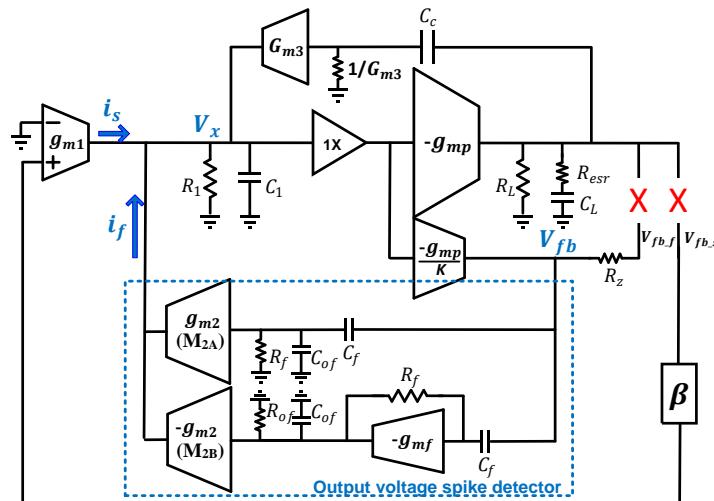


Figure 4.7 Small-signal model of the proposed LDO.

The transfer function of the LDO loop is derived based on the following considerations:

- a) The off-chip capacitor:  $C_L \gg (C_c, C_1)$ .
- b) The overall loop DC gain is  $g_{m1}R_1g_{mp}R_L\beta$ . The gain of the error amplifier remains constant and the pass transistor gain decreases with the load current and it is inversely proportional to  $\sqrt{I_{load}}$ .

The overall loop transfer function  $T(s)$  can be written approximately as (4.10).

$$\begin{aligned}
 T(s) &= \frac{g_{m1}R_1g_{mp}R_L\beta \left( \frac{C_c}{G_{m3}}s + 1 \right) \left( \frac{R_z + KR_{esr}}{K}s + 1 \right) \left( \frac{2R_fC_fg_{m2}}{g_{m1}}s + 1 \right) \left( \frac{R_fC_fC_{of}}{2g_{mf}}s^2 + \frac{R_fC_f}{2}s + 1 \right)}{\left( g_{mp}R_LR_1C_c s + 1 \right) \left( R_fC_f s + 1 \right) \left( \frac{C_1C_L}{G_{m3}g_{mp}}s^2 + \frac{C_1C_L}{g_{mp}C_c}s + 1 \right) \left( \frac{R_fC_fC_{of}}{g_{mf}}s^2 + \frac{C_f}{g_{mf}}s + 1 \right)} \\
 &\approx \frac{g_{m1}R_1g_{mp}R_L\beta \left( \frac{R_z + KR_{esr}}{K}s + 1 \right) \left( \frac{2R_fC_fg_{m2}}{g_{m1}}s + 1 \right) \left( \frac{R_fC_f}{2}s + 1 \right) \left( \frac{C_{of}}{g_{mf}}s + 1 \right) \left( \frac{C_c}{G_{m3}}s + 1 \right)}{\left( g_{mp}R_LR_1C_c s + 1 \right) \left( R_fC_f s + 1 \right) \left( \frac{C_1C_L}{g_{mp}C_c}s + 1 \right) \left( \frac{C_f}{g_{mf}}s + 1 \right) \left( R_fC_{of}s + 1 \right) \left( \frac{C_c}{G_{m3}}s + 1 \right)}
 \end{aligned} \tag{4.10}$$

Re-writing (4.10), we have:

$$\begin{aligned}
 T(s) &= -\frac{v_{fb}(s)}{v_o(s)} \\
 &\approx \frac{A_0 \left( 1 - \frac{s}{z_1} \right) \left( 1 - \frac{s}{z_2} \right) \left( 1 - \frac{s}{z_3} \right) \left( 1 - \frac{s}{z_4} \right)}{\left( 1 - \frac{s}{p_1} \right) \left( 1 - \frac{s}{p_2} \right) \left( 1 - \frac{s}{p_3} \right) \left( 1 - \frac{s}{p_4} \right) \left( 1 - \frac{s}{p_5} \right)}
 \end{aligned} \tag{4.11}$$

$A_0$  is DC gain:

$$A_0 = g_{m1}R_1g_{mp}R_L\beta \quad (4.12)$$

Table 4.1 List of loop poles and zeros of the proposed PMOS LDO.

Zeros	Poles
$z_1 = -\frac{g_{m1}}{2R_fC_fg_{m2}}$	$p_1 = -\frac{1}{R_1g_{mp}R_LC_c}$
$z_2 = -\frac{2}{R_fC_f}$	$p_2 = -\frac{1}{R_fC_f}$
$z_3 = -\frac{1}{\left(\frac{R_z}{K} + R_{esr}\right)C_L}$	$p_3 = -\frac{g_{mp}C_c}{C_1C_L}$
$z_4 = -\frac{g_{mf}}{C_{of}}$	$p_4 = -\frac{g_{mf}}{C_f}$
	$p_5 = -\frac{1}{R_fC_{of}}$

The loop transfer function of the proposed LDO has 4 zeros and 5 poles. They are summarized in Table 4.1. It can be verified by setting  $C_f$  to zero so that the overall transfer function  $T(s)$  can be simplified as the conventional single loop cascode compensated LDO design. The DC loop gain is  $A_0$  and the dominant pole is  $p_1 = -1/R_1g_{mp}R_LC_c$ . The low-frequency pole  $p_2$  and zero  $z_2$  are close to each other. They will cancel each other and have no impact on the overall transfer function. Without adaptive biasing, the gain of the error amplifier, which is  $g_{m1}R_1$ , remains constant regardless of loading current. There are no complex conjugate poles in  $T(s)$ , which makes the loop stability analysis much simpler. The  $p_3$  varies with the load condition, which also determines the UGF. The UGF can be approximated as:

$$\omega_o \approx \frac{\beta g_{m2} R_f C_f}{C_1} \frac{g_{mp}}{C_L} \quad (4.13)$$

which is a function of load current.

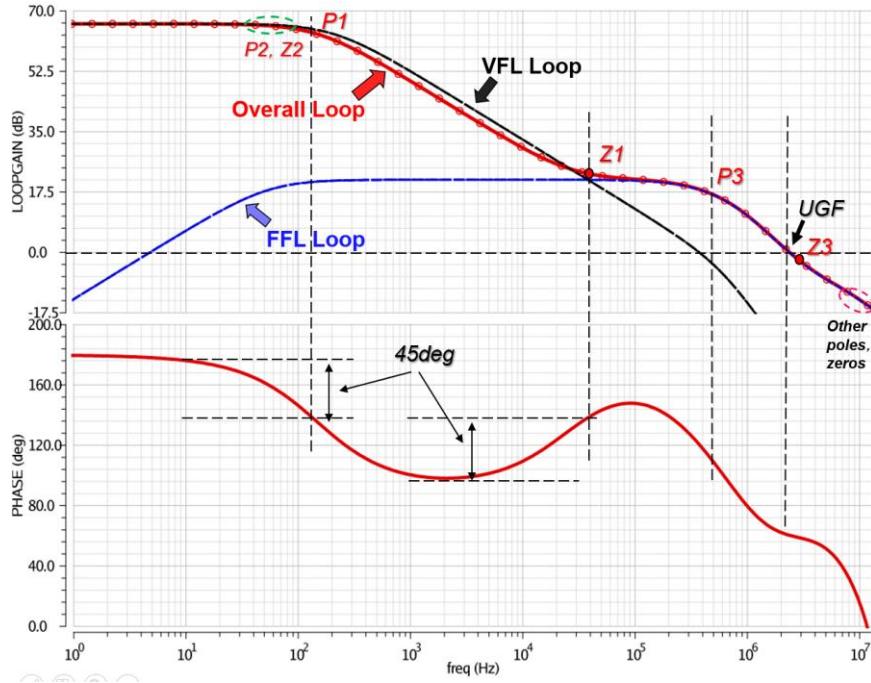


Figure 4.8 Loop frequency response of the proposed LDO at medium to heavy load conditions (simulation).

The gain plot of the VFL, FFL and overall loop are plotted in Figure 4.8 respectively. The VFL is similar to [22] and its UGF is small. The FFL loop is a bandpass function with its UGF in the order of a few MHz at medium and heavy load conditions. Combining the VFL and the FFL, the overall loop gain, and its phase are shown in Figure 4.8, which matches the conceptual diagram of Figure 4.2(b). At full load condition, a DC gain of 60dB and a phase margin of 65 degrees are achieved. The UGF is widely extended comparing to the conventional design.

At light load condition (0-6mA),  $g_{m1}$ ,  $g_{m2}$ ,  $g_{m3}$ ,  $g_{mf}$  remain constant, and  $g_{mp}$  is small, and the DC loop gain  $A_0$  is inversely proportional to  $\sqrt{I_{load}}$ . As the load current decreases, the DC loop gain will increase. In this design, the DC loop gain is approximately 80dB for light load conditions. Under light load condition,  $p_1$  and  $p_3$  move to a lower frequency and the UGF is reduced, which is much smaller than the frequencies of  $z_3$ ,  $z_4$ ,  $p_4$ , and  $p_5$ . The transfer function can be simplified as:

$$T(s) = -\frac{v_{fb}(s)}{v_o(s)} \approx \frac{A_0 \left(1 - \frac{s}{z_1}\right) \left(1 - \frac{s}{z_2}\right)}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) \left(1 - \frac{s}{p_3}\right)} \quad (4.14)$$

$z_2$  and  $p_2$  are in the same order and they cancel each other. Besides,  $z_1$  and  $p_3$  are close to each other so that it is similar to a single-pole system with a dominant pole of  $p_1$ . As compared to the conventional pole-splitting compensation scheme [22], the loop phase margin is not a strong function of  $C_c$ .

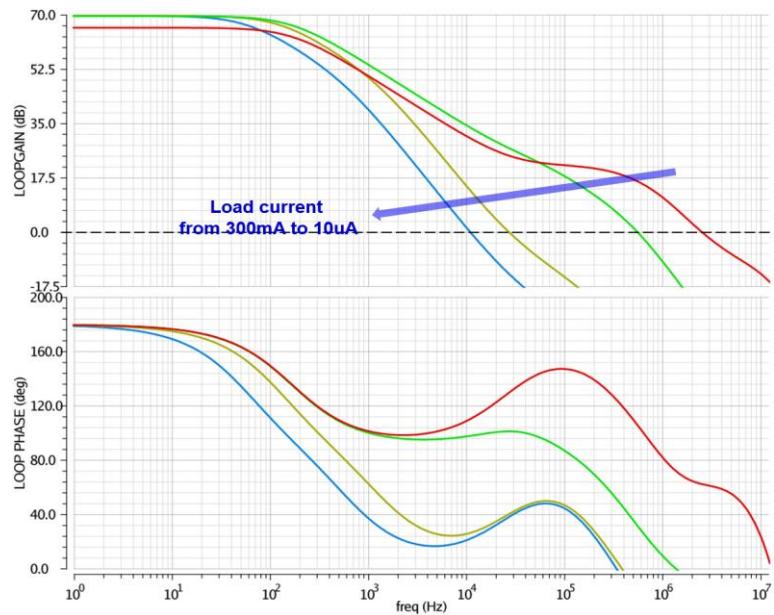
At medium to heavy load condition,  $g_{m1}$ ,  $g_{m2}$ ,  $g_{m3}$ , and  $g_{mf}$  still remain the same as at light load condition. When the load current increases,  $g_{mp}$  becomes much larger. Hence,  $p_3$  frequency becomes higher and it is the dominant pole of the FFL, which determines the overall UGF. The loop magnitude plot is shown in Figure 4.8. The loop gain above  $z_1$  is denoted as  $A_1$  with the expression:

$$A_1 = -\frac{R_f C_f g_{m2}}{C_c} \quad (4.15)$$

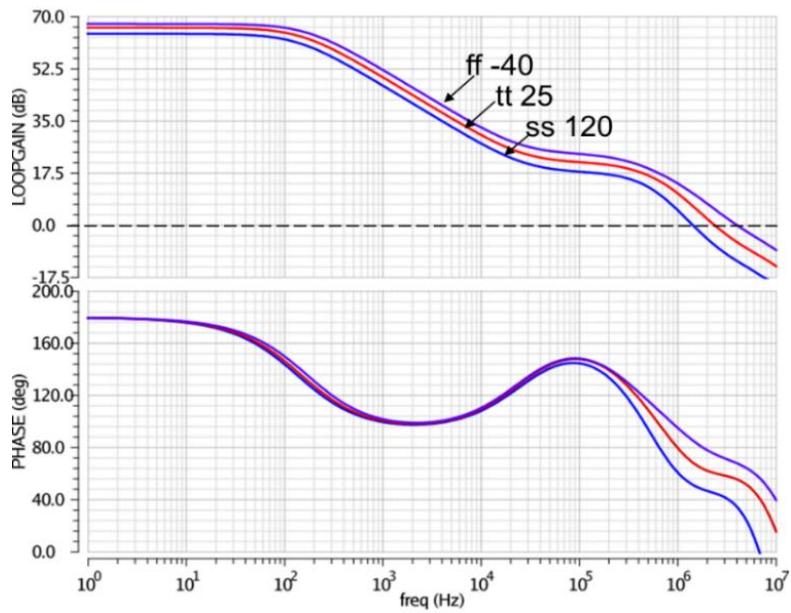
where  $C_c$ ,  $R_f$ ,  $C_f$ , and  $g_{m2}$  determine the magnitude of  $A_1$ . A smaller  $A_1$  could help to improve the loop phase margin. However, there would be less bandwidth extension if  $A_1$  is small. The UGF trades off with the phase margin by  $A_1$

magnitude. In this proposed design,  $A_1$  is close to 20dB. From Figure 4.5, the transistors  $M_{5A}$  and  $M_{5B}$  are reused from the original current bias circuit such that it does not consume extra quiescent current as compared to the original pole-splitting compensation scheme. As the loop bandwidth is extended, the transient response performance is enhanced. Besides, the phase margin and the UGF are not strong functions of  $C_c$  anymore. A smaller size  $C_c$  can be used for area savings and further bandwidth extension. Therefore, the proposed approach is advantageous over the conventional pole-splitting approach.

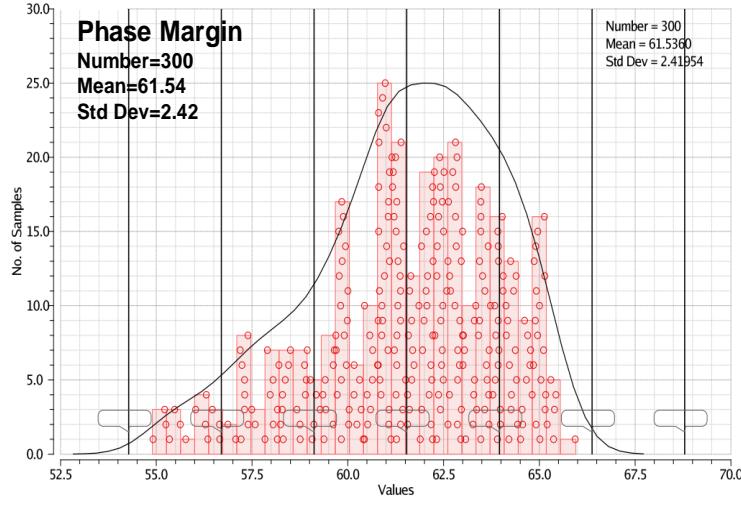
In this proposed design, the pseudo-ESR zero is designed to be close to UGF. The pseudo-ESR resistor  $R_z$  is  $100\Omega$  and the output current sensing transistor ( $M_{PS}$ ) has a ratio of  $K = 2000$ . Figure 4.9(a) depicts the simulated loop gain/phase of the LDO over all the load conditions (from  $10\mu\text{A}$  to  $300\text{mA}$ ). From the simulation, the circuit optimization ensures that the LDO is stable for all load conditions. Besides, as shown in Figure 4.9(b), the loop is stable at different process corners, proving the effectiveness of the proposed technique. The loop DC gain is 67dB at ff -40degC and 64dB at ss 120degC with a  $300\text{mA}$  load. Monte Carlo simulations were performed to verify the effects of process spreads on loop stability. Figure 4.9(c) shows the loop phase margin with the load current of  $300\text{mA}$ . The mean loop phase margin is 61.5 degree and the standard deviation is 2.4 degree with components mismatch.



(a)



(b)



(c)

Figure 4.9 (a) Simulation results of loop gain/phase of the proposed LDO with load current at 300mA, 10mA, 100 $\mu$ A, and 10 $\mu$ A. (b) Loop stability versus process corner/temperature. (c) Monte Carlo simulation result of loop stability of the proposed LDO.

Since the dominant pole ( $p_3$ ) of the fast feedback loop (FFL) is a function of  $g_{mp}C_c/(C_1C_L)$ . A larger off-chip capacitor helps loop stability and transient performance.

#### 4.4. Experimental results

To verify the concept of this dual loop high DC loop gain linear regulator, a prototype IC is implemented and fabricated with a 0.18 $\mu$ m CMOS process with NMOS and PMOS threshold voltage of 0.5V and -0.7V respectively. The layout and micrograph of the proposed design are shown in Figure 4.10. The active area of the whole LDO is 210 $\mu$ m  $\times$  593 $\mu$ m, excluding the PADs for testing. The chip area occupied by the controller is 210 $\mu$ m  $\times$  142 $\mu$ m, which is 24% of the whole LDO. The silicon area of the power FET is 210 $\mu$ m  $\times$  394 $\mu$ m. This LDO can be

used for the supply of DDR or other loads which require a fast-transient response.

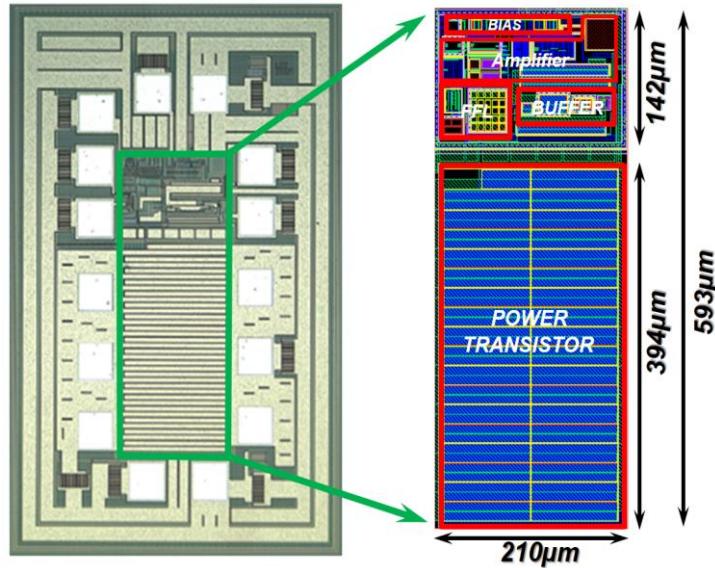


Figure 4.10 Chip micrograph and layout.

Since the output voltage spike detector in the FFL does not require extra bias current, the currents of the LDO is 30 $\mu$ A at light load condition and 700 $\mu$ A at maximum load (600mA). The maximum current efficiency is 99.88% at 600mA load. Transient load regulation was also tested for with an off-chip 1 $\mu$ F capacitor at Vout of 1.8V and Vdd of 2V, as shown in Figure 4.11. When the load current changes with a 600mA/100ns step, the measured undershoot and overshoot are 15.6mV and 15.4mV respectively, as shown in Figure 4.12(a). When measuring with a 600mA/1 $\mu$ s load step, the undershoot and overshoot are 14mV and 12.8mV respectively as shown in Figure 4.12(b). The output voltage errors were less than +/- 1% over the entire operation range. The DC variation across 600mA load is less than 5mV, giving a load regulation of 8.3 $\mu$ V/mA. The good DC load regulation is achieved in such high load current due to the high DC loop gain with a dynamic bias scheme.

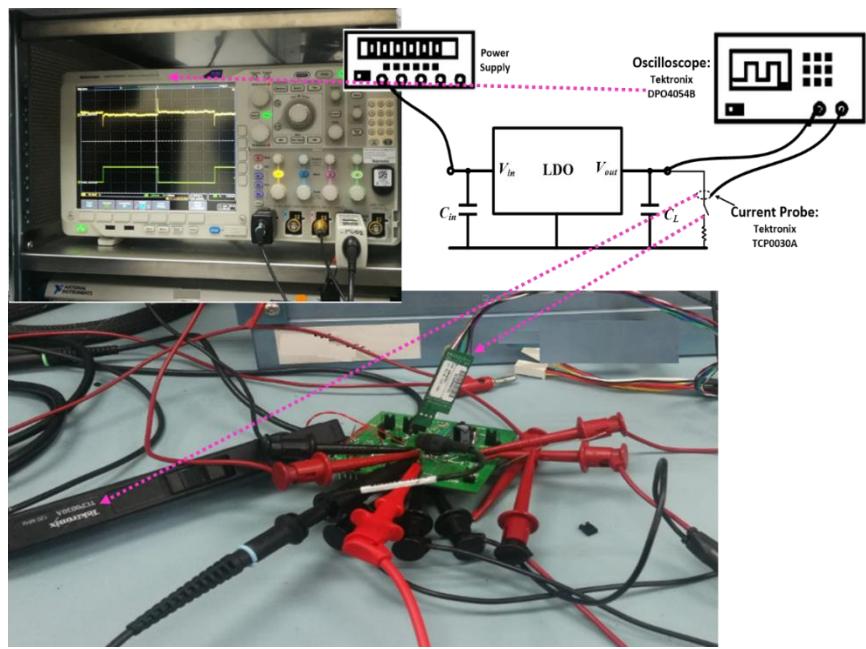
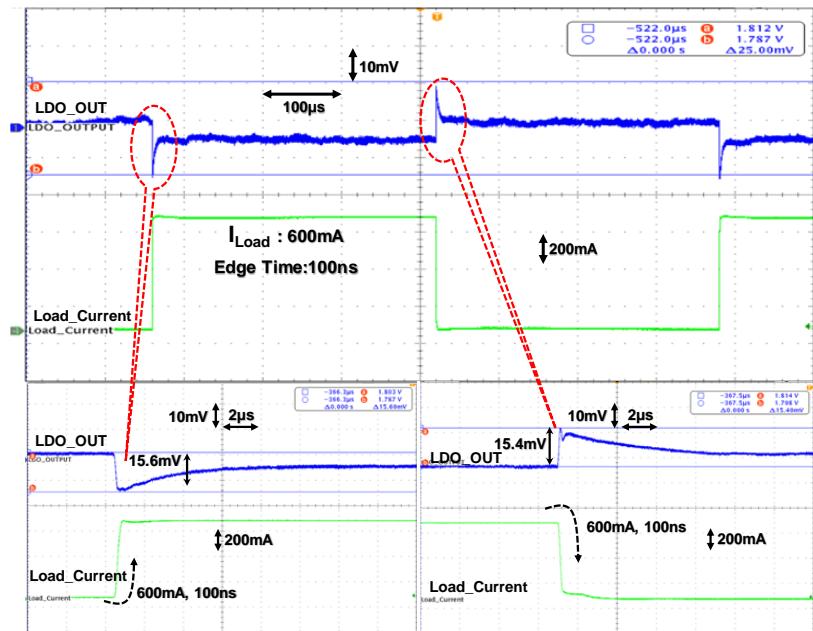
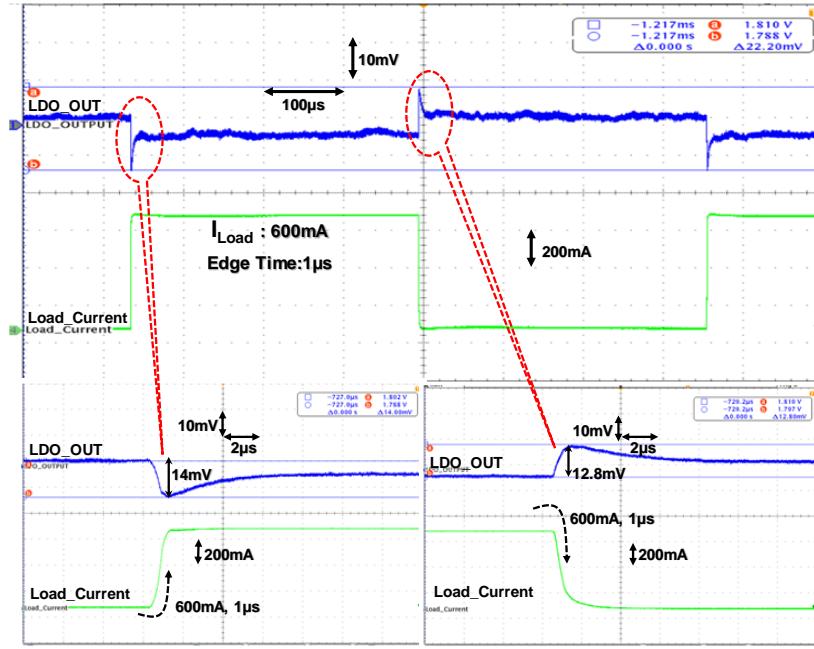


Figure 4.11 Testing setup for the proposed PMOS LDO.



(a)



(b)

Figure 4.12 Measured output transient response of 600mA load step. (a) The transient response of the load current steps of 600mA in 100ns. (b) The transient response of the load current steps of 600mA in 1μs.

The power supply rejection (PSR) was tested by injecting a sinusoidal signal superposed to a DC input voltage of 2V through a bias tee and by observing the output [70]. PSR against different load current is shown in Figure 4.13. PSR at 100kHz is 32dB and 39dB with 300mA and 10mA load current, respectively.

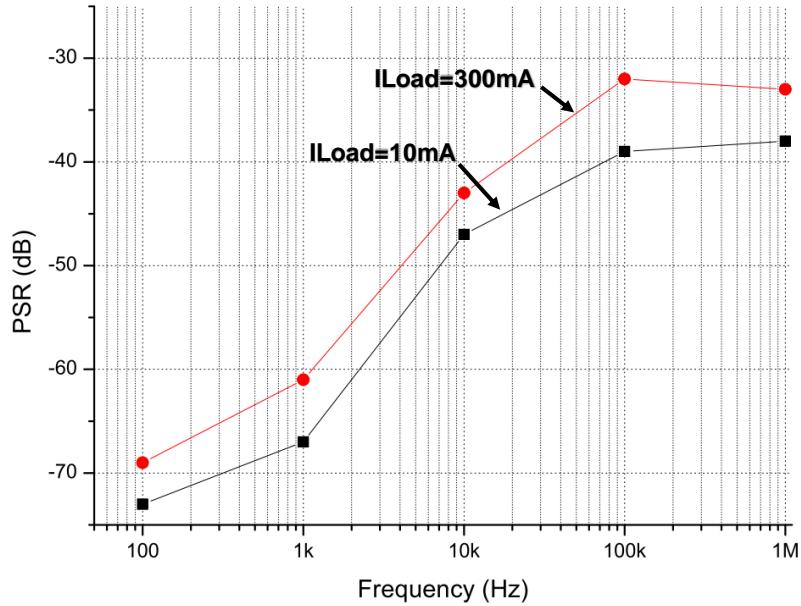


Figure 4.13 Measured PSR versus frequency for  $I_{\text{Load}}=10\text{mA}$  and  $I_{\text{Load}}=300\text{mA}$   
when  $V_{\text{out}}=1.8\text{V}$ ,  $V_{\text{in}}=2\text{V}$ , and  $\text{CL}=1\mu\text{F}$ .

The line transient responses are measured with 300mA load current and  $1\mu\text{F}$  off-chip capacitor. When the input voltage varies from 2V to 2.5V with a rise and fall time of  $10\mu\text{s}$ , as shown in Figure 4.14, the measured LDO output voltage overshoot and undershoot spike in this testing condition are both  $2.5\text{mV}$ .

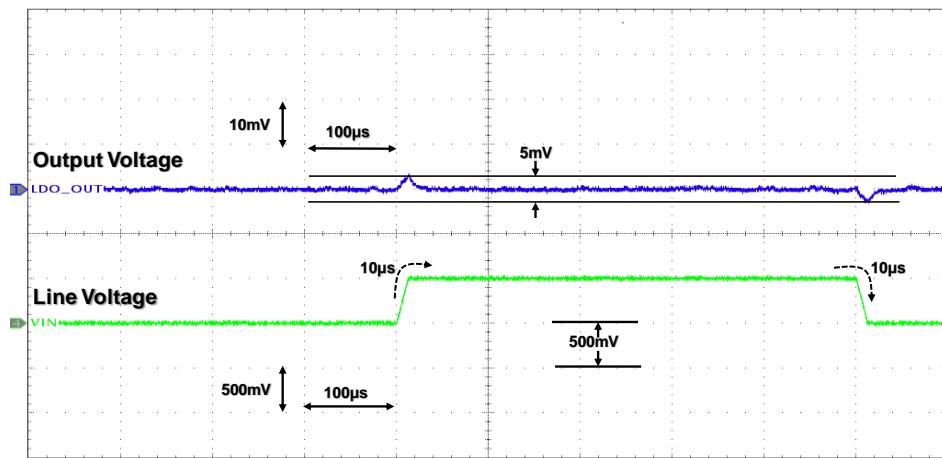


Figure 4.14 Measured line transient response at the load current of 300mA.

A performance comparison with some recent capacitor-based LDO designs is shown in Table 4.2, which provides a clear picture of the performance enhancement of the proposed LDO. The proposed LDO architecture offers many advantages as a regulator for heavy load, which can be widely used in battery-powered systems. Without specifying a requirement for output capacitor ESR, the proposed pseudo-ESR technique makes the loop stable even with an extended loop bandwidth. While delivering the highest load capability among all the reported LDOs, a decent DC loop gain is still maintained to achieve  $8.3\mu\text{V/mA}$  DC load regulation. Since the loop gain of the LDO is inversely proportional to the load current in most LDO design, it is not an easy task to achieve a good load regulation with large load current. The proposed LDO achieves the best load regulation. As the proposed design has a high slew rate during the load transient, it achieves the smallest undershoot and overshoot among these state-of-art LDOs.

Finally, a figure of merit ( $FOM_1 = C_L \Delta V_o I_q / \Delta I_{L,max}^2$  [2]) is adopted for comparison. Where  $C_L$ ,  $\Delta V_o$ ,  $I_q$ ,  $\Delta I_{L,max}$  are the output capacitor, the output voltage variation due to the load transient steps, the quiescent current, and the maximum load current step. This study obtains good FOM factor, making it a good candidate for battery-powered portable applications.

Table 4.2 Performance summary of the proposed PMOS LDO.

References	TPE 2010 [89]	JSSC 2010 [84]	TPE 2016 [82]	TPE 2017 [39]	JSSC 2017 [2]	This work
<b>CMOS technology</b>	0.35μm	90nm	0.18μm	0.18μm	0.13μm	0.18μm
<b>Power-MOS type</b>	PMOS	PMOS	PMOS	PMOS	NMOS	PMOS
<b>Chip area [mm<sup>2</sup>]</b>	0.146	0.00274	0.024	0.0285	0.1825	0.1245
<b>Output capacitor, C<sub>L</sub> [μF]</b>	1	1	1	1	1	1
<b>Nominal output voltage [V]</b>	1.8	0.9	1	1.2	1	1.8
<b>Dropout voltage[mV]</b>	200	100	200	200	30	200
<b>Quiescent current, I<sub>Q</sub> [μA]</b>	30-75	9.3	135.1	1.6-200	14-120	30-700
<b>Max. current efficiency [%]</b>	99.9	99.9	99.86	99.6	99.96	99.88
<b>Max. load current step [mA]</b>	160	50	100	50	300	600
<b>Edge time [μs]</b>	0.1	0.01	0.01	0.01	1	0.1
<b>Load transient undershoot [mV]</b>	30	6	25	24	56	15.6
<b>Load transient overshoot [mV]</b>	65	12.1	7.5	5	24	15.4
<b>Load regulation<sub>1</sub> [μV/mA]</b>	90	82	75	100	6	8.3
<b>Line regulation [mV/V]</b>	6	14	22.7	5.5	0.44	0.23
<b>PSR @ measured frequency and load current [dB]</b>	N/A	-54 (100kHz, 50mA)	-35 (100kHz, 100mA)	-30 (10MHz)	-50 (10kHz, 300mA)	-43 (10kHz, 300mA)
<b>FOM [ps]*</b>	111.3	67.3	439	18.5	12.44	2.58

$$* FOM = C_L \Delta V_o I_q / \Delta I_{L,max}^2$$

## 4.5. Conclusions

In this chapter, a fast-transient response LDO for portable mobile applications with dual loop compensation has been presented. By modifying the amplifier's biasing circuit, a voltage spike detector circuit and the DC biasing circuit form a fast feedback path for the LDO. This significantly enhances the large-signal transient response and extends the loop bandwidth without consuming extra quiescent current as compared to the conventional one. The DC bias of the error amplifier is constant across different load conditions. Thus, a high DC loop gain is kept across different load conditions for a better line regulation and load regulation. The pseudo-ESR technique enables the use of small size multilayer ceramic capacitors in real applications. Since no extra stage is needed for loop gain boosting, the LDO design is much simpler and achieves a better current efficiency. The LDO can deliver up to 600mA load current with 200mV dropout voltage. It achieves 15mV voltage spike with a load step of 600mA within 100ns.

# **Chapter 5**

## **A multi-loop slew-rate enhanced NMOS LDO handling**

### **1A load current transient**

A large portion of this chapter has been published in IEEE Journal of Solid-State Circuits [90].

Compact LDOs with high current handing capability and superior transient response are gaining more and more attention in battery-powered 5G mobile applications. In this chapter, a new multiple-loop design technique for fast-transient response LDO design has been proposed and successfully implemented in 0.13 $\mu$ m SOI CMOS. Its supply current capacity is more than one Ampere, and its output voltage is 1.8V. The proposed LDO features a 10mV undershoot/overshoot with 1A/100ns load current on a 1- $\mu$ F output capacitor. This superior transient performance is achieved by employing a novel frequency compensation scheme without compromise in DC loop gain reduction under heavy load current condition. The DC loop gain is 60dB and constant regardless of the load current between 0 to 1A. This contributes to a small load regulation and line regulation of 0.6 $\mu$ V/A and 0.23mV/V, respectively. The LDO consumes 35 $\mu$ A quiescent current in mission mode, and 5 $\mu$ A in standby mode. The LDO silicon size is 325 $\mu$ m  $\times$  106 $\mu$ m.

This chapter is organized as follows. Section 5.1 delineates the concept and working principle of the proposed LDO. The detail circuit implementations and the loop stability analysis are described in Section 5.2. Section 5.3 discusses the

experiment results and key parameter comparison. In the end, Section 5.4 draws the conclusions.

### 5.1. The proposed LDO architecture

The simplified circuit diagram of the proposed LDO is shown in Figure 5.1. It consists of three feedback loops: one is outer slow response Voltage Feedback Loop (VFL), which consists of a resistive voltage divider composed of  $R_{f1}$  and  $R_{f2}$ , an error amplifier, a voltage buffer and a power pass transistor. Another is the inner Fast-response Feedback Loop (FFL), which consists of a differentiator based output voltage spike detector, a voltage buffer and a power pass transistor. The output voltage spike detector injects an output signal dependent current to the error amplifier's output for slew rate enhancement and loop bandwidth extension. The adaptive biased voltage buffer itself is a current feedback loop (CFL), which not only pushes the pole at power FET gate to high frequency, but also speeds up the response to load changes. The sensed load current  $i_x$  and  $i_{bf}$  can further improve  $V_x$  and  $V_g$  voltage response to output load changes. The error amplifier is a folded cascode structure with a fixed DC biasing current. Hence, the DC gain of the error amplifier does not drop when the load current increases as compared to those adaptive biased error amplifiers. A high DC gain of the error amplifier enables better line regulation and load regulation even with the pass power transistor working in the linear region for smaller dropout voltage, which results in a smaller silicon area [19], [91], [92].

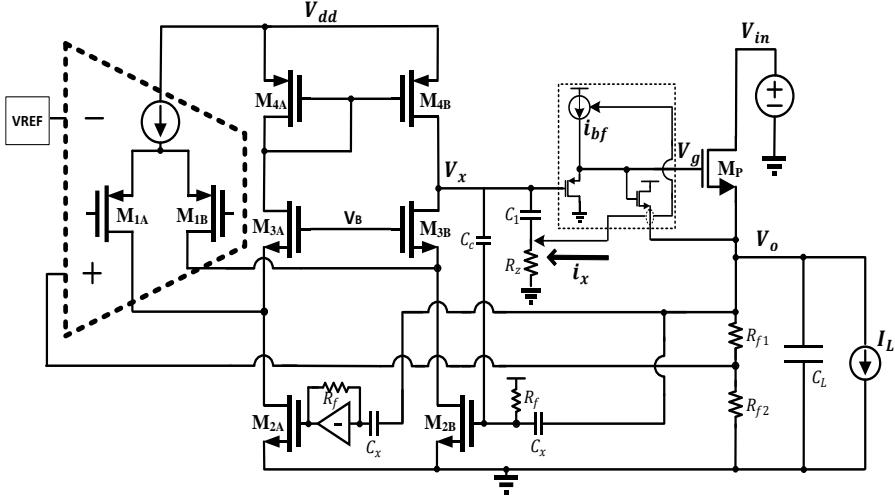
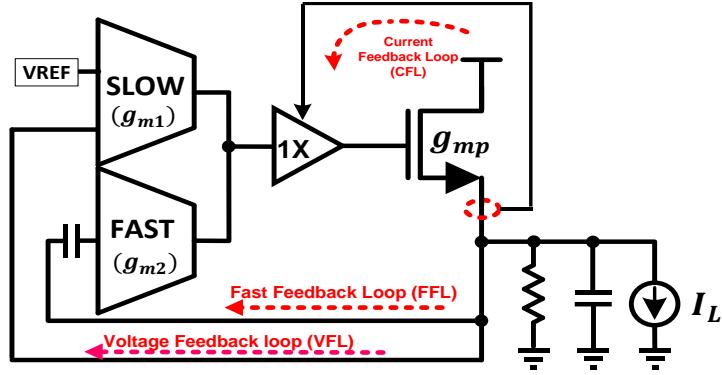


Figure 5.1 System architecture of the proposed LDO.

### 5.1.1. Conceptual stability analysis of multi-loop compensation

The proposed multi-loop compensation concept (MLC) is conceptually described in Figure 5.2(a) [82], [75]. It has three loops: the first one is VFL, it provides a high-precision regulation for the LDO. Second one is the fast response FFL. It provides a fast response to the load changes. The last one is CFL. It senses the load current and directly feedback to  $V_g$ . At light load condition, both VFL and FFL determine the overall loop stability. With medium or heavy load, the loop stability is determined by the FFL only, and the VFL has little impact on loop stability. In Figure 5.2(b),  $A_S(s)$  is the loop transfer function of the VFL. The dominant pole ( $p_1$ ) is located at the error amplifier's output.  $A_F(s)$  is the inner FFL's transfer function, which is a bandpass function. It determines the overall loop stability and the loop Unit-Gain-Frequency (UGF) of the LDO in medium and heavy load conditions. In the stability analysis, we do not break the CFL loop and treat it as part of  $A_S(s)$  and  $A_F(s)$ . Since the VFL and the FFL sum at the error amplifier output in parallel, the overall loop transfer function  $T(s)$  can be obtained as shown in Figure 5.2(b). A zero  $z_1$  is located at the frequency where

the VFL gain is equal to the FFL gain in magnitude since the two loops are summed together in parallel. At a frequency higher than  $z_1$ , the FFL gain is higher than the VFL gain, thus the FFL is the dominant loop at high frequency and determines the overall loop stability. As long as  $z_1$  is designed to be lower than the frequency of the FFL loop's dominant pole ( $p_3$ ), the loop bandwidth extension is achieved. Since the two loops are summing together in parallel instead of in series, the VFL has less impact on the overall loop stability as compared to previous work [83].



(a)

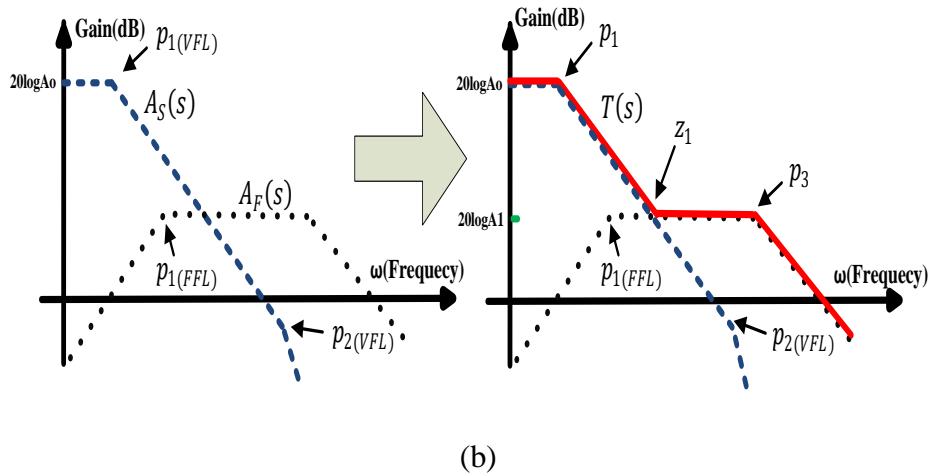


Figure 5.2 (a) Conceptual diagram of the multi-loop compensation. (b) Bode plot sketch of the multi-loop compensation.

### 5.1.2. Large-signal behavior of the fast feedback loop

Both FFL and CFL improve the LDO's load step response. For a large load step, the undershoot and overshoot of the LDO output voltage are dominated by the slew rate (SR) of  $V_x$  and  $V_g$ . The FFL improves SR( $V_x$ ) and the CFL improves SR( $V_g$ ). Figure 5.3(a) and Figure 5.3(b) depict the load step response enhancement mechanism. The mechanism is similar to the PMOS LDO design in Chapter 4.

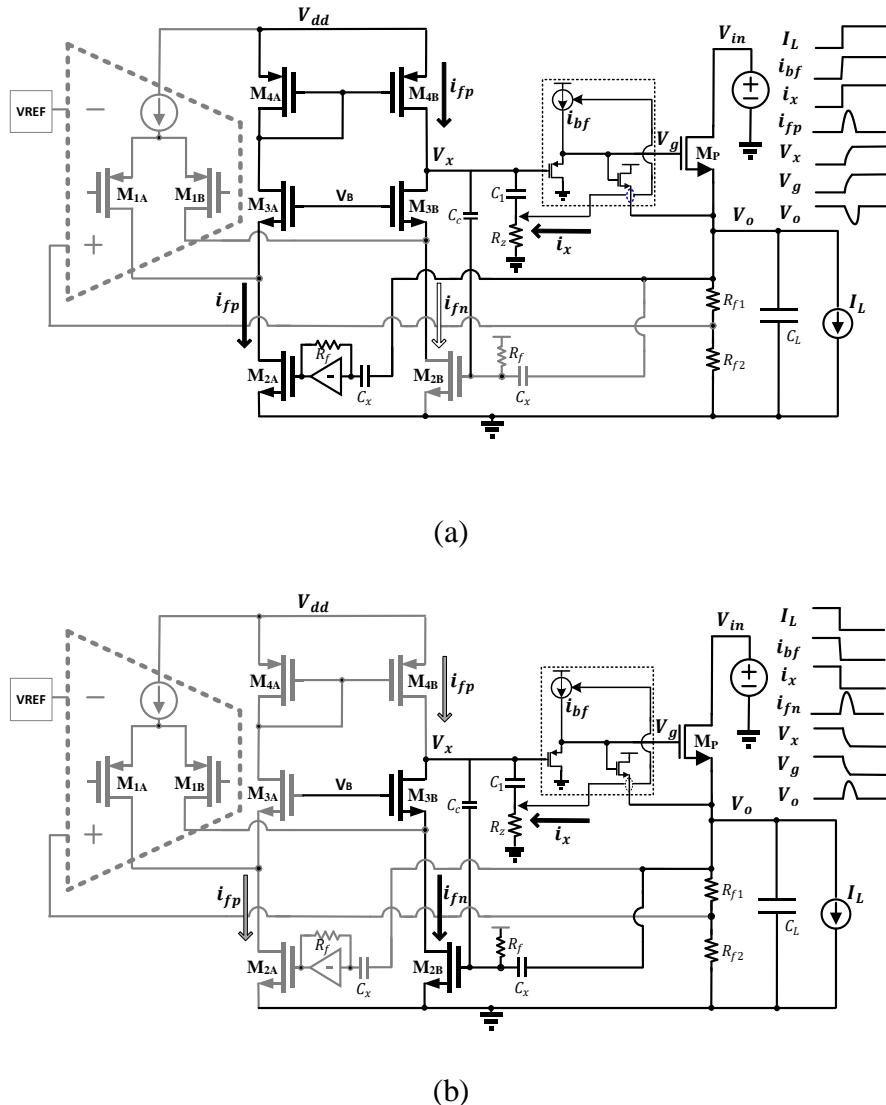


Figure 5.3 (a) Large signal transient response of LDO for load step-up. (b) Large signal transient response of LDO for load step-down.

## 5.2. Circuit implementation and stability analysis

The full transistor level implementation of the proposed LDO is depicted in Figure 5.4. The error amplifier is a folded cascode structure with a PMOS input pair ( $M_{1A}$  and  $M_{1B}$ ). The voltage feedback loop (VFL) consists of a resistor divider, the folded cascode amplifier, buffer and the power FET. The loop gain of VFL is high since the DC bias of  $M_{2A}$  and  $M_{2B}$  is not affected by the load current. It helps to improve the line/load regulation at heavy load condition, which is one of the main challenges of high current LDO design. A simple high-pass trans-impedance amplifier is applied to the existing error amplifier's DC bias circuit. Together with the amplifier output stage, buffer and the power FET, they form the fast feedback loop (FFL). Since the transconductance of  $M_2$  ( $g_{m2}$ ) is larger than  $M_1$  ( $g_{m1}$ ), the loop bandwidth is extended, which helps to speed up the load change transient response. For a heavy load LDO design with large power FET, a strong voltage buffer is typically used to improve the slew rate of the power FET gate voltage ( $V_g$ ). In this design, an adaptively biased super source follower (AB-SSF) is used as a voltage buffer. The buffer consists of  $M_7$ ,  $M_{8A}$ ,  $M_{8B}$ , and a bipolar transistor  $Q_1$ , and it drives the pass transistor  $M_P$ . This voltage buffer pushes the pass transistor gate pole to a frequency that is much higher than the UGF. Hence, this gate pole generally has minimum impact on the loop stability [22], [89]. In the proposed design, the loop dominant pole  $(-\frac{1}{R_1 \cdot (g_{m2} R_f C_c)})$  is determined by  $C_c$  instead of  $C_1$ , which is shown in Figure 5.4. Both  $C_c$  and  $C_1$  are small.  $C_L$  is the off-chip capacitor with the equivalent series resistance (ESR) of  $R_{esr}$

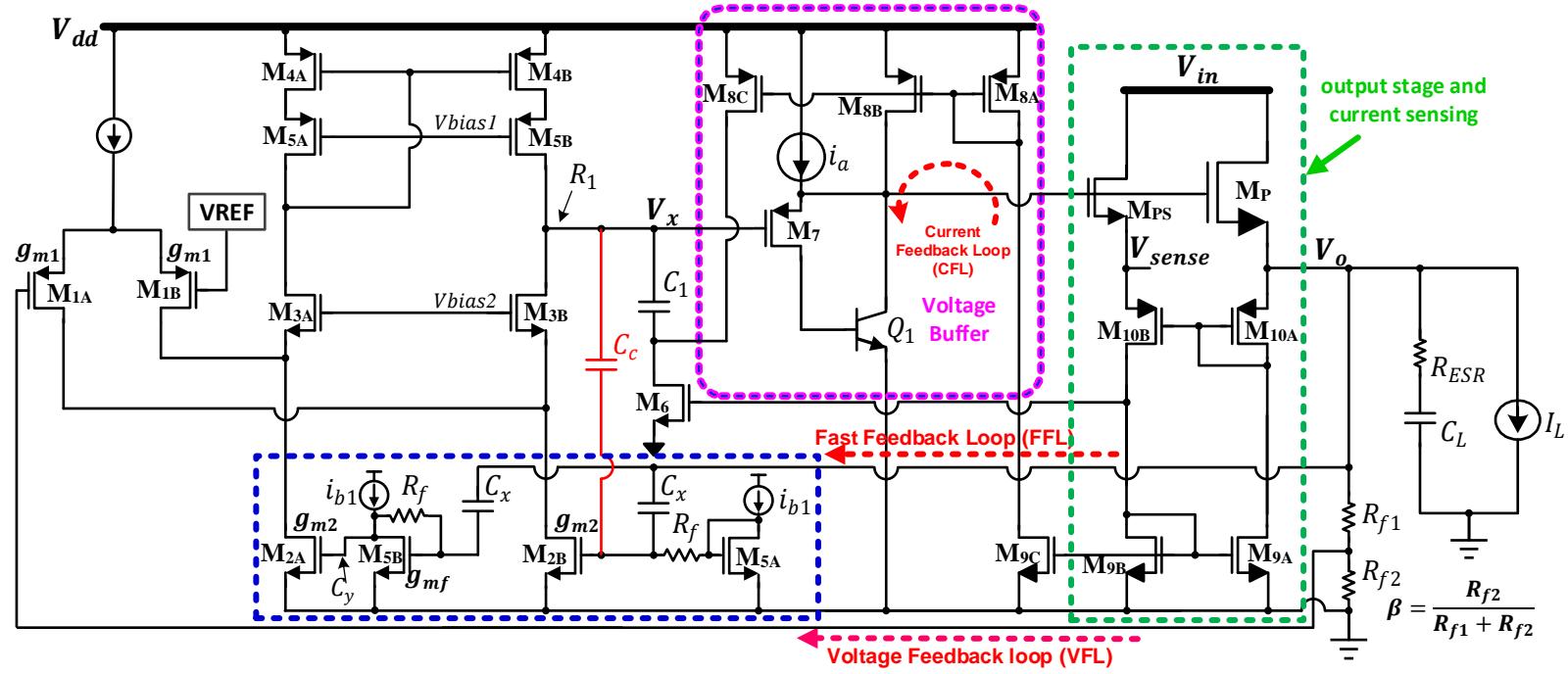


Figure 5.4 Schematic of the proposed NMOS LDO design.

### 5.2.1. The adaptive buffer with the fast current feedback loop

The super source follower voltage buffer with adaptive bias is widely used in PMOS LDO design [22], [39]. The same technique can also be used in this NMOS LDO. Similarly, the power FET gate pole is moved to a higher frequency minimizing its impact on the loop stability. Besides, the unique feature of this adaptive voltage buffer is also a current feedback loop (CFL). When the load current suddenly rises, the sensed current change is instantaneously applied to the gate ( $V_g$ ) of power FET through the current mirror  $M_{9C}$ ,  $M_{8A}$ , and  $M_{8B}$ . Concurrently, the sensed current is also applied to the resistor  $R_z$  (formed by transistor  $M_6$ ), so that the voltage across the resistor  $R_z$  increases proportionally to the load current. Hence, letting aside FFL and VFL, this CFL itself can help reducing the LDO output ( $V_o$ ) drop during the load current stepping events.

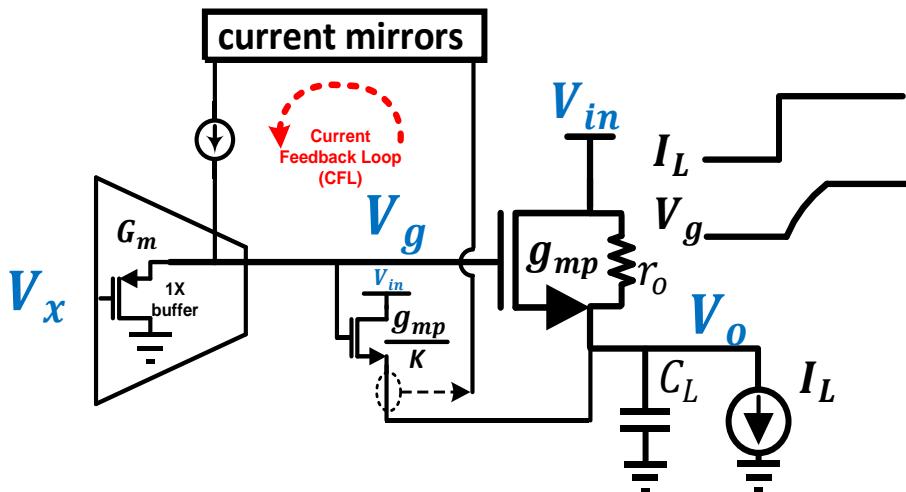


Figure 5.5 Small-signal model of the voltage spike detector

Being part of the main LDO loop, this adaptive biased voltage buffer helps achieving low LDO's output impedance, which is in the order of  $1/g_{mp}$ . The circuit model can be depicted in Figure 5.5. And the output impedance is

$$R_{out} \approx \frac{1}{g_{mp}} * \left( \frac{K * G_m}{g_{mp} + K * G_m} \right), \quad (5.2)$$

where  $K$  is the current sensing ratio,  $G_m$  is effective transconductance of the voltage buffer.  $g_{mp}$  is the power FET's transconductance. The adaptively biased voltage buffer itself further improves the load step response with its lower output impedance. However, the adaptively biased buffer in PMOS LDO does not help to reduce the output impedance.

The transfer-function from  $V_x$  to  $V_g$  can be derived as:

$$\frac{V_g}{V_x} = \frac{G_m K (sC_L + g_{mp})}{C_L C_g K s^2 + C_L G_m K s - C_L g_{mp} s + G_m g_{mp} K} \quad (5.3)$$

Its bandwidth is much higher than the loop UGF, and it has no impact on the loop stability.

### 5.2.2. The auto-self-voltage-shift circuit network (ASVS)

Although the dominant pole is no longer a function of  $C_1$  anymore,  $C_1$  is kept for transient enhancement by voltage steps across  $R_z$ . A large  $R_z$  and small  $C_1$  enhance the  $V_x$  response, while not loading the node  $V_x$ . As shown in Figure 5.3, an automatic self-voltage-shift network (ASVS) is formed by  $R_z$ ,  $C_1$  and the load current sensor. The voltage across  $R_z$  is proportional to the load current. It lifts or suppresses  $V_x$  node voltage when load current changes:

$$\Delta V_x = \frac{\Delta I_L}{K_e} R_z \quad (5.4)$$

Here,  $K_e$  is the current sensing ratio from  $I_L$  to the drain current of M<sub>8C</sub>. A properly designed  $K_e$  and  $R_z$  can enhance the transient response significantly.

The optimized value of  $K_e$  and  $R_z$  are shown in the equation:  $\frac{K_e}{R_z} \approx \frac{1}{g_{mp}}$ . Since the power FET's transconductance  $g_{mp}$  varies with the DC load current.  $R_z$  is realized by the transistor M<sub>6</sub>, which is reverse-proportional to the load current. It compensates the  $g_{mp}$  variation by first order.

The complete equivalent small-signal model of the whole LDO is depicted in Figure 5.6. The transconductance of the error amplifier input pair is modeled as  $g_{m1}$ . While the error amplifier's output impedance is denoted as  $R_1$ . The drain resistance of M<sub>6</sub> is  $R_z$ . While the effective output impedance of the super voltage source follower (M<sub>7</sub> and Q<sub>1</sub>) is  $1/G_m$ .  $g_{mp}$  represents the power FET transistor. For analysis purpose, the loop is broken at the common path of the VFL and FFL. The transfer function from  $V_x$  to  $V_g$  is represented by (5.3). Note that the capacitor  $C_x$  is in the order of pF range, which is considerably smaller than the off-chip capacitor. The current through the resistor divider is only 1  $\mu$ A, which is absorbed by the load current. In this way, the resistor divider ( $R_{f1}$  and  $R_{f2}$ ) can be modeled as the scaling factor  $\beta$  without loading effect.

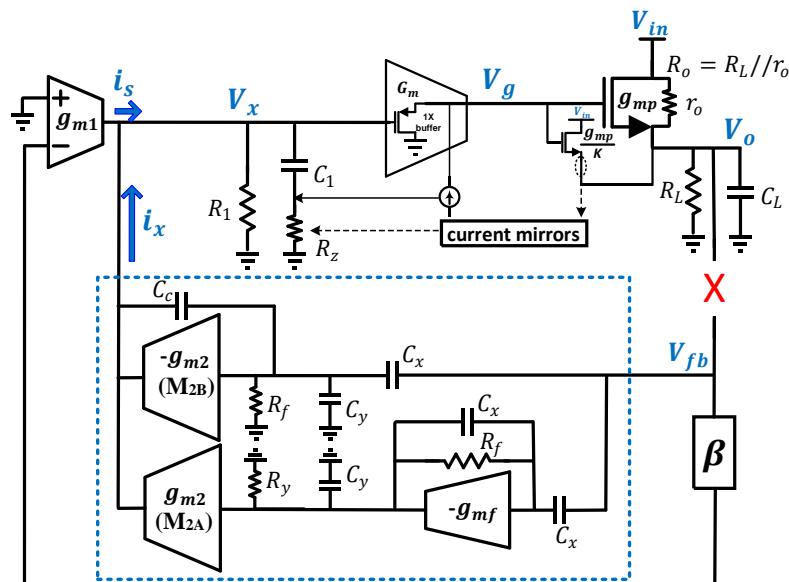


Figure 5.6 Small-signal model of the proposed LDO.

The transfer function of the LDO loop is derived based on the following considerations:

- c) The off-chip capacitor:  $C_L \gg (C_c, C_1)$ .
- d) The overall loop DC gain is  $g_{m1}R_1\beta$ . The gain of error amplifier remains constant.
- e)  $G_m$ ,  $g_{mp}$  and  $R_o$  vary with the load current.

The overall loop transfer function  $T(s)$  can be written as (5.5), (5.6), shown at the end of following page. The DC loop gain is  $A_0$ , which is expressed as (5.7).

$$A_0 = \frac{g_{mp}R_o}{g_{mp}R_o + 1} \beta g_{m1}R_1 \quad (5.5)$$

$$\begin{aligned} T(s) &= \frac{-g_{m1}R_1g_{mp}R_o\beta(R_zC_1s + 1)\left(\frac{2R_fC_xg_{m2}}{\beta g_{m1}}s + 1\right)(R_fC_xs + 1)}{(R_oC_ls + g_{mp}R_o + 1)(g_{m2}R_fR_zC_1R_1C_c s^2 + g_{m2}R_fR_1C_c s + 1)\left(\frac{C_x^2R_f}{g_{mf}}s^2 + R_fC_xs + 1\right)\left(\frac{C_g}{G_m}s + 1\right)} \\ &\approx \frac{-g_{m1}R_1g_{mp}R_o\beta(R_zC_1s + 1)\left(\frac{2R_fC_xg_{m2}}{\beta g_{m1}}s + 1\right)(R_fC_xs + 1)}{(R_oC_ls + g_{mp}R_o + 1)(\gamma R_zC_1s + 1)(g_{m2}R_fR_1C_c s + 1)\left(\frac{C_x^2R_f}{g_{mf}}s^2 + R_fC_xs + 1\right)\left(\frac{C_g}{G_m}s + 1\right)} \end{aligned} \quad (5.6)$$

$$T(s) = \frac{V_o(s)}{V_{fb}(s)} = \frac{-A_0\left(1 - \frac{s}{z_1}\right)\left(1 - \frac{s}{z_2}\right)\left(1 - \frac{s}{z_3}\right)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)\left(1 - \frac{s}{p_3}\right)\left(1 - \frac{s}{p_4}\right)\left(1 - \frac{s}{p_5}\right)\left(1 - \frac{s}{p_6}\right)} \quad (5.7)$$

In the light load condition,  $g_{mp}R_o \gg 1$ . The loop gain is  $\beta g_{m1}R_1$ . With heavy load,  $g_{mp}R_o$  could be less than 1. Hence, the loop gain is a few dB lower than the light load condition, which agrees with the simulation results. While most of the

reported LDO either only deliver less than 100mA current or suffer a load/line regulation drop due to adaptive biased error amplifier design, this design achieves a loop gain of 61dB even when the load current reaches 1A, giving a much better load/line regulation.

Table 5.1 List of loop poles and zeros of the proposed NMOS LDO.

Zeros	Poles
$z_1 = -\frac{\beta g_{m1}}{2R_f C_x g_{m2}}$	$p_1 = -\frac{1}{g_{m2} R_f R_1 C_c}$
$z_2 = -\frac{1}{R_z C_1}$	$p_2 = -\frac{1}{\gamma R_z C_1}$
$z_3 = -\frac{1}{R_f C_x}$	$p_3 = -\frac{g_{mp}}{C_L}$
	$p_4 = -\eta_1 \frac{g_{mf}}{2C_x}$
	$p_5 = -\eta_2 \frac{g_{mf}}{2C_x}$
	$p_6 = -\frac{G_m}{C_g}$

The loop transfer function  $T(s)$  has 3 zeros and 6 poles. They are summarized in Table 5.1. It can be verified by setting  $C_x$  to zero so that the overall transfer function  $T(s)$  can be simplified to the transfer-function of conventional single loop LDO. The loop dominant pole is  $p_1$ , which is a function of the compensation

capacitor  $C_c$  instead of  $C_1$  in the conventional NMOS LDO. Since the size of  $C_1$  does not affect the loop stability, a smaller size  $C_1$  is used for a better slew rate at  $V_x$  node. To simplify the derivation, an adjusting parameter  $\gamma$  (close to 1) is introduced for  $p_2$ .  $z_2$  and  $p_2$  are very close. Hence, effectively they cancel each other. The third pole  $p_3$  varies with the load condition, and it determinates the loop Unit-Gain-Frequency (UGF).  $z_3$  locates between  $p_4$  and  $p_5$  to improve the loop phase margin. Here,  $p_5 > \text{UGF}$ .  $p_6$  is always far away from UGF and it has no impact on loop stability.  $p_4$  and  $p_5$  are the eigenvalues of the second-order polynomial in the denominator. The two parameters  $\eta_1$  and  $\eta_2$  are:

$$\eta_1 = 1 - \sqrt{\left(1 - \frac{4}{g_{mf}R_f}\right)} \quad (5.8)$$

$$\eta_2 = \sqrt{\left(1 - \frac{4}{g_{mf}R_f}\right)} \quad (5.9)$$

It requires  $g_{mf}R_f > 4$  to avoid the complex conjugate poles in  $T(s)$ , which makes a more stable loop.

In medium and heavy load condition ( $>10\text{mA}$ ),  $g_{mp}$  is large and it is sqrt-proportional to the load current. The third pole  $p_3$  varies with load current. When the load current increases,  $g_{mp}$  becomes larger. Hence,  $p_3$  moves to high frequency and it becomes the dominant pole of the FFL, which determines the overall UGF. Meanwhile,  $g_{m1}$ ,  $g_{m2}$ ,  $g_{mf}$ , and  $R_1$  remain same as their values at light load condition. The loop magnitude plot is shown in Figure 5.7. The loop gain at  $z_1$  is denoted as  $A_1$  with the expression:

$$A_1 \approx \frac{2C_x}{C_c} \quad (5.10)$$

Where the ratio of  $C_x$  and  $C_c$  determines the magnitude of  $A_1$ . A smaller  $A_1$  helps to improve the loop phase margin, but results in narrower bandwidth extension. Therefore, the UGF trades off with the phase margin on  $A_1$  magnitude. In this proposed design,  $A_1$  is close to 20dB. The UGF can be approximated as

(5.11) .

$$\omega_o \approx A_1 * p_3 = \frac{2C_x}{C_c} \frac{g_{mp}}{C_L} \quad (5.11)$$

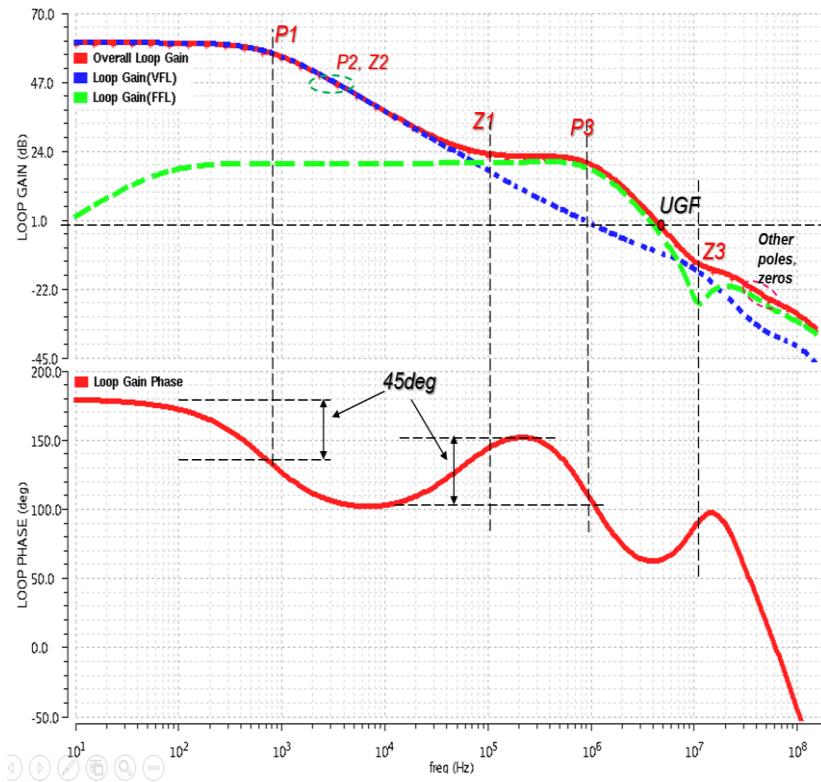


Figure 5.7 Loop frequency response (simulation) of the proposed LDO at medium to heavy load conditions.

It is a function of load current. The gain plot of the VFL, FFL and overall loop are shown in Figure 5.7. The VFL is the slow feedback loop and its UGF is small.

The FFL loop is a bandpass function with its UGF in the order of a few MHz at medium and heavy load conditions. Combining the VFL and the FFL gives the overall loop gain and its phase. At full load condition, a 61dB DC gain and a 60° phase margin are achieved. The UGF is widely extended compared to the counterpart conventional design without consuming extra quiescent current.

At light load condition (0-10mA),  $g_{m1}$ ,  $g_{m2}$ ,  $g_{mf}$  maintain constant, and  $g_{mp}$  is small, and the DC loop gain  $A_0$  is equal to the gain of the error amplifier. In this design, the DC loop gain is approximately 61dB for light load conditions. Under light load condition,  $p_3$  moves to a lower frequency and the UGF is reduced, which is much smaller than the frequencies of  $z_3$ ,  $z_4$ ,  $p_4$ ,  $p_5$ , and  $p_6$ . The transfer function can be simplified as:

$$T(s) = \frac{V_o(s)}{V_{fb}(s)} \approx \frac{A_0 \left(1 - \frac{s}{z_1}\right) \left(1 - \frac{s}{z_2}\right)}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) \left(1 - \frac{s}{p_3}\right)} \quad (5.12)$$

$z_2$  and  $p_2$  are in the same order and they cancel each other.  $z_1$  and  $p_3$  are also close to each other. The overall loop now becomes a single-pole system with a dominant pole of  $p_1$ . The UGF can be simplified to (5.13).

$$\omega_o \approx A_0 * p_1 = \frac{\beta g_{m1}}{g_{m2} R_f C_c} \quad (5.13)$$

At both heavy load and light load conditions, the loop UGF does not depend on  $C_1$ . As a small size  $C_c$  is used as the compensation capacitor instead, it benefits the slew rate during the load transient response and extends loop bandwidth. From Figure 5.4,  $M_{4A}$  and  $M_{4B}$  are reused from the original current bias circuit such that it does not consume extra quiescent current as compared to the

conventional counterpart. In the simulation,  $R_{esr}$  value is set to a few mΩ to emulate the ceramic capacitor. The off-chip capacitor ESR zero has minimum impact on the stability of the regulator. Figure 5.8. depicts the simulated loop gain/phase of the LDO over different load conditions (from 10μA to 1000mA). However, Equation (5.12) does not exact match the simulation because we have to do some simplifications. The circuit simulation optimization ensures that the LDO is stable for all load conditions.

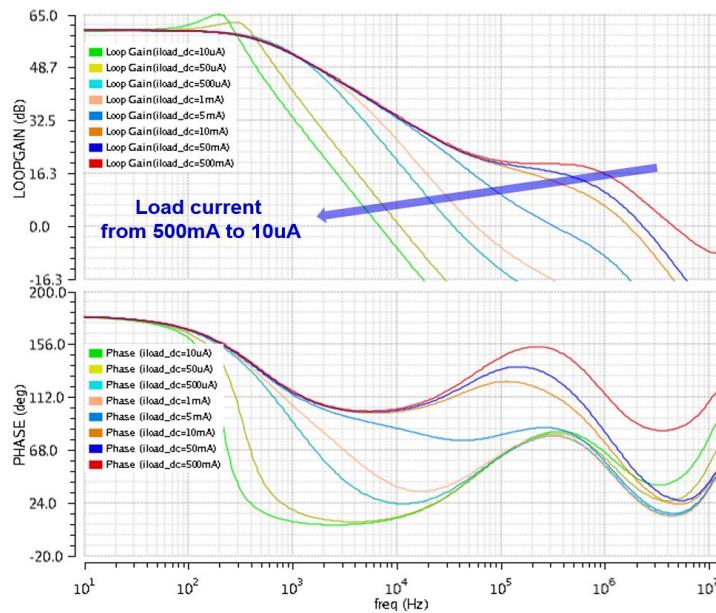


Figure 5.8 Simulation results of loop gain/phase of the proposed LDO with load current of 10μA, 50μA, 500μA, 1mA, 5mA, 10mA, 50mA, 500mA.

### 5.3. Experimental results

To verify the concept of this multi-loop high DC loop gain NMOS linear regulator, a prototype IC is implemented and fabricated with a 0.13μm SOI CMOS process where NMOS' and PMOS' threshold voltages 0.5V and -0.7V respectively. The layout and micrograph of the proposed design are shown in Fig. 10. The active area of the whole LDO is 325μm × 106μm, excluding the PAD

for testing. The chip area occupied by the controller is  $161\mu\text{m} \times 106\mu\text{m}$ , which is 49% of the whole LDO. To provide high output current ( $>1\text{A}$ ), power FET size is  $25000\mu\text{m}/200\text{nm}$  (W/L) with a silicon area of  $164\mu\text{m} \times 106\mu\text{m}$ . This LDO can be used for the supply of DDR or other loads which require fast transient response and small voltage variation window.

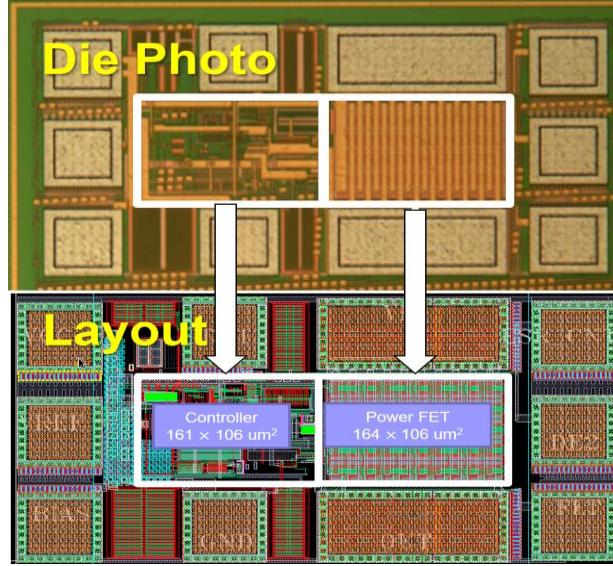
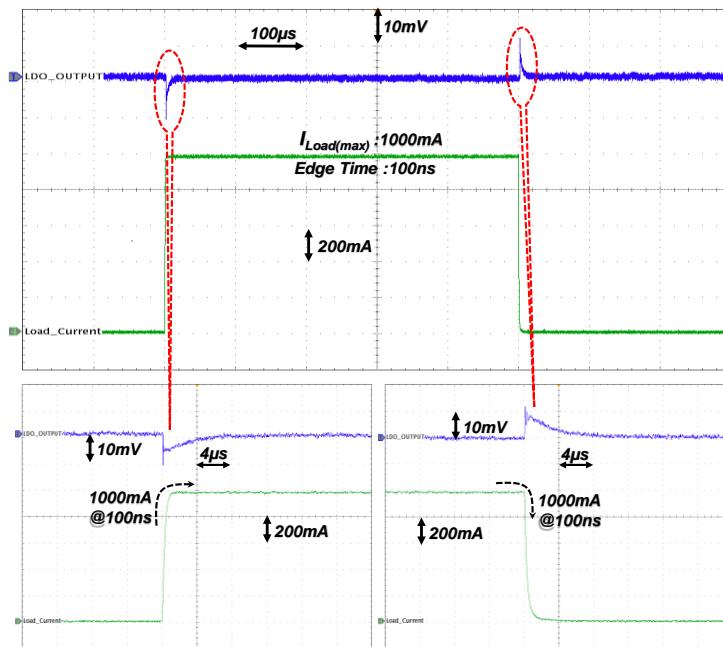


Figure 5.9 Chip micrograph and layout.

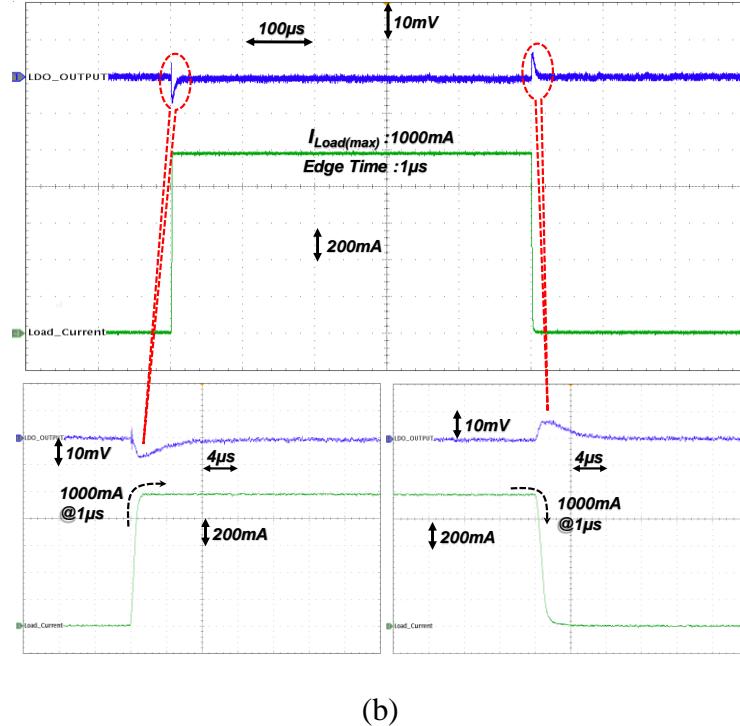
Since the FFL circuit does not require extra bias current, the quiescent current for the error amplifier is  $25\mu\text{A}$  regardless of the load condition. The quiescent current for the voltage buffer is  $9\mu\text{A}$  at light load condition and  $1000\mu\text{A}$  at maximum load ( $1000\text{mA}$ ) respectively. The maximum efficiency is 99.9% with  $1000\text{mA}$  load. For stability, the compensation capacitor  $C_c$  is  $120\text{fF}$ , which is much smaller than the compensation capacitor (typically,  $5-15\text{pF}$ ) in the conventional LDO. In this design,  $C_1$  is  $1\text{pF}$ , which is for the transient voltage boost rather than loop stability compensation.

The fabricated silicon has been tested for transient load regulation with an off-chip  $1\mu\text{F}$  capacitor at  $V_o$  of  $1.8\text{V}$ . The results are shown in Figure 5.10. When the

load current changes at the 1000mA/100ns step, the measured undershoot and overshoot are 11mV and 12mV respectively as shown in Figure 5.10(a). When the load current changes at the 1000mA/1μs step, the measured undershoot and overshoot are both 8mV as shown in Figure 5.10(b). The output voltage error is less than  $\pm 1\%$  over the entire operating range. The DC variation across 1000mA load is around 600  $\mu$ V, giving a load regulation of 0.6  $\mu$ V/mA. This good DC load regulation is achieved with very high current loading, thanks to the high DC loop gain with dynamic bias scheme.



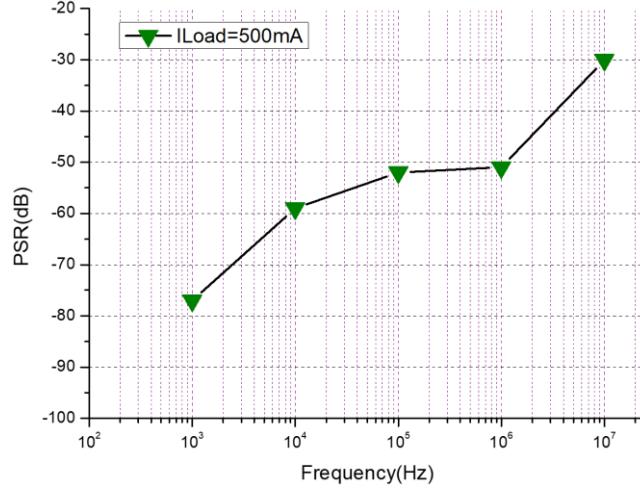
(a)



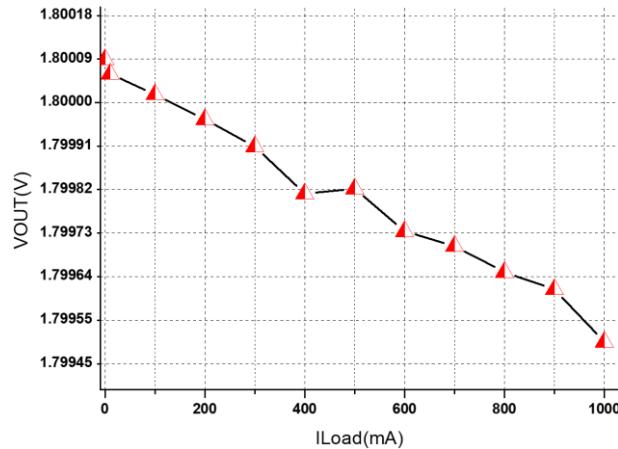
(b)

Figure 5.10 Measured output transient response of 1000mA load step. (a) The transient response of the load current steps of 1000mA in 100ns. (b) The transient response of the load current steps of 1000mA in 1μs.

The power supply rejection (PSR) was tested by injecting a sinusoidal signal superposed to a DC input voltage supply through a bias tee and observing the output voltage ripple amplitude [70]. is shown in Figure 5.11(a). The proposed LDO achieves -51dB PSR at 100kHz, -50dB PSR at 1MHz when  $I_{Load}=500mA$ . The measured load regulation is shown in Figure 5.11(b).



(a)



(b)

Figure 5.11 (a) Measured PSR versus frequency for  $I_{Load}=500mA$  when  $V_{out}=1.8V$ ,  $V_{in}=2V$ , and  $CL=1\mu F$ . (b) Measured load regulation when  $V_{out}=1.8V$ ,  $V_{in}=2V$ .

A performance comparison with some recent capacitor-based LDO designs is shown in Table 5.2, which clearly proves the performance enhancement of this design. The proposed LDO architecture offers many advantages for a regulator with heavy load applications, which is widely used in battery-powered systems nowadays. Without specifying a requirement for output capacitor ESR, the

proposed multi-loop design technique makes the loop stable even with an extended loop bandwidth. Meanwhile, to the best of our knowledge, the maximum 1000mA load is also the highest load capability over current state of arts. A decent DC loop gain is still maintained to achieve  $0.6\mu\text{V/mA}$  DC load regulation.

As the proposed design has a very high slew rate during the load transient, it achieves the smallest undershoot and overshoot with heavy load attack. Finally, a figure of merit ( $FOM = C_L \Delta V_o I_q / \Delta I_{L,max}^2$ ) (written as a new formula) from [2] is adopted for a fair comparison, where  $C_L, \Delta V_o, I_q, \Delta I_{L,max}$  are the output capacitor, the output voltage variation due to the load transient steps, the quiescent current, and the maximum load current step. This study obtains the smallest FOM, which demonstrates to be a good candidate for battery-powered portable applications.

Table 5.2 Performance summary of the proposed NMOS LDO.

References	TPE 2010 [89]	JSSC 2010 [84]	TPE 2016 [82]	TPE 2017 [39]	JSSC 2017 [2]	This work
<b>CMOS technology</b>	0.35μm	90nm	0.18μm	0.18μm	0.13μm	0.13μm
<b>Power-MOS type</b>	PMOS	PMOS	PMOS	PMOS	NMOS	NMOS
<b>Chip area [mm<sup>2</sup>]</b>	0.146	0.00274	0.024	0.0285	0.1825	0.0345
<b>Output capacitor, C<sub>L</sub> [μF]</b>	1	1	1	1	1	1
<b>Nominal output voltage [V]</b>	1.8	0.9	1	1.2	1	1.8
<b>Dropout voltage[mV]</b>	200	100	200	200	30	200
<b>Quiescent current, I<sub>Q</sub> [μA]</b>	30-75	9.3	135.1	1.6-200	14-120	35-1000
<b>Max. current efficiency [%]</b>	99.9	99.9	99.86	99.6	99.96	99.9
<b>Max. load current step [mA]</b>	160	50	100	50	300	1000
<b>Load transient undershoot [mV]</b>	30	6	25	24	56	11
<b>Load transient overshoot [mV]</b>	65	12.1	7.5	5	24	12
<b>Load regulation<sub>1</sub> [μV/mA]</b>	90	82	75	100	6	0.6
<b>Line regulation [mV/V]</b>	6	14	22.7	5.5	0.44	0.23
<b>PSR(dB)@ measured frequency and load current</b>	N/A	-54 (100kHz, 50mA)	-35 (100kHz, 100mA)	-30 (10MHz)	-50 (10kHz, 300mA)	-51 (100kHz, 500mA)
<b>FOM [ps]*</b>	111.3	67.3	439	18.5	12.44	0.805

$$* FOM = C_L \Delta V_o I_q / \Delta I_{L,max}^2$$

## **5.4. Conclusions**

In conclusion, a fast-transient response low-dropout regulator (NLDO) for portable mobile applications with multi-loop compensation has been presented. By modifying the amplifier's biasing circuit, a voltage spike detector circuit together with the DC biasing circuit forms a fast feedback path for the LDO. This adaptive biased voltage buffer is the part of the whole LDO loop, which makes the LDO's output impedance lower compared to the conventional design. These significantly enhance the large-signal transient response and extends the loop bandwidth without consuming extra quiescent current as compared to the conventional one. Without using the adaptive bias scheme to adjust the DC bias of the error amplifier, a high DC loop gain ( $>60\text{dB}$ ) is kept across different load conditions for a better line regulation and load regulation performance. The proposed compensation scheme relaxes the output capacitor's requirement, which enables the usage of small size multilayer ceramic capacitors in real applications. The LDO can deliver as high as 1000mA load current with 200mV dropout voltage. It achieves a 10mV voltage spike with a load step of 1000mA within 100ns.



# **Chapter 6**

## **Conclusions and future works**

This Chapter draws the conclusions of the work reported in this Ph.D. research program and delineates recommendations for future work.

### **6.1. Conclusions**

This work pertains to the design and realization of the high-performance analog linear voltage regulators in the CMOS process. The target applications for these LDOs are the battery-powered portable devices. The conclusions of this research work are as follows.

With a clear understanding on the background and motivation, objective has been set to explore techniques that could advance the PMIC design for battery-powered portable devices, with better transient response, smaller area and lower quiescent current.

LDO Architecture, performance metrics, and general design considerations have been discussed and summarized. A comprehensive literature review is done on loop stability compensation techniques, where Ahuja compensation, multi-loop compensation, and pole-zero cancellation techniques are discussed in detail. Prior-art transient response enhancing methods are also reviewed.

Several novel techniques have been developed to improve loop stability, transient response, and line/load regulations, while maintaining low quiescent current and

small silicon area. Three LDOs have been designed, fabricated and tested to verify the proposed solutions.

The first LDO features a novel buffer design, which reduces output impedance for better loop stability while giving rail-to-rail output swing that enables a smaller power transistor for cost saving. A dynamic sensing scheme is also used to make the design robust. And a low-cost offset trimming method is introduced for high production yield.

The second LDO uses a dual-loop compensation scheme, where the fast feedback loop (FFL) employs direct output voltage spike detection through the capacitive coupling, resulting in significantly improved, large-signal transient response and extended loop bandwidth, and the constant biased voltage feedback loop (VFL) has a loop gain larger than 60 dB, ensuring a good line and load regulation. A pseudo-equivalent series resistance (ESR) technique is also proposed to further improve loop stability and makes it possible to use low-cost, multilayer ceramic capacitors. This LDO can drive up to 600mA load current with good transient response.

The third LDO implements a novel multi-loop feedback scheme, which delivers superior transient response, achieving 10mV overshoot/undershoot at 1A/100ns load steps. It also includes an unique frequency compensation method that enables a stable 60dB DC gain across 1A load current variation. Significant improvement on load/line regulation is thus achieved compared to state-of-art LDO designs.

The designs achieve decent performance metrics while consuming reasonable quiescent currents when they are benchmarked against several state-of-the-art counterparts.

As a general conclusion, we have made significant contributions to the design and realization of a high-performance LDO with fast transient and good load line regulation performance for portable battery-powered applications.

## 6.2. Future works

Based on the literature review and the research work in this research program, we recommend the design of low noise, high PSR LDO for the mobile cameras as future work.

Modern mobiles often integrate multiple high-resolution cameras. Image sensors for these cameras are very sensitive to supply noise. In view of this, low noise LDOs are in great demand and is becoming the key for high-resolution mobile camera.

(1) An investigation into the design of an LDO with the extremely low noise level for camera sensor applications. Figure 6.1 depicts the block diagram of the typical low noise LDO design.

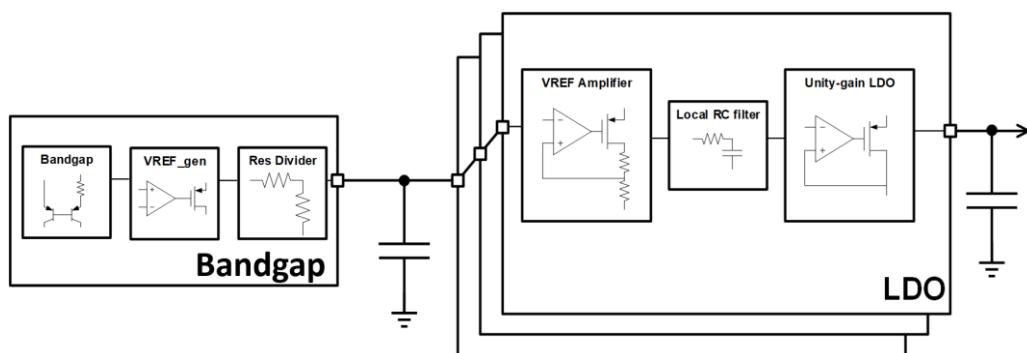


Figure 6.1 The typical circuit diagram of the low noise LDO design.

With a feedback factor of one, the error amplifier's input-referred noise is not amplified. A local RC filter is added to filter away the majority of the noise from bandgap and voltage reference (vref) generator. However, the overall output noise is still dominated by the bandgap reference noise. To achieve a noise level  $V_{rms}(\text{noise}) < 10\mu\text{V}$ , the design of a low noise bandgap reference is as important as the design of a low noise LDO itself. Figure 6.2 depicts the system solution of the extremely low noise LDO design.

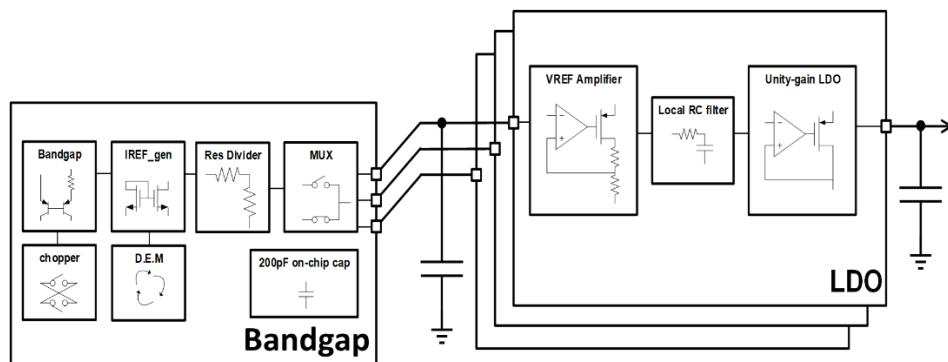


Figure 6.2 The system solution of the extremely low noise LDO design.

The flick noise of the bandgap is the main noise contributor for the whole system. A chopper stabilization and dynamic elements matching (DEM) can be used for noise reduction.

(2) An investigation into the design of an LDO with high power supply rejection for camera sensor applications.

As delineated in Chapter 3, the Ahuja compensated LDO structure has a superior power supply rejection compared to the normal Miller compensated LDOs with the same designed loop bandwidth. In the design examples in Chapter 4 and Chapter 5, the multi-loop compensation techniques are used not only to extend the loop bandwidth to improve the load transient response performance, but also

to improve the supply rejection. However, the supply rejection at the frequency of zero ( $z_1$  in Table 4.1 and Table 5.1) is not improved as compared to Ahuja compensated LDOs. It is worthy studying further on the mechanism of supply rejection of the bandwidth-extended LDO. A feedforward path from supply to an internal node can be added to achieve supply ripple cancellation while not impacting the original frequency compensation scheme for transient response enhancement.



## **Author's publications**

### **Journal publications**

1. K. Li, C. Yang, T. Guo and Y. Zheng, "A Multi-Loop Slew-Rate-Enhanced NMOS LDO Handling 1-A-Load-Current Step With Fast Transient for 5G Applications," in *IEEE Journal of Solid-State Circuits*, doi: 10.1109/JSSC.2020.3005789.
2. K. Li, X. Xiao, X. Jin, and Y. Zheng, "A 600-mA, Fast-Transient Low-Dropout Regulator With Pseudo-ESR Technique in 0.18- $\mu$ m CMOS Process," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, pp. 1–11, 2019, doi: 10.1109/TVLSI.2019.2947534.
3. Kan Li, Yuanjin Zheng, Siek Liter, "A transient-enhanced low dropout regulator with rail-to-rail dynamic impedance attenuation buffer suitable for commercial design." *Microelectronics Journal*, 63 (2017): 27-34.

### **Conference publications**

1. K. Li, C. Yang, T. Guo and Y. Zheng, "A multi-loop slew-rate enhanced NMOS LDO handling 1A load current step with fast transient" *IEEE, International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, May 17-20 2020.



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