A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors

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***Abstract*— In this article, we present a pseudoflash-based digital low dropout (Digital LDO) voltage regulator. The novelty of our pseudoflash-based Digital LDO (PFD-LDO) voltage regulator lies in the fact that we use pseudoflash (or alternately, flash) transistor subarrays for voltage regulation. By changing the threshold voltage (and thereby, the ON resistance) of these transistors, we can use the *same* design to meet different regulator specifications. The threshold voltage can be programed either at the factory by the manufacturer or in the field by the user. This gives the manufacturer the ability to offer a *family* of LDO regulators with a *single* design, a significant economic advantage. In addition, aging effects and temperature variations are effectively erased since the threshold voltage of the pseudoflash (or flash) transistors can be tuned to a fine degree in the field. Similarly, process variations can be canceled after manufacturing in the factory. These advantages are absent in traditional LDO regulators. Our design uses two subarrays. A coarse subarray is used to reduce the recovery time and output voltage overshoot/undershoot, while a fine subarray regulates the output voltage, minimizing the output voltage ripple. Unlike state-of-the-art LDO regulators, our design can realize multiple specifications with the *same* circuit. For example, we demonstrate that the V_{out} of the proposed PFD-LDO regulator can range from 0.7 to 1.7 V when the supply voltage V_{IN} ranges from 0.8 to 1.8 V, using the *same* circuit design. Over this voltage range, the proposed PFD-LDO regulator achieves V_{shoot} < 573 mV, t_{rec} < 0.50 μs, and V_{ripple} < 7.4 mV when the I_{max} ranges from 15 to 250 mA.**

***Index Terms*— Digital low dropout (LDO) regulator, low output voltage ripple, multiple current ranges, pseudoflash transistor.**

I. Introduction

RECENTLY, there has been significant adoption of low-power internet of things (IoT) devices. For these applications, as well as for integrated circuits (ICs) that utilize advanced fabrication processes, the supply voltage of ICs has been decreasing. Conventional analog low dropout (Analog LDO) regulators exhibit poor regulation because of an insufficient gain of analog error amplifiers when operated at low supply voltages. To handle this problem, Digital low dropout (Digital LDO) regulators have gradually attracted attention.

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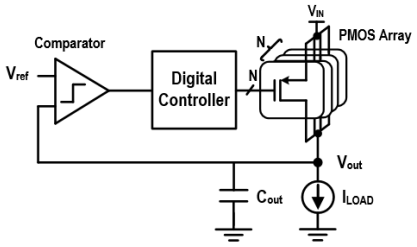

Fig. 1. Conventional Digital LDO regulator.

Unlike Analog LDO regulators, Digital LDO regulators are able to work at lower supply voltages due to the absence of a need for analog error amplifiers. Furthermore, passive components (capacitors) are not required to increase stability in Digital LDO regulators [1]. At last, it takes less time and design resources to build Digital LDO regulators since most circuit components are automatically synthesized using standard cells [1], while Analog LDO regulators require manually designed circuit components.

Fig. 1 illustrates a conventional Digital LDO regulator. It comprises a comparator, a digital controller, and an array of N equal-sized pMOS transistors. The comparator monitors the difference between the output voltage (V_{out}) and a reference (V_{ref}). The digital controller receives the error signal from the comparator and adjusts the number of transistors of the pMOS array that are turned on based on the control algorithm that it implements. The circuit thus produces enough current to match the output load current (I_{LOAD}) while maintaining a constant V_{out}. Each transistor in the pMOS array can be modeled as a fixed resistor since it is operated in the deep linear region [as shown in Fig. 2(a)]. The impedance of each pMOS device is obtained by (1), where μ_p is the hole mobility, C_{ox} is the capacitance of the gate oxide per unit area, W and L are the width and length of the pMOS transistor, respectively, and V_{SG} and V_{tp} are the voltage from source to gate and the threshold voltage of the pMOS transistor, respectively

$$R_{ds,\,on} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{tp}|)}. \tag{1}$$

For an LDO regulator, the performance metrics of interest are as follows.

1) The minimum and maximum output current (I_{min} and I_{max}, respectively).
2) The output voltage ripple V_{ripple} (which is defined as the change in V_{out} under steady-state operation).

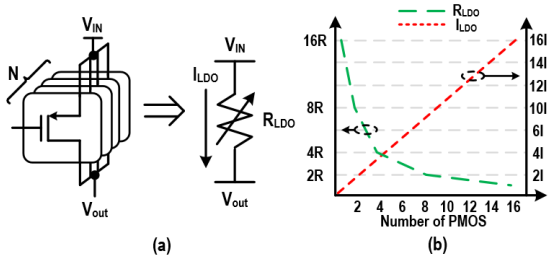

Fig. 2. (a) pMOS array equivalent model and (b) digital LDO regulator output resistance and current with different number of pMOS transistors turned on.

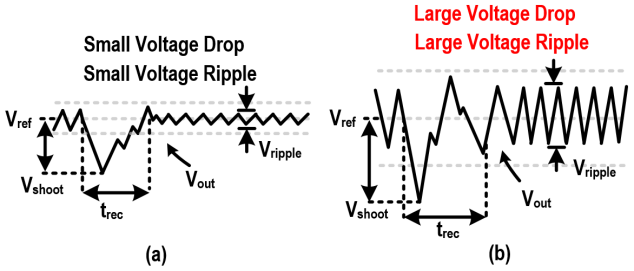

Fig. 3. (a) Correct current range and (b) wrong current range using the same Digital LDO regulator.

3) The output voltage overshoot/undershoot V_{shoot} (which is defined as the instantaneous change in V_{out} when the I_{LOAD} changes from I_1 to I_2).
4) The recovery time t_{rec} (which is defined as the time that it takes for V_{out} to return to within $V_{\text{ref}} \pm V_{\text{ripple}}$ after the I_{LOAD} changes from I_1 to I_2).

These parameters are pictorially described in Fig. 3(a).

A Digital LDO regulator linearly regulates the current by controlling the number of pMOS transistors that are turned on in parallel, as shown in Fig. 2(b). The size and number of pMOS devices determine the Digital LDO regulator's performance metrics like I_{max}, I_{min}, V_{ripple}, t_{rec}, and V_{shoot}. Some Digital LDO regulators use two or more pMOS subarrays to reduce the output voltage ripple [2], [3], [4], [5], [6].

In traditional Digital LDO regulators, the size (which corresponds to the resistance) of the transistors in the pMOS arrays cannot be modified once the circuit is manufactured. As a result, such Digital LDO regulators can only operate with a fixed current and voltage specification. Moreover, the impedance of each pMOS transistor in the pMOS array is sensitive to device width, length, and threshold voltage (V_t) variations. Each pMOS transistor is therefore not able to provide the same current, negatively affecting V_{ripple}, V_{shoot}, V_{out}, and t_{rec}, thereby making such a Digital LDO regulator susceptible to process variations.

For example, if the Digital LDO regulator is operated outside its current or voltage specification, its regulation capability is degraded, and V_{out} is no longer stable. This is because the impedance of the pMOS used in the pMOS array is fixed. Fig. 3(a) shows the V_{out} with low V_{ripple}, and a small V_{shoot} when the I_{LOAD} changes instantaneously. Fig. 3(b) shows the case when V_{shoot} and V_{ripple} are unacceptably large, when the Digital LDO regulator is operated in an incorrect current range. A similar problem can occur if the Digital LDO regulator is operated outside its V_{out} specification.

In this article, a pseudoflash[1]-based Digital LDO (henceforth referred to as PFD-LDO) regulator is proposed. We use a vanilla CMOS process to achieve the same behavior of the flash transistor [7], [8], [9]. Hence, we name it a "pseudoflash transistor." This article does not claim to invent the Digital LDO architecture, nor does it claim to invent a coarse-fine LDO subarray topology. Our key contribution is the *use* of pseudoflash pMOS transistors in the coarse and fine subarrays. This choice gives our proposed PFD-LDO regulator several advantages over a traditional Digital LDO regulator.

1) Manufacturers can tune the V_t of the pseudoflash subarrays and thus use the *same* circuit design to realize various Digital LDO regulators with varying specifications such as V_{IN}, V_{out}, I_{max}, I_{min}, and V_{ripple}, thereby reducing design costs remarkably, and achieving an economic advantage.
2) We can vary the V_t of the pseudoflash transistors (at the factory or even in-field) to tune the current range, voltage, and other characteristics of the regulator.
3) Using pseudoflash transistors, we are able to cancel device width, length, and V_t variations (after manufacturing, in the factory) that conventional Digital LDO regulators cannot do. Hence, our design is tolerant to process variations.
4) By using pseudoflash transistors, the V_t can even be adjusted in the field by the user, to cancel temperature or aging effects.
5) The impedance of each pseudoflash transistor can be altered precisely by programming its V_t precisely.
6) The use of pseudoflash transistors instead of traditional flash transistors reduces the cost of fabrication significantly, since flash transistors need additional processing steps.

We note that the pseudoflash transistors in our PFD-LDO regulator could be replaced by traditional flash transistors as well, since they both have the same electrical behavior.

The organization of this article is as follows. Section II presents a brief background on flash and pseudoflash transistors. Section III provides the architecture of our proposed PFD-LDO regulator, and Section IV presents an analytical model to analyze the stability of our coarse-fine controller. Section V discusses the experimental results of our implementation and compares our implementation with prior works. Finally, in Section VI, we present our conclusions.

II. Background: Flash and Pseudoflash Transistors

A. Flash Transistor

Fig. 4 illustrates a floating gate (flash) transistor [7], [8], [9], which is a field-effect transistor (FET) having two gates. The first gate is a control gate and it is similar to a regular MOSFET's gate, both physically and functionally. Additionally, a flash transistor has a second buried (and uncontacted)

[1]Although we use pseudoflash transistors in this article, one could use flash transistors as well.

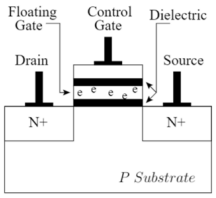

Fig. 4. Flash transistor.

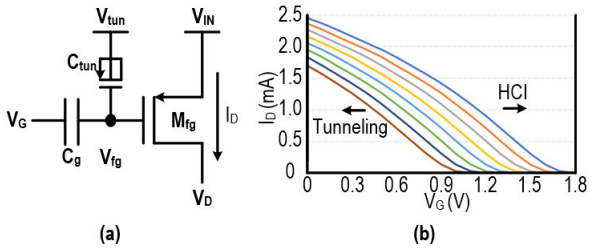

Fig. 5. (a) Circuit diagram and (b) I_{D}–V_{G} curve of pseudoflash transistor.

floating gate. Programming and erasure of the flash device are achieved by electrons tunneling into (or out of) the floating gate, respectively, via Fowler–Nordheim (FN) tunneling [10]. Erasure causes a drop in the threshold voltage (V_t) of the transistor, and programming causes an increase in the V_t of the transistor.

To cause erasure, we elevate the substrate (bulk) voltage of the flash transistor, drive the control gate to GND, and float the source/drain terminals. Programming is done by increasing the gate voltage of the device, while driving the bulk, source and drain terminals to GND. Programming is done individually for each device. The final value of the V_t is determined by the duration and magnitude of the programming pulses, as dictated by the incremental step pulse programming (ISPP) model [11]. In general, the device is subjected to many program-verify cycles until the desired V_t is achieved.

Once electrons are trapped in the floating gate, they remain trapped for several years [12], [13], or until removed by an erase operation. Also, flash transistors reside on the same IC die as a CMOS transistor. Finally, flash transistors have a finite number of programming cycles (10–100 K [12] [13]) that they can endure. This is not a problem in our approach since we only program any flash FET at most a few times in the lifetime of the PFD-LDO regulator.

B. Pseudoflash Transistor

To fabricate a flash transistor, special manufacturing steps are necessary to create the floating gate, which increases fabrication complexity and cost. Thus, there is a strong motivation to use a vanilla CMOS process to implement the flash transistor's behavior, while avoiding the extra manufacturing steps. Such a "pseudoflash" transistor has been extensively studied [14], [15], [16], [17], [18], [19], [20], [21]. The pseudoflash transistor is well understood and has been fabricated at various feature sizes and for several applications [14], [15], [16], [17], [18], [19], [20], [21].

Fig. 5(a) and (b) illustrates the circuit diagram and I_{D}–V_{G} curve of a pseudoflash transistor. A pseudoflash transistor is composed of a pMOS transistor (M_{fg}), a poly-poly capacitor (C_g), and a MOS capacitor (C_{tun}). The two capacitors are coupled to the gate terminal of M_{fg}. The pseudoflash transistor is surrounded by an excellent electrical insulator (SiO_2) [14]. No dc path exists from node V_{fg}, thus allowing electrons to be stored on node V_{fg}. As a result, the pseudoflash device achieves the same programming and erasure characteristics as a flash transistor, while using a vanilla CMOS fabrication process (unlike flash transistors [7] or charge-trap transistors [22] which need special fabrication steps). This has been theoretically shown, and practically validated [14], [15], [16], [17], [18], [19]. We use FN tunneling [10] and hot carrier injection (HCI) [23] to "erase" or "program" the pseudoflash transistor, respectively. FN tunneling is utilized to remove electrons from node V_{fg} and thereby increase its V_t. By applying a high voltage (8–10 V) to the node V_{tun}, a high electric field is created across C_{tun}. The effective oxide thickness shrinks, enhancing the probability of electrons moving across the oxide potential barrier, and V_{fg} is increased. The I_{D}–V_{G} curve is thereby shifted left as shown in Fig. 5(b). HCI is utilized to inject electrons into the node V_{fg}. By applying a high voltage (3–4 V) between the drain and source of M_{fg}, we generate a high electric field region across the drain and source terminals. Electrons that move across the high electric field region have a boosted energy. If the electron energy is higher than the potential SiO_2-Si barrier (3.0 eV) of the gate oxide of M_{fg}, some electrons move into the oxide and are trapped in the node V_{fg}. Thus, V_{fg} is decreased, causing the I_{D}–V_{G} curve to shift right as shown in Fig. 5(b), which corresponds to a decrease in V_t. The node V_{fg} of the pseudoflash transistor is able to be tuned to various voltage levels (with V_{fg} precision of up to 1 mV [24]), by exploiting FN tunneling and HCI, effectively modifying the V_t of M_{fg}. In pseudoflash transistors (like in traditional flash transistors), once electrons are trapped in the node V_{fg}, they remain trapped for several years [15], [18], [19], or until removed by an erase operation. To adjust V_{fg} precisely, a lookup table is used. This table [11] enumerates the duration and magnitude of the V_{DS} pulses required for each value of V_t. Therefore, the impedance of the pseudoflash transistor is "dialed-in" with precision. Fig. 6 shows that the impedance can be made substantially identical by programming the pseudoflash transistor to different values of V_{fg} for different corners, in HSPICE.

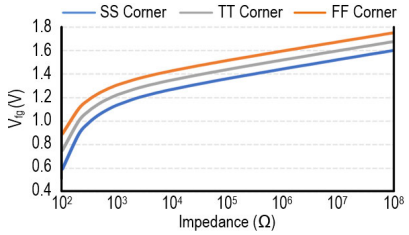

Fig. 6. Values of V_{fg} with different impedance of pseudoflash transistor under different corners.

As mentioned earlier, the pseudoflash transistors in our proposed design could be replaced by using flash transistors as well.

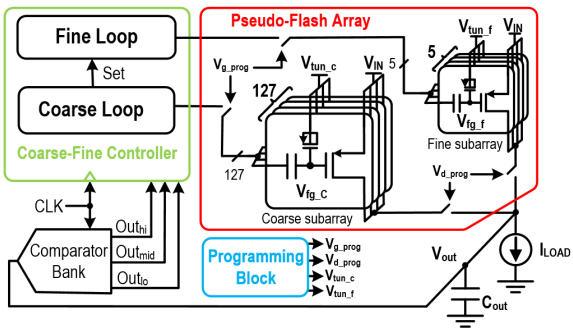

Fig. 7. Schematic of proposed PFD-LDO regulator.

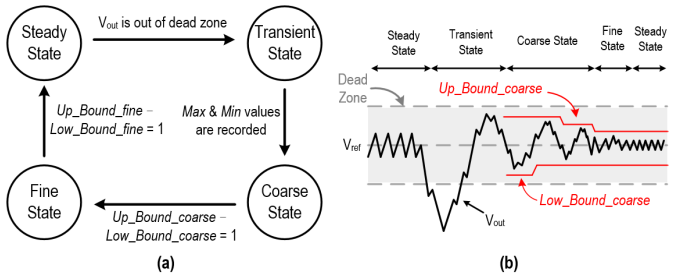

Fig. 8. (a) FSM of the coarse-fine controller and (b) operation waveform of the coarse-fine controller.

We also present two other structures of pseudoflash transistors [20], [21]. The 3T pseudoflash transistor [20] has the same functionality as shown in Fig. 5(a) but is completely implemented by three CMOS transistors. Both the erasing and programming of the 3T pseudoflash transistor structure are realized by removing/adding electrons from/to the V_{fg} node through FN tunneling. To remove electrons, we increase V_{tun} to create a large electric field across C_{tun}. This results in a reduced effective gate oxide thickness and an increased probability of electrons leaving node V_{fg}. To add electrons, we increase V_g, resulting in the insertion of electrons into the node V_{fg}. During the procedure of erasing/programming, a high voltage (8–10 V) is required to tunnel electrons through the gate oxide. Such a high voltage may cause program disturbance to nearby 3T pseudoflash transistors when programming a selected 3T pseudoflash transistor. This program disturbance phenomenon affects the programming time and accuracy. To mitigate the program disturbance, a 5T pseudoflash transistor [21] is proposed. The 5T pseudoflash transistor structure is based on the structure of the 3T pseudoflash transistor, with two additional switches (S_1 and S_2) added to the source and drain terminals of M_{fg}. The selected 5T pseudoflash transistors can be programed accurately by turning on their corresponding switches, while keeping the unselected 5T pseudoflash transistors from being disturbed by turning off their switches. However, the additional switches increase the complexity of the control circuitry.

III. Proposed Architecture

A. Proposed PFD-LDO Regulator

Fig. 7 illustrates the proposed PFD-LDO regulator which is comprised of a comparator bank, a coarse-fine controller, a programming block, and two pseudoflash arrays. The two pseudoflash arrays consist of a coarse subarray using $N = 127$ pseudoflash transistors and a fine subarray using $M = 5$ pseudoflash transistors. The voltages V_{fg_c} (for the coarse subarray) and V_{fg_f} (for the fine subarray) are tuned to different voltage levels by the programming block [16], which generates corresponding V_{g_prog}, V_{d_prog}, V_{tun_c}, and V_{tun_f} signals, to regulate and maintain the V_t of the coarse and fine subarray devices, respectively. This in turn regulates the impedance of the pseudoflash transistors of the coarse and fine subarrays, which allows the *same* Digital LDO regulator to operate under various V_{IN}, V_{out}, I_{max}, I_{min}, and V_{ripple} specifications.

The comparator bank (which is comprised of three dynamic latched comparators [25]) generates output signals Out_{hi}, Out_{mid}, and Out_{lo} which are logic "1" when V_{out} is greater than $V_{\text{ref}} + 20$ mV, V_{ref}, and $V_{\text{ref}} - 20$ mV, and at logic "0" otherwise, respectively. We generate a signal DeadZone $= \overline{\text{Out}_{\text{hi}}} \cdot \text{Out}_{\text{lo}}$, which is at logic "1" when $V_{\text{ref}} + 20$ mV $> V_{\text{out}} > V_{\text{ref}} - 20$ mV. The PFD-LDO regulator forces V_{out} to operate with DeadZone $= 1$ during steady-state operation. If I_{LOAD} undergoes a sufficiently large instantaneous change, V_{out} changes in response and DeadZone changes to logic "0." The coarse-fine controller then starts to regulate V_{out} instantly. The third comparator in the comparator bank (whose output is Out_{mid}) is used to regulate V_{out} around V_{ref}.

The coarse-fine controller includes a coarse control loop and a fine control loop. The coarse control loop computes the number n of coarse transistors to turn on, in order to adjust V_{out} to within $(V_{\text{IN}} - I_{\text{LOAD}} \cdot (R_C/n)) < V_{\text{ref}} < (V_{\text{IN}} - I_{\text{LOAD}} \cdot (R_C/(n+1)))$, where R_C is the impedance of each coarse pseudoflash transistor. When the coarse control loop has found n, we set the signal found_n to be logic "1." We generate a signal set which is the logical AND of DeadZone and found_n. When set $= 1$, we exit the coarse control loop and move to the fine control loop. The fine control loop computes the number m of fine transistors to regulate V_{out} so that it stays in the range of $(V_{\text{IN}} - I_{\text{LOAD}} \cdot ((R_C/n)||(R_F/m)))$ and $(V_{\text{IN}} - I_{\text{LOAD}} \cdot ((R_C/n)||(R_F/(m+1))))$, where R_F is the impedance of each fine pseudoflash transistor. The algorithms used for the coarse and fine control loops are described next.

B. Operation of the Coarse-Fine Controller

Fig. 8(a) illustrates the state transition diagram of the finite state machine (FSM) of the coarse-fine controller, and Fig. 8(b) illustrates a sequence of states encountered during the operation of the FSM. In Fig. 8(b), suppose the I_{LOAD} undergoes a sufficiently large instantaneous change, and DeadZone $= 0$ (i.e., V_{out} is no longer in the dead zone, due to the undershoot). The controller switches to the *transient* state of the FSM from the *steady* state of the FSM. In the *transient* state, it enables more coarse transistors in order to generate more instantaneous current to compensate for the increased I_{LOAD}. Starting with the number n of coarse transistors that were turned on in steady state, we increment n by 2 in every clock cycle until V_{out} is within the dead zone (indicated by Out_{low} going high).

Then, we increment n by 1 in every clock cycle until V_{out} exceeds V_{ref} (indicated by Out_{mid} going high). The controller now stores the number of coarse transistors which are enabled, in a *Max* register. However, a small overshoot occurs due to an excess number of coarse transistors being enabled. So, the controller reduces the number of enabled coarse transistors by 1 in every clock cycle to stabilize V_{out}. Once V_{out} falls below V_{ref} (indicated by Out_{mid} going low), the controller stores the number of coarse transistors which are enabled, in a *Min* register. Once the controller records the *Max* and *Min* values, the controller enters the *coarse* state of the FSM. In this state, the controller first averages the value of *Max* and *Min* to calculate *Mean*. We add/subtract 2 to/from *Mean* to generate Up_Bound_coarse/Low_Bound_coarse, respectively. Now, we begin the iterations of the coarse control loop, which are designed to find the optimal number of coarse transistors to enable. In the coarse control loop, we alternatively increase V_{out}, and then decrease it, until convergence. In the increasing phase, we cause the V_{out} to increase (by increasing the number of enabled coarse transistors from Low_Bound_coarse to Up_Bound_coarse with an increment of 1 in every clock cycle). We measure the number of cycles $N_{\text{Low\_coarse}}$ that are required for V_{out} to increase beyond V_{ref} (as indicated by Out_{mid} changing from logic "0" to logic "1"). In the decreasing phase, we cause V_{out} to decrease (by decreasing the number of enabled coarse transistors from Up_Bound_coarse to Low_Bound_coarse with a decrement of 1 in every clock cycle). We measure the number of cycles $N_{\text{Up\_coarse}}$ that are required for V_{out} to decrease below V_{ref} (as indicated by Out_{mid} changing from logic "1" to logic "0"). If $N_{\text{Up\_coarse}} > N_{\text{Low\_coarse}}$, it means that the duration of V_{out} above V_{ref} is longer than the duration of V_{out} below V_{ref}, and the value of Up_Bound_coarse exceeds the number of transistors required for regulation. Thus, the value of Up_Bound_coarse is decreased by 1. Conversely, if $N_{\text{Up\_coarse}} \leq N_{\text{Low\_coarse}}$, the value of Low_Bound_coarse is increased by 1. We iterate this process until the difference between Up_Bound_coarse and Low_Bound_coarse is eventually reduced to 1. At this point, the coarse control loop has converged, and determined the number of coarse transistors required to provide current for the I_{LOAD}. The controller sets the number of coarse transistors to the value of Low_Bound_coarse, and moves to the *fine* state of the FSM (where goal it is to decrease V_{ripple}).

The fine control loop uses the same control algorithm to select the number of fine transistors to enable. Starting with Up_Bound_fine $=$ 5 and Low_Bound_fine $=$ 0, the algorithm compares $N_{\text{Up\_fine}}$ and $N_{\text{Low\_fine}}$ until the fine control loop converges V_{out}. The algorithmic approach is the same as that of the coarse algorithm. After convergence, we enter the *steady* state of the FSM in which we alternately turn on Up_Bound_fine and Low_Bound_fine fine transistors in alternating clock cycles.

C. Dynamic Latched Comparator

Fig. 9(a) and (b) illustrates the circuit diagram and the waveform of the dynamic latched comparator [25]. It is composed of a differential pair (M_2–M_3), two cross-coupled inverters (M_6–M_8 and M_7–M_9), four clock gated switches

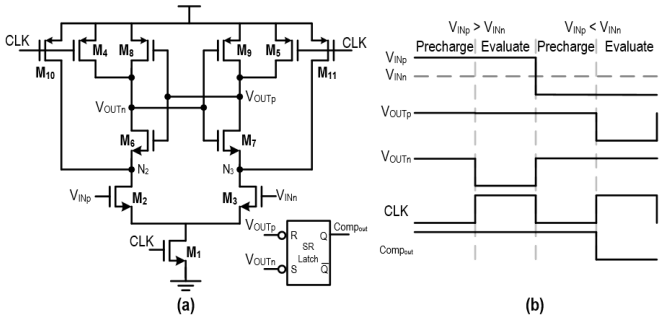

Fig. 9. (a) Circuit diagram and (b) waveform of the dynamic latched comparator.

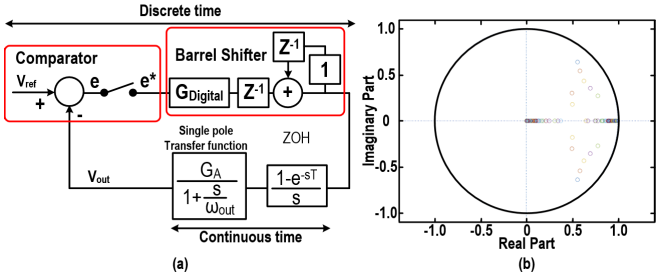

Fig. 10. (a) Digital LDO regulator analytical model from [26] and (b) pole-zero plot using the five specifications for stability analysis.

(M_4, M_5, M_{10}, and M_{11}), and an SR latch. When the clock signal (CLK) is low, the comparator is in the precharge phase, and the transistors M_4, M_5, M_{10}, M_{11} are turned on, pulling node V_{OUTn}, V_{OUTp}, N_2, and N_3 to high. When CLK is high, the comparator enters the evaluation phase, and the transistors M_4, M_5, M_{10}, and M_{11} are turned off. During the evaluation phase, If V_{INp} is greater than V_{INn}, node V_{OUTn} is discharged to low, and due to the M_7–M_9 inverter of the cross-coupled inverter pair, V_{OUTp} is set to high. Otherwise, if V_{INn} is greater than V_{INp}, V_{OUTn} and V_{OUTp} are set to high and low, respectively. Finally, V_{OUTn} and V_{OUTp} are sent to the SR latch to hold the output value (Comp_{out}) during the precharge phase.

IV. Analytical Model

To assess the behavior of the digital controller used in Digital LDO regulators, z-domain models have been utilized for analysis. Fig. 10(a) shows a system model of a Digital LDO regulator using a barrel shifter for the digital control which was described in [26]. The comparator is modeled as a subtraction operation. The digital controller accumulates the error from the comparator and can be modeled as a digital integrator. G_{Digital} represents the gain of the digital controller. The output of the digital controller serves as a bridge between discrete-time and continuous-time models. This can be modeled by a zero-order hold (ZOH) and a single pole transfer function ($G_A/(1 + (s/\omega_{\text{out}}))$), where G_A is a proportionality constant, and ω_{out} is the output load frequency ($\omega_{\text{out}} = (1/((R_{\text{Load}}//R_{\text{pMOS}}) * C_{\text{Load}}))$). The open-loop transfer function is obtained by (2), where T is the sampling period. With the use of unity feedback, the closed-loop transfer function of the Digital LDO regulator in the z domain is obtained by (3), where $G = G_{\text{Digital}} G_A (1 - e^{-\omega_{\text{out}} T})$. For the

stability of the system, the poles of the closed-loop transfer function must lie inside the unit circle

$$\mathrm{TF}_{\mathrm{open}}(z) = G_{\mathrm{Digital}} G_A (1 - e^{-\omega_{\mathrm{out}} T}) \frac{1}{(z-1)(z - e^{-\omega_{\mathrm{out}} T})} \tag{2}$$

$$\mathrm{TF}_{\mathrm{close}}(z) = \frac{G(z)}{1 + G(z)} = \frac{G}{z^2 - (1 + e^{-\omega_{\mathrm{out}} T}) z + (G + e^{-\omega_{\mathrm{out}} T})}. \tag{3}$$

To model the behavior of our coarse-fine controller, we use this system model for stability estimation due to the similarity of our control algorithm with that of [26]. During the *transient* state of the operation, our controller turns on/off 1 or 2 coarse pseudoflash transistors if V_{out} is below/above V_{ref}. Hence, we can set the parameter G_{Digital} to 1 or 2 in the above model. For the *coarse* and *fine* states of the operation, both use the same control algorithm with the parameter G_{Digital} being 0 or 1. When the number of enabled pseudoflash transistors reaches the value of *Up_Bound* or *Low_Bound*, the controller maintains the number of enabled transistors. That is, the parameter G_{Digital} is set to 0. Otherwise, the controller turns on/off 1 pseudoflash transistor if V_{out} is below/above V_{ref}, and G_{Digital} is set to 1. To ensure that our coarse-fine controller is stable, the poles of the closed-loop transfer function must be within the unit circle. We performed the stability analysis for the five specifications shown in Section V-J. Fig. 10(b) shows the pole-zero plot using MATLAB [27]. We set the parameter G_{Digital} to 0.5 for the analysis since the value of G_{Digital} of the coarse state operation, which is used to stabilize V_{out}, toggles between 0 and 1. The value of G_A for our PFD-LDO regulator is obtained by (4), where R_C is the impedance of each coarse pseudoflash transistor. We vary I_{LOAD} from 1% to 99% of the corresponding I_{max} with an increment of 1%. All the poles are located within the unit circle, indicating that our PFD-LDO regulator system is stable for different I_{LOAD} conditions, for each of the five specifications we tested

$$G_A = \frac{V_{\mathrm{out}}}{n} = \frac{(V_{\mathrm{IN}} - V_{\mathrm{out}}) * V_{\mathrm{out}}}{R_C * I_{\mathrm{LOAD}}}. \tag{4}$$

V. Experimental Results

In this section, we describe the results of multiple experiments that do the following: 1) illustrate that our proposed PFD-LDO regulator has very competitive electrical characteristics compared with existing Digital LDO regulators and 2) show how the *same* design can be used to meet different regulator specifications. We first describe our simulation environment setup (Section V-A). We next present how our PFD-LDO regulator can meet multiple regulator specifications (V_{IN}, V_{out}, V_{ripple}, I_{max}, and I_{min}) using the *same* design (Section V-B), followed by transient response and ripple behavior (Sections V-C and V-D). Then, we present results for the performance of our PFD-LDO regulator for several regulator metrics (Sections V-E–V-I). At last, we compare the results of our PFD-LDO regulator (for several regulator specifications) with five recent works in Section V-J.

A. Simulation Environment Setup

The proposed PFD-LDO regulator is simulated using a 45 nm PTM [28] CMOS process using Synopsys HSPICE [29]. The digital coarse-fine controller circuitry is synthesized from Verilog using a 45 nm CMOS cell library using Synopsys Design Compiler (DC) [29]. We use a device length of 55 nm for the pseudoflash transistor devices. The resistance of each pseudoflash transistor in the coarse pseudoflash subarray is designed to be nominally 50Ω when the pseudoflash transistor (with no charge stored on node V_{fg_c}) is operated in the deep linear region. With a maximum of 127 coarse pseudoflash transistors, this would result in a nominal power supply impedance of 0.4Ω. The size of a pseudoflash transistor in the fine pseudoflash subarray is 5× smaller than its coarse counterpart. Hence, its resistance is nominally 250Ω (with no charge stored on node V_{fg_f}).

B. Implementing Multiple Regulator Specifications With a Single Pseudoflash-Based Design

We perform several experiments to demonstrate that the proposed PFD-LDO regulator can realize various regulator specifications (like V_{out}, V_{ripple}, I_{max}, and I_{min} values for different V_{IN}) by adjusting the V_{fg_c} and V_{fg_f} in the *same* circuit. I_{max} and I_{min} can be modified by varying V_{fg_c}, and V_{ripple} can be regulated by varying V_{fg_f}. Hence, the *same* proposed PFD-LDO regulator design can achieve a variety of regulator specifications like V_{IN}, V_{out}, I_{max}, I_{min}, and V_{ripple}. A manufacturer can preprogram values of V_{fg_c} and V_{fg_f} in the factory, based on different applications and their regulator specifications (V_{IN}, V_{out}, I_{max}, I_{min}, and V_{ripple}). The manufacturer can alternatively provide the ability to the customer to do this in the field, at design time. In addition, a customer can fine-tune V_{fg_c} and V_{fg_f} to correct for device aging or temperature changes. This reduces design cost and increases flexibility by using the *same* design for several regulator specifications. Table I(a)–(c) shows ten regulator specifications (one per row) achievable using the *same* PFD-LDO regulator circuit. Each specification in these tables uses different V_{fg_c} and V_{fg_f} (i.e., programming the coarse and fine pseudoflash subarrays to different V_t values). Table I(a) [Table I(b)] illustrates the results when the I_{LOAD} is altered from 20%I_{max} to 40%I_{max} (40%I_{max} to 80%I_{max}). When the I_{LOAD} is altered from 20%I_{max} to 40%I_{max}, the average of V_{shoot}, t_{rec}, and V_{ripple} are 44 mV, 0.16 μs, and 4.1 mV, respectively. The average of V_{shoot}, t_{rec}, and V_{ripple} are 84 mV, 0.39 μs, and 4.4 mV, respectively, when the output load current is altered from 40%I_{max} to 80%I_{max}. We also did the simulations with a larger current change. Table I(c) illustrates the results when the I_{LOAD} is altered from 20%I_{max} to 80%I_{max}. The average value of V_{shoot}, t_{rec}, and V_{ripple} are 299 mV, 0.44 μs, and 4.3 mV, respectively, when the I_{LOAD} is altered from 20%I_{max} to 80%I_{max}.

Note that our PFD-LDO regulator can operate across a wide range of V_{out} (0.7–1.7 V) and I_{max} (15 to 250 mA).

TABLE I

SIMULATION RESULTS WITH A I_{LOAD} CHANGE FROM (a) $20\%I_{\text{max}}$ TO $40\%I_{\text{max}}$, (b) $40\%I_{\text{max}}$ TO $80\%I_{\text{max}}$, AND (c) $20\%I_{\text{max}}$ TO $80\%I_{\text{max}}$

V_{IN} (V)	V_{out} (V)	I_{max} (mA)	I_{min} (mA)	V_{shoot} (mV)	t_{rec} (μs)	V_{ripple} (mV)
1.8	1.7	250	2	40	0.16	3.6
1.8	1.7	190	1.5	38	0.16	3.5
1.5	1.4	200	1.6	42	0.16	3.6
1.5	1.4	127	1	46	0.16	3.7
1.2	1.1	152	1.2	44	0.16	3.9
1.2	1.1	113	0.89	46	0.16	3.9
1.0	0.9	101	0.8	43	0.15	4.0
1.0	0.9	61	0.48	40	0.16	4.5
0.8	0.7	61	0.48	40	0.16	3.6
0.8	0.7	15	0.12	66	0.15	6.2
Average				44	0.16	4.1

(a)

V_{IN} (V)	V_{out} (V)	I_{max} (mA)	I_{min} (mA)	V_{shoot} (mV)	t_{rec} (μs)	V_{ripple} (mV)
1.8	1.7	250	2	109	0.40	3.5
1.8	1.7	190	1.5	66	0.41	3.7
1.5	1.4	200	1.6	64	0.40	3.5
1.5	1.4	127	1	69	0.39	3.8
1.2	1.1	152	1.2	71	0.37	3.7
1.2	1.1	113	0.89	75	0.33	4.2
1.0	0.9	101	0.8	66	0.41	4.0
1.0	0.9	61	0.48	87	0.40	4.8
0.8	0.7	61	0.48	87	0.41	5.0
0.8	0.7	15	0.12	144	0.41	7.3
Average				84	0.39	4.4

(b)

V_{IN} (V)	V_{out} (V)	I_{max} (mA)	I_{min} (mA)	V_{shoot} (mV)	t_{rec} (μs)	V_{ripple} (mV)
1.8	1.7	250	2	177	0.45	3.3
1.8	1.7	190	1.5	186	0.42	3.4
1.5	1.4	200	1.6	183	0.41	3.5
1.5	1.4	127	1	215	0.40	3.8
1.2	1.1	152	1.2	212	0.43	3.8
1.2	1.1	113	0.89	265	0.42	4.1
1.0	0.9	101	0.8	227	0.46	4.0
1.0	0.9	61	0.48	474	0.50	4.8
0.8	0.7	61	0.48	474	0.50	4.8
0.8	0.7	15	0.12	573	0.45	7.4
Average				299	0.44	4.3

(c)

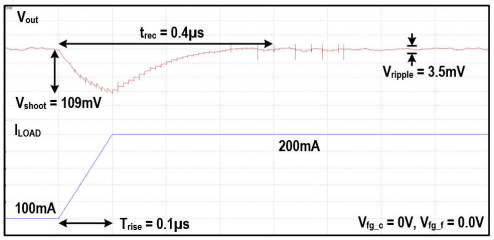

Fig. 11. Transient response of the proposed PFD-LDO regulator.

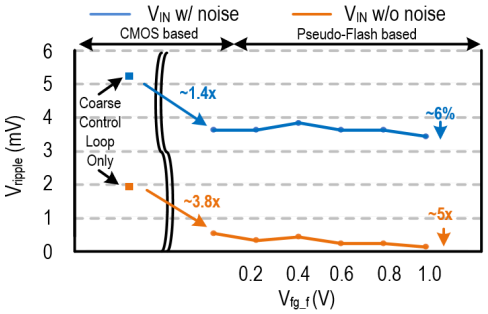

Fig. 12. Simulation results of V_{ripple} under different cases.

C. Transient Response

Fig. 11 illustrates the HSPICE output of the transient response of the proposed PFD-LDO regulator when the I_{LOAD} is altered from 100 to 200 mA. V_{IN} is 1.8 V, and V_{out} is regulated to 1.7 V. The V_{shoot} is 109 mV and the t_{rec} is 0.40 μs. When V_{out} is stable, the fine pseudoflash subarray reduces V_{ripple} to 3.5 mV.

D. Ripple Behavior

In this section, we validate the usefulness of the adding fine control loop and the fine pseudoflash transistors, and also measure V_{ripple} with/without noise on the V_{IN} input. This is done for both the CMOS-based Digital LDO regulator and the proposed PFD-LDO regulator, simulated under different cases (Fig. 12). We note that using *only* the coarse control loop for the CMOS-based Digital LDO regulator, the V_{ripple} is 5.2 mV (1.9 mV) under the noisy (ideal) V_{IN}.

When the fine control loop is utilized along with the coarse control loop, the CMOS-based Digital LDO regulator reduces the V_{ripple} to 3.6 mV (0.5 mV) under the noisy (ideal) V_{IN}. This is a 1.4× (3.8×) V_{ripple} reduction compared to a coarse-only Digital LDO regulator under noisy (ideal) V_{IN} conditions.

The proposed PFD-LDO regulator is able to further reduce the V_{ripple} of the CMOS-based Digital LDO regulator because of its ability to adjust the V_{fg_f} of the fine transistors. Under the ideal V_{IN}, the proposed PFD-LDO regulator can achieve an additional improvement of 5× in V_{ripple} compared to the case using CMOS-based Digital LDO regulator. Under a noisy V_{IN}, the proposed PFD-LDO regulator can achieve an additional improvement of 6% in V_{ripple} compared to the CMOS-based Digital LDO regulator. The V_{ripple} does not change much because the proposed PFD-LDO regulator has regulated the V_{ripple} to the minimum value, and the V_{ripple} is dominated by the noise on V_{IN}. However, with a less noisy V_{IN}, we would be able to reduce V_{ripple} to a greater degree.

E. Monte Carlo Simulation

We also perform Monte Carlo simulations to verify the functionality of the proposed PFD-LDO regulator under process [30] and V_{IN} [31] variations. We varied the devices width (W) and length (L), with $\sigma = 3.25$ nm, for all transistors used in the comparator bank and the controller, to model process variations. The V_t values of the pseudoflash transistors used in the subarrays are programmable to adjust their impedance and cancel any W and L variations, so we did not apply variations to them. In our Monte Carlo simulations, we vary V_{IN} in a dc manner, with $\sigma = 18$ mV (1% of nominal V_{IN}). We also vary V_{IN} in an ac manner with $\sigma = 0.8$ mV to model the situation in which the proposed PFD-LDO regulator is powered by a dc/dc converter which has a voltage variation [31]. These variations are assumed to be normal. For both ac and dc simulations of V_{IN}, we apply $\pm 3\sigma$ variations. We assumed the distribution of W and L to be normal, and conducted our simulations assuming that these parameters vary up to $\pm 3\sigma$.

Fig. 13 illustrates the effect of process and V_{IN} variations on the proposed PFD-LDO regulator, as reported by the Monte Carlo simulations. We performed 500 Monte Carlo simulations.

Fig. 13(a) shows the results for both process and V_{IN} variations. The specified V_{ref} was 1.7 V, and V_{IN} varied from 1.74 to 1.85 V. We found V_{out} to be stable with a minimum (maximum) value of 1.65 V (1.75 V) and a standard

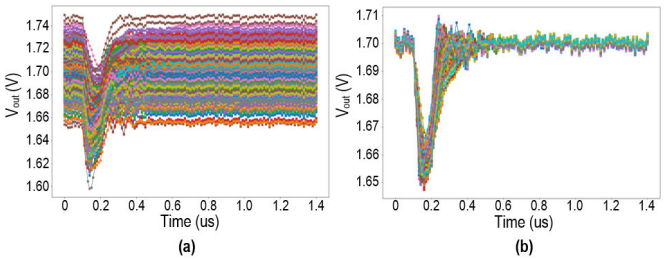

Fig. 13. Simulation results of V_{out} under (a) process and V_{IN} variations and (b) V_{IN} variation only.

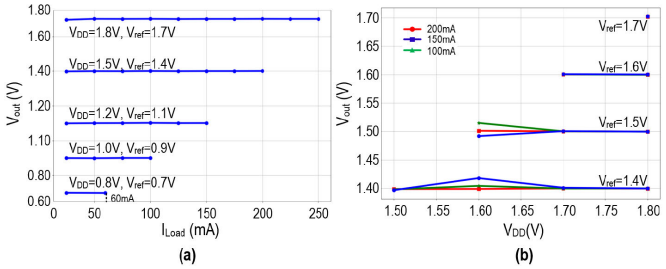

Fig. 14. Simulation results of (a) load regulation and (b) line regulation.

TABLE II
SIMULATION RESULTS OF TEMPERATURE VARIATIONS

Temperature (°C)	V_{out} (V)	V_{shoot} (mV)	V_{ripple} (mV)	t_{rec} (μs)
25°C	1.700	40	3.6	0.16
50°C	1.702	38	3.8	0.18
75°C	1.700	51	3.5	0.20

deviation of 15 mV. The proposed PFD-LDO regulator is able to converge the V_{out} with a V_{ripple} ranging from 3.2 to 4.7 mV, with a mean V_{ripple} of 3.7 mV and a standard deviation of 0.4 mV.

To further understand the factors contributing to the V_{out} variation, we perform a Monte Carlo simulation of the proposed PFD-LDO regulator with only V_{IN} variation but no process variations. The results are shown in Fig. 13(b). We observe that the proposed PFD-LDO regulator is able to converge V_{out} between 1.698 to 1.702 V (with a standard deviation of 0.5 mV) even though the V_{IN} ranges from 1.75 to 1.84 V. The V_{ripple} varies from 3.2 to 4.4 mV (with a standard deviation of 0.2 mV).

These experiments show that the V_{ripple} variation is dominated by the V_{IN} variation, while the V_{out} variation is dominated by CMOS process variations.

F. Temperature Variation

We simulate our PFD-LDO regulator at different temperatures to measure its regulation capability. Table II illustrates the simulation results of our PFD-LDO regulator operated at three different temperatures, when I_{LOAD} is altered from $20\%I_{max}$ to $40\%I_{max}$. Due to increased temperature, the current provided by each pseudoflash transistor decreases, resulting in an increase in t_{rec} and V_{shoot} as temperature increases. Nevertheless, the coarse-fine controller is able to regulate V_{out} at the correct voltage level and minimize V_{ripple}.

G. Load Regulation

Load regulation is used to measure the capability of a regulator to maintain a constant steady-state output voltage V_{out} level while output load current I_{Load} is changed. In other words, load regulation is $(\Delta V_{out}/\Delta I_{LOAD})$. Fig. 14(a) illustrates the load regulation of our design. We report the maximum value of this quantity over different values of V_{out} and I_{LOAD}, using a ΔI_{LOAD} value of 50 mA. In our experiments, we simulate supply voltage V_{IN} from 0.8 to 1.8 V (the corresponding regulated output voltage V_{out} varies from 0.7 to 1.7 V). We apply I_{Load} from 25 mA to the corresponding I_{max}. We found that the maximum load regulation is 0.1 mV/mA. We will compare this metric with state-of-the-art regulators in Section V-J.

H. Line Regulation

Line regulation is used to measure how well a regulator is capable of maintaining a constant steady state V_{out} level while the supply voltage V_{IN} is changed. In other words, line regulator is $(\Delta V_{out}/\Delta V_{IN})$. Fig. 14(b) illustrates the line regulation of our design. The supply voltage V_{IN} is nominally between 1.5 and 1.8 V, and the regulated output voltage V_{out} varies from 1.4 to 1.7 V. We simulate I_{LOAD} values of 100, 150, and 200 mA. Even though the current provided by each pseudoflash transistor increases because of the increase between V_{IN} and V_{out}, our PFD-LDO regulator is able to regulate V_{out} to be close to V_{ref}. Across all the simulated values of V_{IN}, V_{ref}, and I_{LOAD}, the maximum line regulation was found to be 0.2 mV/mV. We will compare this metric with that of other regulators in Section V-J.

I. Power Supply Rejection

Power supply rejection (PSR) measures the ability of a regulator to reject noise (of various frequencies) on V_{IN}. PSR is the ratio of the ripple on V_{out} (i.e., V_{ripple}) to the ripple on V_{IN}, in dB. In our experiments, we first measure PSR by applying a sine wave with an amplitude of 100 mV to V_{IN} and varying the frequency of the sine wave. As shown in Fig. 15(a), our PFD-LDO regulator is able to compensate for V_{IN} variation at frequencies below 100 kHz, achieving a PSR less than -9.5 dB for frequencies below 100 kHz. As the frequency increases, the PSR degrades, and the PSR becomes 0 dB for the frequencies higher than 5 MHz. In our second PSR experiment, we measure PSR with different values of ripple on V_{IN} at the 100 and 500 kHz [Fig. 15(b)]. Since our PFD-LDO regulator starts to regulate V_{out} only when V_{out} exceeds the dead zone ($V_{ref} \pm 20$ mV), the PSR is marginal (-2 dB) when the voltage amplitude is 25 mV. If the voltage amplitude is greater than 25 mV, our PFD-LDO regulator achieves a healthy PSR of -8 dB or better when the frequency is 100 kHz. However, if the frequency increases, the ability for the voltage regulation degrades, as discussed in Fig. 15(a), and the PSR is close to 0 dB.

J. Comparison With State-of-the-Art Regulators

There have been several past research efforts focusing on improving the performance of Digital LDO regulators.

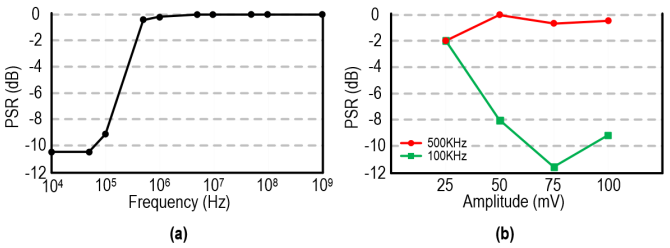

Fig. 15. Simulation results of PSR by varying (a) frequency and (b) amplitude.

TABLE III
COMPARISON OF THE PFD-LDO REGULATOR WITH PRIOR WORKS

	This work					[2] ISSCC'20	[3] JSSC'17	[4] EDSSC'19	[5] ICTA'20	[6] TCAS-I'19
Type	Digital					Digital	Digital	Digital	Digital	Digital
Process (nm)	45nm					28nm	28nm	65nm	65nm	65nm
Operating Frequency	100MHz					168MHz-2.0GHz	N.A.	10MHz	10MHz	100MHz
V_{IN} (V)	0.8	1.0	1.2	1.5	1.8	0.5-1.0	1.1	0.6-0.8	N.A.	0.6
V_{out} (V)	0.7	0.9	1.1	1.4	1.7	0.45-0.95	0.9	0.5-0.75	0.5-0.95	0.5
V_{ripple} (mV)	5.0	4.0	3.7	3.5	3.5	N.A.	N.A.	N.A.	N.A.	N.A
Max Current (mA)	61	101	152	200	250	160-480	200	N.A.	N.A.	100
V_{shoot} @ ΔI_{load}	87mV@ 24mA	66mV@ 40mA	71mV@ 60mA	64mV@ 80mA	109mV@ 100mA	112mV@ 430mA	120mV@ 180mA	90mV@ 15mA	16.4mV@ 5mA	53mV@ 100mA
t_{rec} (μs)	0.41	0.41	0.37	0.40	0.40	0.31	64*	4*	18*	0.7*
Quiescent Current (μA)	30	47	72	615	15800	7.7-241	110	20	64	34.6
Load Regulation (mV/mA)	0.1					N.A.	2.8*	0.77	N.A.	N.A.
Line Regulation (mV/mV)	0.2					N.A.	N.A.	0.04	N.A.	N.A.
PSR	-10.5dB@50KHz, 0dB@1MHz					N.A.	N.A.	N.A.	N.A.	N.A.
C_{out} (nF)	0.1					Cap-free	23.5	0.13	0.052	1
Area (mm^2)	0.005 (active area)					0.049	0.021	N.A.	N.A.	0.17
Area normalized to 45nm process (mm^2)	0.005 (active area)					0.127	0.054	N.A.	N.A.	0.081

*Estimated data from figures.

For example, [2], [3], [4], [5], [6] implement two pMOS arrays for coarse and fine regulation. This reduces the V_{ripple} and t_{rec}. Tseng et al. [32] implement different sizes of pMOS transistors in each subarray. Also, the MOS subarrays are arranged in a series connection topology. This results in a more complex controller than our solution, and also a larger circuit than our approach. Unlike our solution, these previous approaches do not use pseudoflash or flash transistors, and hence do not allow the pMOS transistor resistances to be tuned in the factory or in the field. As a result, their specifications for V_{IN}, V_{out}, I_{max}, I_{min}, and V_{ripple} are fixed.

Table III shows the comparison of the proposed PFD-LDO regulator with prior works. Among prior works, the results of [2], [3], and [6] are from chip measurements, and the results of [4] and [5] are from circuit simulations. To make our simulation results more realistic, we have included device parasitics in all our circuit simulations. Our proposed PFD-LDO regulator is designed to regulate V_{out} which ranges from 0.7 to 1.7 V with the V_{IN} operated at 0.8–1.8 V, as described in Table I. The quiescent current ranges from 30 μA to 15.8 mA. The output capacitance (C_{out}) is set to 0.1 nF, the operating frequency is 100 MHz, and the active area is 0.005 mm^2 (including the pseudoflash devices as well).

Unlike other state-of-the-art approaches, our PFD-LDO regulator can operate over a large range of V_{IN} and V_{out}, as shown in Table III. We also adjust a large range of I_{max}, I_{min} (by tuning V_{fg_c} for the coarse subarray discussed in Section V-B), and V_{ripple} (by varying V_{fg_f} for the fine subarray discussed in Section V-D). It should be noticed that the current provided by each coarse pseudoflash transistor changes when our PFD-LDO regulator is operated at different V_{IN} values. I_{max} and I_{min} are therefore different even though we utilize the same coarse subarray. When I_{LOAD} is altered from 40% to 80% of the corresponding I_{max}, the values of V_{shoot} are therefore different across columns 2 through 6. Our $V_{\text{shoot}}@\Delta I_{\text{load}}$ and t_{rec} are competitive compared to prior works [4], [5], [6], even though these prior works use an undershoot detector [4], [5] or an auxiliary power block [6] to immediately detect a load transient event or provide an additional current for fast V_{out} recovery. We achieve a low V_{ripple} with the use of the fine subarray, which comprises a smaller size of pseudoflash transistors (with larger ON resistance) than their coarse counterparts. This allows our PFD-LDO regulator to regulate V_{out} with a small V_{ripple}. We use a smaller C_{out} compared to other approaches [3], [4], [6]. Our maximum load regulation is at least 7× better compared to [3] and [4]. The load regulation measures the V_{out} change as a result of a ΔI_{LOAD} change. Note that we estimate the maximum load regulation from [3, Fig. 18], since [3] does not present the maximum load regulation quantity and ΔI_{LOAD}, while [4] presents the maximum load regulation quantity without specifying ΔI_{LOAD}. None of the five prior art references presents PSR value. Since the process nodes of [2], [3], [4], [5], and [6] are different from ours, we also present area numbers normalized to a 45 nm process. Even though our area is between 10× and 25× lower than the other works, we note that since our area is active, these area improvements may change in practice.

VI. CONCLUSION

In this article, we present a PFD-LDO regulator. Instead of using pMOS transistors, we use pseudoflash transistors to build the coarse and fine subarrays. The threshold voltage of the pseudoflash transistors of our proposed PFD-LDO regulator can be programed to meet a wide range of regulator operational specifications using the *same* PFD-LDO regulator design. This ability to program threshold voltages also allows us to cancel process variations in the subarray transistors. The coarse pseudoflash subarray provides instantaneous current, and performs V_{out} recovery when the I_{LOAD} changes instantaneously. The fine pseudoflash subarray further reduces the V_{ripple} once the coarse pseudoflash subarray has stabilized V_{out}. The *same* digital LDO regulator is able to operate with V_{IN} ranging from 0.8 to 1.8 V and for V_{out} ranging from 0.7 to 1.7 V, and a I_{max} ranging from 15 to 250 mA with $V_{\text{shoot}} <$ 573 mV, $t_{\text{rec}} < 0.50$ μs, and $V_{\text{ripple}} < 7.4$ mV. Among all the various PFD-LDO regulator specifications that we tested, the V_{shoot}, t_{rec}, and V_{ripple} are on average 44 mV, 0.16 μs, and 4.1 mV (84 mV, 0.39 μs, and 4.4 mV and 299 mV, 0.44 μs, and 4.3 mV), respectively, when the I_{LOAD} changes from 20%I_{max} to 40%I_{max} (40%I_{max} to 80%I_{max} and 20%I_{max} to 80%I_{max}) under different V_{IN} and V_{out}.

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