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DESIGN OF A LOW DROP-OUT VOLTAGE REGULATOR USING 0.13 µm CMOS TECHNOLOGY

NORHAIDA BINTI MUSTAFA[1], FLORENCE CHOONG[2]
MAMUN BIN IBNE REAZ[3], WAN IRMA IDAYU WAN MOHD NASIR[4],
NOORFAZILA KAMAL[5], ABDUL MUKIT[6]

[2]School of Engineering and Physical Science, Heriot Watt University,
No. 1 Jalan Venna P5/2, Precinct 5, 62200, Putrajaya, Malaysia
[1,3,4,5,6]Department of Electrical, Electronic and Systems Engineering,
Universiti Kebangsaan Malaysia, 43600 Bangi, Selangor, Malaysia
*Corresponding Author: f.choong@hw.ac.uk

Abstract

In this paper, the design of a 4.5 V low drop out voltage regulator is proposed. Two-stage cascaded operational transconductance amplifier has been used as error amplifier. The two-stage amplifier is designed with body bias technique to reduce the drop out voltage of LDO regulator. In addition, PMOS is employed as a pass transistor yielding a more stable output voltage. The proposed regulator has a drop out voltage of 32.06 mV and power dissipation of 1.3593 mW. It is designed using a 0.13 µm standard CMOS process using Mentor Graphics software. The proposed design showed superiority over recent work yielding the lowest drop out voltage. The performance of the proposed design shows a promising opportunity to enhance chip level power management for SoC applications.

Keywords: Body driven technique, Low drop out, Pass transistor, Transconductance amplifier, Voltage regulator.

1. Introduction

A linear voltage regulator which is an inductor-less, ripple-less and low-noise power converter with a bulk line frequency transformer is used to power an integrated circuit (IC). Due to the increasing demand for portable, handheld battery such as smartphones, tablet PCs, camera, MP3 player and PDA, the use of efficient power management systems to prolong battery life cycle and operating time, provide reliable, stable and constant voltage for these devices has become

Nomenclatures

C_L	Load capacitance
Gm	Transconductance of OTA
I_{bias}	External bias current
I_{LOAD}	Load current
I_o	Single ended output current
R_L	Load resistance
V_o	Output voltage
V_{PT}	Pass transistor voltage
V_{ref}	Reference voltage
V_{TH}	Body effect
V_{TH0}	Threshold voltage

Greek Symbols

α	Gain factor
γ	Technology dependent parameter for a p-channel transistor
$\Delta V_{ou}t$	Variation in output voltage
$\emptyset_F$	Technology dependent parameter for a p-channel transistor

the utmost importance [1-2]. LDOs can operate at a low supply voltage and are able to provide nearly constant dc voltage which is suitable for single-cell and two-cell battery applications. To regulate the performance of a voltage regulator in terms of line and load regulation, important parameters such as transient overshoot and undershoot and close monitoring of the output current, quiescent current, input voltage, output voltage, power, current efficiency [3] and transient settling time is necessary [4].

A basic LDO voltage regulator topology usually consists of a voltage reference, an error amplifier, a pass device, an external load capacitor with small value of internal resistance (ESR) and a feedback network. Figure 1 shows the overall topology of LDO voltage regulator. An error amplifier in negative feedback condition detects an error signal when there is a difference between the feedback voltage and reference voltage. The error signal will control the gate of the pass transistor for maintaining constant output voltage to supply a variable current to the load circuit. OTA is suitable for error amplifier since the output of error amplifier is used to drive the gate of the pass transistor [5].

Several types of pass transistors have been proposed including NMOS transistor and PMOS transistor. The drawback of the NMOS when used as the pass transistor is large dropout voltage. Hence PMOS pass transistor is favorable due to its good performance in dropout voltage, quiescent current flow, output current and speed [6]. The pass device also influences the loop gain, bandwidth and stability. In order to drive the maximum load current and achieve low drop-out performance, the pass transistor should have large ratio of width and length. However, by using large size of pass transistor, the gate capacitance will be increased and causes instability in the system [7]. The voltage reference provides the nominal output voltage. In Fig. 1, R_{f1} and R_{f2} are the resistors to set the output voltage (V_{out}).

There are numerous works on LDO voltage regulator reported in the literature. Body bias technique was applied in the design of a two-stage operational amplifier to improve its gain [3]. A two-stage OTA with cascoded current mirroring

technique used to boost up the output impedance is proposed in [3]. Abiri et al. [8] designed a LDO voltage regulator with small output voltage variations and the ability of wide load current range support. A recycling folded cascode OTA is used as an error amplifier. The LDO proposed by [9] uses a double recycling folded cascode error amplifier and offers good stability. It also offers a fast transient response through implementing a refined frequency compensation scheme to enable the LDO to remain stable over entire load current range.

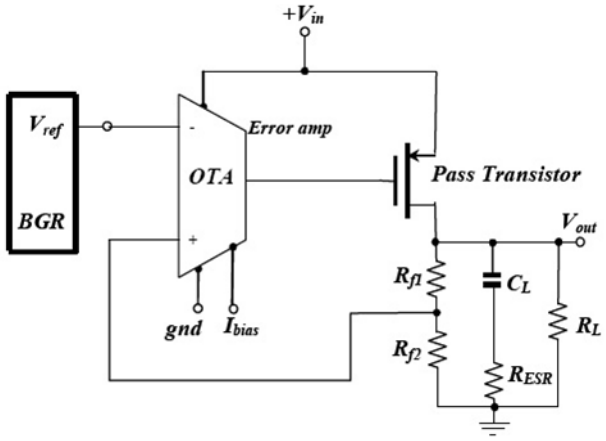

Fig. 1. Basic low dropout regulator topology [5].

Patri et al. [10], proposed an error amplifier by recycling the shunt current sources of a conventional folded cascode amplifier. Although these work showed improvements to the design of a voltage regulator, the drop-out voltage is still significant. In this paper, an enhanced two-stage OTA for error amplifier with body bias technique has been proposed using 0.13 um CMOS technology designed in Design Architect-IC (DA-IC) in Mentor Graphics software. The body bias technique is applied only to the transistor in the error amplifier. The proposed design showed good performance with low drop out voltage of 32.06 mV at full load condition and low power dissipation of 1.3593 mW.

The organization of the paper is as follows. Firstly, the proposed design is discussed in detail. This is followed by presentation of results and discussion along with the comparison with related work. The paper concludes with a summary and future work.

2. Methodology

In this paper, a two-stage cascoded OTA as error amplifier is proposed. In addition, PMOS pass transistor and body bias voltage are used to improve the drop-out voltage of the LDO voltage regulator. The drop out voltage is the minimum differential voltage between the output and input voltage at the point where the circuit stop to regulate. It is also defined as the minimum voltage drop across the pass device to maintain regulation. The dropout voltage is typically specified at maximum load current. The maximum load current specifications determine the size of the pass device, dropout voltage and power dissipation constraints. When the maximum load

current specification increases, the overall die area of the pass device, the control circuitry and the ground pin current increases in order to drive the additional parasitic capacitances of the increased device sizing. The proposed design will be compared against the classical two-stage OTA and other related work.

2.1. Two-stage cascaded OTA

Figure 2 shows a classical two-stage OTA in CMOS technology proposed by Kim et al. [11]. It is operated in *+Vdd* and *–Vss* power supply with an external bias current *Ibias* and having a single ended output. The first stage is the *n*-channel differential input pair (m_1 and m_2) with *p*-channel current mirror as its active load (m_3 and m_4). The drain currents of m_1 and m_2 are mirrored to m_6 and m_5, respectively, which is the second (gain) stage through the classical current mirroring technique with the current ratio of 1:α [5].

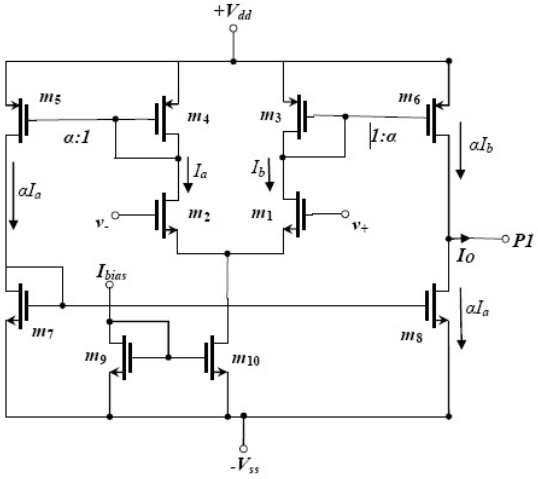

Fig. 2. Classical two-stage OTA in CMOS technology [11].

From Fig. 2, I_a and I_b can be obtained from Eq. (1) and (2):

$$I_a = \frac{I_{bias}}{2} - g_{m(2)} v_i \quad (1)$$

$$I_b = \frac{I_{bias}}{2} - g_{m(1)} v_i \quad (2)$$

The single ended output is taken from point *P*1 with current flow as shown in Eq. (3):

$$I_o = 2 g_{m(1,2)} \alpha v_i \quad (3)$$

where *vi*=(*v*+)–(*v*–) is called the differential input. Therefore, the voltage controlled current source is obtained and the transconductance of this OTA, *Gm*, is given by Eq. (4):

$$G_m = \frac{I_o}{V_i} = 2\alpha g_{m(1,2)} \quad (4)$$

It should be noted that according to Eq. (4), the transconductance of the OTA is dependent on the *gm* of the MOS transistors in the input differential pair which is in-turn dependent on the DC current through. Therefore, it can be said that it is a current controlled gain OTA. The parameter alpha (α) is called the gain factor which is modified by varying the ratio *W*/*L* of the second stage with respect to the input stage (*W*/*L*(6,5):*W*/*L*(3,4)).

Martinez-Garcia [5] proposed an error amplifier using two-stage cascoded OTA by adding m_{11}, m_{12}, m_{16} to be mirrored to m_{13}, m_{14} and m_{15} into the classical design of OTA. This technique is able to boost up the output impedance of OTA. This is shown in Fig. 3.

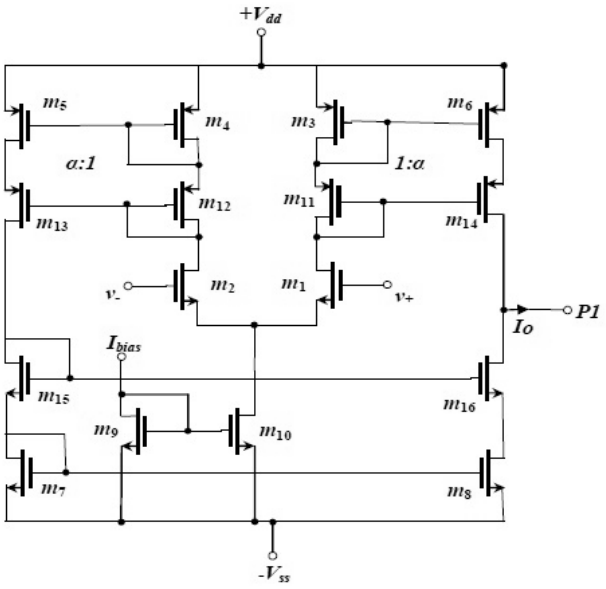

Fig. 3. Two-stage cascoded OTA in CMOS technology [5].

A constant output voltage can be achieved by controlling the load current flow through the pass device. By choosing appropriate values of resistor and reference voltage, the output voltage can be set as shown in Eq. (5).

$$V_0 = V_{ref} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

2.2. Body driven technique

The drain current is dependent on the gate-source and body-source voltages. The gate-source voltage is responsible for the vertical electric field, channel conductivity and drain current while the body-source voltage controls the drain current when the gate-source voltage is fixed. This effect stems from the influence of the substrate acting as a second gate and is called the body effect [7]. The threshold voltage scaling is performed at a rate that maintains constant electric

fields within the device and at the same time produces minimal power dissipation while having high efficiency.

The Body driven technique as shown in Fig. 4 has been proposed by Kim et al. [7] to decrease the threshold voltage and increase the drain current flowing from drain to source. This technique can be applied to error amplifier, voltage buffer and pass transistor to reduce chip size and maintain the same performance as a conventional LDO regulator. There are two types of body bias; forward body bias to decrease threshold voltage and reverse body bias to increase threshold voltage. The forward body bias is chosen because it reduces the size of transistor and reduce drop out voltage as compared with conventional transistor with the same threshold voltage.

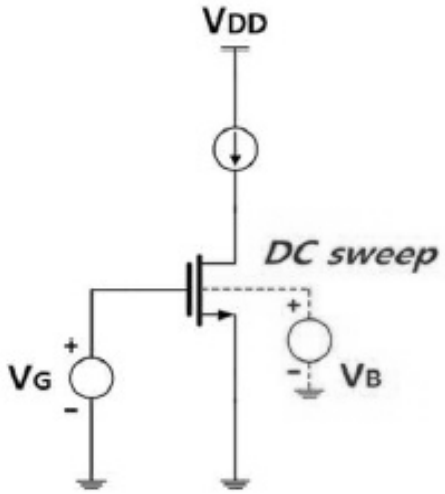

Fig. 4. Body bias technique [7].

The body effect is formulated as shown in Eq. (6):

$$V_{TH} = V_{TH0} - \gamma \left(\sqrt{|2\emptyset_F| + V_{BS}} - \sqrt{|2\emptyset_F|}\right) \quad (6)$$

where V_{TH0} denotes the threshold voltage with V_{BS} =0 and γ and $\emptyset_F$ are technology dependent parameters for a p-channel transistor [9].

2.3. Proposed LDO voltage regulator with two stage OTA using body driven technique

Figure 5 shows the improved two-stage OTA using body driven technique in 0.13 um CMOS technology. In the proposed design, the voltage body bias is applied to p-channel transistor *M13* with 0.4 V to reduce the drop-out voltage in LDO regulator. The pass transistor used is PMOS to increase the stability performance of LDO. In the proposed design, (*M4, M5*) and (*M13, M12*), (*M3, M6*) and (*M11, M14*), (*M15, M16*) and (*M7, M8*) form the cascoded pairs with current mirroring. The main design criteria of the proposed OTA is same as the classical OTA design.

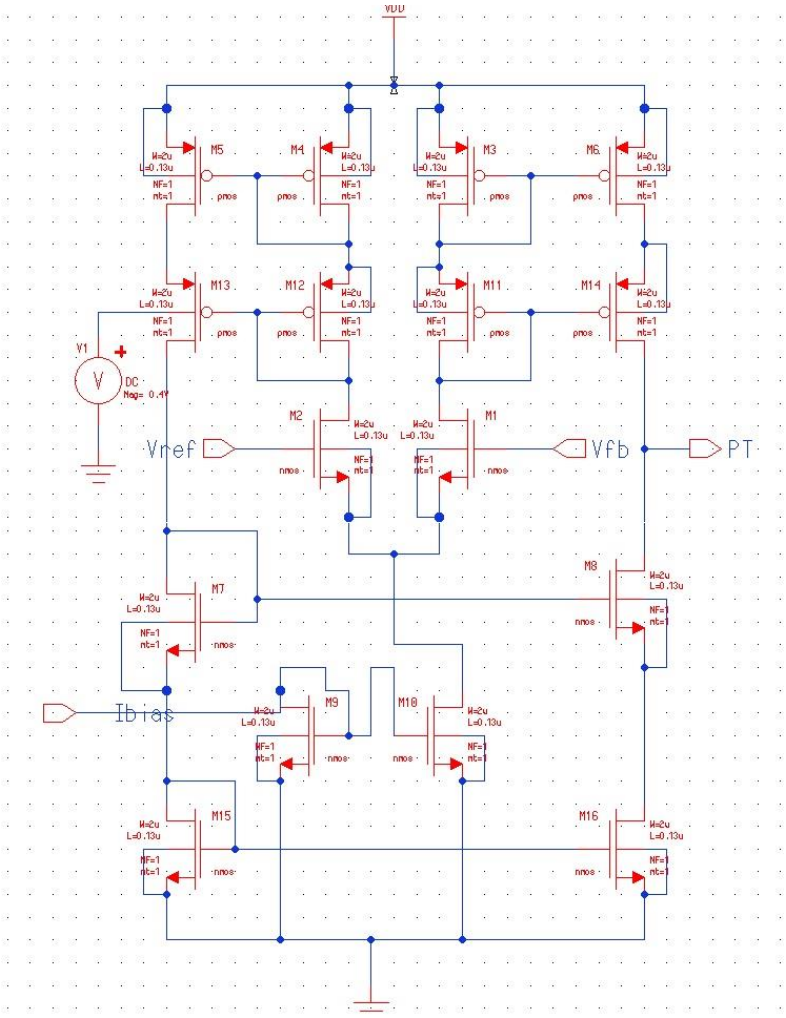

Fig. 5. Proposed two stage OTA with body effect technique.

The proposed LDO regulator is as shown in Fig. 6. The optimized parameters for the proposed LDO regulator in order to obtain a value of 4.5 V for V_{out} is as listed in Table 1.

Table 1. Optimized parameter for proposed LDO regulator.

Component	Value
R_{f1}	14.8kΩ
R_{f2}	2.5kΩ
R_{ESR}	0.05Ω
C_L	400pF
C_1	40pF
R_L	1MΩ

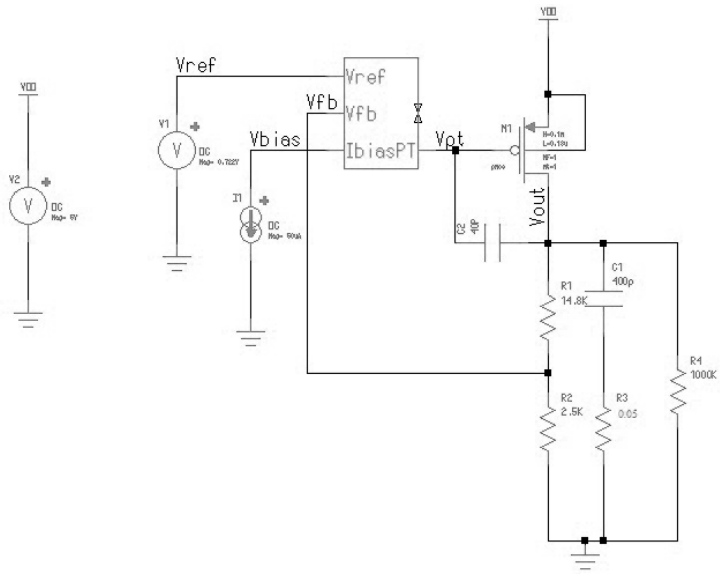

Fig. 6. Proposed LDO regulator.

In this paper, the value of R_{ESR} is 0.05Ω. If a larger value of R_{ESR} is used, it will increase the overshoot drastically. According to Kayal et al. [12], the value of R_{ESR} should be in the range of 0.05-10Ω. Dimensions of the transistors in the proposed LDO regulator are represented in Table 2.

Table 2. Dimensions of transistors in the proposed LDO regulator.

Transistor	Width(W) in um	Length (L) in um
*M*1, *M2*	65	0.13
*M*3, *M*4, *M*11, *M*12	5.2	0.13
*M*5, *M*6, *M*14, *M*13	100	0.13
M7, *M*8, *M*15, *M*16	100	0.1
*M*9, *M*10	13	0.13
PT (pass transistor)	0.5	0.13

Some study and analysis have been done in order to get the optimized parameters for the proposed LDO regulator. Analysis on the classical two stage OTA [11] using 0.13 TSMC technology yielded the dimension values as shown in Table 3.

Table 3. Dimensions of transistors in the classical LDO regulator [11].

Transistor	Width(W) in um	Transistor	Width(W) in um
*m*1, *m*2	65	m9, m10	13
*m*3, *m*4	5.2	m7, m8	100
*m*5, *m*6	100	Pass transistor	0.5

Analysis was also performed on the two stage OTA proposed by Martinez-Garcia [5] using 0.13 TSMC technology by using the dimension as shown in Table 4 and varying the width of the pass transistor.

Table 4. Dimension of transistors proposed by Martinez-Garcia [5].

Transistor	Width(W) in um	Length (L) in um
*m*1, *m*2	65	0.13
*m*3, *m*4, *m*11, *m*12	5.2	0.13
*m*5, *m*6, *m*14, *m*13	100	0.13
*m*7, *m*8, *m*15, *m*16	100	0.13
*m*9, *m*10	13	0.13

In addition, different values of load resistor, R_L (0 Ω, 10 Ω, 45 Ω 1 kΩ, 10 kΩ, 100 kΩ, 1 MΩ), load capacitor, C_L (400 pF, 1 uF, 4.7 uF, 1 pF, 500 nF) and input voltage (3.3 V, 3.4 V, 4.8 V, 5 V, 5.1 V, 5.2 V) were used in the analysis. The body bias technique was applied to the transistor *M13* in the OTA circuit.

3. Results and Discussion

The design and simulation of the proposed design are performed in 0.13 um CMOS technology. The proposed circuit is operating in low power and high voltage circuit. The proposed design is novel as it combines a two-stage OTA with body bias technique to reduce the drop out voltage of LDO regulator. In addition, PMOS is employed as a pass transistor yielding a more stable output voltage. The properties of voltage and current bias used in the simulation are described in Table 5. According to Eq. (5), to obtain the value of V_{out}=4.5 V, R_{f1}=14.8$k\Omega$ and R_{f2}=2.5$k\Omega$ are to be selected. The capacitor *C1* (Miller capacitor) is attached between two high impedance points in the circuit to ensure a good phase margin to the design. The value of *C1* is set to 40pF and the load capacitance, C_L is set to 0.4nF.

Table 5. Design specification for proposed LDO regulator.

Parameter	Value
Variation output voltage (ΔV_{out})	500 mV
Reference voltage (V_{ref})	650 mV
Bias Current (I_{bias})	50 uA

The simulation results of all the analysis performed on the different designs are as described in Fig. 7.

3.1. Analysis on classical two stage OTA using 0.13 TSMC technology

Classical two-stage OTA has been proposed by Kim et al. [11] as shown in Fig. 2. The OTA is built and simulated with +*Vdd*=5 V as shown in Fig. 7. This performance of the classical two stage OTA is shown in Fig. 8. From the results, it is found that the pass transistor voltage, V_{PT} also known as drop out voltage is 89.579 mV and the power dissipation is 1.358 mW.

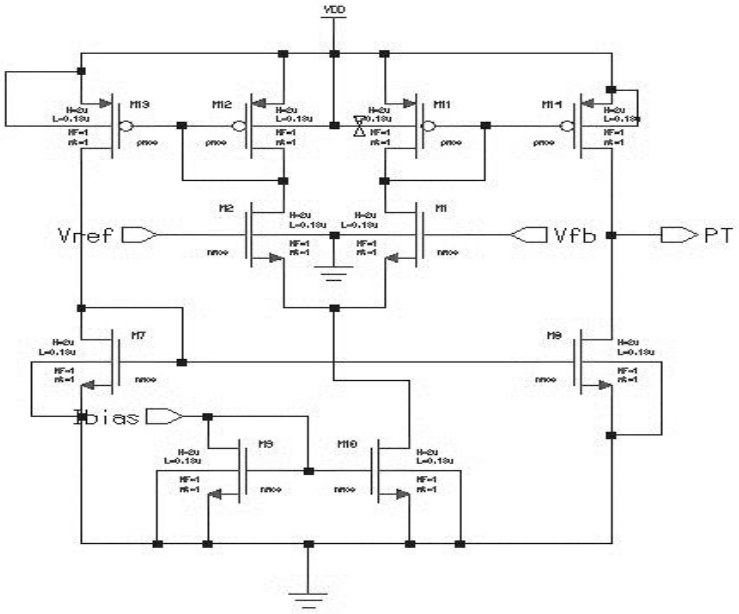

Fig. 7. Classical two-stage OTA in CMOS technology [11].

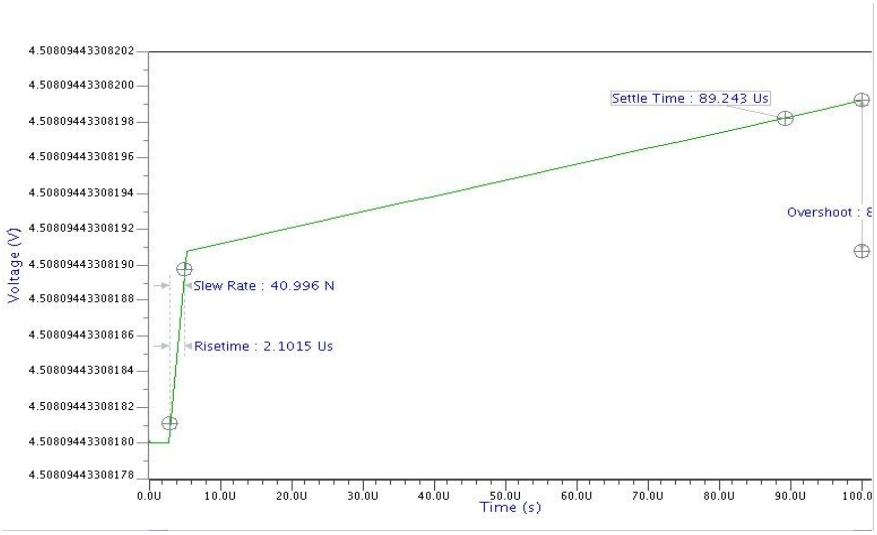

Fig. 8. Performance V_{out} for classical two-stage OTA using in LDO regulator.

3.2. Analysis on two stage OTA using 0.13 TSMC technology proposed by Martinez-Garcia [3] and with varying width of pass transistor

Two-stage OTA proposed by Martinez-Garcia [5] shown in Fig. 9 was designed using the dimension of transistor for OTA as given in Table 4. The body of all transistors used in this design is assumed without bias.

From the simulation results shown in Table 6, it is observed that when the width of the pass transistor is varied, the V_{out} and power dissipation will be affected.

However, there is no effect on the drop out voltage. When the width is increased, the power dissipation and output voltage also increase. Figure 10 shows the performance of V_{out}. It is observed that the settling time is 29. 275 us.

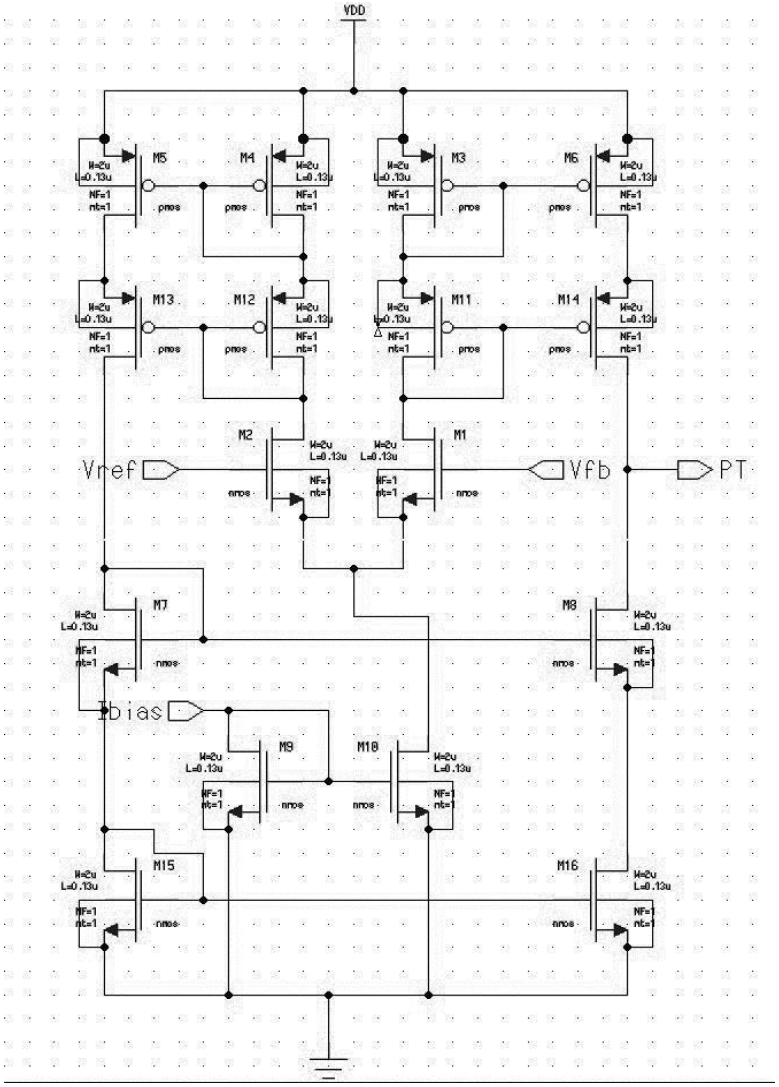

Fig. 9. Two stage OTA proposed by Martinez-Garcia [5].

Based on the analysis performed on the different designs, the performance comparison between the classical OTA [11], two-stage OTA proposed by Martinez-Garcia [5] with 0.13 um CMOS technology and with 0.35 um CMOS technology [5] is summarised in Table 7. It is observed that by using 0.13 um CMOS technology, the low drop out voltage can be improved from 60 mV to 33.0631 mV. In addition, the circuit proposed by Martinez-Garcia [5] is able to improve the low drop out by about 63 percent as compared to the classical OTA circuit.

Table 6. Simulation results for two-stage OTA in LDO regulator proposed by Martinez-Garcia [5].

Parameter	V_{out}/V	V_{PT}/mV	$P_{dissipation}$/mW
W_{PT} = 0.5 um	4.5123	33.0631	1.3593
W_{PT} = 2 um	4.9141	33.0631	1.4753
W_{PT} = 10 um	4.9851	33.0631	1.496
W_{PT} = 50 um	4.997	33.0631	1.4997
W_{PT} = 100 um	4.9985	33.0631	1.5

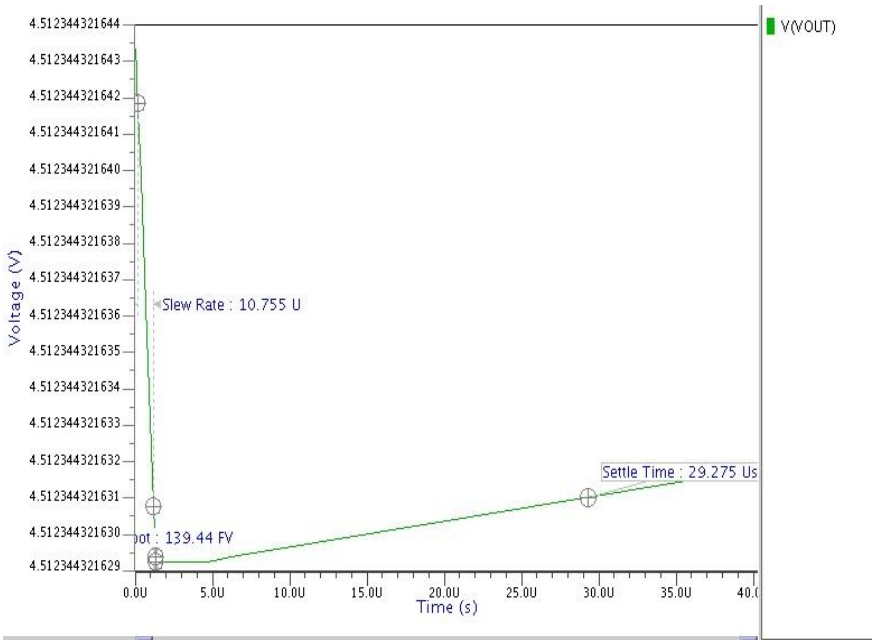

Fig. 10. Performance V_{out} for two-stage OTA proposed by Martinez-Garcia [5].

Table 7. Comparison between two-stage OTA.

Parameter	V_{out}/V	V_{PT}/mV	V_{fb}/mV	P_{diss}/mW
Classical two-stage OTA 0.13 um tech [11]	4.5081	89.5785	651.4587	1.358
Two-stage OTA 0.13 um tech [5]	4.5123	33.0631	652.0729	1.3593
Two-stage OTA 0.35 um tech [5]	4.5	60	NA	0.54

Table 8 shows the effect of varying the load resistance, R_L on the voltage and power dissipation. The value of feedback voltage to the error amplifier will vary as well. The error amplifier in the negative feedback condition will decide the output voltage (V_{out}) by comparing the error signal with V_{ref} that is set to 0.65V. The load resistance will also have an impact on the power dissipation (P_{diss}). When R_L is increased, P_{diss} also increases. So, the optimized value of R_L needs to be chosen when designing the LDO regulator in order to minimise power dissipation in the circuit.

Table 8. Simulation results for two-stage OTA with different load resistor value.

Parameter	V_{out}/V	V_{PT}/mV	V_{fb}/mV	P_{diss}/mW
R_L = 10Ω	0.259	33.0631	37.4415	129.6634
R_L = 45Ω	1.1536	33.0631	166.7023	128.5394
R_L = 1kΩ	4.7293	33.0631	683.4301	25.044
R_L = 10kΩ	4.9599	33.0631	716.748	3.9439
R_L = 100kΩ	4.9828	33.0631	720.0557	1.7197
R_L = 1MΩ	4.9851	33.0631	720.38	1.496

Table 9 shows the effect of varying the load capacitor, C_L on the voltage and power dissipation. It is observed that the load capacitor has no effect on the values of the parameters.

Table 9. Simulation results for two-stage OTA with different load capacitor value.

Parameter/nF	V_{out}/V	V_{PT}/mV	V_{fb}/mV	P_{diss}/mW
C_L = 0.001	4.9854	33.0631	720.429	1.4713
C_L = 0.4	4.9854	33.0631	720.429	1.4713
C_L =500	4.9854	33.0631	720.429	1.4713
C_L = 1000	4.9854	33.0631	720.429	1.4713
C_L = 4700	4.9854	33.0631	720.429	1.4713

Table 10 shows the effect of varying the input voltage, V_{in} on the voltage and power dissipation. By varying the input voltage, all parameter taken for analysis varies as well. The value of V_{out} varies in the range of 1.4-1.5 mV from the input voltage.

Table 10. Simulation results for two-stage OTA with different input voltage.

V_{in}/V	V_{out}/V	V_{PT}/mV	V_{fb}/mV	P_{diss}/mW	ΔV_{out}/mV
3.3	3.2986	19.637	476.6723	0.6618	1.4
3.4	3.3986	20.561	491.1219	0.7005	1.4
4.8	4.7985	32.874	693.4287	1.3699	1.5
5	4.9985	33.0631	722.3279	1.5022	1.5
5.1	5.0985	33.1527	751.2349	1.5951	1.5
5.2	5.1985	33.2463	751.2349	1.5951	1.5

3.3. The application of body bias technique to the transistor in OTA

The two-stage OTA with body bias technique shown in Fig. 5 is designed based on the dimensions of transistor for OTA as in Table 2. Body bias technique of 0.4V is applied to transistor M_{13} in the two-stage OTA. This LDO regulator is simulated with V_{in} ranging from 3.3 V to 5.2 V. It is found that the designed circuit fits the specifications as shown in Table 5. Table 11 shows the summary of the simulation results obtained.

Table 11. Simulation results obtained for proposed two-stage OTA with body bias technique.

Parameter	V_{out}/V	V_{PT}/mV	V_{fb}/mV	P_{diss}/mW	I_{LOAD}
Two-stage OTA by body bias technique	4.5115	32.060	651.9559	1.359	265.092uA

Figure 11 shows the waveform result for the proposed designed with the input voltage of 5V to provide a regulated output voltage of 4.5 V, drop out voltage of 32.06 mV and a load current of 0.265 mA at full load condition. From Fig. 12, the settling time for this technique is 16.744 us which is much faster than using the proposed OTA by Martinez-Garcia [5] which is 29.275 us and classical OTA [11] at 89.243us using 0.13 um CMOS technology. In terms of stability, it is observed that after 25 us the value of V_{out} is constant. Comparing to the result reported by Martinez-Garcia [5], it is found that after 25us the output voltage is still increasing.

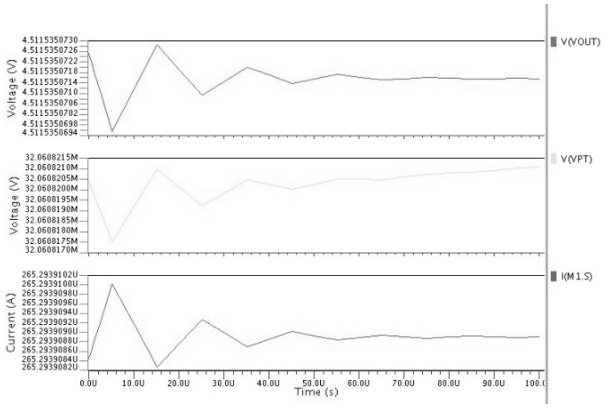

Fig. 11. Simulation result for V_{out}, V_{PT} and I_{load}.

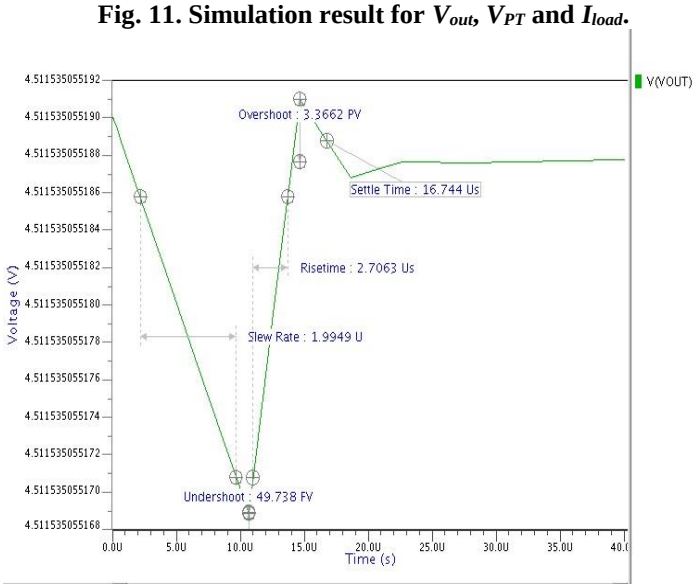

Fig. 12. Performance V_{out} for two-stage OTA with body bias technique.

Table 12 shows the comparison between the proposed OTA design with other related work. It is observed that by using the body bias technique of 0.4 V at transistor M_{13}, the performance of the low drop out voltage is better. The drop out voltage difference is 1 mV as compared to the method used by Martinez-Garcia [5].

Figure 13 shows the layout of the proposed two-stage OTA. The total layout area obtained for OTA is (16.75×42) um^2.

Table 12. Comparison between two-stage OTA for classical [11] and two-stage OTA proposed by Martinez-Garcia [5] using 0.13 um CMOS technology.

Parameter	V_{out}/V	V_{PT}/mV	V_{fb}/mV	P_{diss}/mW
Classical two-stage OTA 0.13 um tech [11]	4.5081	89.5785	651.4587	1.358
Two-stage OTA 0.13 um tech [5]	4.5123	33.0631	652.0729	1.3593
Two-stage OTA 0.35 um tech [5]	4.5	60	NA	0.54
Proposed Two-stage OTA using body bias technique	4.5115	32.060	651.9559	1.3593

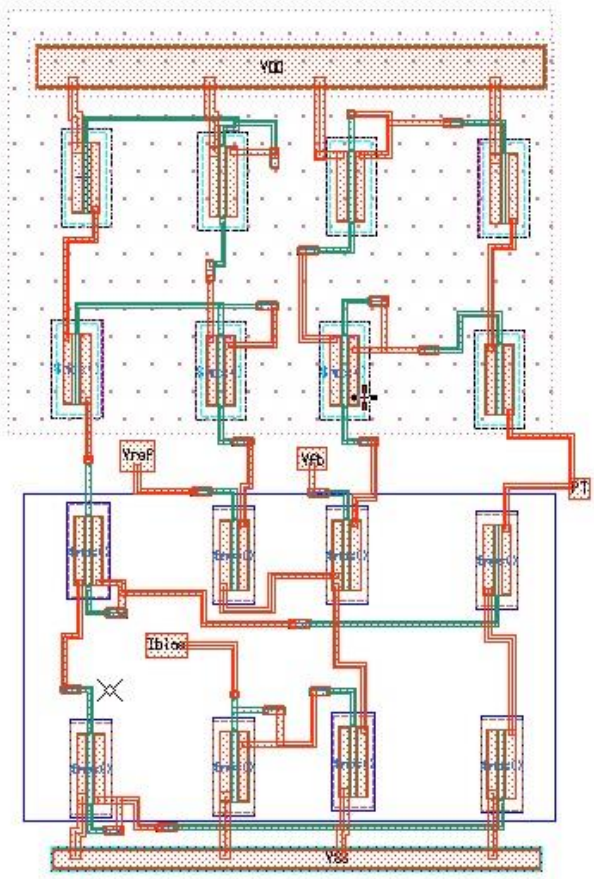

Fig. 13. Layout for proposed two-stage OTA.

Finally, the performance comparisons of the proposed LDO regulator with various techniques is shown in Table 13. Compared to the other techniques, it is found that the proposed two-stage OTA in LDO regulator with body bias technique is giving the lowest drop out voltage which is 32.060 mV. This shows a very promising opportunity to apply the proposed technique to enhance chip level power management for SoC applications.

Table 13. LDO voltage regulator performance comparison.

Performance	2014 [3]	2014 [10]	2014 [9]	2013 [8]	2013 [5]	This work
Technology (µm)	0.18	0.18	0.18	0.18	0.35	0.13
Supply Voltage (V)	1.8	1.8	1.45	1.8	5	5
Output Voltage (V)	1.6	1.6	1.4	1.64	4.5	4.5
Drop Out Voltage (mV)	200	200	200	160	60	32.060
Load current (mA)	50	0.5	100	150	450	0.265
Settling time (us)	6	1.147	0.5	NA	40	16.744

4. Conclusions

A low drop out (LDO) voltage regulator based on two-stage cascoded operational transconductance amplifier (OTA) with body bias technique is proposed in a 0.13 um CMOS technology. The technique is applied to the OTA as an error amplifier in this design. It is designed with the input voltage of 5 V to provide a regulated output voltage of 4.5 V. The LDO regulator has the drop out voltage of 32.06 mV at full load condition. The power dissipation also has a good performance which is 1.3593 mW. The proposed technique shows promising results and improvement when compared with other related work.

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