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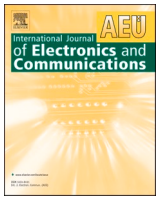

Regular paper

Design of a capacitor-less adaptively biased low dropout regulator using recycling folded cascode amplifier

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ABSTRACT

This paper starts with a comprehensive analysis of the trade-offs among various performance parameters in conventional adaptively biased low dropout regulator (AB-LDO) and then proposes a new structure of output capacitor-less AB-LDO, employing recycling-folded-cascode(RFC) amplifier, to optimize the different trade-offs. With this special structure, the proposed AB-LDO finally achieves faster dynamic response, better linear and load regulation without increasing power consumption. In addition, cascode compensation is employed to bring a wider load range while ensuring loop stability. Finally, the proposed AB-LDO is implemented in 0.18μ m CMOS process and experimental results show that a low quiescent current (10–50.25μA), good load regulation of 0.48 mV/mA, undershoot of 92 mV and overshoot of 86 mV with high current efficiency of 99.95% have been achieved.

1. Introduction

Low Dropout Regulators (LDO) are key components in System-on-Chip (SoC) designs, supplying well-regulated output voltages to noise-sensitive blocks [1,2,3,4,5]. Among all the designed regulators, the adaptively biased low dropout regulator (AB-LDO) is the most widely used due to its unique adaptive biasing design. In fact, with adaptive biasing scheme, the quiescent current of the AB-LDO is determined by the fixed bias current, adaptive biasing ratio and the load current, which indicates that the dc operating point of the AB-LDO is not fixed and can be specifically set as needed, making the AB-LDO perform differently at different load conditions [6,7,8,9]. On the one hand, when it operates at high load current condition, the AB-LDO can achieve faster dynamic response with high loop bandwidth and dynamic current of the amplifier. On the other hand, AB-LDO can achieve higher current efficiency with a lower fixed bias current when it operates at low load current condition.

Although there are many advantages, several limitations still exist in the AB-LDO [10,11,12,13,14]. For instance, it is still challengeable for the AB-LDO to achieve faster dynamic response with a lower fixed bias current which brings lower loop bandwidth and dynamic current when it operates at low load current condition. In other words, the trade-off between dynamic response and current efficiency of AB-LDO still need consideration and improvements. Besides, loop gain of the conventional AB-LDO is relatively low when it operates at high load condition, mainly due to low DC gain of error amplifier under high load current, which in turn causes worse regulation. While the method of increasing the quiescent current to increase the loop gain will lead to a decrease in current efficiency, so there is a trade-off between loop gain, regulation and current efficiency [15].

Most of the AB-LDOs proposed in the past researches use two-stage or multi-stage amplifier as the error amplifier, just as shown in Fig. 1(a), to achieve better performance in regulation and dynamic response. For example, the paper [11] proposes an output-capacitor-free AB-LDO, which uses two-stage amplifier combined with Q-reduction compensation to achieve both high-precision regulation and extended loop bandwidth. And another output capacitor-less AB-LDO proposed in the paper [12] also employs two-stage amplifier and subthreshold undershoot-reduction technique to achieve faster dynamic response. Although the two structures in [11,12] have achieved the optimization of several parameters, they both use two-stage amplifiers, leading to excess power consumption and lower current efficiency. Therefore, it is more desirable to use single-stage amplifier to guarantee higher current efficiency for an AB-LDO at first. For instance, conventional AB-LDO employing single-stage folded-cascode(FC) amplifier and Miller compensation is the most widely used, but its loop bandwidth under low load condition is relatively low due to the fixed small quiescent current and its loop gain under high load condition is not so high, causing worse

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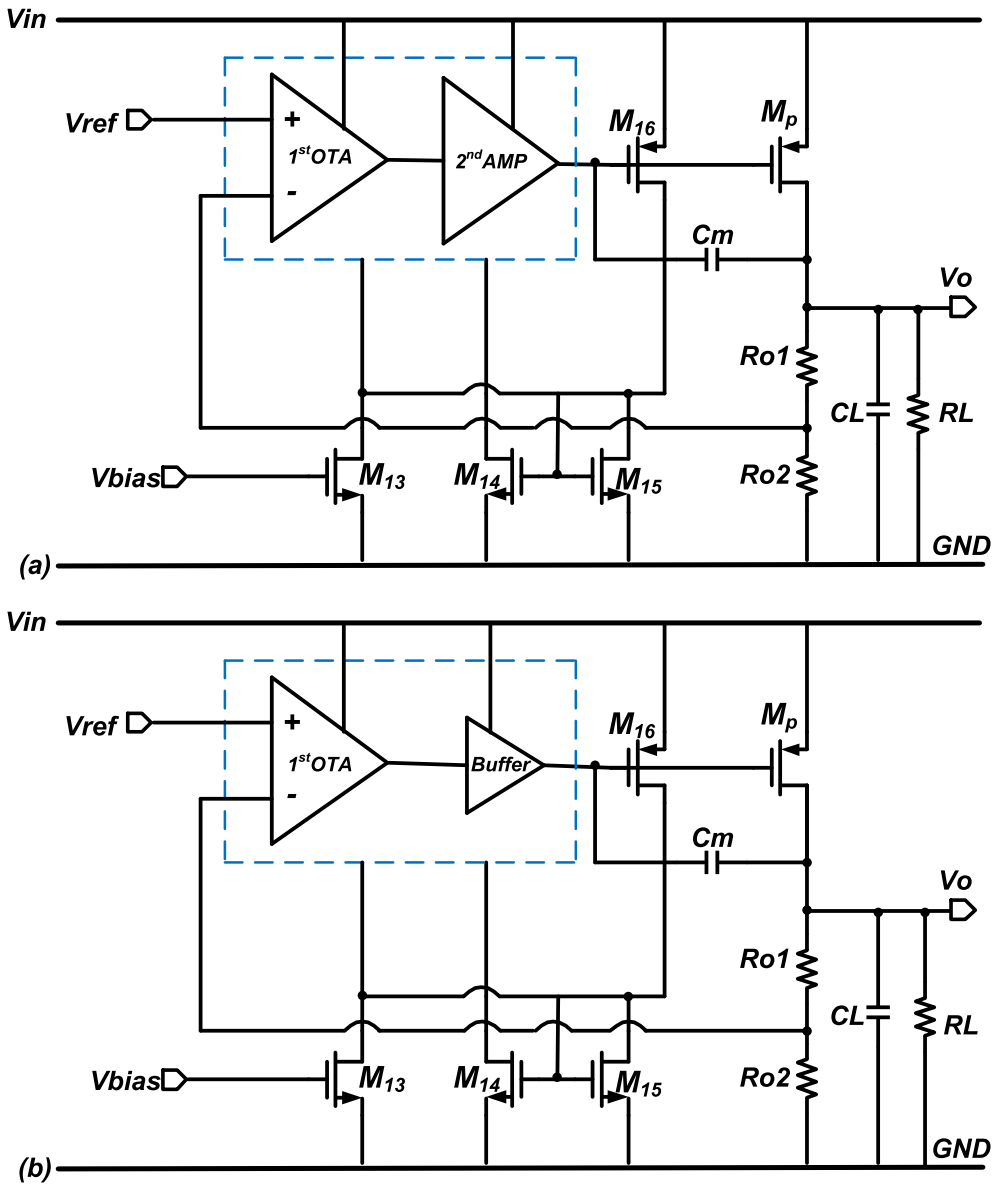

Fig. 1. Typical block diagram of (a)AB-LDO with two-stage amplifier (b)AB-LDO with transient enhanced buffer.

regulation and slower transient response. To further optimize this issue, several past AB-LDOs using single-stage amplifier combined with transient-enhanced buffer technique were proposed, as shown in the Fig. 1(b). Specifically, the paper [13] employs a single-stage amplifier combined with transient-enhancing buffer, finally achieving faster transient response, but the added buffer technique also makes the circuit more complicated and power consumption increased and loop gain of the conventional AB-LDO can not be improved by this structure.

Consequently, to further optimize the performance of the conventional AB-LDO and trade-offs among them, this paper proposes a new structure of output capacitor-less AB-LDO, which is mainly composed of recycling-folded-cascode(RFC) amplifier and cascode compensation. First, with the single-stage RFC amplifier, the proposed AB-LDO can achieve higher loop gain than the conventional AB-LDO using FC amplifier when they both operate at high load condition, ensuring better regulation for the regulator. Second, with the improved loop bandwidth and dynamic current of RFC amplifier, the proposed AB-LDO can achieve faster dynamic response than its conventional counterpart. Moreover, the above optimizations are all achieved under the premise that current efficiency of the proposed AB-LDO is the same as the conventional AB-LDO using FC amplifier. In addition, cascode compensation is used to guarantee better loop stability for the proposed AB-LDO and to optimize the trade-off between loop stability and load range. In conclusion, different parameters and the trade-offs among them can be comprehensively optimized by the proposed AB-LDO using RFC amplifier combined with cascode compensation.

This paper is organized as follows. Section 2 introduces the conventional output capacitor-less AB-LDO about its structure and analysis of the different trade-offs. Section 3 mainly presents the detailed design and analysis of the proposed AB-LDO. Section 4 and 5 respectively gives experimental results and the final conclusion about this approach.

2. Analysis of the conventional AB-LDO

This paper takes the AB-LDO using FC amplifier as an example to analyze the different trade-offs for conventional AB-LDO. The schematic of the conventional AB-LDO is shown in Fig. 2. It can be seen from the figure that this topology uses Folded-Cascode(FC) amplifier as the error

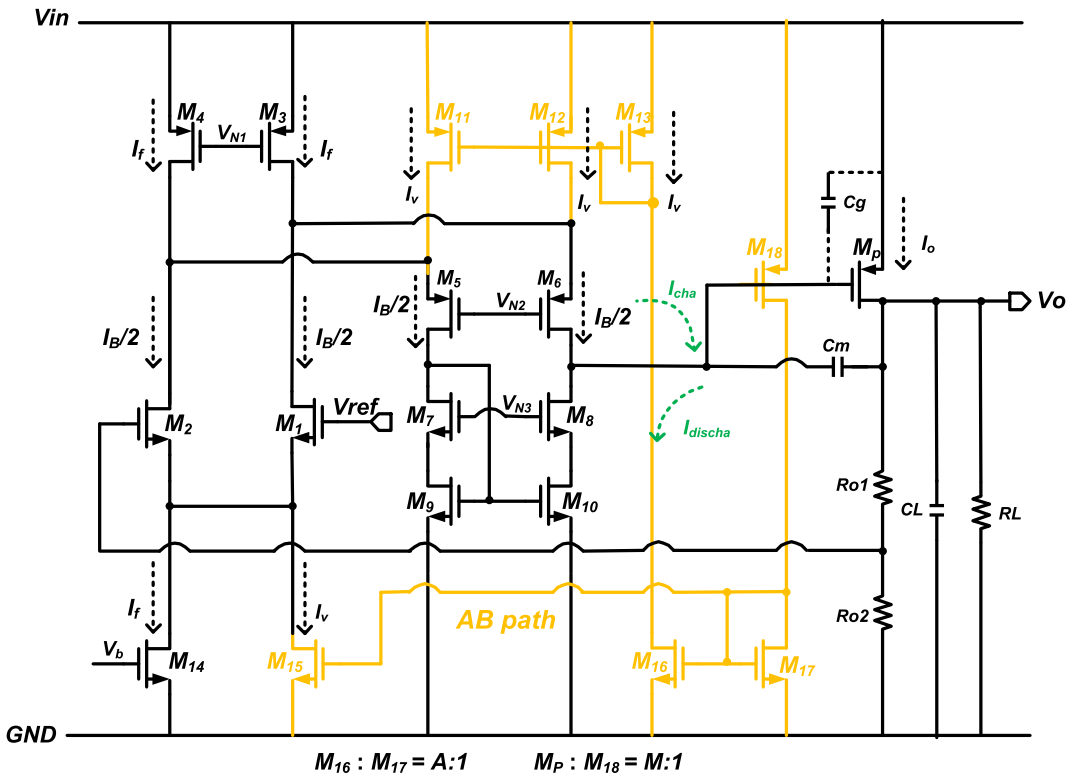

Fig. 2. Schematic of conventional output capacitor-less AB-LDO using FC amplifier.

amplifier and two adaptive bias paths($M_{18}-M_{17}-M_{16}-M_{15}$, $M_{18}-M_{17}-M_{16}-M_{13}$) are used to adjust the quiescent current of the amplifier to change with the load current, so as to realize the function of adaptive bias. Meanwhile, Miller compensation technology is used in the conventional AB-LDO to ensure the loop stability.

2.1. Trade-offs among quiescent current of amplifier, dynamic response and current efficiency of conventional AB-LDO

With adaptive biasing scheme, the bias current of the amplifier is composed of the fixed bias I_f and the adaptive bias current I_v, which is given by $I_B=I_f+I_v=I_f+\alpha I_o$, where α is the adaptive biasing (AB) ratio (A/M) and I_o is the load current. It can be seen that the value of I_B is mainly determined by I_f when the AB-LDO operates at low load current condition and by αI_o at high load current condition. For the output capacitor-less AB-LDO, the amount of the undershoot $\Delta V_{o,under}$ and overshoot $\Delta V_{o,over}$ with a load step of ΔI_o across the output capacitor C_L should be expressed as

$$\Delta V_{o,under} \approx \frac{\Delta I_o}{C_L}\left(\frac{1}{2\pi UGF_H}+\frac{(C_g+C_m)\Delta V_g}{I_{discha}}\right) \tag{1}$$

$$\Delta V_{o,over} \approx \frac{\Delta I_o}{C_L}\left(\frac{1}{2\pi UGF_L}+\frac{(C_g+C_m)\Delta V_g}{I_{cha}}\right) \tag{2}$$

where UGF_H and UGF_L respectively represent the loop bandwidth of AB-LDO operating at high and low load current condition, ΔV_g is the voltage variation of the gate of the power transistor, and I_{cha}, I_{discha} respectively represent the charging and discharging current of the Miller capacitor C_m and the large parasitic capacitor C_g. For conventional AB-LDO, when the load current switches from low to high load condition, the ability of the regulator to charge and discharge the capacitors will be limited due to the relatively small quiescent current of the amplifier, and the amount of undershoot $\Delta V_{o,under}$ is mainly determined by the value I_{discha}. Conversely, when the load current switches from high to low load condition, the charging and discharging capacity of AB-LDO is relatively strong, and the size of overshoot $\Delta V_{o,over}$ mainly depends on UGF_L. Specifically, for the conventional AB-LDO using FC amplifier and Miller compensation, the two parameters can be expressed as

$$UGF_{L,con} = \frac{G_{mL,con}}{C_m} = \frac{g_{m1}}{C_m} \tag{3}$$

$$I_{discha,con} = I_f = I_{dm,con} \tag{4}$$

Here, $G_{mL,con}$ is the effective transconductance of FC amplifier [25] at low load current condition and it is equal to g_{m1}, $I_{discha,con}$ is the discharging current of the conventional AB-LDO and $I_{dm,con}$ represents the dynamic current of FC amplifier. Generally, the input transistor of the FC amplifier M_1 is set to work in the weak inversion region and $G_{mL,con} \propto I_f$ at this time.

Increasing the quiescent current consumed by the conventional AB-LDO at low load condition I_f can indeed improve the loop bandwidth and discharging current to reduce the amount of ΔV_o, but it will also cause a decrease in current efficiency, which is described as the Eq. (5).

$$\eta_{Low} = \frac{I_o}{I_f + I_o} \tag{5}$$

Therefore, it is necessary to consider the trade-off between quiescent current, current efficiency and dynamic response. In fact, it is better to employ single-stage amplifier which can achieve higher transconductance and dynamic current without consuming more quiescent current to optimize this trade-off.

2.2. Trade-offs among load range, loop stability and dynamic response of AB-LDO

The major role of the PMOS power transistor is to deliver load current whereas the value of the delivered load current is always limited to a range called load range varying from I_{omin} to I_{omax}. According to the

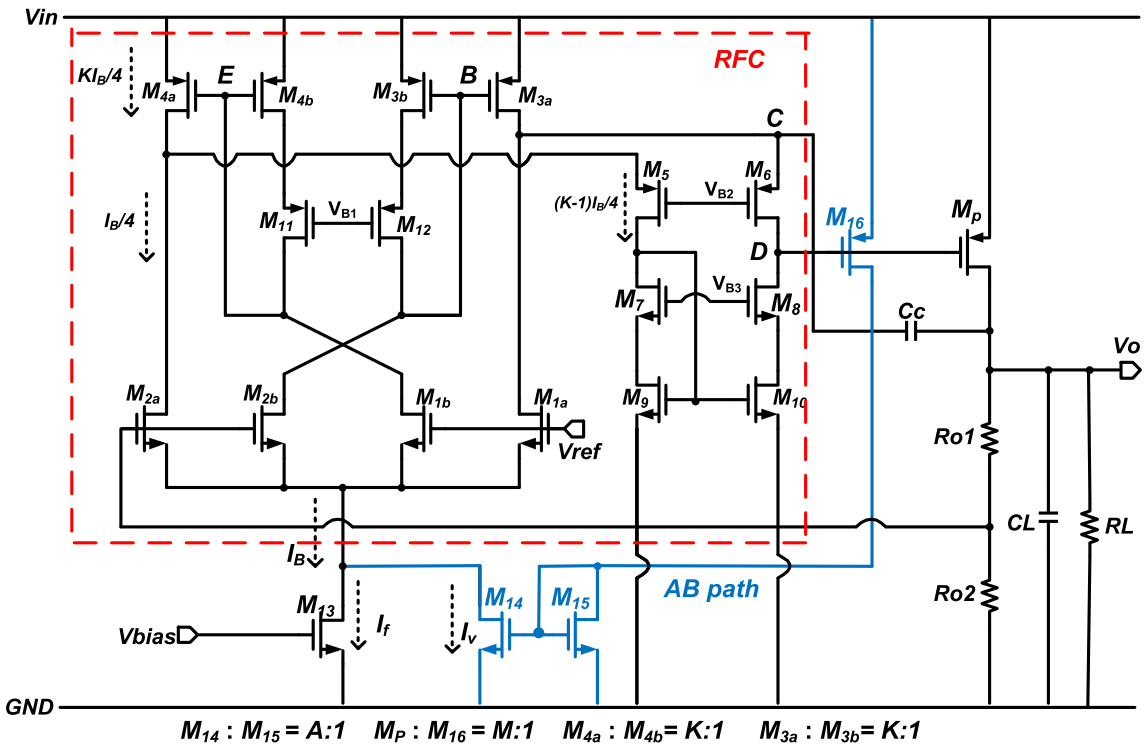

Fig. 3. Schematic of the proposed AB-LDO.

past researches in FC amplifier and Miller compensation, the transfer function of the conventional AB-LDO should be given by

$$H(s)_{con} = \frac{-\beta g_{m1} g_{mp} r_{o1} R_L \left(1 - s\frac{C_m}{g_{mp}}\right)}{\left(1 + sC_m g_{mp} r_{o1} R_L\right)\left(1 + s\frac{C_L}{g_{mp}}\right)} \tag{6}$$

where β represents the feedback coefficient $R_{o2}/(R_{o1} + R_{o2})$, r_{o1} is the output resistance of the FC amplifier and $r_{o1}=g_{m6}r_{ds6}r_{ds3}//g_{m8}r_{ds8}r_{ds10}$. And the two LHP poles and one RHP zero of the conventional AB-LDO can be specifically described as $p_{1,con}$, $p_{2,con}$, and $z_1=(g_{mp}/C_m)$. In detail,

$$p_{1,con} = \frac{1}{C_m g_{mp} r_{o1} R_L} \tag{7}$$

$$p_{2,con} = \frac{g_{mp}}{C_L} \tag{8}$$

It is known that the power transistor operates in the weak inversion region under low load condition and $g_{mp} \propto I_{omin}$ at this time. Usually, the conventional AB-LDO uses Miller compensation technology to push the dominant pole $p_{1,con}$ to a lower frequency by increasing the value of the compensation capacitor C_m, or increases the value of I_{omin} to push the dominant pole $p_{2,con}$ to a higher frequency, so as to achieve the separation of the two poles to improve loop stability. But the two methods will also cause the loop bandwidth and load range to decrease.

Therefore, the trade-off among loop stability, load range and loop bandwidth which is correlated with dynamic response needs to be considered. It is hoped that better compensation technology can be adopted to broaden the load range while still ensuring stability for AB-LDO. In addition, for the purpose of achieving enough loop phase margin to guarantee the stability of conventional AB-LDO, the achievable maximum loop bandwidth UGF_{max} at low load condition and $p_{2,con}$ should satisfy the formula (9)

$$UGF_{max} \approx \frac{1}{2} p_{2,con} \tag{9}$$

This equation also proves that if the non-dominant pole is increased, the achievable maximum loop bandwidth of the conventional AB-LDO can also be increased and the trade-off between loop stability and dynamic response will be optimized.

2.3. Trade-offs among DC gain of amplifier, regulation and current efficiency of AB-LDO

Line regulation and load regulation are significant parameters to measure the DC operating performance of AB-LDO. Usually, the two types of regulations are mostly affected by the loop gain of AB-LDO, which is also correlated with the DC gain of amplifier. According to the Eq. (6), the loop gain of conventional AB-LDO is given by

$$LG_{con} = \beta g_{m1} r_{o1} g_{mp} R_L \tag{10}$$

One disadvantage of the conventional AB-LDO is that the loop gain under high load condition is relatively low due to the lower DC gain of the FC amplifier under high load condition. In order to increase the loop gain, it is necessary to increase the quiescent current of the FC amplifier or continuously increase the size(W/L) of the input transistor to increase the transconductance g_{m1}. On the one hand, increasing the size of the input transistor will not only increase the area of the chip but also have a limit on the improvement effect of transconductance. On the other hand, increasing the quiescent current of the FC amplifier will also result in a decrease in current efficiency.

Considering the trade-off between loop gain, regulation and current efficiency, it is better to employ a single-stage amplifier which can also achieve high DC gain without consuming more quiescent current at the same time.

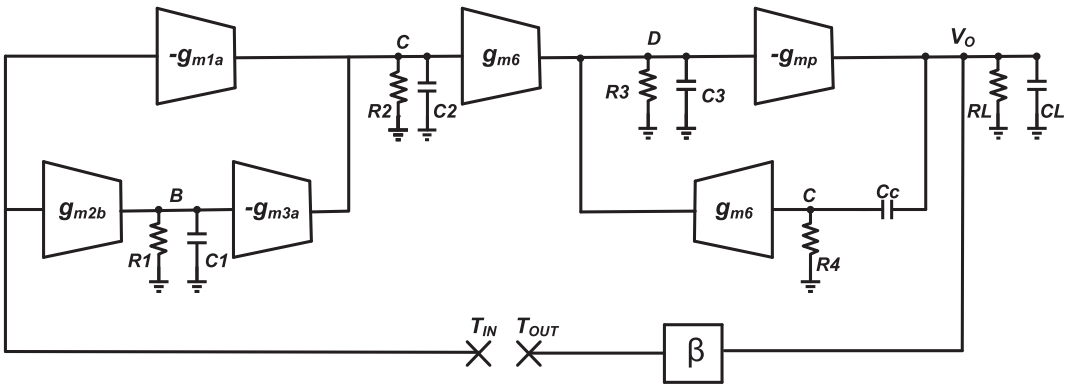

Fig. 4. Small-signal block diagram of the proposed AB-LDO.

3. Design and analysis of the proposed AB-LDO

To optimize the trade-offs analyzed in Section 2, this paper proposes a new structure of output capacitor-less AB-LDO presented in Fig. 3, which mainly employs recycling folded cascode amplifier [26,27] combined with cascode compensation. It can be clearly seen from the figure that due to the special current recycling structure, the proposed AB-LDO needs only one adaptive bias loop (M_{16} $-M_{15}$ $-M_{14}$) to realize the adaptive bias function. For a clearer and more consistent comparison with conventional AB-LDO, it is designed that quiescent current consumed by the proposed AB-LDO at different load conditions and AB ratios (in detail, A:1 = 8:1 and M:1 = 100:1) are the same with the conventional AB-LDO. Therefore, to meet this assumption, the size of the input transistor of the RFC amplifier in the proposed AB-LDO is designed to be half of that of the FC amplifier in conventional AB-LDO and g_{m1a}=g_{m1}/2.

3.1. Small signal analysis of the proposed AB-LDO

The small-signal block diagram of the proposed AB-LDO is shown in Fig. 4, which is employed to analyze the loop-gain transfer function of the proposed AB-LDO. Here, g_{m1a}, g_{m2b}, g_{m3a}, g_{m6}, g_{mp} respectively represent the transconductance of the different transistors displayed in Fig. 2, R_L and C_L respectively represent the load resistance and capacitance of the proposed AB-LDO, R_1, R_2, R_3 and R_4 respectively stands for the node resistance at different nodes. In particular, R_3=$g_{m6}r_{ds6}(r_{ds3a}//r_{ds1a})//g_{m8}r_{ds8}r_{ds10}$, R_1=$1/g_{m3b}$, R_2=$1/g_{m6}$, R_4=$1/g_{m6}$, C_3 is the large parasitic capacitance of the power transistor, C_1 and C_2 are very small so two large high-frequency poles will be generated at the nodes B and C, which could be negligible in this paper. In consideration of this point, the transfer function of the proposed AB-LDO can be given by

$$H(s)_{pro} = \frac{-\beta(1+K)g_{m1a}g_{mp}R_3R_L\left(1+s\frac{C_c}{g_{m6}}\right)}{1+as+bs^2+cs^3} \tag{11}$$

$$a = g_{mp}C_cR_3R_L \tag{12}$$

$$b = C_3R_3C_LR_L \tag{13}$$

$$c = \frac{C_3R_3C_LR_LC_c}{g_{m6}} \tag{14}$$

In detail, Eq. (11) indicate that the proposed AB-LDO has three poles and one LHP zero. The proposed AB-LDO is designed to be output capacitor-less and a large g_{mp} will be obtained when the PMOS power transistor is on its normal operation, which means that $g_{mp}C_cR_3R_L >> C_LR_L$ and the transfer function can be approximately described as

$$\begin{aligned} H(S)_{pro} &\approx \frac{-\beta(1+K)_{g_{m1a}g_{mp}R_3R_L}\left(1+s\frac{C_c}{g_{m6}}\right)}{\left(1+sg_{mp}C_cR_3R_L\right)\left(1+s\frac{C_3C_L}{g_{mp}C_c}\right)\left(1+s\frac{C_c}{g_{m6}}\right)} \\ &= \frac{-\beta(1+K)g_{m1a}g_{mp}R_3R_L}{\left(1+sg_{mp}C_cR_3R_L\right)\left(1+s\frac{C_3C_L}{g_{mp}C_c}\right)} \\ &= \frac{-\beta(1+K)g_{m1a}g_{mp}R_3R_L}{\left(1+\frac{s}{p_{1,pro}}\right)\left(1+\frac{s}{p_{2,pro}}\right)} \end{aligned} \tag{15}$$

it can be seen that there are two poles, which should be expressed as the dominant pole $p_{1,pro}$ and the non-dominant pole $p_{2,pro}$ respectively.

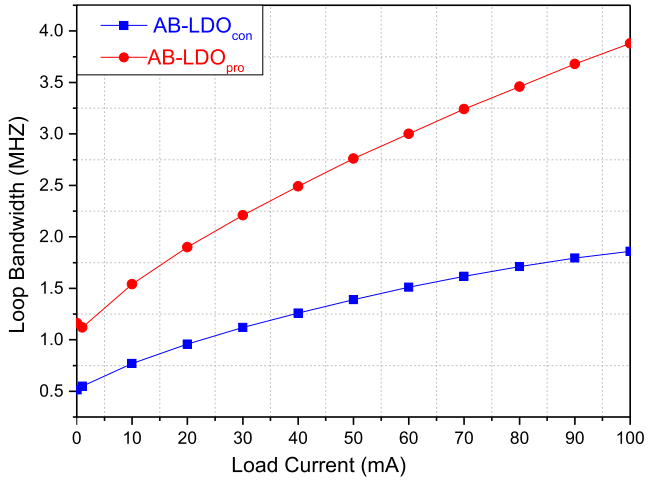

Fig. 5. Comparison of simulated loop bandwidth of conventional and proposed AB-LDOs at different load currents.

3.2. Optimizing the trade-off between current efficiency and dynamic response of the proposed AB-LDO

The proposed AB-LDO employs RFC amplifier, which performs well in improving loop bandwidth and loop gain. First, analogy to the Eq. (3), the loop bandwidth of the proposed AB-LDO at low load current condition $UGF_{L,pro}$ should be described as

$$UGF_{L,pro} = \frac{G_{mL,pro}}{C_c} = \frac{(1+K)g_{m1a}}{C_c} \tag{16}$$

$$G_{mL,pro} = (1+K)g_{m1a} = \frac{(1+K)}{2}g_{m1} \tag{17}$$

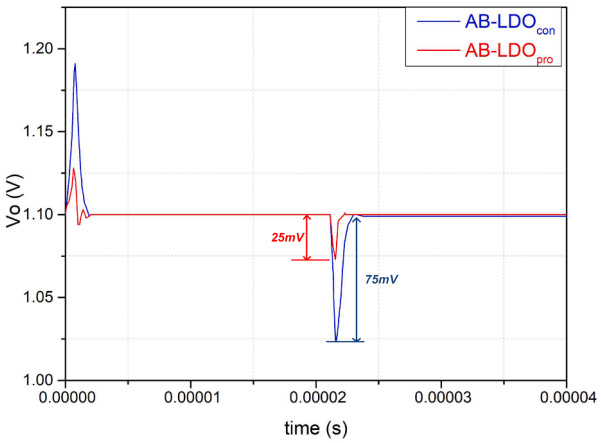

Fig. 6. Comparison of simulated transient response of conventional and proposed AB-LDOs with a 1μ s load step varying from 0.1 mA to 100 mA.

Here, K is the ratio of the current mirror marked in Fig. 3, $G_{mL,pro}$ is the effective transconductance of the proposed AB-LDO and C_c is equal to the Miller compensation capacitor C_m in the conventional AB-LDO. Comparing the Eqs. (3) and (16), it can be seen that with the improved transconductance $G_{mL,pro}$, the loop bandwidth of the proposed AB-LDO at low load condition is extended to a higher value, which is (1 + K)/2 times higher than its conventional counterpart $UGF_{L,con}$. Fig. 5 also proves this improvement, displaying that the simulated loop bandwidth of the conventional AB-LDO ranges from 0.5 MHz to 1.7 MHz, which has been increased by the proposed AB-LDO to 1.2 MHz-3.88 MHz when the load current varies from 0.1 mA to 100 mA. In addition, the discharging current of the proposed AB-LDO is given by

$$I_{discha,pro} = I_{dm,pro} = KI_f \tag{18}$$

where $I_{dm,pro}$ stands for the dynamic current of the RFC amplifier. Comparing the Eqs. (4) and (18), it is obvious to find that the discharging current of the proposed AB-LDO is K times that of the conventional AB-LDO when the same quiescent current are consumed by the two AB-LDOs, which should be mainly attributed to the enhanced dynamic current of the RFC amplifier. Both the improved loop bandwidth $UGF_{L,con}$ and discharging current $I_{discha,pro}$ will contribute to smaller $\Delta V_{o,under}$ and $\Delta V_{o,over}$ and bring faster dynamic response for the proposed AB-LDO.

Specifically, Fig. 6 gives a clear comparison of the simulated transient response of the two AB-LDOs, from which it is obvious to find that with the load current varying from 0.1 mA to 100 mA, both the output voltage variation ΔV_o and settling time of the proposed AB-LDO are much smaller than that of the conventional AB-LDO, indicating that the proposed AB-LDO achieves faster dynamic response.

Meanwhile, the proposed AB-LDO does not consume more quiescent current when achieving better performance in loop bandwidth and dynamic response, meaning that the trade-off between current efficiency and dynamic response can be optimized by the proposed AB-LDO.

3.3. Optimizing the trade-off between current efficiency and regulation of the proposed AB-LDO

According to the small-signal analysis in Section 3.1, loop gain of the proposed AB-LDO can be expressed as

$$\begin{aligned} &LG_{pro} \\ &= \beta(1+K)g_{m1a}R_3g_{mp}R_L \\ &= \beta\frac{(1+K)}{2}g_{m1}R_3g_{mp}R_L \end{aligned} \tag{19}$$

Here, g_{mp}, R_L and R_3 are designed to be the same with their

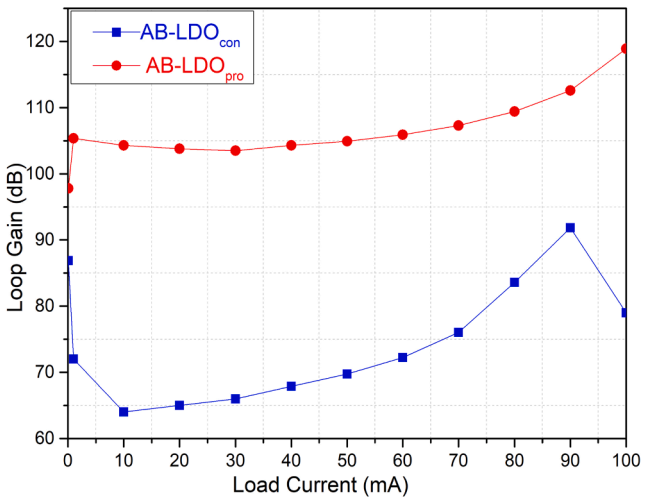

Fig. 7. Comparison of simulated loop gain of conventional and proposed AB-LDOs under different load currents.

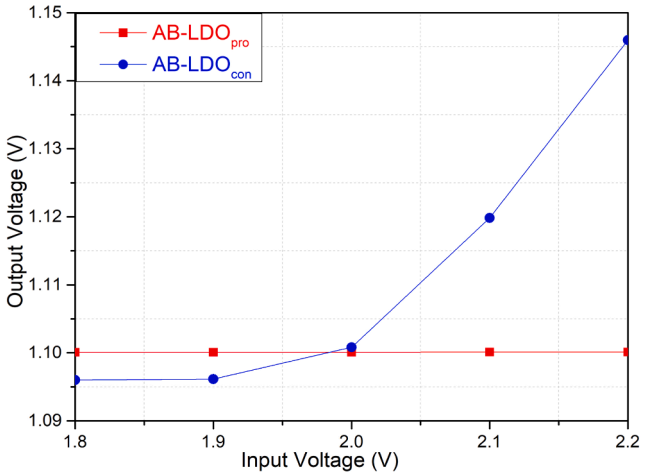

Fig. 8. Comparison of simulated line regulation of conventional and proposed AB-LDOs.

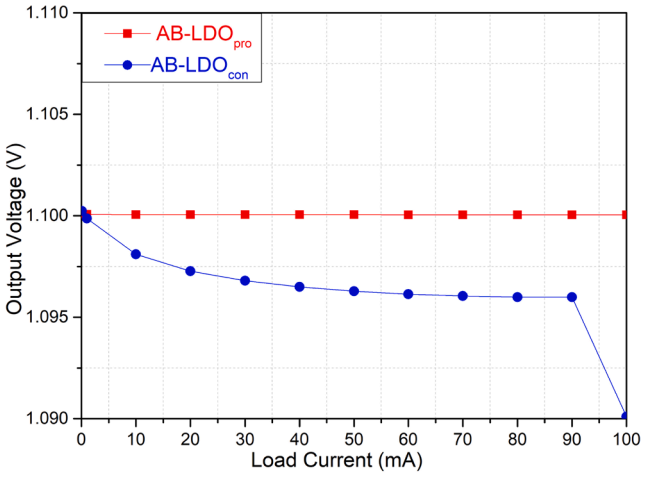

Fig. 9. Comparison of simulated load regulation of conventional and proposed AB-LDOs.

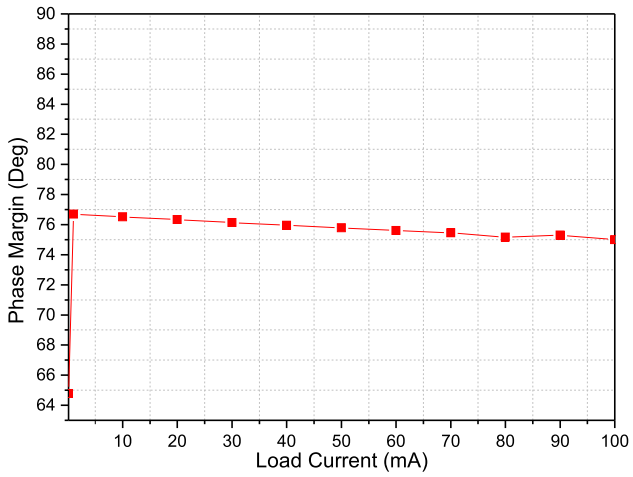

Fig. 10. Simulated phase margin of the proposed AB-LDO at different load currents.

counterparts in conventional AB-LDO and$R_3 = r_{o1}$. Supposing that both the conventional and the proposed AB-LDO operate at the high load condition, it is not difficult to conclude from the Eqs. (10) and (19) that the loop gain will be effectively improved by the proposed AB-LDO, which is (1 + K)/2 times higher than that of the conventional AB-LDO. Meanwhile, the improved loop gain will contribute better line and load regulation for the proposed AB-LDO working at high load condition.

Fig. 7 shows the comparison of the simulated loop gain of the two different AB-LDOs under different load currents, it can be seen that the loop gain of the proposed AB-LDO at all load currents are more than 97 dB, which are about 30 dB higher than the loop gain of the conventional AB-LDO. At the same time, it can be seen from the Fig. 8 that with the input voltage varying from 1.8 V to 2.2 V, the output voltage of the proposed AB-LDO is basically stable at 1.1 V, which is much better than the line regulation performance of the conventional AB-LDO. Besides, Fig. 9 shows the output voltage variation of the two AB-LDOs when the load current varies from 0.1 mA to 100 mA, from which the simulated load regulation of the proposed AB-LDO is calculated as 0.3uV/mA, which has been significantly improved compared with 42.3uV/mA of conventional AB-LDO.

From another perspective, attributed to the existence of the coefficient (1 + K)/2, it can be found that the proposed AB-LDO only needs smaller value of g_{m1} to achieve the same loop gain as the conventional AB-LDO, which also means that when achieving the same performance, the proposed AB-LDO will consume less quiescent current and therefore achieve higher current efficiency. In summary, the optimization of trade-off between current efficiency, loop gain and regulation can be achieved by the proposed AB-LDO.

3.4. Optimizing the trade-off between loop stability, transient response and load range of the proposed AB-LDO

The proposed output capacitor-less AB-LDO employs cascode compensation technology, mainly aiming to improve the stability and the load range. With cascode compensation, the non-dominant pole will be obtained at a higher frequency, according to the small-signal analysis, the detailed equation of $p_{1,pro}$ and $p_{2,pro}$ can be expressed as

$$p_{1,pro} = \frac{1}{C_c g_{mp} R_3 R_L} \tag{20}$$

$$p_{2,pro} = \frac{C_c}{C_3}\frac{g_{mp}}{C_L} \tag{21}$$

where the cascode compensation capacitor C_c is the same with Miller

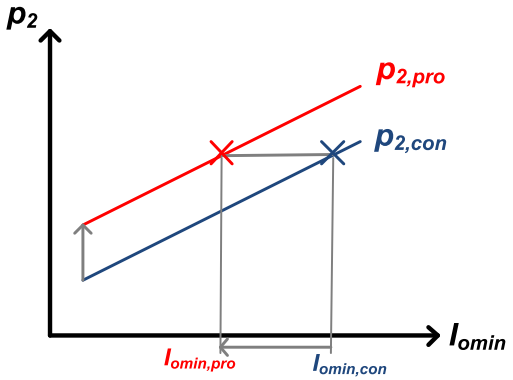

Fig. 11. Comparison between p_2 and I_{omin} of different AB-LDOs under low load condition.

capacitor C_m and it is much larger than the output capacitance of the amplifier C_3 so $(C_c/C_3) >> 1$. The Eqs. (7) and (20) indicate that both the dominant pole of the two AB-LDOs are located at the same frequency. Comparing the Eqs. (8) and (21), it can be found that due to the existence of C_c/C_3, the non-dominant pole of the proposed AB-LDO $p_{2,pro}$ is pushed to a higher frequency than $p_{2,con}$, indicating that better loop stability will be achieved by the proposed AB-LDO.

Fig. 10 gives the simulated phase margin curve of the proposed AB-LDO under the full load range where the load current varies from 0.1 mA to 100 mA. It is obvious to see that the phase margin of the proposed AB-LDO at all load conditions are quite high, ranging from 64 deg to 76.38 deg, which is enough to meet the require of the loop stability for the regulator. In addition, at the design stage, the loop stability of the proposed AB-LDO will continue to improve with the increase of C_c, but according to the equation (16), the increase of the compensation capacitor C_c will cause $UGF_{L,pro}$ to decrease, thereby slowing down the transient response of the proposed AB-LDO. At the same time, too large capacitance will cause the increase of the overall area of the chip. Therefore, the trade-off between loop stability, transient response, and chip area should be considered when choosing the value of C_c.

On the other hand, according to Eq. (9) in Section 2.2 and Eq. (1) in 2.1, it can be seen that with cascode compensation, the achievable maximum loop bandwidth UGF_{max} will be extended with an improved $p_{2,pro}$, which in turn reduces the amount of overshoot and brings faster dynamic response for the proposed AB-LDO.

Fig. 11 displays the comparison between the non-dominant pole $p_{2,con}$, $p_{2,pro}$ and load current I_{omin} when the two AB-LDOs operate at the low load condition. In fact, according to the analysis about the load range(I_{omin}-I_{omax}) in 2.2 and Eq. (21), it can be known that $p_2 \propto g_{mp} \propto I_{omin}$ under low load condition. Supposing that I_{omax} remains the same, it is obvious to find that in the case of the same load range is achieved(that is, I_{omin} is the same), the value of non-dominant pole of the proposed AB-LDO $p_{2,pro}$ is higher than its counterpart of the conventional AB-LDO $p_{2,con}$, while in the case of the same phase margin is achieved(that is, $p_{2,pro}$=$p_{2,con}$), the value of I_{omin} of the proposed AB-LDO will be smaller than its conventional counterpart, both indicating that the improved non-dominant pole $p_{2,pro}$ ensures a wider load range for the proposed AB-LDO.

With the above three points in mind, it can be shortly concluded that with cascode compensation, the proposed AB-LDO can firstly increase the non-dominant pole to a higher frequency than that of the conventional AB-LDO, thereby achieving better loop stability. Second, with the increased non-dominant pole, the maximum achievable loop bandwidth will be extended, bringing faster transient response for the proposed AB-LDO. Besides, the increased non-dominant pole also ensures smaller I_{omin} and wider load range for the proposed AB-LDO. In summary, the trade-off between loop stability, dynamic response and load range can be fully optimized by the proposed AB-LDO using cascode compensation.

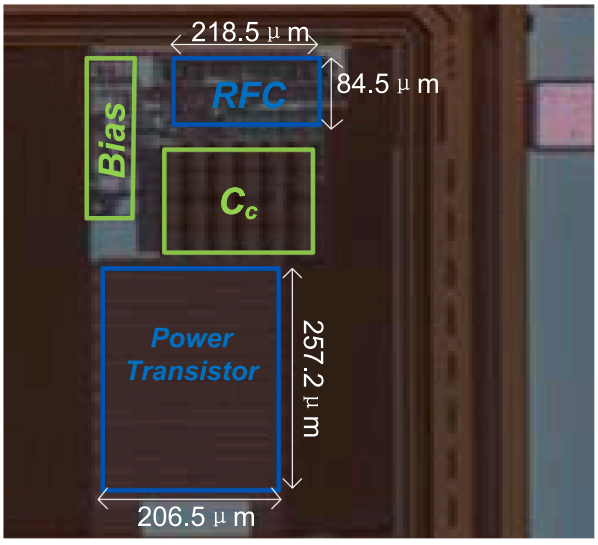

Fig. 12. The microphotograph of the proposed AB-LDO.

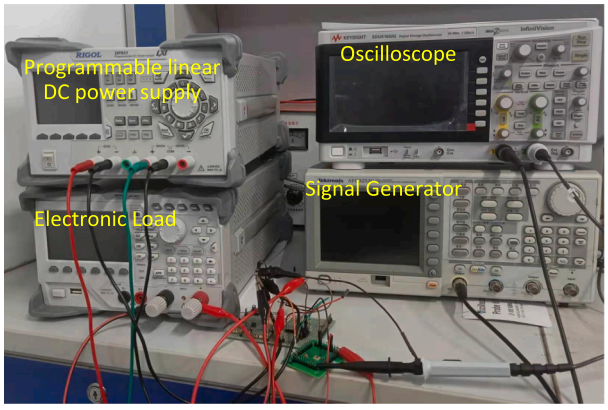

Fig. 13. The measurement setup for the proposed AB-LDO.

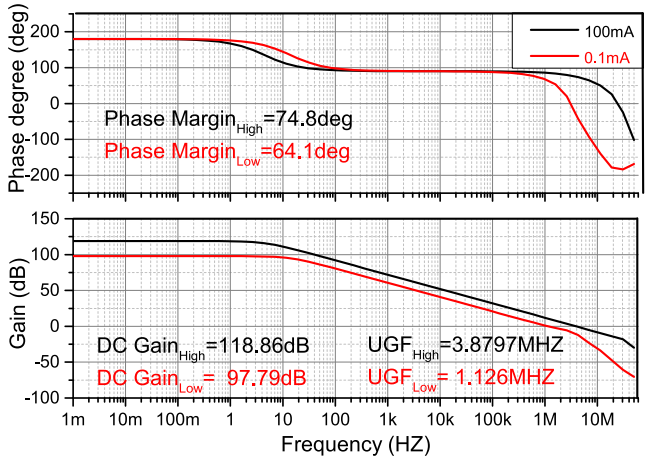

Fig. 14. Simulated frequency response of the proposed AB-LDO with a 100pF output capacitor.

4. Experimental results of the proposed AB-LDO

The AB-LDO using RFC amplifier was fabricated in SMIC 0.18μ m CMOS process and the die photo is shown in Fig. 12. The proposed AB-LDO is designed to achieve maximum output voltage of 1.6 V with an input voltage 1.8 V and drive a maximum output current of 100 mA. Specifically, the actual output voltage is set to 1.1 V as required. Besides, the value of K is set to 3, cascode compensation capacitor C_c in this paper is 12pF and a capacitor of 100pF is added at output port during experiment. Fig. 13 shows a picture of the measurement setup, where the four devices which have been employed can be seen: oscilloscope, signal generator, electronic load and power supply.

Fig. 14 shows the simulated frequency response of the proposed AB-LDO at low and high load current conditions, it can be seen that the loop bandwidth at high load current of 100 mA and low load current of 0.1 mA are specifically 3.879 MHz and 1.126 MHz and the loop gain under the two conditions are specifically 118.86 dB and 97.79 dB, both confirming that loop gain and bandwidth have been effectively improved by the AB-LDO using RFC amplifier. Meanwhile, the phase margin of the proposed AB-LDO at the two load conditions are more than 64 deg, which is enough to meet the require of the loop stability.

Fig. 15 shows the measured line regulation of the proposed AB-LDO at different load currents. It can be seen that with the input voltage varying from 1.8 V to 2.2 V, the output voltage is approximately 1.1 V and the variation are respectively 0.35 mV, 0.2 mV, 0.3 mV and 0.6 mV under the load current of 0.1 mA, 1 mA, 10 mA and 100 mA, through which the line regulation can be specifically calculated as 0.875 mV/V, 0.5 mV/V, 0.75 mV/V and 1.5 mV/V, proving that high loop gain has

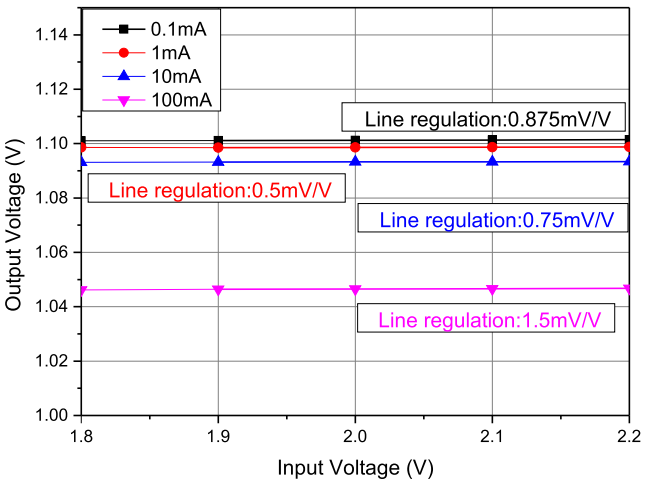

Fig. 15. Measured Line Regulation at different load conditions of the proposed AB-LDO.

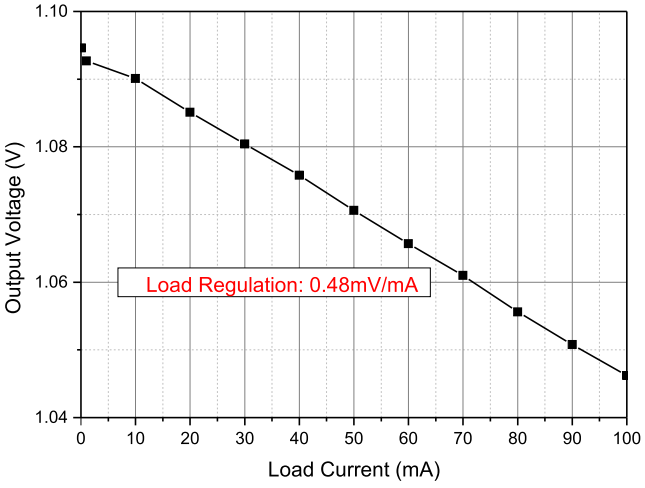

Fig. 16. Measured Load Regulation of the proposed AB-LDO with a 100pF output capacitor.

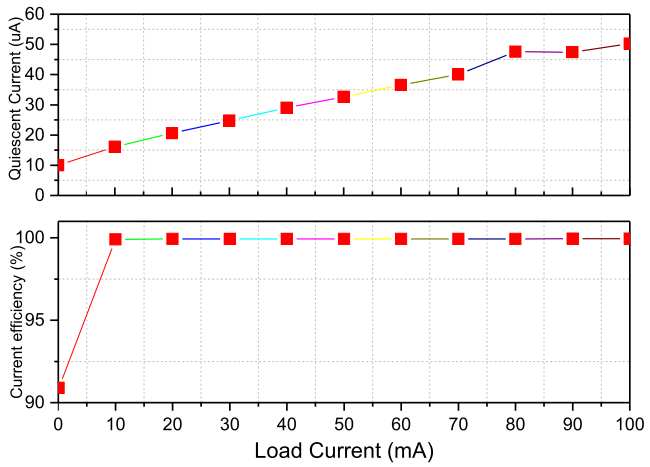

Fig. 17. Simulated quiescent current and current efficiency of the proposed AB-LDO at different load currents.

indeed brought excellent performance in line regulation for the proposed AB-LDO.

The measured load regulation is shown in Fig. 16, which displays that the output voltage varies from 1.0946 V to 1.0462 V with the load current ranging from 0.1 mA to 100 mA, and it can be translated to a load regulation of 0.48 mV/mA.

Fig. 17 displays the specific value of quiescent current consumed by the proposed AB-LDO and current efficiency at different load conditions. For AB-LDO, the quiescent current will continue to increase with the load current increases, it is obvious to find that the proposed AB-LDO consumes small quiescent of 10μA under low load current 100μA and only of 50.25μA under the high load current 100 mA. And the current efficiency curve indicates that the proposed AB-LDO achieves high current efficiency of 99.95% under most load conditions.

Fig. 18 shows the measured transient response of the proposed AB-LDO with a 500 ns load step varying from 0.1 mA to 100 mA, displaying that the overshoot of the output voltage is 162 mV and the undershoot is 174 mV. Similarly, Fig. 19 shows the measured transient response when the edge time is 1μ s, displaying that the overshoot of the output voltage is 86 mV and the undershoot is about 92 mV.

Fig. 20 gives the comparison of the simulated and the measured power supply rejection ratio (PSRR), where the PSRR was measured in the frequency range of 10 kHz-1 MHz. The measured PSRR are respectively calculated as −36.4 dB, −30.1 dB, −29.4 dB and −25.9 dB under the frequency of 10 kHz, 50 kHz, 100 kHz and 500 kHz. Additionally, the Taable 1 also provides one of the experimental results of the oscilloscope, displaying that the PSRR is measured by using a sinusoidal signal of 496 mV at 1 MHz added to the input port V_{in} and the output voltage of 37.3 mV makes the PSRR at 1 MHz obtained as –22.5 dB.

Table 1 displays performance comparison with the previous researches. Specifically, FoM is a figure of merit to measure the comprehensive performance of the regulators. And the smaller the value of FoM, the better the comprehensive performance of the LDO. The paper [16] proposed a popular formula to calculate FoM, which is expressed as

$$FoM = T_R \times \frac{I_{qmin} + I_{qmax}}{2K_2 \Delta I_{omax}} \tag{22}$$

where K_2 is the ratio of the technology used in the previous work to this paper, I_{qmin} represents the minimum quiescent current, I_{qmin} is the maximum quiescent current and ΔI_{omax} represents the maximum load current. T_R [24] represents the transient response time, which is calculated by an approach based on the output voltage variation and the load transient measurement edge time T_{edge} and it should be expressed as

$$T_R = \begin{cases} \sqrt{\dfrac{2C_L \Delta V_{out} T_{edge}}{\Delta I_{omax}}}, & T_R \le T_{\text{edge}} \\ C_L \dfrac{\Delta V_{out}}{\Delta I_{omax}} + \dfrac{T_{edge}}{2}, & T_R > T_{\text{edge}} \end{cases} \tag{23}$$

Comparing the detailed performance parameters in the listed researches, it can be found that the proposed AB-LDO performs well in consuming a small I_{qmin} of 10μA and driving a load current $\Delta I_{o,max}$ of 100 mA with a 100pF output capacitor C_L. Consequently, an optimal FoM of

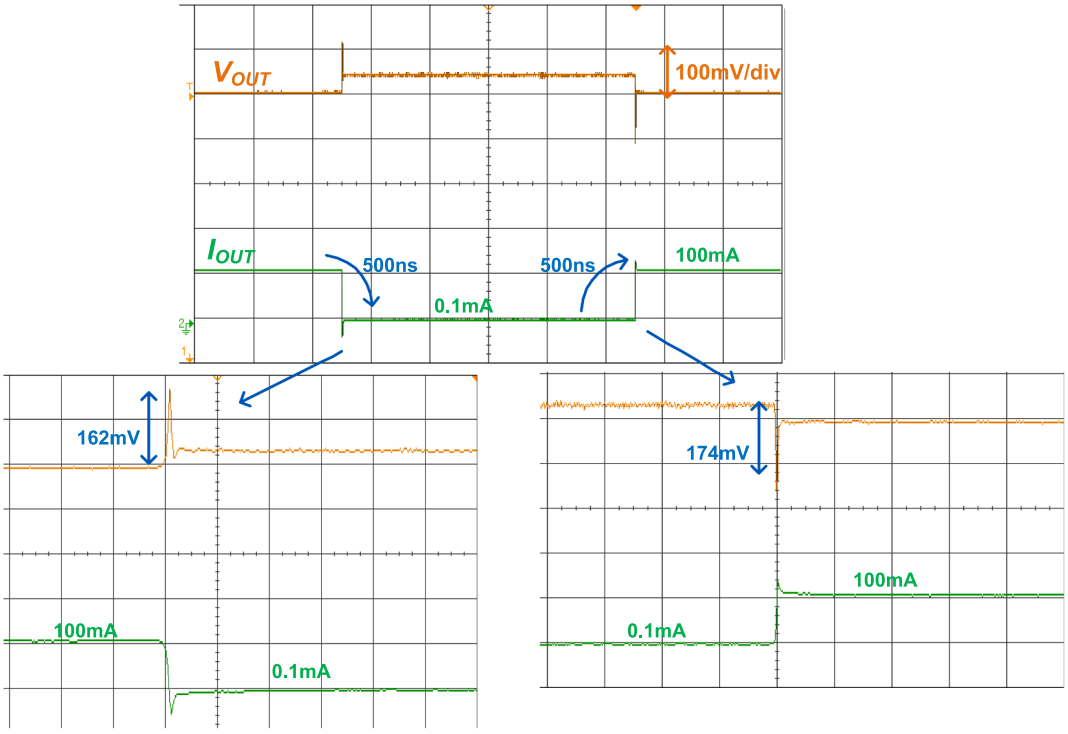

Fig. 18. Measured transient response of the proposed AB-LDO for a 500 ns step varying from 100μA to 100 mA.

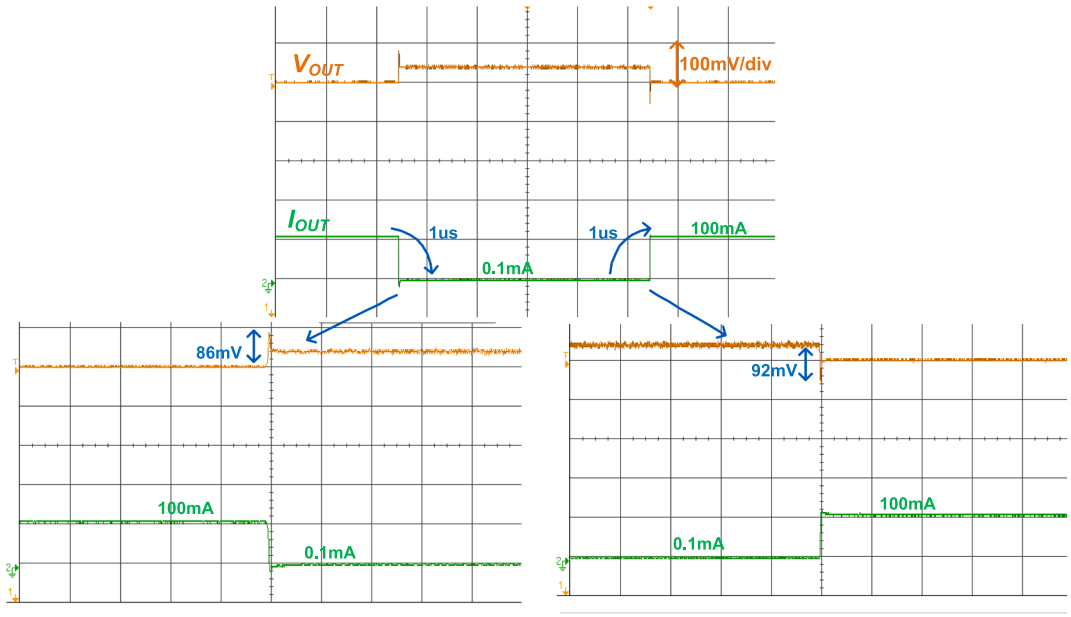

Fig. 19. Measured transient response of the proposed AB-LDO for a 1μ s step varying from 100μA to 100 mA.

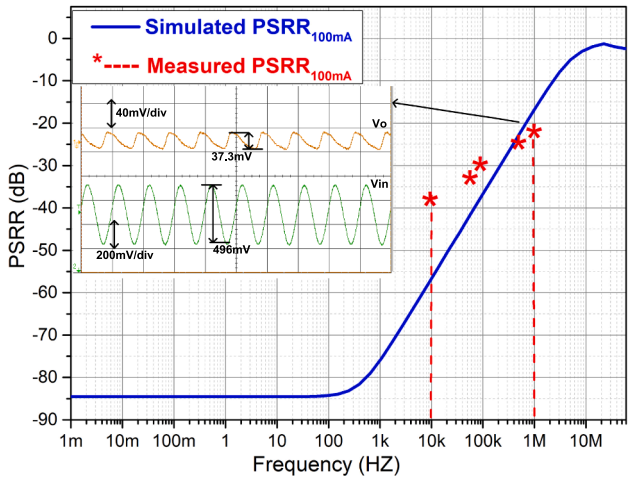

Fig. 20. Measured and Simulated PSRR versus frequency under the load current of 100 mA of the proposed AB-LDO.

4.04 ps in this paper has been obtained, verifying that the proposed AB-LDO can indeed achieve excellent performance.

5. Conclusion

This paper gives a comprehensive analysis about trade-offs among different parameters of the conventional AB-LDO using FC amplifier, and proposes a new structure of AB-LDO employing RFC amplifier and cascode compensation to optimize these trade-offs. With this special structure, the proposed AB-LDO finally achieves faster dynamic response, better linear and load regulation without increasing power consumption. In addition, the proposed AB-LDO is implemented in 0.18μ m CMOS process and the experimental results further prove that a wide load current range(0.1–100 mA), high current efficiency of 99.95%, good regulation and an optimal FoM have been achieved by the proposed AB-LDO.

Declaration of Competing Interest

The authors declare that they have no known competing financial

Table 1
Performance Comparison with Previous Reported Capacitor-less Low Dropout Regulator.

Parameter	[12]	[17]	[18]	[19]	[20]	[21]	[22]	[23]	This work
Year	2012	2014	2016	2016	2018	2019	2019	2020	2021
Technology	0.35μ m	0.065μ m	0.18μ m	0.18μ m	0.18μ m	0.065μ m	0.065μ m	0.065μ m	0.18μ m
Chip Area(mm^2)	0.0987	0.0133	0.037	0.07	0.02	0.055	0.01	0.01	0.104
Dropout Voltage(mV)	200	200	200	200	200	200	200	150	200
Output Capacitance C_L(pF)	100	470	100	100	50	100	2000	100	100
Quiescent Current I_q(μA)	28–380.1	15.9–487	0.8–154	0.61–141	3.2–208	0.407–245	50–190	65	10–50.25
Maximum Load Current(mA)	100	50	100	100	25	100	50	20	100
Load Regulation(mV/mA)	0.078	0.18	10	0.6	0.124	0.077	0.04	–	0.48
Line Regulation(mV/V)	0.39	4	0.1	0.27	0.308	0.283	1	–	0.75
PSRR(dB)	<-13.15	−51	−28	−26	−56	−37.7	–	−23	−22.5
@(Hz)	@1M	@1K	@1M	1 M	@1M	@1M	–	@1M	@1M
undershoot(mV)	105	113	45	110	59	117	83	88	92/174
overshoot(mV)	50	29	52	85	40	35.33	52	35	86/162
Current Efficiency(%)	99.62	99.04	99.84	99.85	99.92	99.75	99.90	99.70	99.95
Edge Time(μs)	1	0.1	1	1	0.1	0.3	0.002	0.005	1/0.5
K_2	1.94	0.36	1	1	1	0.36	0.36	0.36	1
FoM(ps)	13.1	160.1	7.55	9.87	18.8	23.02	9.11	15.75	4.04/3.92

interests or personal relationships that could have appeared to influence the work reported in this paper.

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