Review, Survey, and Benchmark of Recent Digital LDO Voltage Regulators

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Abstract: This paper presents a review of the recent digital low-dropout voltage regulators (DLDOs). We have reviewed them in five aspects: control laws, triggering methods, power-FET circuit design, digital-analog hybridization, and single vs. distributed architectures. We then have surveyed and benchmarked more than 50 DLDOs published in the last decade. In addition, we have offered a new figure-of-merit (FoM) to address the shortcomings of the previously proposed FoMs. The benchmark provides insights on which techniques contribute to better dynamic load regulation performance. The survey and benchmark results are uploaded to a public repository.

Introduction: Low-dropout voltage regulators (LDOs) are key building blocks in the system-on-chips (SoCs). An LDO requires no bulky components such as inductors, and therefore multiple of them can be integrated on a chip (Fig. 1). Furthermore, since an LDO can create an independent voltage domain, each core/block of an SoC can operate at the optimal voltage, maximizing performance and energy efficiency.

Recently, the digital version of an LDO (DLDO) has gained much research and development (R&D) interest for input voltage scalability, technology portability, and other benefits associated with digital-oriented design. This interest has driven researchers to propose a large number of new DLDO architectures and circuits.

This paper aims to introduce those DLDOs and review them based on the architecture and circuit-level features. Through this, we hope to provide insights on which architectures and circuits enable the improvement in the DLDO's key performance metric, dynamic load regulation performance.

The rest of the paper is organized as follows. First, we will introduce the typical architecture of DLDOs. Then, we will review the recent DLDOs in terms of the chosen control laws, triggering/clocking methods, DAC/power-FET circuits, digital and analog hybridization, and single vs. distributed architectures. Finally, we will survey and benchmark the recent DLDOs using a new FoM to evaluate dynamic load regulation performance.

Typical DLDO Architecture: Fig. 1 shows the typical architecture of a DLDO [1]. It consists of an analog-to-digital converter (ADC), a digital controller, a power-FET array that works as a digital-to-analog converter (DAC), and an output capacitor (C_{out}). A typical DLDO employs a binary clocked (synchronous) voltage comparator, such as a strongARM, for the ADC. It also uses a simple integral control (I-control) law. The DAC/power-FET array produces current proportionally to its digital input. The PMOSs of the power-FET array are sized uniformly or in a power-of-2 manner.

The operation of a DLDO is as follows. The ADC quantizes the error between a reference voltage (V_{ref}) and output voltage (V_{out}) at the rising edge of the sampling clock (clk_s), where clk_s operates at a target sampling frequency (f_s). The digital controller maps the error value to digital output (V_g) based on a control law. This digital output selectively turns on/off the PMOSs in the power-FET array to modulate the power-FET current (I_{pwr}). In the steady-state, V_{out} approaches V_{ref}, and I_{pwr} is matched with load current (I_{load}). If I_{load} changes rapidly, the digital feedback loop may not respond immediately, and V_{out} may deviate from V_{ref}. To quickly recover from such a deviation, a DLDO employs a sufficient amount of output capacitance (C_{out}) at the output node, which can instantly supply the needed current to the load during fast load transients.

Fig. 1 also notes several essential parameters. The current that the smallest PMOS in the power-FET array can supply is called unit power-FET current (I_u). The bit count of the power-FET array (or DAC) is called N_{pwr}. The load current (I_{load}) ranges from the maximum load current ($I_{load,max}$) to the minimum load current ($I_{load,min}$). R_{load} denotes a load-equivalent resistor. The supply voltage of a DLDO (V_{DD}) is also called input voltage (V_{in}). The dropout voltage ($V_{dropout}$) is defined as the difference between V_{in} and V_{out} in the steady-state.

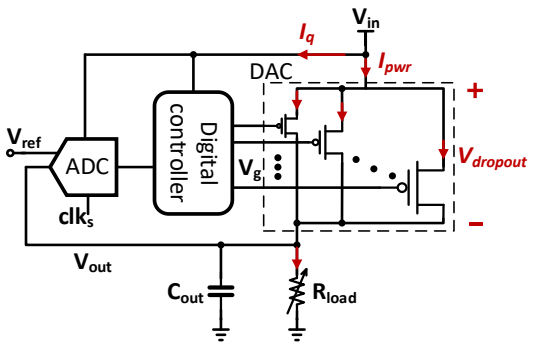

Fig. 1. A typical DLDO architecture

Finally, quiescent current (I_q) is the current that flows to the ADC and the controller in the steady-state.

Control Law: To implement feedback control, DLDOs adopted a range of control laws from (i) integral feedback, (ii) deadzone control, (iii) linear proportional, integral, derivative (PID) feedback control, (iv) feedforward control, and (v) non-linear control.

I-Control: The most typically-used control law in DLDOs is the integral control (I-control) [1,2]. In this control, the controller's output is defined to:

$$V_g[k] = V_g[k-1] + K_I \cdot err[k], \quad (1)$$

where $V_g[k]$ is the controller's digital output at the k-th time step, err[k] is the digitized error value, and K_I is the integral gain coefficient. If a DLDO adopts a binary voltage comparator for the ADC, err[k] is either +1 or -1. Typically, K_I is set equal to 1 to use the resolution of the DAC/power-FET array fully.

Fig. 2 shows the waveform of the I-control in a DLDO, where the sudden increase of I_{load} causes V_{out} to droop. The ADC (a binary comparator in this example) samples this V_{out} droop, and the digital controller updates the output. Assuming K_I is equal to 1 and the PMOSs in the power-FET array are sized in a power-of-2 manner, the controller will increase its output by 1 to turn on more power-FETs, thereby supplying more I_{pwr}. But, the I_{pwr} is still smaller than I_{load}, and as a result, V_{out} is still less than V_{ref}. Therefore, the controller keeps increasing its output by 1 for several more cycles. Eventually, this makes V_{out} close to V_{ref}.

In the worst case where I_{load} changes from the minimum ($I_{load,min}$) to the maximum value ($I_{load,max}$), it takes approximately 2^N cycles to settle V_{out} close to V_{ref}, where N is the bitwidth of the controller output. This sets the worst case of settling time (t_{settle}) to $2^N \cdot 1/f_s$.

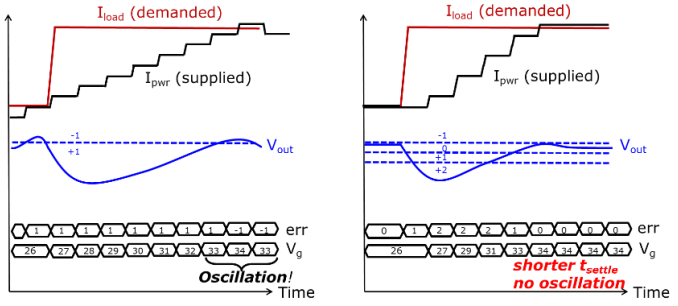

Fig. 2. Operational waveforms of a DLDO with (a) an I-controller with a binary error input; (b) an I-controller with multi-bit error input, and the deadzone control

Deadzone: In the above example, we assume a binary ADC, which makes the controller keeps updating the output every cycle even the DLDO reaches the steady-state. This unnecessary output update causes the output voltage (V_{out}) to have a ripple. To eliminate the output voltage ripple, recent works have adopted the deadzone control [3]. This control sets a deadzone around V_{ref}. For example, as shown in Fig. 3, the deadzone is set between V_{ref2} and V_{ref1}. If the ADC finds the V_{out} is in the deadzone, it produces 0 such that the

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digital controller does not change the output. To implement the deadzone, indeed, the ADC should have more than 1-bit resolution.

The deadzone control can remove the output voltage ripple. As shown in Fig. 2(b), as the controller output stays with the same value, V_{out} has no ripples. It is also noteworthy that the multi-bit ADC now can distinguish the voltage droop size in two levels (i.e., err[k] is +1 or +2). This can allow the controller to change the output by a larger amount in case it sees a larger voltage droop, improving the settling time (t_{settle}) of a DLDO.

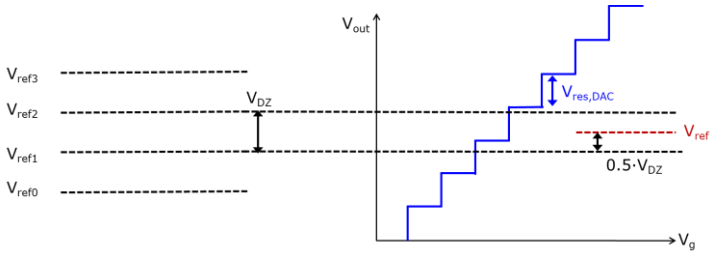

Fig. 3. Deadzone set between V_{ref2} and V_{ref1}. If V_{out} is in the deadzone, the ADC produces 0, which stops the controller from updating its output and thereby eliminating the output ripple.

The size of the deadzone, i.e., $V_{DZ}=V_{ref2}-V_{ref1}$, needs to be set carefully. On the one hand, we should put V_{DZ} coarser than the DAC/power FET's voltage resolution ($V_{res,DAC}$). Otherwise, V_{out} may not be able to settle in the deadzone and V_{out} can have the ripple whose size is larger than V_{DZ}. On the other hand, V_{DZ} poses the worst-case error of V_{out} since if V_{out} is in the deadzone, the controller considers it reaches the steady-state and does not make further correction/regulation.

Linear Control: The proportional, integral, and derivative (PID) control is the most popular feedback control scheme. It is also called linear control since it updates the controller's output in a linear fashion. The simplest linear control scheme is the I-control mentioned above, where we use only the integral portion of the PID control. The I-control is essential to ensure a minimal steady-state error. We can also make PI control by adding the proportional part, which improves the transient response and improves dynamic load regulation performance such as t_{settle} [4]. On the other hand, we can add the derivative portion and make ID or PID control, where the D-control helps to reduce the sharp spikes in the V_{out} of a DLDO [5].

Feedforward: Recent DLDOs have adopted feedforward control (also known as initialization) and feedback control to further improve dynamic load regulation performance. Upon observing a significant voltage droop, the feedforward control immediately supplies an estimated amount of charge to recover V_{out} from the voltage droop. Differently from the feedback control, the feedforward control performs such charge supplying only once per droop event. The lack of the feedback loop makes the feedforward control little suffer from any stability issues.

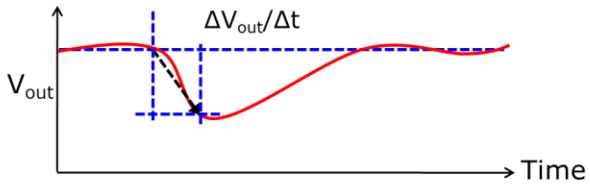

Fig. 4. The feedforward control measures the slope of V_{out} at the beginning of a droop event and then estimates the needed amount of charge, for example, using a pre-characterized LUT.

To supply the right amount of charge, the feedforward control often measures the slope of V_{out} at the beginning of a droop event (Fig. 4) since the slope (dV_{out}/dt) is proportional to the current flowing from the output capacitor (I_{cap}). Multiple techniques are available to measure the slope. One method is to use a multi-bit clocked ADC [6]; the other way is the continuous-time ADC along with a time-to-digital converter [7, 8]. Once we measure the slope, we can estimate the needed amount of charge based on a pre-characterized look-up table (LUT).

Non-Linear Control: Recent DLDOs also adopted non-linear control and non-linear search schemes to improve the dynamic load regulation performance. It is called non-linear since the output of the controller changes in a non-linear fashion. Non-linear schemes aim to speed up the controller to find an optimal output faster than the linear control. For example, if the controller performs the binary search, it can achieve t_{settle} of N cycles where N is the bitwidth of the controller's output [9]. In the search process, however, the controller updates its output in a non-linear fashion, producing spikes in V_{out}. To mitigate it, recent works additionally employed D-control [9]. Another notable non-linear control is employing an optimization solver that solves for the settings of a DLDO that minimize a specific loss function. This approach helps a DLDO to find a more optimal setting. However, it often causes longer computational latency [10].

Multi-Loop: Recent DLDOs also employed more than one feedback control loop [8, 11–15]. For example, a dual-loop DLDO uses one type of feedback loop if the output error is large and the other if small. By doing so, the DLDO can future improve dynamic load regulation performance while reducing power and area overhead [15].

Triggering/Clocking Method: Recent DLDOs proposed a range of triggering/clocking methods for sampling the controller's input and updating the output to improve transient performance and minimize power consumption.

Synchronous (Time-Driven) Triggering: The synchronous, a.k.a. time-driven, triggering is the most common technique adopted in a DLDO [1, 9, 16]. It uses a clock with a fixed frequency. Synchronously with the clock, the ADC samples the output voltage, and the digital controller updates its output. The synchronous triggering enables the area- and power-efficient hardware implementation. It also simplifies verification, such as stability analysis. However, the synchronous triggering often incurs long feedback latency. For example, as shown in Fig. 5(a), if a droop event occurs right after the rising edge of the clock, the synchronous clocking requires two cycles, one for input sampling and the other for updating the controller's output, to respond and take regulatory action. We can reduce the latency using a high-frequency clock. However, it indeed increases power overhead.

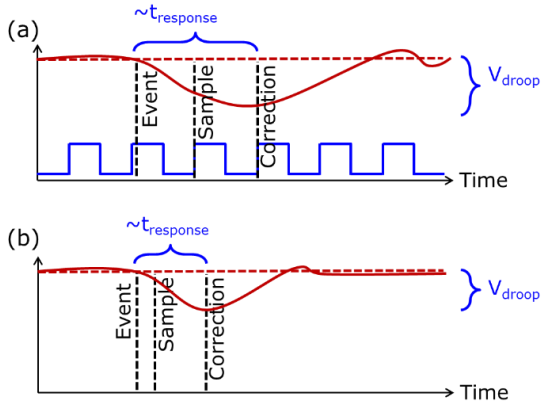

Fig. 5. (a) Synchronous clocking has two-clock-cycle latency to update the controller's output; (b) Event-driven (asynchronous) triggering can update the controller's output immediately without waiting for the following clock edges.

Asynchronous (Event-Driven) Triggering: The asynchronous, a.k.a. event-driven, triggering does not use the clock. Instead, it employs circuits that can immediately respond to the change of input. For example, a continuous-time (CT) voltage comparator compares input voltage with the reference level and updates the output if input voltage crosses the reference level [4, 17]. Such an asynchronous operation can reduce the feedback latency, enabling better transient response performance.

However, the asynchronous triggering requires complex hardware, resulting in larger power and area consumption [17]. For example, suppose we aim to implement the asynchronous version of I-control, we need to change the control law to:

$$V_g[k] = V_g[k-1] + K_I \cdot err[k-1] \cdot (t[k] - t[k-1]), \quad (2)$$

where the last term (t[k]-t[k-1]) represents the time interval between two samples that the CT ADC makes [18]. Recall that the CT ADC makes a sample whenever input crosses a reference level. For this reason, the time interval is no longer uniform and must be accounted in the integral calculation. Fig. 6 describe such non-uniform sampling and the asynchronous Euler integration using non-uniform samples.

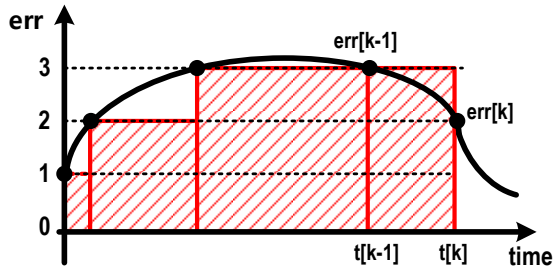

Fig. 6. Euler integration with non-uniform samples in the I-control using asynchronous triggering.

Also, the asynchronous I-control demands two pieces of additional hardware: (i) a time-to-digital converter (TDC) to measure the interval and (ii) a multiplier for the multiplication of err[k-1] and (t[k]-t[k-1]). Note that K_I is typically set to 1 (or a power-of-two number). Thus, for the K_I multiplication, we can use bit-shifting hardware *instead of* a real multiplier. However, we cannot assume neither of err[k-1] nor (t[k]-t[k-1]) to be constants (or a power-of-two number). This forces to employ a real multiplier.

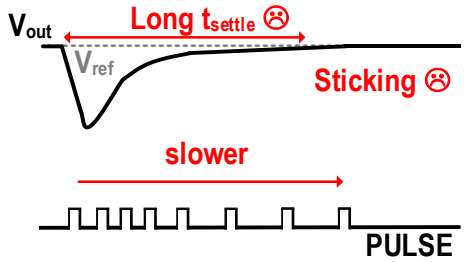

Fig. 7. The sticking problem. As the DLDO's output is getting closer to the reference level, the CT ADC makes an increasingly smaller number of samples, which increases t_{settle}.

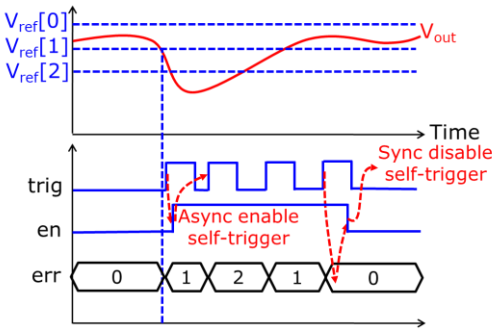

Fig. 8. Self-triggering can bypass the requirement to measure the time difference between samples while retaining most of the benefits of asynchronous triggering.

Self-Triggering: The asynchronous triggering has another notable challenge, called a sticking problem, which stems from the fact that the triggering rate is a function of the rate of DLDO's output voltage change [4, 8]. Recall that the CT ADC makes a sample whenever its input voltage crosses one of the reference levels. Therefore, as shown in Fig. 7, as the input voltage of the CT ADC, which is the output voltage of a DLDO, changes slowly near the reference voltage (for example, $V_{ref}[0]$), it makes fewer samples, and as a result, it slows down the transient response. This typically results in a longer settling time (t_{settle}).

Recent works have proposed a self-triggering technique to address the problems of asynchronous triggering. They hybridize asynchronous and synchronous triggering [8, 12]. It has a CT comparator that monitors if V_{out} crosses the first low reference level (i.e., $V_{ref}[1]$ in Fig. 8). If it does, the DLDO *asynchronously* enables a clock generator and thereby produces a periodic triggering signal. This signal is then processed by the synchronous controller of the DLDO for regulation. Once V_{out} enters the deadzone, i.e., between $V_{ref}[0]$ and $V_{ref}[1]$ in Fig. 8, the DLDO disables the clock generator to save the power consumption.

The self-triggering provides a similar level of feedback latency with the asynchronous counterpart. Still, it does not suffer from the aforementioned asynchronous-specific drawbacks, namely complex hardware requirements and sticking problems. Thanks to this benefit, it improves various metrics of dynamic load regulation such as V_{droop} and t_{settle}.

Adaptive Clocking: The synchronous triggering has also improved to reduce the feedback latency at minimal power and area overhead. One of the notable approaches is to use two or multiple clocks with different frequencies and adaptively use them. For example, as proposed in [2], if the load current is small, a slow clock is used, while if the load current is large, a fast clock is used. This adaptive clocking improves the output ripple size and t_{settle}.

Power-FET Circuits: Recent DLDOs proposed multiple methods to implement the DAC/power-FET array to improve transient response, output ripple, and power supply rejection (PSR) performance.

Digital PMOS: Using digital PMOSs is the most common design approach. The digital output of the controller directly drives the PMOSs of the power-FET array. The digital output swings from 0 to V_{in}. Therefore, the Vsg of each digital PMOS is either V_{in} or 0V.

The PMOSs in the power-FET array can be sized in a power-of-2 manner, e.g., $2^0 \cdot W_0$, $2^1 \cdot W_0$, $2^2 \cdot W_0$, … $2^{N-1} \cdot W_0$, where W_0 is the unit size of PMOS and N is the bit count of the power-FET array [4]. In addition, some works sized PMOSs uniformly to improve the linearity of the power-FET array's output current [5, 19, 20].

The PMOSs typically operate in the linear region for a small dropout voltage. The PMOSs do not need to be used in the saturation mode since they work as digital switches, and the analog small-signal parameters such as transconductance (g_m) do not impact the loop gain. However, if the load just requires a small V_{out} (i.e., large dropout voltage), the PMOS power-FETs can operate in saturation.

Digital NMOS: The digital PMOS in the power-FET array, either operating in the linear or saturation mode, has an output current that varies with V_{in}, which results in poor power supply rejection (PSR). To improve PSR, recent DLDOs proposed to use digital NMOSs in the power-FET array (Fig. 9) [21]. If the NMOS operates in the saturation region, the output current does not vary much across V_{in} variations, which improves PSR. However, to have NMOSs work in the saturation region requires a larger dropout voltage, degrading the power conversion efficiency (PCE) of the DLDO.

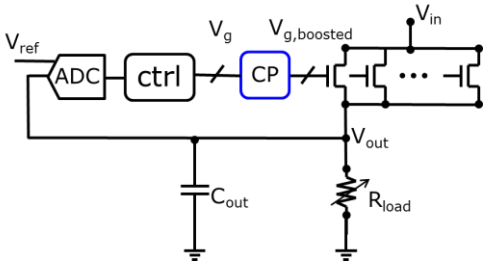

Fig. 9. The digital NMOS based power-FET array and the charge pump (CP) in a DLDO.

Also, to entirely turn on the NMOSs in the power-FET array, the gate voltage needs to be greater than ($V_{out}+V_{th}$), where V_{th} is the threshold voltage of the NMOSs. This gate voltage ($V_{out}+V_{th}$) can be larger than V_{in} ($V_{in}=V_{out}+V_{dropout}$) if the dropout voltage ($V_{dropout}$) is smaller than V_{th}. In this case, the DLDO needs a charge pump (CP) since the digital controller operates under V_{in}, and therefore it cannot produce such an output voltage swing without a CP.

AMS Power-FET: To improve PSR, recent works have proposed a new power-FET array design that is more complex than simple digital switches. For example, the current-source-based power-FET employs V_{in}-insensitive current sources that are digitally switchable through digital PMOS headers/switches (Fig. 10) [7]. The current

sources are essentially NMOSs operating in the saturation region, which makes the drain current insensitive to V_{in} change.

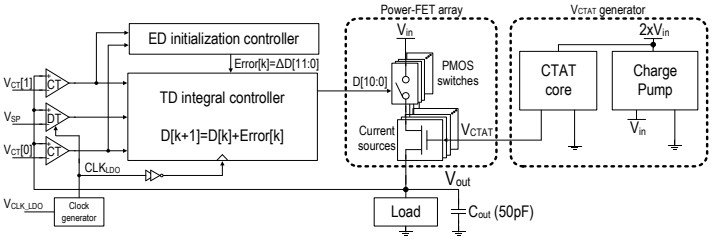

Fig. 10. A DLDO featuring the current-source-based power-FET array [7].

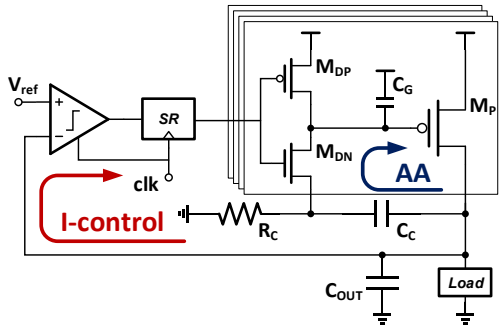

Fig. 11. A DLDO with the *nested* analog feedback in the digital feedback control.

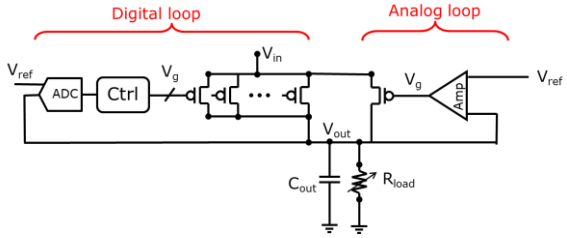

Fig. 12. A DLDO with both analog and digital feedback loops.

It is also critical to make the drain current of the current source stable across temperatures. For the temperature stability, in [7], the NMOSs are biased with CTAT (complementary to absolute temperature) voltage (V_{CTAT}) because the NMOSs are in the near-threshold region and, therefore, their drain current is PTAT (proportional to absolute temperature). On the other hand, if the NMOSs are in the super-threshold region, the drain current becomes CTAT, and the NMOSs need a PTAT voltage (V_{PTAT}).

PWM/FM: The aforementioned power-FET arrays have the inputs, which are digital numbers typically encoded with the 2's complement, the thermometer, or unsigned integer formats. However, some of the recent works employ a power-FET array whose input is the pulse-width modulated (PWM) signal. Such PWM-based power-FET array supplies the current when the input pulse is high [22–26]. Similarly, some recent works employ a switch-capacitor-based power-FET whose input is the frequency-modulated (FM) signal [27]. The input signal sets the effective resistance of the switch-capacitor-based power-FETs.

Digital Analog Hybridization: While a DLDO provides multiple benefits over an analog counterpart such as small dropout voltage, digital technology scalability, etc., a DLDO exhibits poor performance in several metrics, such as PSR, output ripple, and accuracy. To compensate these problems, recent works have proposed to hybridize digital and analog circuits in a DLDO.

Nested Control: Recent works proposed to nest analog feedback in a digital feedback loop [16, 21]. As shown in Fig. 11, this architecture still has a digital feedback control that dynamically turns on/off the part of the power-FET array. However, it also contains analog feedback (AA) that modulates the *gate voltage* of the power-FETs, as highlighted in a blue arrow in Fig. 11. Moreover, this analog feedback operates in the analog domain, enabling vastly improved dynamic load regulation performance.

Hybrid Control: Recent works also proposed to employ multiple digital and analog feedback and feedforward controls [3, 6, 7, 19, 28–35]. Usually, such DLDOs may require the coordination of those multiple feedbacks. For example, in [3, 35], the DLDOs activate the digital loop for the coarse-grained control (when V_{out} largely deviates from V_{ref}), whereas using the analog loop for the fine-grained control (when V_{out} is close to V_{ref}). This helps to reduce the output ripple size while still achieving fast droop voltage recovery.

Single and Distributed Architecture: Recent DLDO works have proposed a single (centralized) and a distributed architecture for supporting the different types of loads.

Single Architecture: The single (centralized) architecture typically refers to a DLDO whose sub-blocks such as an ADC, a power-FET array, a digital controller are closely integrated. It also refers to a DLDO, which has only one sensing point and one actuation point (Fig. 13(a)), but it could include a DLDO with multiple sensing points that monitor multiple locations (Fig. 13(b)). This architecture leads to a simple implementation.

Distributed Architecture: In a large-scale system-on-chip (SoC), each voltage domain can be spatially large and demand a large amount of current in the order of a few Amperes. However, to increase the size of a power-FET array while keeping the single DLDO architecture leads to multiple problems, mainly because of the power grid resistance (R_g).

One of the problems is the IR drop (V_{IR}) in the power grid during the steady-state. For instance, in Fig. 13(a), to supply the current to a load distant from the DLDO (defined as a far load), the power transistor current (I_{pwr}) has to flow through the power grid and thereby causing IR drop. The DLDO, however, cannot correct this IR drop because it cannot sense that drop.

Potentially, one can consider moving the sensing point to the problematic area or even implement multiple sensors (as described in Fig. 13 (b)), but it would increase the wire length between the sensing point and the DLDO's power-FET array. Also, the new sensing point in the problematic area forces the voltage of other locations suboptimal because the IR drop causes a voltage margin (V_{margin}, Fig. 13 (b)). This IR drop problem is exacerbated with a larger power grid size and a more significant current draw. The current practice in the single LDO architecture is to add a guard-band to the reference voltage of the LDO to ensure that the LDO's output voltage always stays above a critical voltage even with V_{IR}, which indeed degrades the power efficiency.

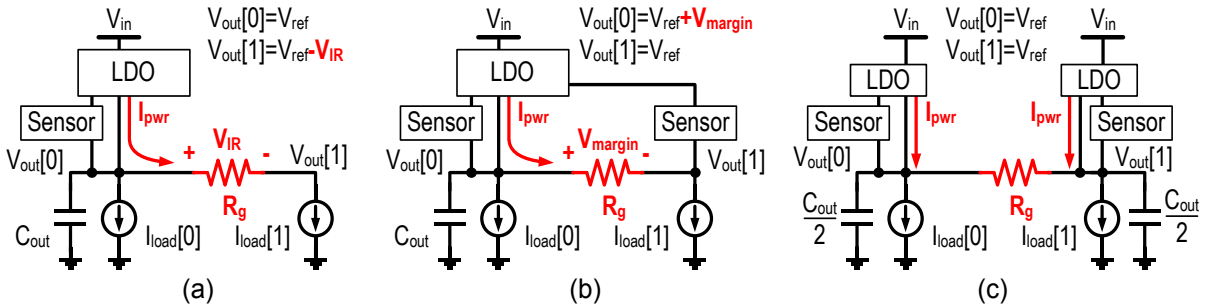

Fig. 13.(a) Illustration of (a) single DLDO, (b) single DLDO with multiple sensors, and (c) distributed DLDO architecture

The second problem of the single architecture is about the dynamic load regulation. In Fig. 13(b), let's consider the case when a far load suddenly draws a large amount of current and thereby causes a voltage droop (V_{droop}). The DLDO, which is located far away from this load event, can only sense the V_{droop} after several clock cycles because the change in V_{out} at the location of the DLDO is slower and smaller due to the parasitic R_g and C_{out}. Thus, until a DLDO senses the droop and responds, V_{droop} can be further developed. What is worse, even after the LDO detects the droop, it cannot provide enough current immediately to the far load because the grid resistance (R_g) impedes the current flow.

To mitigate these V_{IR} and V_{DROOP} problems, several works proposed the distributed architecture [5, 12, 26, 30], where multiple DLDOs are distributed spatially across the power grid. For instance, as shown in Fig. 13(c), two DLDOs can be employed, each supporting half of the total load. The two DLDOs can directly sense local voltages and supply currents more effectively address the problems mentioned above.

Survey and Benchmark: We have surveyed the recent DLDO prototypes published from 2010 to 2021 [1-52]. We recorded the detailed survey results in the spreadsheet, which can be downloaded from the GitHub repository [54].

Figure of Merits: As most of the DLDOs aim to support a digital load, the dynamic load regulation performance such as droop voltage (V_{droop}) has been considered the key metric. To capture the dynamic load regulation performance and its power and hardware cost, the IC design community has introduced several FoMs; namely, i) ps-FoM [53], ii) edge-adjusted ps-FoM [31], and pF-FoM [18].

However, the recent DLDO works have targeted the various loads with different characteristics. For example, some DLDOs target a tiny load current of the sub-μA level while others focus on a large load of more than 1A. Also, some DLDOs consider a digital load operating at the kHz to MHz clock frequency, while others aim to support a load operating at multi-GHz. For this reason, they have used different test setups, e.g., μs to sub-ns edge time (T_{edge}), and nA to 100's mA load current step (ΔI_{load}), to model different load current change dynamics.

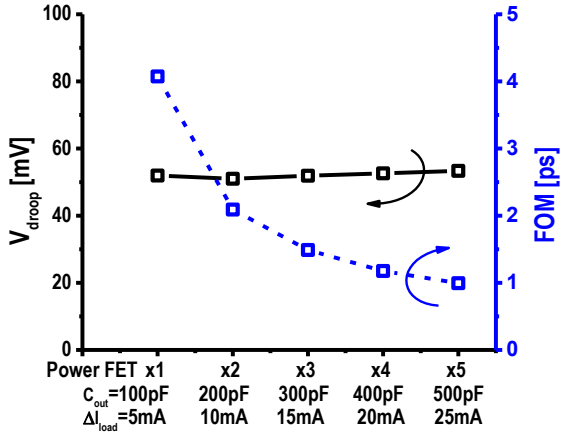

Fig. 14. If we increase ΔI_{load} and C_{out} by the same ratio, we can achieve a better ps-FoM artificially for the same hardware. Based on the simulation of the DLDO in [12].

Such diversities make it difficult for the existing FoMs to accurately capture the dynamic load regulation performance and the associated cost. For example, regarding the ps-FOM and the edge-adjusted ps-FoM, by simply changing the test setup, we can achieve an artificially better FoM. Fig. 11(a) shows such a case, where we employ increasingly larger C_{out} and ΔI_{load} for the same DLDO presented in [12]. By increasing both C_{out} and ΔI_{load} by 5X, we can improve the ps-FoM by 4.1X even for the same hardware. Similarly, regarding ps-FoM and pF-FoM, if someone tested the DLDO with a longer T_{edge}, they can achieve an artificially better FoM again for the same DLDO hardware.

To properly account for various T_{edge} and ΔI_{load} settings used in the design and measurement, we propose a new FoM for DLDO, titled pico-coulomb (pC) FoM, which can be formulated to:

$$pC\ FoM = \left(\frac{\Delta V_{out} + 0.5T_{edge} \cdot \Delta I_{load}/C_{out}}{\Delta I_{load}}\right) \cdot \left(I_q \cdot C_{out}\right) \quad (3)$$

This pC-FoM is similar to the pF-FoM except for two changes. First, since as pointed in [31], the increment of T_{edge} would artificially reduce V_{droop}, we add the edge-adjusted term on V_{droop} to compensate for the impact of T_{edge}. The edge-adjusted V_{droop} is normalized with ΔI_{load} and multiplied with the cost, i.e., I_q and C_{out}. This is the same approach adopted in the edge-adjusted ps-FoM, but as we mentioned above, the edge-adjusted ps-FoM still unnecessarily favors the DLDOs with larger C_{out} and ΔI_{load}. The proposed pC-FoM does not favor such DLDOs.

Second, we remove V_{out} in the denominator. It was unnecessary since V_{out} has little impact on the dynamic load regulation performance. Adding the V_{out} term would only favor a DLDO targeting a small V_{out}.

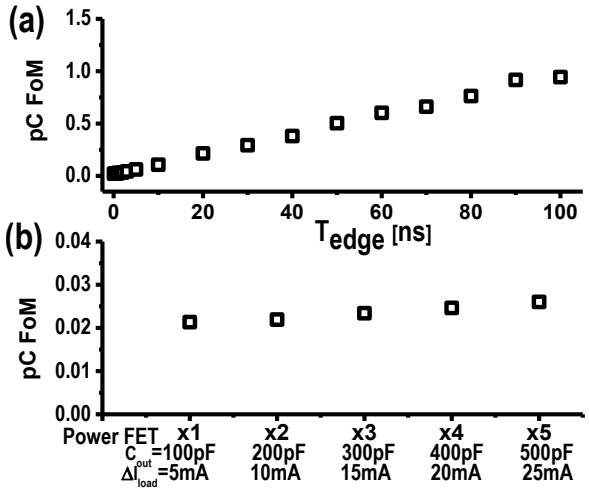

Fig. 15. (a) The pC-FoM can adequately account for different T_{edge}s. (b) pC-FoM remains accurate even if one increases ΔI_{load} and C_{out} by the same ratio. Based on the simulation of the DLDO in [12].

Fig. 15 shows the pC-FoM values from the simulations of the DLDO in [12]. The pC-FoM successfully compensates for the artificial impact of T_{edge} (Fig. 15(a)). It also maintains a similar FoM value for a given DLDO hardware even if we increase ΔI_{load} and C_{out} together (Fig. 15(b)).

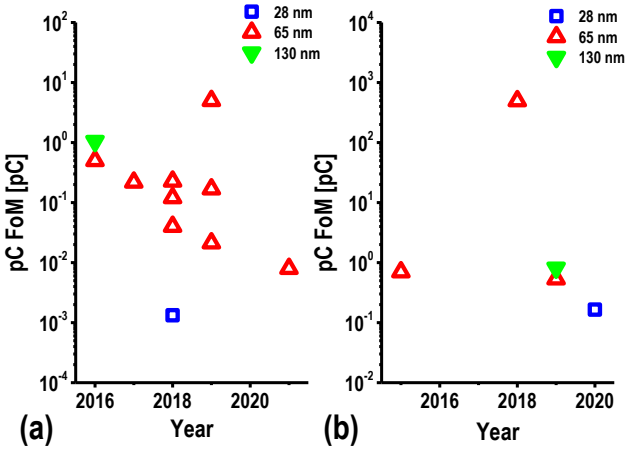

Fig. 16. DLDO benchmarks using the pC-FoM. (a) V_{in}=0.5V (b) V_{in}=1V, both across years.

Benchmark Results: Using the proposed pC-FoM, Fig. 16(a) shows the benchmark results of the recent DLDO prototypes which report the measurement results with V_{in}=0.5V. The different symbols represent the process nodes. The dynamic load regulation performance has indeed improved rapidly from 1.05 pC in 2016 to 0.008 pC in 2021 by about 131X. The 28-nm chip [21] achieves the best pC-FoM of 0.0013 pC, and the 65-nm chips [43, 11] following. [21] is: based on (i) I-control, dead-zone, multi-loop, (ii) synchronous

triggering, (iii) digital NMOS, (iv) nested loop, and (v) single architecture. [43] is based on (i) PI-control, (ii) asynchronous, (iii) digital PMOS, (iv) fully digital, and (v) single architecture. [11] is based on (i) non-linear control, I-control, and multi-loop, (ii) synchronous, asynchronous, (iii) digital PMOS, digital NMOS, (iv) fully digital, and (v) single architecture.

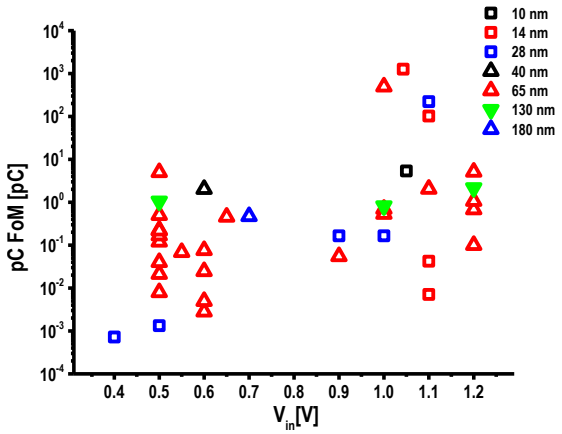

Fig. 17. DLDO benchmarks using the pC-FoM across V_{in}=0.4-1.2V

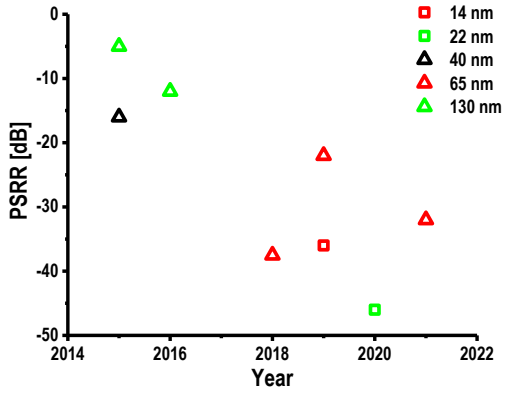

Fig. 18. DLDO benchmarks in the PSRR performance across years.

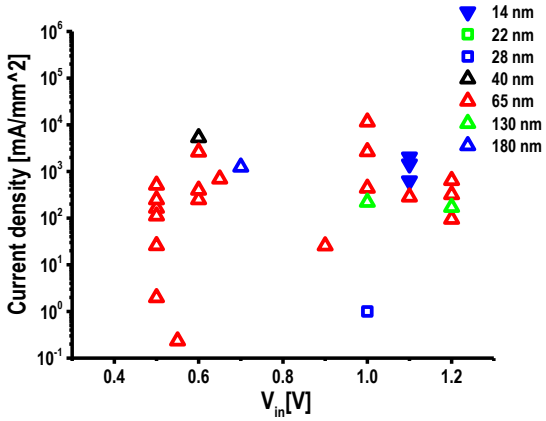

Fig. 19. DLDO benchmarks using the current density across V_{in}=0.5-1.2V.

The pC-FoM of the DLDOs with V_{in}=1V also shows a trend of improving (Fig. 16(b)). [19] in 28 nm achieved the best pC-FoM of 0.17 pC, closely followed by [12, 47] in 65 nm. [19] is: based on (i) I-control, feedforward, multi-loop, (ii) self-triggering, synchronous, asynchronous, (iii) digital PMOS, (iv) hybrid loop, and (v) single architecture. [12] is based on (i) P-control, I-control, multi-loop, (ii) self-triggering, (iii) digital PMOS, digital NMOS, (iv) fully digital, and (v) distributed architecture. [47] is based on (i) I-control, multi-loop, (ii) asynchronous, adaptive clocking, (iii) digital PMOS, (iv) fully digital, and (v) single architecture.

Some DLDOs do not report the dynamic load regulation performance at neither 0.5V nor 1V V_{in}. It is not easy to compare DLDOs with different V_{in}'s since V_{in} strongly impacts the digital feedback control latency. Therefore, we benchmark all of them using the pC-FoM at each V_{in} (Fig. 17). For V_{in}=0.6V, [45] in 65nm gets the best pC-FoM of 0.0028 pC. [45] is based on (i) I-control, dead-zone, multi-loop, (ii) asynchronous, synchronous, (iii) AMS power-FET, (iv) nested loop, and (v) single architecture. For V_{in}=1.1V, [31] in 14nm achieves the best pC-FoM of 0.0071 pC. [31] is based on (i) non-linear control, (ii) asynchronous triggering, (iii) digital PMOS, AMS power-FET, (iv) hybrid loop, and (v) single architecture. For V_{in}=1.2V, [20] in 65nm achieves the best pC-FoM of 0.1 pC. [20] is based on (i) PI control, feedforward control, (ii) self-triggering, asynchronous, (iii) digital PMOS, (iv) hybrid loop, and (v) single architecture.

Additional Benchmark: While the dynamic regulation performance is typically considered the most critical metric for DLDOs, other metrics, such as power supply rejection ratio (PSRR), maximum current density, and steady-state output accuracy, also carry significant importance. Therefore, we benchmarked the recent DLDOs in PSRR and maximum current density.

Fig. 18 shows the PSRR benchmark results across published years. In this benchmark, we surveyed the PSRR values at 1 MHz because the switching converter that supplies power to a DLDO uses that frequency range for switching. The PSRR shows a trend of improvement as more researchers find it one of the limitations of existing DLDOs and try to improve it. [33] in 22nm achieves the best PSRR of -46dB at 1 MHz. It is based on digital PMOS, AMS power FET, hybrid loop, and single architecture.

Fig. 19 shows the current density at different V_{in}s. We benchmarked those DLDOs that use no off-chip capacitor since it is difficult to estimate the equivalent silicon area of an off-chip component. [12] using distributed architecture achieves the largest current density of 11.5 A/mm^2 at V_{in}=1V in a 65nm CMOS. [12] is based on (i) P-control, I-control, multi-loop, (ii) self-triggering, (iii) digital PMOS, digital NMOS, (iv) fully digital, and (v) distributed architecture.

Conclusion: In this paper, we have reviewed, surveyed, and benchmarked the DLDOs that were recently prototyped. We have categorized them based on the techniques that each work proposed and adopted. We can categorize most of the DLDOs with the categories that we created. However, we also have found that some of the works are unique and do not fit nicely with our categories. Should more of such DLDOs be published in the future, we will need to expand the categories. Nonetheless, our current categories cover most of the works. Along with the newly-proposed, more accurate FoM, we identified the leading DLDO architectures for a range of target load specifications and, subsequently, the techniques that those leading works have proposed. The survey and benchmark results are uploaded to a public repository and continue to provide insights to any future DLDO designers.

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