Design of a Pixel Readout ASIC Using Super Pixel Circuits With a Built-In LDO Regulator for Hybrid X-Ray Imaging Detectors

Jingsi Cheng, Wu Gao, *Member, IEEE*, Chunyang Yu, and Xiaoyu Wu

***Abstract*—A pixel readout application-specific integrated circuit is a key device to construct a hybrid pixel detector for X-ray imaging applications. Voltage drop problems due to parasitic resistance in the power network of the pixel matrix introduces nonuniformity of circuit performance such as dynamic range, gain and noise characteristics among readout pixels. Thus, improving the uniformity of the measured data from each pixel readout circuit is critical for the development of such pixel readout ASIC. This brief presents a novel super pixel circuit topology with a built-in pixelated low-dropout regulator to enhance uniformity. A 16 × 16 prototype is fabricated with 180nm CMOS process. The die size of the prototype chip is 1.8 mm × 2.2 mm with a pixel pitch of 100 μm. The dynamic range of input charges is 1 fC ∼ 10 fC. The equivalent noise charge is 200 e-(rms). The power consumption per single pixel with low-dropout regulator in the photon counting mode and energy resolution mode is about 40 μW and 54 μW. The simulated maximum IR drop is only 80 μV. The tested CSA gain variance of the proposed scheme is only 0.379 mV/fC. The measured data indicate that the proposed scheme can well enhance the uniformity of the output data from each pixel readout circuit.**

***Index Terms*—Application-specific integrated circuit, built-in low-dropout regulator, super pixel circuits, uniformity, x-ray imaging detector.**

I. Introduction

HYBRID pixel detectors (HPDs) are widely applied in high-energy physics experiments, nuclear physics experiments, and photon scientific experiments [1], [2]. A domain-specific HPD is required for a next-generation high-performance X-ray imaging system. It requires measuring both the number and energy of the injected photon with an energy range of 1 keV to 140 keV, simultaneously. The term "hybrid" stems from the fact that the two key components containing a semiconductor sensor and a readout application-specific integrated circuit (ASIC) are connected by the flip-chip bonding techniques [2], [3] as shown in Fig. 1(a) and Fig. 1(b). Often, semiconductor materials like Si, CdTe, CdZnTe, etc. are suitable for the pixilated sensor. Notably, this kind of hybridization has many advantages since with the pitch-adapter the geometry of ASIC is virtually independent of the geometry of detector without strict constraints.

The pixel readout circuit consists of a two-dimensional (2D) pixel array and a peripheral digital readout control circuit. However, this 2D organization results in challenges for nonuniformity due to voltage drop problems of the power supply in each pixel-level analog readout circuit. Furthermore, as the array size increases, voltage drop induced uniformity deteriorates. Generally, ASICs designed for photon-counting (PC) X-ray imaging typically utilize much larger pixel array and much smaller pixel sizes than conventional. For example, Timepix4 chip consists of 448 × 512 pixels [4].

In general, there are two traditional voltage mode power supply schemes including global power supply [5] and column power supply [1]. It is obvious that the farthest pixel in the matrix suffers from a voltage drop problem induced by the parasitic resistance of the metal layers. The voltage drop can be expressed as:

$$\Delta V_{ij} = \left\{ \frac{m\times\left[n+(n-j+1)\right]\times j}{2} R_1 + \frac{[m+(m-i+1)]\times i}{2} R_2 \right\} \times I_0 \tag{1}$$

$$\Delta V_{i,*} = \left\{ m\times R_1 + \frac{[m+(m-i+1)]\times i}{2} R_2 \right\} \times I_0 \tag{2}$$

where i and j is the row and column coordinates of pixels, respectively; the R_1 and R_2 is the parasitic resistance of the metal layers; the I_0 is the current of one pixel. At the same time, random noise in Fig. 1(c) and fixed-pattern noise (FPN) in Fig. 1(d) are exist. To address this issue, RD53A chip adopts the serial powering scheme to alleviate the IR drop of the metal layers [6]. The modules are placed in series and fed by a constant current source realized by shunt-LDO regulator. However, this scheme has high power consumption and FPN. Moreover, HYLITE0.2 [7] adopts a architecture of distributed in-array low-dropout regulators (LDOs). A distributed LDO generate supply voltages to the analog circuits of 16 pixels.

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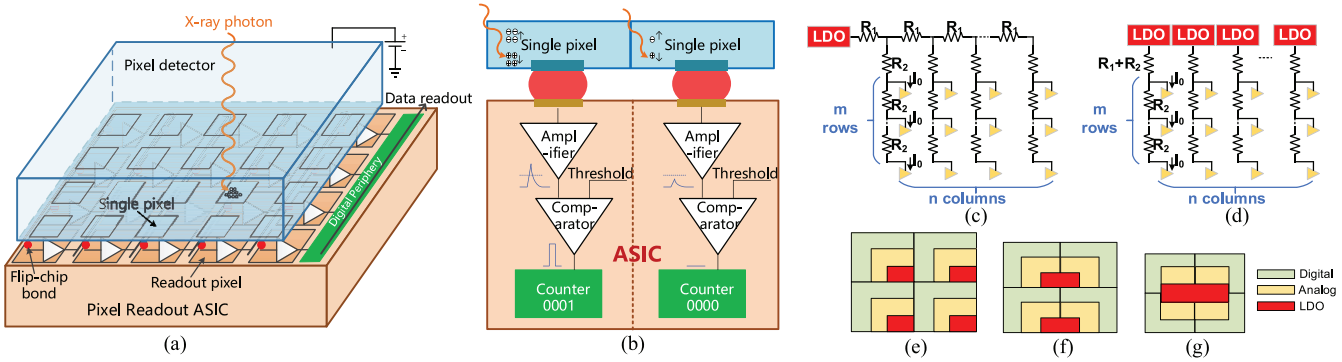

Fig. 1. (a) System diagram of the HPDs. Pixel readout ASIC and pixel detector are vertically integrated point-to-point through flip-chip bonding. (b) The basic readout signal chain in an ASIC channel. (c) Traditional global power supply scheme and the parasitic resistance models of the metal layers. (d) Traditional column power supply scheme and the parasitic resistance models of the metal layers. There are three possible power supply schemes with pixel-level LDO, including 1 LDO in 1 Pixel (e), 1 LDO in 2 Pixels (f) and 1 LDO in 4 Pixels (g).

TABLE I
EVALUATION OF POWER SUPPLY SCHEMES FOR PIXEL READOUT ASIC

Schemes	LDO size in 4 Pixels (μm^2)	1 Pixel size (μm^2)	LDO power in 4 Pixels (μW)
1 LDO in 1 Pixel	5088	120×120	105
1 LDO in 2 Pixels	2928	110×110	60
1 LDO in 4 Pixels	1848	100×100	25

In this case, it is difficult to ensure uniformity among various parts of LDO and form "analog island" in "digital sea". Above all, there is no solution for meeting the requirements of area, noise and uniformity. In this brief, a novel pixel circuit structure is presented focus on the power supply uniformity of pixel-level analog circuits.

The rest of this brief is organized as follows. Section II gives the requirements of the ASIC. Section III provides the architecture details of readout ASIC with the focus on voltage drop minimization and presents the proposed super pixel structure. Section IV demonstrates the simulations and measurement results. Finally, Section V concludes this brief.

II. DESIGN REQUIREMENTS

A power supply scheme considering pixel size, power consumption and noise is important to pixel readout ASICs. LDOs are commonly used in electronic systems particularly in low-power applications. Their main function is to provide a stable supply voltage by minimizing the ripples and noises caused by imperfect power sources and/or variable load currents [8]. Due to the small area, low load capacity, and low power consumption of LDO, it is necessary to consider how to integrate LDO into digital sea simulation islands.

The possible power supply schemes with pixel-level LDO are one LDO providing power supply for different numbers of pixels. The evaluated area and power consumption are listed in TABLE I. One LDO and 4 analog front-end (AFE) cells are close together and surrounded by digital cells (see Fig. 1(g)), which meets the requirements of digital sea and analog island. Compared with Fig. 1(e) and Fig. 1(f), the pixel area, the power consumption of LDO, and noise between digital and analog and can be decreased simultaneously. A super pixel with digital sea and analog island allows to provide an optimized isolation from the digital domain, minimizing potential noise injections [6].

III. KEY TECHNIQUES OF THE PROPOSED ASIC

A. Overall Pixel Architecture

A simplified diagram of the proposed ASIC is shown in Fig. 2(a). A matrix of 16 × 16 square-shaped pixels (8 × 8 super pixels) with 100 μm pitch and peripheral digital readout circuits are integrated. Each pixel can measure the number and energy of photons in a range from 1 fC to 10 fC independently. The count rate is $\sim 10^6$ photons/mm^2/sec. The periphery blocks contain an address generator (AG), row decoder, column decoder, end of columns (EOCs), I^{2}C and shift register. Counters in each pixel are connected to EOCs at the bottom of ASIC. The data of counters are read out under the control of AG and Shutter signal.

B. Single Pixel Element

The diagram of pixel element is illustrated in Fig. 2(e), a charge-sensitive amplifier (CSA), a pulse shaper (SHPR), a discriminator (DIS) with a threshold voltage signal, a voltage-controlled oscillator (VCO), a 4-bit counter (CNT_PC) for photon counting (PC) and an 8-bit counter (CNT_TOT) for time-over-threshold (TOT) are integrated. The ASIC is mainly working in TOT mode. The 4-bit in PC is mainly used to evaluate the count rate. The input of CSA has two sources, including detector current and test pulse voltage controlled by Test_bit. The input of DIS has two choices that are the CSA output or SHPR output. The simulated charge gains for CSA and SHPR are 28.36 mV/fC and 72.78 mV/fC, respectively. The output of DIS is applied to VCO or the clock of counter. The readout of a hybrid pixel detector can operate in the PC mode for imaging and TOT mode for energy measurement. When Shutter is high, the value of counter is increased with the number of pulses from the discriminator output.

C. CSA With Krummenacher Feedback Structure

The CSA feedback loop contains a capacitor (20 fF) and the Krummenacher structure that can discharge the feedback

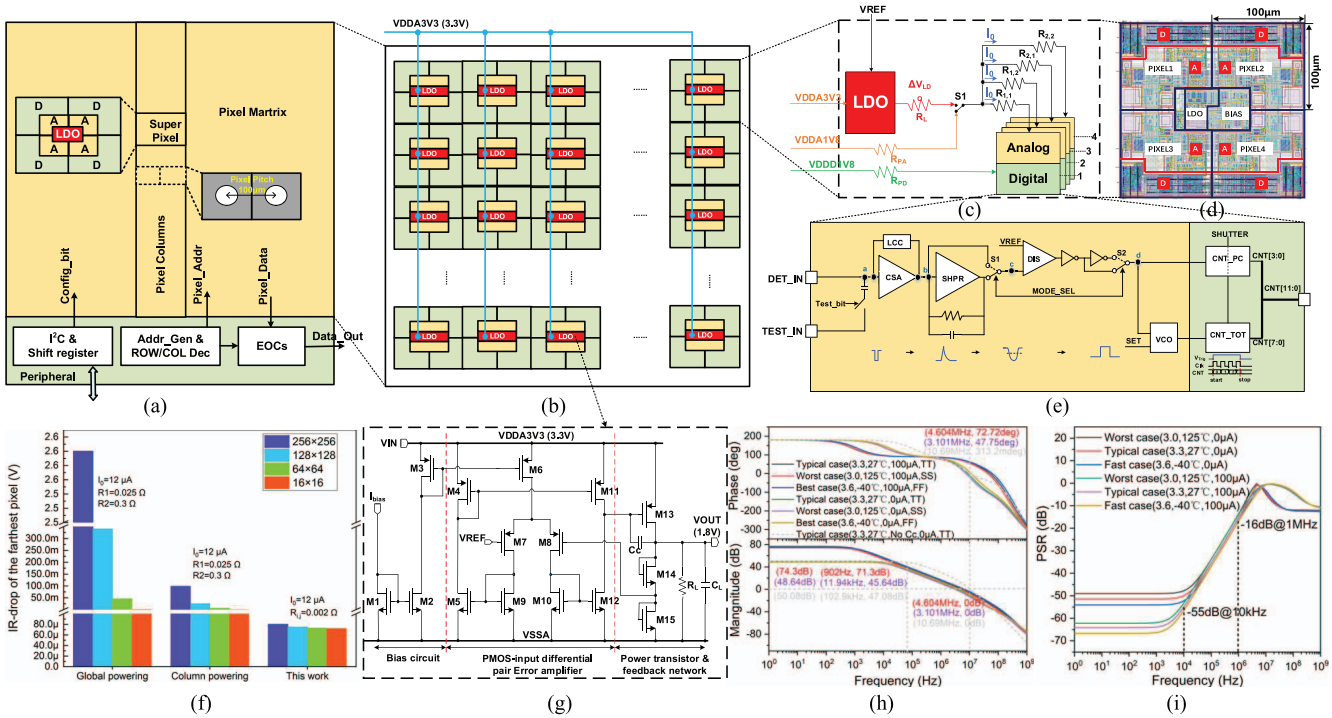

Fig. 2. (a) The overview of the proposed ASIC. (b) The layout of the proposed pixel matrix. (c) The diagram of the proposed super pixel element with built-in LDO. (d) The layout of super pixel with built-in LDO and bias. (A: Analog, D: Digital) (e) Block diagram of single pixel element. (f) Simulated results of the IR drop of the farthest pixel with different array sizes. The parameters in Fig. 1(c), Fig. 1(d) and (c) are indicated. (g) The simplified schematic of pixel-level built-in LDO. (h) Simulated results of loop stability in the pixel-level built-in LDO with full load, zero load and without frequency compensation. (i) Simulated closed-loop PSR the LDO regulator with full load and zero load.

capacitor and implement detector leakage current compensation (LCC) [9]. The feedback resistance value is set by the Krummenacher current and for the nominal setting of the 40 nA, the effective resistance is 4.6 MΩ. The designed CSA core is based on an inverter with a common-gate preamplifier topology [10]. The AFE energy efficiency can be improved by inverter-based amplifier design and inverter stacking to reduce overall energy consumption of sensor [11].

The peak time of CSA output is 58.24 ns when the time width of input photon is 49 μs and detector capacitance is $\sim$ 200 fF.

D. Power Supply Strategies

The proposed super pixel circuit is organized by 2 × 2 pixels with a pixel level built-in LDO regulator. The simplified schematic with the parasitic resistors is shown in Fig. 2(c). To avoid the noise between analog and digital circuits, the power supply is separated. In addition, to compare the measured data of traditional mode and proposed mode, the switch S1 is used to select one of two modes. Considering the mismatch between various components during the integrated circuit manufacturing process, the voltage drops of each pixel unit is

$$\Delta V_{ij} = \Delta V_{LDO} + I_0 \times R_{ij} + V_{OS} \tag{3}$$

where:

$$\Delta V_{LDO} = 4I_0 \times R_L \tag{4}$$

and: R_L is the internal resistor of the power line from the LDO output pin to the pixel; R_{ij} is the internal resistance of the power supply line in the pixel; I_0 is the current inside the pixel; V_{OS} represents offset voltage induced by device mismatch. ΔV_{ij} is very small because the R_L and R_{ij} can be ignored.

The layout of a super pixel with built-in LDO and bias is shown in Fig. 2(d). Fig. 2(b) plots the layout of super pixel matrix. The LDO and bias circuits are placed at the center of 2×2 pixel matrix. This is because the hybrid pixel detectors are mixed signal circuits with analog islands in digital Sea. Meanwhile, the power supply, manufacturing and isolation are considered. The reference voltage of LDOs is provided by the off-chip global voltage.

The comparison of simulated maximum voltage drop in the matrix is shown in Fig. 2(f). The maximum simulated IR drop of the proposed architecture is only ~80 μV, which is greatly reduced compared with traditional power supply schemes.

E. Pixel Level Built-In LDO Circuit

The pixel level built-in LDO is designed to provide stable supply voltage for analog blocks of four adjacent pixels. The proposed built-in LDO with a power supply range from 2.6 to 3.3 V achieves a s table 1.8 V output. The voltage drop induced by the metal layers mainly affects the power supply of the LDOs. Thus, the power supply of all pixels can be stable at 1.8V. Fig. 2(g) shows the schematic topologies of LDO containing the symmetrical CMOS operational transconductance amplifier (OTA), power transistor M13, a feedback resistor network and a capacitor for the frequency compensation of LDO. To meet the area requirement of pixel level LDO, the feedback resistor network is realized by transistors (M14 and

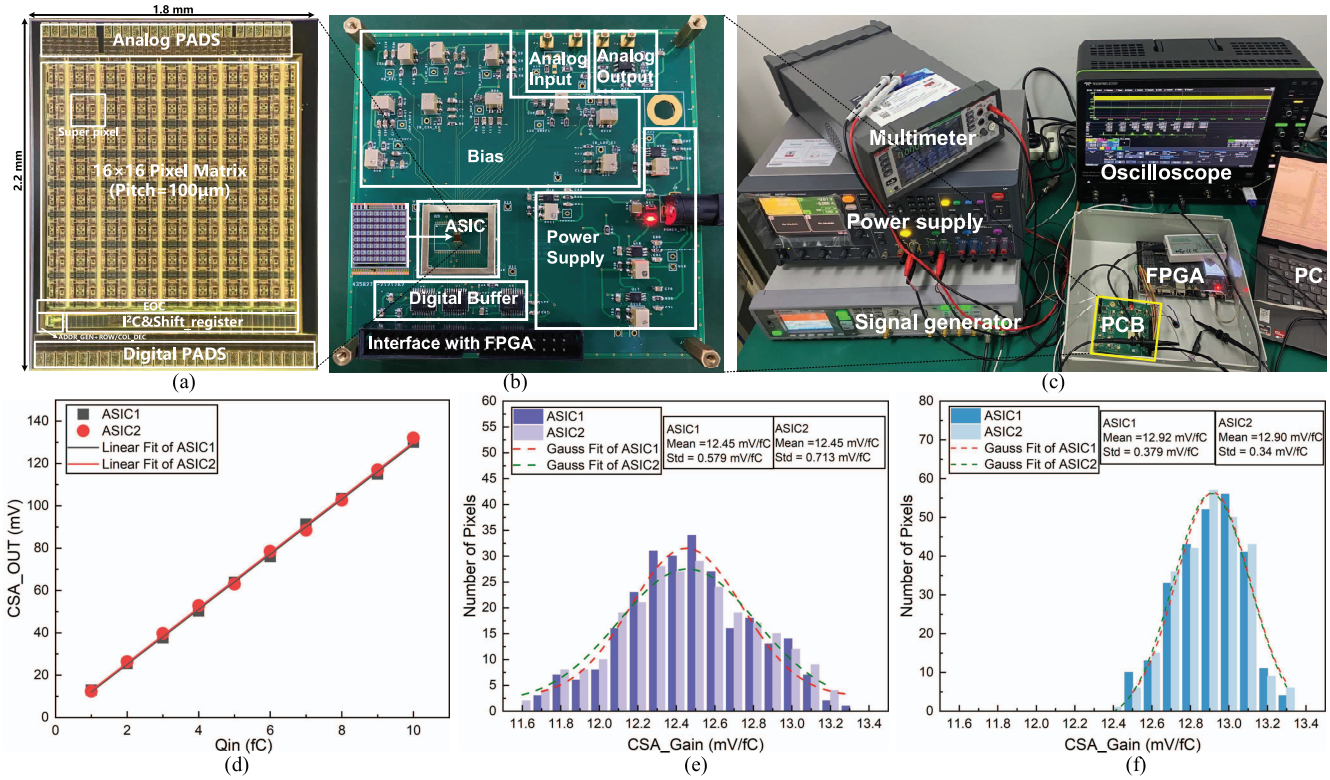

Fig. 3. (a) The microphotograph of the fabricated ASIC. (b) The photograph of the PCB for the complete test of the ASIC. The size of PCB is 100 × 100 mm^2. (c) The experimental setup. (d) Tested results of input charge range and CSA output range. (e) Histogram of measured CSA gain in pixel matrix using the traditional column powering. (f) Histogram of measured CSA gain in pixel matrix using the proposed super pixel with built-in LDO.

M15). The transfer function of LDO is

$$H(s)=\frac{R_{M15}}{R_{M14}+R_{M15}}\times\frac{g_{mE}R_ER_O\left[sC_O-g_{m,M13}\right]}{\left(1+sg_{m,M13}R_ER_OC_O\right)\left[sR_O(C_O+C_L)+1\right]} \quad (5)$$

where:

$$R_O = R_L//R_{on,M13} \quad (6)$$

$$C_O = C_c+C_{GD,M13} \quad (7)$$

and: R_L and C_L are the load resistance and load capacitance of LDO, respectively; C_c is the miller compensation capacitor. g_{mE} and R_E are the equivalent transconductance and resistor of error amplifier, respectively; $g_{m,M13}$ and $C_{GD,M13}$ are the equivalent transconductance and gate capacitance of pass transistor, respectively; $R_{on,M13}$ is the on-state resistance of pass transistor.

The simulated loop response is shown in Fig. 2(h). The dashed line represents uncompensated Bode plot. The miller compensation capacitor Cc is applied to improve the stability of supply. The RHP zero is located at high frequency, without compromising stability. Moreover, as load current increases, the loop gain as well as Phase Margin increases. This is because power transistor gradually enters into a saturation region with increasing load current, resulting in a higher loop gain. The PSR of proposed design is –55 dB and –16 dB at 10 kHz and 1 MHz in full load condition, respectively. Fig. 2(i) illustrates the PSR of the proposed LDO in different load currents.

IV. Experimental Results and Discussion

A. Prototype ASIC and Experimental Setup

The proposed ASIC is implemented in a CMOS 180 nm mixed-signal technology with single poly and 6 metal layers. The die size is 1.8 mm × 2.2 mm. The microphotograph of the fabricated ASIC is shown in Fig. 3(a). The ASIC is bonded on a dedicated Printed-Circuit Board (PCB) using the chip-on-board package, as shown in Fig. 3(b). Lab measurement setup is shown in Fig. 3(c). The testing is performed before hybridization with the pixel detector. The proposed ASIC allows the possibility to input and visualize the signals by a pattern generator and an oscilloscope. A commercial FPGA is connected with the interface of PCB to provide control functions. In this ASIC, 67-bit register files are integrated. In addition, the input charge is replaced by a test pulse generated externally. The output of CSA in each pixel is readout by the design-for-test circuit. Two ASICs have been measured and evaluated. Other ASICs are used for radiation experiment and flip-chip bonding. The power supplies are 3.3 V and 1.8 V.

B. Input Range, Gain, and Nonlinearity

During the test phase, the input charge (Qin) is determined as 1∼10 fC, which is determined by the step voltage (ΔV= 50 ∼ 500 mV) and on-chip 20 fF capacitance. There is a fact that the ASIC can bypass the shaper and only the output of CSA at the analog readout part can be observed. Therefore, the tested gain of CSA is approximately 13 mV/fC. As is seen

TABLE II
THE OVERALL PERFORMANCE COMPARISON OF THE READOUT ASICS

Parameters	RD53A [12]	Medipix2 [1]	Medipix4[13]	HYLITE0.2 [7]	This work
Process	CMOS 65 nm	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm	CMOS 180 nm
Array size	400×192	256×256	320×320	16×24	16×16
Pixel size (μm^2)	50 × 50	55 × 55	75 × 75	100 × 100	100 × 100
Operation Mode	TOT	PC	PC	Charge integration	PC/TOT
Data width/pixel	16 bits	13 bits	12 bits	10 bits	4 bits+8 bits
ENC	140e^- (rms)	140e^- (rms)	100e^- (rms)	0.35~12.6/Photons	200e^-(rms)
Power consumption	NA	8 μW/pixel	15 μW/pixel	19 μW/pixel	40/54 μW/pixel
Power supply schemes	Serial powering	Column powering	Three sides biasing	Distributed LDO	Super pixel with LDO
Worst voltage drop	NA	92 mV	13 mV	NA	80 μV

in Fig. 3(d), the nonlinearity of the CSA output is less than 1%. In addition, the measured average equivalent noise charge (ENC) is 200 e-(rms) at CSA output.

C. The Uniformity of Pixel Matrix

The uniformity of ENC is vital to X-ray imaging quality when the minimum energy detection threshold is less than 5 keV. Additionally, the ENC is mainly determined by the gain of CSA. For the traditional mode, the measured mean CSA gain and variance are 12.45 mV/fC and 0.579 mV/fC, respectively (see the histogram in Fig. 3(e)). For the proposed scheme, the measured mean CSA gain and variance are 12.92 mV/fC and 0.379 mV/fC, respectively (see the histogram in Fig. 3(f)). In this case, the variance of CSA gain is less than traditional mode, the distribution is more centralized.

D. Overall Performance Comparison

Table II lists the overall performance of the proposed readout ASIC with prior works focused on power architecture. The worst voltage drop of the proposed ASIC is minimum among the ASICs in [1], [13]. This feature shows that the proposed ASIC has the advantage of enhancing the matrix uniformity of measured data and the quality of X-ray imaging.

V. CONCLUSION

In this brief, a pixel readout ASIC using the super pixel structure with built-in pixelated LDO is designed and fabricated in CMOS 180 nm process. The super pixel is organized by embedding a pixel level LDO into a matrix of 2 × 2 pixels with analog island separated with digital sea layout scheme. The variance of CSA of proposed super pixel circuit is only 0.379 mV/fC, which means the uniformity of pixel power supply is enhanced. The measured pixel electrical noise is around 200 e^- (rms). The possible reason for high noise is the quality of the preamplifier.

For the future work, the ENC should be optimized to 100 e-(rms) for the detection threshold (5 keV) and imaging quality. A matrix of 256 × 256 pixels readout ASIC will be developed to evaluate the proposed supply architecture.

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REFERENCES

[1] X. Llopart, M. Campbell, R. Dinapoli, D. S. Segundo, and E. Pernigotti, "Medipix2: A 64-k pixel readout chip with 55-μm square elements working in single photon counting mode," *IEEE Trans. Nuclear Sci.*, vol. 49, no. 5, pp. 2279–2283, Oct. 2002.

[2] P. Grybos et al., "SPHIRD–single photon counting pixel readout ASIC with pulse pile-up compensation methods," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 9, pp. 3248–3252, Sep. 2023.

[3] R. Kleczek, P. Kmon, P. Maj, R. Szczygiel, M. Zoladz, and P. Grybos, "Single photon counting readout IC with 44 e-RMS ENC and 5.5 e-RMS offset spread with charge sensitive amplifier active feedback discharge," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 5, pp. 1882–1892, May 2023.

[4] X. Llopart et al., "Timepix4, a large area pixel detector readout chip which can be tiled on 4 sides providing sub-200 ps timestamp binning," *J. Instrum.*, vol. 17, no. 1, Jan. 2022, Art. no. C01044.

[5] A. E. Zadeh, "Higher quality images for a visible-light CMOS sensor by suppressing spatial row-wise noise with an output-capacitor-less, internal low-dropout regulator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2020, pp. 1–4.

[6] E. Monteil et al., "RD53A: A large scale prototype for HL-LHC silicon pixel detector phase 2 upgrades," in *Proc. Topical Workshop Electron. Particle Phys. (TWEPP)*, Antwerp, Belgium, 2019, pp. 1–5.

[7] M. Li et al., "A charge-integration pixel readout chip features IR-drop effect mitigation by distributed LDOs," *J. Instrum.*, vol. 17, no. 9, 2022, Art. no. P09043.

[8] K. Keikhosravy and S. Mirabbasi, "A 0.13 μm CMOS low-power capacitor-less LDO regulator using bulk-modulation technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 11, pp. 3105–3114, Nov. 2014.

[9] F. Krummenacher, "Pixel detectors with local intelligence: An IC designer point of view," *Nucl. Instrum. Methods Phys. Res. Sect. A*, vol. 305, no. 3, pp. 527–532, 1991.

[10] B. Wang et al., "Design of a low-power front-end readout ASIC based on energy-efficient amplifiers, featured 126 e-(RMS), 0.6 mW/channel for Si-PIN detectors," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, 2021, pp. 1–2.

[11] S. Sadasivuni, S. P. Bhanushali, I. Banerjee, and A. Sanyal, "In-sensor neural network for high energy efficiency analog-to-information conversion," *Sci. Rep.*, vol. 12, no. 1, 2022, Art. no. 18253.

[12] A. Dimitrievska and A. Stiller, "RD53A: A large-scale prototype chip for the phase II upgrade in the serially powered HL-LHC pixel detectors," *Nucl. Instrum. Methods Phys. Res. Sect. A*, vol. 958, Apr. 2020, Art. no. 162091.

[13] V. Sriskaran et al., "New architecture for the analog front-end of Medipix4," *Nucl. Instrum. Methods Phys. Res. Sect. A*, vol. 978, Oct. 2020, Art. no. 164412.