Transactions Briefs

Scalable All-Analog LDOs With Reduced Input Offset Variability Using Digital Synthesis Flow in 65-nm CMOS

Shourya Gupta, Shuo Li, and Benton H. Calhoun

***Abstract*— The design and verification process for analog circuits can be long and tedious, wherein designers rely heavily on manual effort to create circuits and draw layouts, thereby limiting turn-around-time and design scale and increasing costs. Various previous works have tried to solve this issue by leveraging digital automated place-and-route (APR) tools, but they involve replacing analog elements with digital counterparts, thereby dampening performance. In this work, we propose a digital flow-based approach to design all-analog circuits that dramatically speeds up the design and layout process while retaining the benefits of true analog topologies and demonstrate the performance for three low-dropout regulators (LDOs). Fabricated in 65-nm CMOS, measurement results show that the generated LDOs achieve up to 99.95% peak current efficiency, a figure-of-merit (FOM) of 4.6 ps, and up to 63.93% reduction in input offset variability with respect to their manually designed counterparts.**

***Index Terms*— Analog circuit design automation, digital synthesis, high efficiency, input offset, low power, low-dropout regulator (LDO), place-and-route, transient response.**

I. Introduction

Analog circuit designs rely heavily on manual efforts, wherein circuit designers must select and iterate on the architecture of the system, circuit topology, and device sizing. In addition, layout engineers must draw the layout and wire routing. This highly customized and manual approach of building analog circuit designs greatly limits the turn-around-time and design scale, thereby making it challenging to keep up with the pace of the ever-expanding network of the Internet of Things (IoT) devices and their heterogeneous circuit needs. While digital circuit design has well-established automated flows that have allowed scaling to billions of transistors, analog and mixed-signal design methodologies are still mostly manual. Thus, there is a desire for developing analog design automation techniques to speed up the current manual design approach. Previous works have tried to solve these issues using various algorithmic and optimization techniques. Previous works, such as BAG [1], ALIGN [2], and OpenSAR [3], use template-based procedural layout automation, optimization-based layout generation, and a combination of template-based and optimization-based layout generation, respectively. However, these tools provide limited flexibility in circuit design and do not offer the same flexibility and scalability like digital synthesized circuits. OpenSerDes [4], FASoC [5], and the work in [6] can generate various analog circuit solutions, including PLLs, low-dropout regulators (LDOs), SerDes, and temperature sensors by leveraging digital automated place-and-route (APR) tools. However, these analog blocks are redesigned to use structures composed largely of digital components, which limits performance and circuit design flexibility.

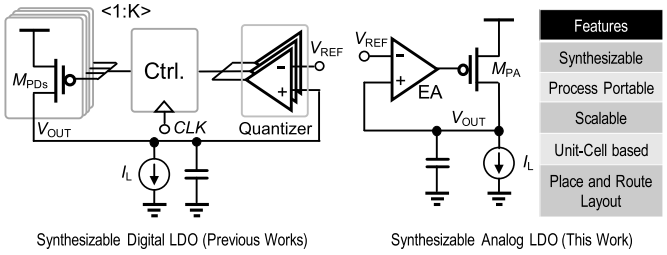

Fig. 1. This work targets solely the analog LDOs, allowing for the first time, fully synthesizable analog and hybrid LDOs.

This is also the case with the LDO (as shown in Fig. 1), whose digital circuit implementations replace analog elements with digital switches and controllers [7], [8], [9], [10], [11]. Analog LDOs still outperform digital LDOs (DLDOs) in transient response and power supply rejection ratio (PSRR), stemming from the DLDOs' discontinuous operation, especially at low frequencies. In this work, we present three all-analog LDO designs at different design points that were generated using a synthesizable unit-cell-based approach. We leverage the well-established digital synthesis-based tools to synthesize RTL descriptions of the analog LDOs that retain their analog circuits and topology, significantly cutting back on manual layout and verification efforts. Prior to this work, synthesizable LDOs had to use entirely digital topologies, but our approach to all-analog synthesizable LDOs can also pave the way to combine elements from both digital and analog designs to enable automatic generation of fully end-to-end synthesizable hybrid LDOs, thereby allowing reduced manual effort, improved scalability, and easier process portability.

The following are the contributions of this work.

1) We leverage existing template-based approach to help design and generate LDO SPICE schematics. These allow to quickly run a whole suite of technology agnostic design and verification SPICE simulations.
2) We create synthesizable RTL descriptions of analog LDOs using analog unit cells and LDO SPICE schematic.
3) We leverage existing digital tools to synthesize and auto-place-and-route the RTL netlists to generate fully analog LDOs.

The generated LDOs achieve up to 99.95% peak current efficiency, a figure-of-merit (FOM) of 4.6 ps, and up to 63.93% reduction in input offset variability with respect to their manually generated layout counterparts. This brief has been constructed as follows. Section II discusses the analog LDO schematic generation, analog unit-cell implementation, and the digital-synthesis-flow-based generation methodology. Section III discusses the measurement results, including input offset and performance comparisons between LDOs. Section IV summarizes and concludes this brief.

II. Analog-LDO Generation Methodology

Fig. 2(a) shows the flow diagram of the synthesizable methodology used to generate the LDOs. It involves the creation of aux-cells (aux-

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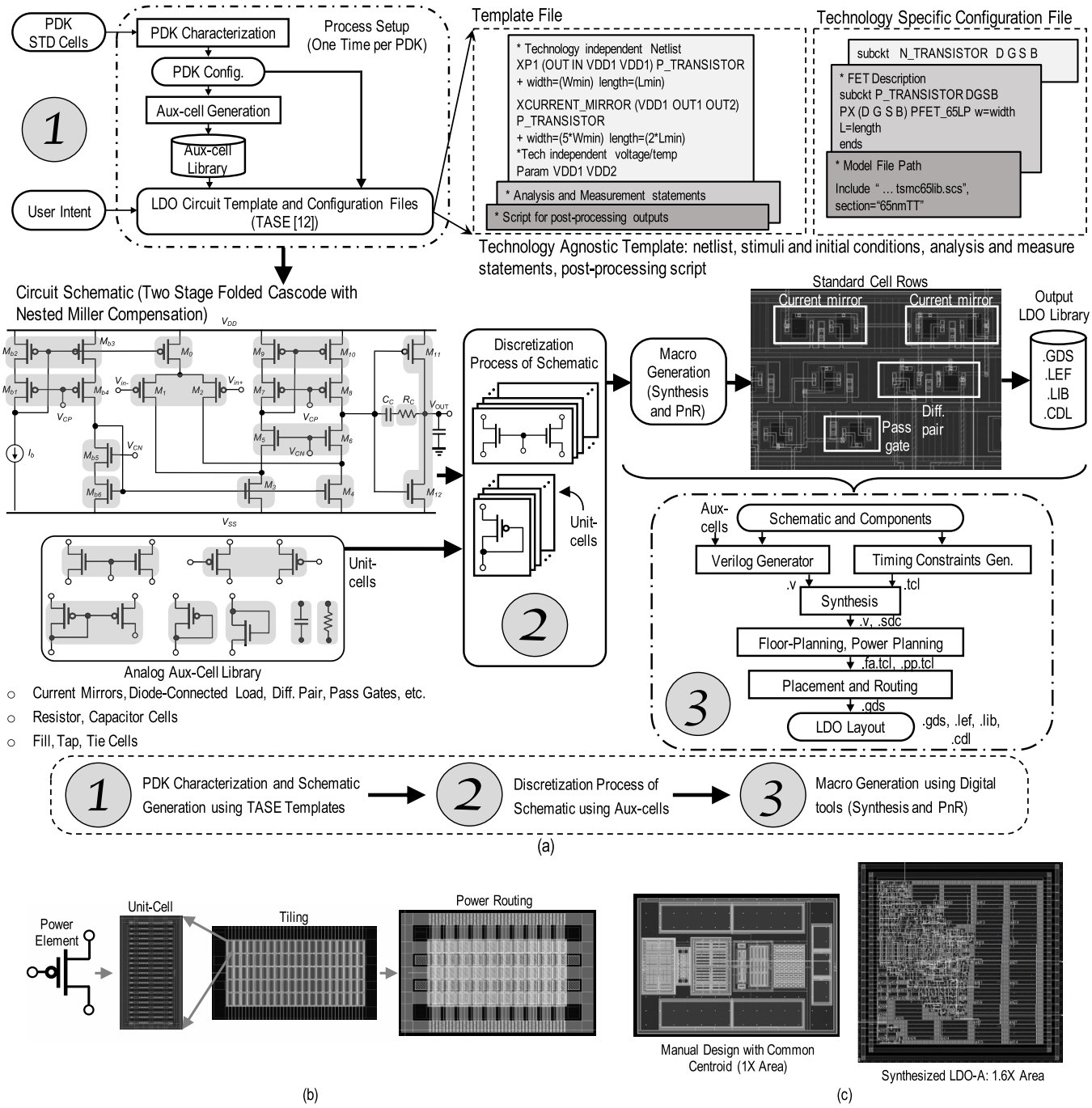


Fig. 2. (a) Digital-flow-based generation methodology for analog LDOs using synthesizable unit-cell-based approach. (b) Layout generation of power element using unit-cell-based construction. (c) Comparison between manually created common centroid layout and synthesized layout generated using unit aux-cells.

iliary unit cells), characterization scripts, and circuit design models and templates as a one-time effort per process design kit (PDK). Aux-cells in this work are small analog circuits that make up the analog aux-cell cell library and provide specific analog functionality (unlike aux-cells in prior works that are digital in function, e.g., [5]).

Examples include analog circuits, such as current mirrors, diode-connected loads, differential pairs, and so on, passives like resistors and capacitors, and miscellaneous fill, tap, and tie cells, as shown in Fig. 2(a). The aux-cell generation flow and the layout of a typical aux-cell are shown in Fig. 3. Most aux-cells are similar in size to a D flip-flop and can be placed on standard cell rows but with ports that allow their connection by the APR tool into analog structures. The creation of aux-cells is simplified by using design templates in tandem with PDK characterization scripts. The templates capture the aux-cell's precise circuit behavior in a SPICE simulation. The characterization scripts operate on the PDK to derive technology-specific parameters (threshold voltage, metal parasitics, etc.) required to set knobs within the templates. If the designer wishes to implement a new aux-cell, they can simply create a new template as a one-time effort and add its layout to the aux-cell library as a one-time effort per PDK. Basic analog aux-cells including any that the designer creates later can be used to build larger circuits. This makes it faster and convenient as newer aux-cells are created as a one-time effort to add new functionality to the existing circuits or new circuits, all the while being compatible with the existing flow. The aux-cell generation includes the netlist, layout, (dummy)

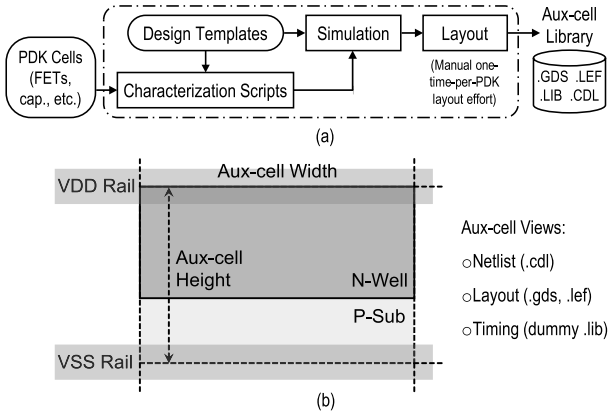


Fig. 3. (a) Aux-cell generation flow. (b) Layout of a typical aux-cell.

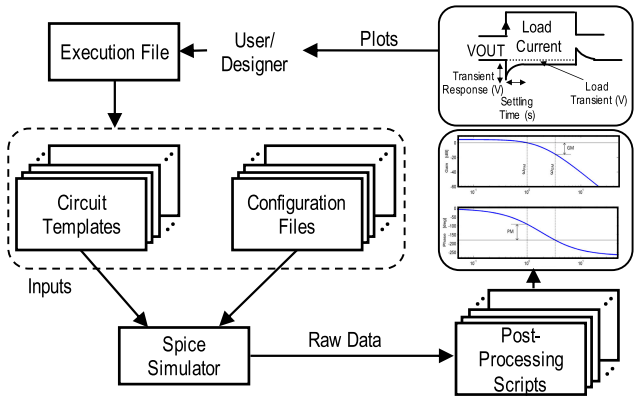


Fig. 4. User can quickly run a whole suite of simulations to design and verify LDOs using one-time generated technology agnostic circuit templates.

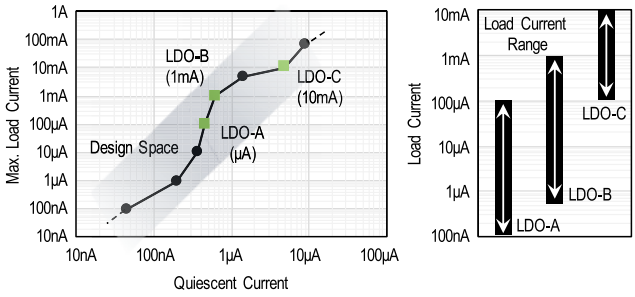
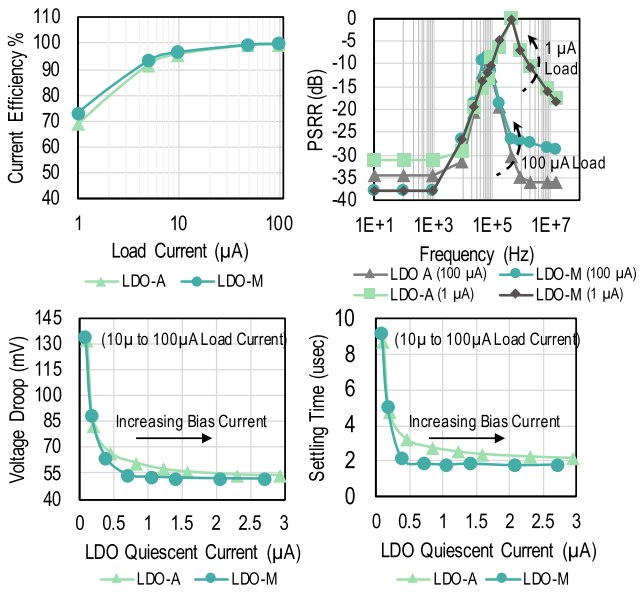


Fig. 5. Design space for synthesizable analog LDOs and load current range for three design points (LDO-A, -B, and -C) spanning a maximum load current range of 100×.

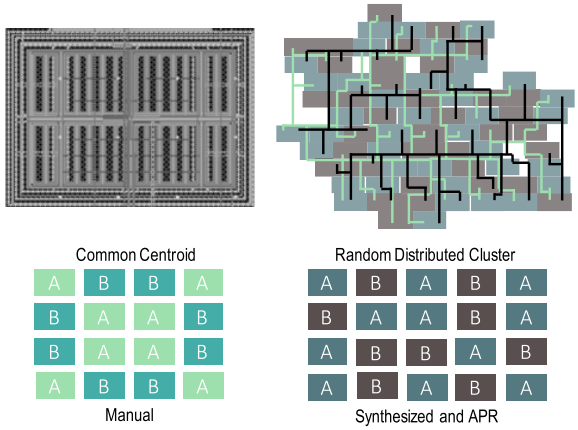
timing library, and other files required to proceed with synthesis and APR. Presently, the layouts for the aux-cells are manually created as a one-time effort per PDKL, similar to how digital standard cell libraries are built, although layout tools like ALIGN and BAG could be used for autogeneration of aux-cell layouts.

The LDO generation begins by using circuit design templates along with high-level analog specifications that satisfy the user intent. The circuit design is derived from the parameterized templates using TASE [12], [13] and circuit equations [14], as shown in Fig. 2(a). These templates are technology agnostic and include information about the netlist, stimuli and initial conditions, measure and analysis statements, and postprocessing scripts. The user intent along with simulation parameters (e.g., Monte Carlo seed), template parameters (e.g., device sizes), temperature and voltage, and model files form the configuration files. The circuit templates and configuration files are a one-time effort for each circuit. Once the circuit template has



(LDO-M and LDO-A are manual and synthesizable versions of the same LDO design)

Fig. 6. Performance comparison between synthesized LDO-M and LDO-A for various metrics. LDO-M and LDO-A are manual and synthesizable versions of the same LDO design (load current step time: 1 ns).



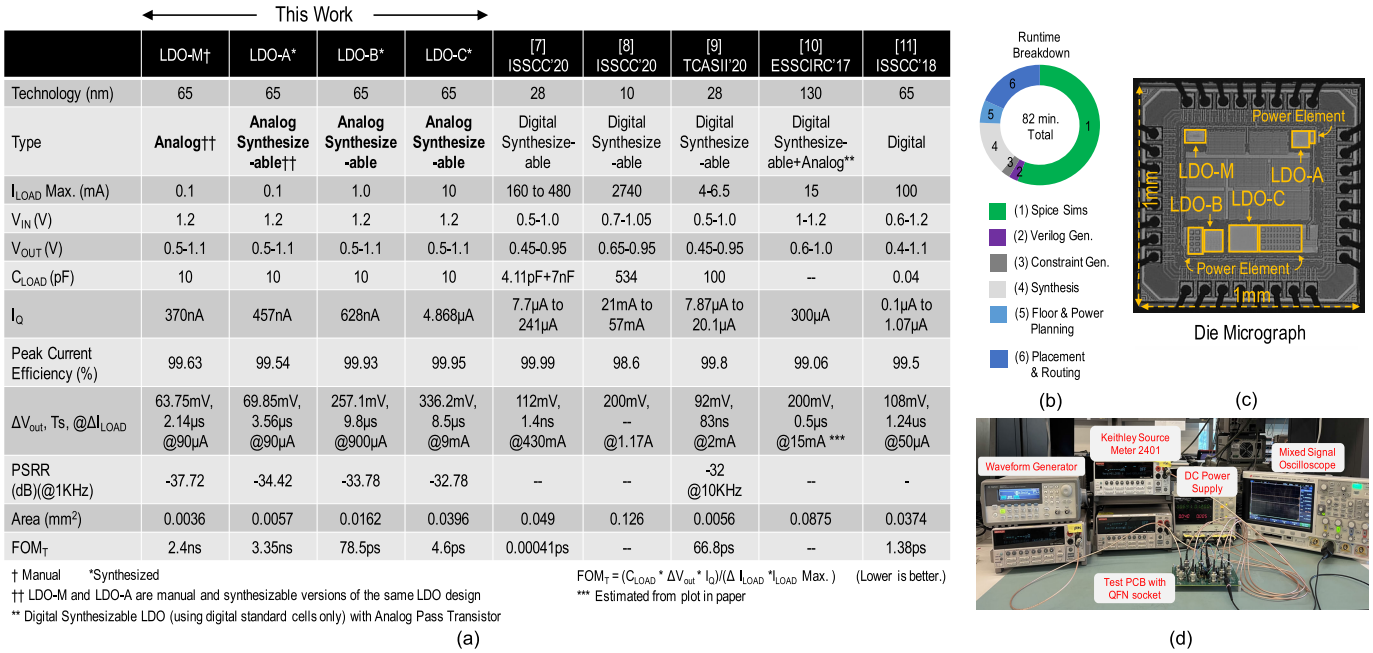
Input Offset	LDO-M (Manual)	LDO – A*	LDO – B*	LDO – C*
Mean (mV)	4.61	5.67	2.23	1.22
Sigma (mV)	11.34	6.98	7.95	4.09

(Measurement results from 20 Chips) *Synthesized
LDO-M and LDO-A are manual and synthesizable versions of the same LDO design

Fig. 7. Input offset comparison between manually drawn common centroid layout and random distributed cluster generated by the auto-place-route.

been created, the user can quickly run a whole suite of design (as shown in Fig. 4) and verification simulations using these technology agnostic circuit templates and design the LDO, thereby cutting back significantly on design time. If the designer wishes to implement a new circuit architecture or topology, they can create a new circuit template as a one-time effort and rerun the same flow to quickly generate the circuit.

The next phase is the Verilog generation that leverages the schematics to produce a synthesizable Verilog description of the block that incorporates the analog aux-cells. Fig. 2(a) shows the circuit diagram of our two-stage amplifier with Miller frequency compensation and pole-zero cancellation. The analog subcomponents that make up the amplifier are also highlighted. Each analog subcomponent is



This Work

	LDO-M†	LDO-A*	LDO-B*	LDO-C*	[7] ISSCC'20	[8] ISSCC'20	[9] TCASII'20	[10] ESSCIRC'17	[11] ISSCC'18
Technology (nm)	65	65	65	65	28	10	28	130	65
Type	**Analog††**	**Analog Synthesize -able††**	**Analog Synthesize -able**	**Analog Synthesize -able**	Digital Synthesize-able	Digital Synthesize -able	Digital Synthesize -able	Digital Synthesize-able+Analog**	Digital
I_{LOAD} Max. (mA)	0.1	0.1	1.0	10	160 to 480	2740	4-6.5	15	100
V_{IN} (V)	1.2	1.2	1.2	1.2	0.5-1.0	0.7-1.05	0.5-1.0	1-1.2	0.6-1.2
V_{OUT} (V)	0.5-1.1	0.5-1.1	0.5-1.1	0.5-1.1	0.45-0.95	0.65-0.95	0.45-0.95	0.6-1.0	0.4-1.1
C_{LOAD} (pF)	10	10	10	10	4.11pF+7nF	534	100	--	0.04
I_Q	370nA	457nA	628nA	4.868µA	7.7µA to 241µA	21mA to 57mA	7.87µA to 20.1µA	300µA	0.1µA to 1.07µA
Peak Current Efficiency (%)	99.63	99.54	99.93	99.95	99.99	98.6	99.8	99.06	99.5
ΔV_{out}, Ts, @ΔI_{LOAD}	63.75mV, 2.14µs @90µA	69.85mV, 3.56µs @90µA	257.1mV, 9.8µs @900µA	336.2mV, 8.5µs @9mA	112mV, 1.4ns @430mA	200mV, -- @1.17A	92mV, 83ns @2mA	200mV, 0.5µs @15mA ***	108mV, 1.24us @50µA
PSRR (dB)(@1KHz)	-37.72	-34.42	-33.78	-32.78	--	--	-32 @10KHz	--	-
Area (mm^2)	0.0036	0.0057	0.0162	0.0396	0.049	0.126	0.0056	0.0875	0.0374
FOM_T	2.4ns	3.35ns	78.5ps	4.6ps	0.00041ps	--	66.8ps	--	1.38ps

† Manual *Synthesized
†† LDO-M and LDO-A are manual and synthesizable versions of the same LDO design
** Digital Synthesizable LDO (using digital standard cells only) with Analog Pass Transistor
$FOM_T = (C_{LOAD} * \Delta V_{out} * I_Q)/(\Delta I_{LOAD} * I_{LOAD}$ Max.) (Lower is better.)
*** Estimated from plot in paper

(a)

Fig. 8. (a) Comparison of synthesized analog LDOs with prior state-of-the-art synthesizable LDOs. (b) Runtime breakdown for the generation of the LDO. (c) Die photograph of the synthesized analog LDOs. (d) Photograph of the testing bench setup and PCB.

discretized into small aux-cells using the unit cells from the analog standard cell library. These aux-cells are placed in series or parallel according to the schematic of the LDO and can be aggregated to vary the effective device width of a particular transistor or cell. Fig. 2(a) shows the process of discretization of the analog circuit subcomponents and its APR. The Verilog is then passed on to a digital flow step to perform synthesis, APR, DRC, and LVS verification. The last step is a verification and reporting of the generated LDO. The full circuit goes through parasitic extraction, SPICE simulations, and other verification to generate performance numbers.

III. Performance Evaluation and Measurement Results

Fig. 5 shows the design space for various LDO designs. Three design points (LDO-A, -B, and -C) spanning a maximum load current range of 100× were selected for measurement and verification purposes to showcase and prove the synthesizable analog unit-cell-based approach. A manually drawn LDO-M, identical in schematic design to LDO-A was also generated and measured to compare it with the synthesized approach in terms of performance. The four LDO designs (LDO-A to -C and LDO-M) were fabricated in a 65-nm LP process. Fig. 2(c) shows the layout comparison between the manually created common centroid layout (LDO-M) and the synthesized version (LDO-A). Fig. 6 shows the measurement results comparing the performance between the manually created LDO-M and synthesized LDO-A. Table I shows the performance evaluation for the LDO-A before splitting into unit aux-cells (pre-PEX) and after the synthesis and APR process (post-PEX) across corners and compares it against measurement results. As seen in the table, the results from simulations using post-APR extracted netlist and measurement results match closely. The combination of variability due to small transistors in unit aux-cells and mismatch from parasitics associated with the interconnect from the autorouting leads to increase in input offset, and some loss in transient response and PSRR, but the difference in performance is minimal.

It is desirable to have low input offset variability in LDOs, especially in precision circuit applications. Within-die variations

TABLE I
Summary of Performance Evaluation for LDO-A

Metric	Pre-PEX			Post-PEX			Meas.
	TT 27°C	SS -20°C	FF 80°C	TT 27°C	SS -20°C	FF 80°C	
Current Efficiency (%)	99.64	99.68	99.63	99.59	99.67	99.61	99.54
ΔV_{out} (mV), Ts (µs)*	57.5, 0.414	71.7, 2.13	64.4, 0.287	64.9, 0.538	85.3, 3.4	70.2, 0.342	69.85, 3.56
PSRR (dB)	-37.25	-35.89	-37.97	-36.04	-34.68	-36.77	-34.42
Input Offset (µ,σ)** (mV)	0.94, 2.33	-	-	5.95, 7.19	-	-	5.56, 6.85

*@ΔI_{LOAD}=90µA **5K MC runs

affect devices differently based on their location on a chip, resulting in differential mismatch. Within-die systematic variations are often modeled by linear gradients, while random variations are modeled with distributions. Random variations have uncorrelated and spatially correlated components characterized by a correlation distance [15]. Fig. 7 shows the input offset variability comparison between a manually drawn common-centroid (CC) layout and our APR-based random-distributed cluster of unit cells. The standard deviation for the CC version is 11.34 mV, which is common for untrimmed, unchopped LDOs. In comparison, the synthesized LDO-A reduces variability by 38.4% down to 6.98 mV.

The APR of unit cells in the synthesized version splits large transistors into many small unit cells and spatially distributes them over a large area, reducing variability due to gradients and spatially correlated randomness by averaging those affects across multiple distributed copies. The LDO-C, which has the largest area, reduces variability by up to 63.93%. We note that if correlation distance is reduced due to either the use of smaller transistors or larger discretization steps in unit-cell sizing, the trend in variability can be expected to reverse in comparison to CC strategy.

Fig. 8 shows the performance comparison of the synthesizable analog LDOs with other state-of-the-art works. When comparing the synthesized analog LDO with the manually drawn version, the key

performance parameters, such as the current efficiency, the transient response, and the FOM, show minimal deviation. In addition, the synthesized version allows for reduced input offset variability. As seen in Fig. 8, the synthesized LDOs achieve up to 99.95% peak current efficiency, a PSRR of −34.42 dB, and an FOM of 4.6 ps, which is comparable to other state-of-the-art LDOs.

IV. Conclusion

In this work, we proposed a digital flow-based approach to design all-analog circuits that dramatically speeds the design and layout process while retaining the benefits of true analog topologies and demonstrated its performance for three LDO. Measurement results showed minimal loss in performance between manually generated LDO and its synthesized counterpart and showed up to 63.93% reduction in input offset. Using the synthesizable analog unit-cell-based approach allowed us to significantly cut back on manual layout and verification efforts and improve turn-around-time and design scalability, pointing to an analog design approach, in which components can be automatically optimized and implemented for each instance based on the precise context.

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