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A Fast Transient Response Capacitorless LDO Designed in 22FDX® Technology

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Abstract - **This paper presents a low-dropout capacitorless linear regulator using a low output resistance buffer, designed in GlobalFoundries 22nm fully depleted silicon on insulator technology. The proposed LDO consumes 85 µA from 1.8 V power supply. The output voltage is configurable in the range of 0.9–1.25 V. The target maximum output current is 30 mA. The load transient response time is about 15 ns. The target is to have at least 20 dB Power Supply Rejection Ratio (PSRR) at 5 MHz (the frequency that the digital is operating on). The compact design is occupying area of only 0.18 mm^2.**

Keywords - ***LDO design, fast LDO, capacitorless LDO, 22FDX® technology***

I. Introduction

GlobalFoundries's proprietary FDX® technology is based on fully depleted silicon-on-insulator technology (FDSOI). Incredibly well suited for efficient single-chip integration of digital and analog signals. In addition, features such as ultra-high speed and ultra-low leakage, make the FDX® process technology platform especially well matched for periphery designs like LDOs or low-power bandgaps.

There is no actual bulk in the conventional meaning of the word. There are no body diodes. Underneath the ultra-thin buried oxide is the body biasing layer (Figure 1). It can be connected to ±2V driving the threshold voltage up or down, for ultra-low leakage or ultra-high speed. In the case of a LDO, the pass P-MOS transistor body biasing layer can be connected to a voltage lower than the power supply for active mode (for lower threshold), and to the power supply for when the LDO is disabled (for lower leakage).

Low-dropout regulators (LDO) are widely used in modern electronic devices for providing a constant supply-independent output voltage in the presence of varying load and supply ripples. The ever-growing demand for RF/photonic communication puts a high strain on the modern regulators. The need for high bandwidth LDO with good PSRR at the frequency of the main noise contributor emerges. Often this low frequency noise generator is the digital control block. Electrical spikes at low frequencies 1–10 MHz are appearing as DC offset at the RF outputs that are working at 20–200 GHz.

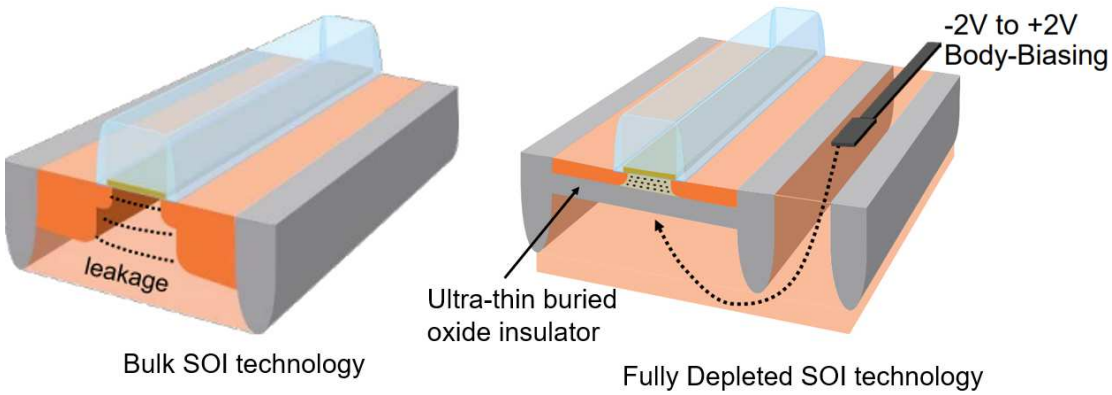

Fig 1. 22FDX® Technology essentials

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In this paper, the authors are presenting a design of fast, capacitorless LDO with source inputs and common source buffer for driving the pass transistor gate capacitance. The design is described in Section II. The simulation results are described in Section III along with some DC measurement results. Section IV gives the conclusion of the paper.

II. Proposed Architecture

A. Circuit Design

There are many architectures for Low-Dropout regulators that are seeing wide use in today's electronics [1][2][3]. The proposed LDO design (Figure 2) is basically a low ohmic buffer for the reference voltage [4][5]. There is 100% negative feedback provided by connecting the source of P_2 to V_{OUT}. The transistors P_1 and P_2 are acting as differential pair with source inputs (common gate amplifier stage). They are having maximum bandwidth since the Miller effect coming from the drain-gate capacitor is a lot smaller comparing to the common source stage used in the conventional architectures. Since this is common gate stage, the input resistance is sacrificed and 15µA are sunk by P_1 from the reference voltage (and another 15µA by P_2 from the output). The common source driver comprised of N_1 and I_3 is working as a buffer that drives P_P.

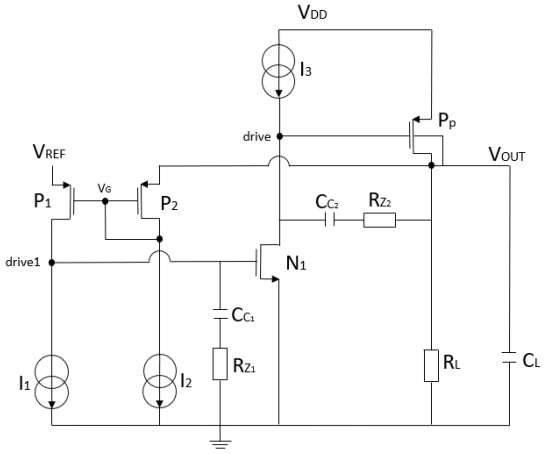

Fig 2. Block schematic of the LDO

B. Sizing and Routing

P_2-should be sized so that I_2 continues working even when the V_{REF} is at its minimum. P_1 should be sized so that P_1V_{DS} is not compromised at the maximum output load by the V_{GS} of N_1. P_1 and P_2 should be equal as they are acting as differential pair. N_1 will decide the size of the pass transistor. If W/L ratio of N_1 is high, then the drive point will be able to get closer to 0 V during high loads. This will decrease the size of the pass transistor and will boost the gain of the common source stage; the circuit will become hard to compensate.

P_P is using the fully depleted 22FDX® technology by connecting the substrate to the output. That is lowering the threshold significantly and making P_P smaller by 35% to 200 µm by 0.15 µm (Figure 3). Following this logic, the pass transistor can be made even smaller by connecting the substrate to the power supply. If that is the case, there will be another issue occurring. The common source stage will not be able to turn off the transistor, in the case when the load is 0.

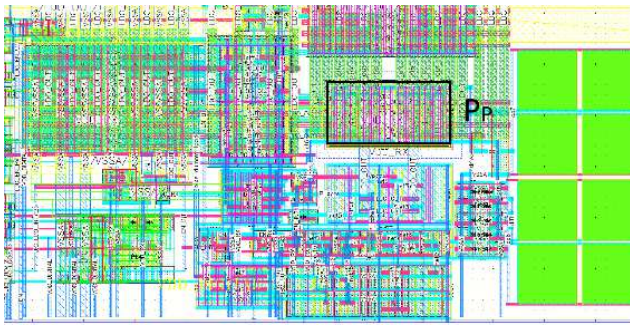

Fig 3. The pass transistor

The routing of the node *drive*, that is the output node of the common source stage (Figure 4), should result in as less as possible parasitic capacitance since it has a significant impact over the main pole.

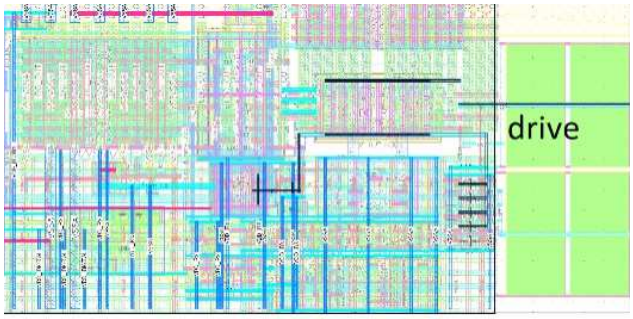

Fig 4. Drive node highlighted in black

C. Stability

The circuit consist of one input common gate stage and two consequence common source stages. We can use common formulas to determine the frequencies of the different poles and zeros in the transfer functions [6].

If we assume that the output resistance of the transistors is much lower than the output resistance of the current mirrors, the transfer function of the uncompensated LDO can be written with formula (1) below [7]:

$$\frac{V_{out}(S)}{V_{in}(S)} = \frac{(-gm_{P1}\cdot R_{P1})(-gm_{N1}\cdot R_{N1})(-gm_{Pp}\cdot R_L \| R_{Pp})}{(1+\frac{S}{\omega_1})(1+\frac{S}{\omega_2})(1+\frac{S}{\omega_3})} \quad (1)$$

The circuit has 3 poles:

$$\omega_{P1} = \frac{1}{C_L\cdot R_L \| R_{Pp}} \quad (2)$$

$$\omega_{P2} = \frac{1}{C_{gsN1}\cdot R_{I1} \| R_{P1}} \approx \frac{1}{C_{gsN1}\cdot R_{P1}} \quad (3)$$

$$\omega_{P3} = \frac{1}{C_{gsPp}\cdot R_{I3} \| R_{N1}} \approx \frac{1}{C_{gsPp}\cdot R_{N1}} \quad (4)$$

Due to the presence of 3 poles in the transfer characteristics, the scheme needs 2 zeros provided by a compensation in order to stay stable. The first stage is compensated directly with resistor and capacitor connected to ground. That adds another pole (5)

$$\omega_{P4} = \frac{1}{(C_{gsN1}+C_{C1})\cdot R_{P1}} \quad (5)$$

If assume that $C_{C_1} \gg C_{gsN1}$ then the frequency for the zero should be (6)

$$\omega_{Z_1} = \frac{1}{R_{Z_1}\cdot C_{C_1}} \quad (6)$$

That moves ω_{P2} to (7)

$$\omega_{P2} = \frac{1}{C_{gsN1}\cdot R_{P1} \| R_{Z1}} \quad (7)$$

There is a Miller type compensation connected between the output of the second stage and the output of the third stage. This compensation is placing high frequency zero at (8)

$$\omega_{Z2} \approx \frac{-gm_{Pp}}{C_{C_2}} \quad (8)$$

Because for high frequencies, the compensation shortens the 2 stages and combining them into one first order stage, thus +20dB/Dec, but by adding a resistor in the compensation we can move the zero to much lower frequency, helping with the stability (9)[8]

$$\omega_{Z2} = \frac{1}{(\frac{1}{gm_{Pp}} - R_{Z2})\cdot C_{C2}} \quad (9)$$

The value of the resistor R_{Z2} should be kept higher than $\frac{1}{gm_{Pp}}$.

The dominant pole (4) moves to (10)

$$\omega_{P3} = \frac{1}{(C_{C_2}+C_L)\cdot R_L + (C_{gsPp}+C_{C_2})\cdot R_{N1} + gm_{Pp}\cdot R_{N1}\cdot R_L\cdot C_{C_2}}$$

$$\approx \omega_{P3} = \frac{1}{gm_{Pp}\cdot R_{N1}\cdot R_L\cdot C_{C_2}} \quad (10)$$

The output pole (2) moves to (11)

$$\omega_{P1} = \frac{1}{(C_L + C_{C_2})\cdot R_L + (C_{gsPp} + C_{C_2})\cdot R_{Pp} + \cdots \ldots}$$

$$\frac{1}{\ldots\ldots + gm_{Pp}\cdot R_{N1}\cdot R_L\cdot C_{C_2} + (C_{C_2}\cdot C_L + C_{gsPp}\cdot C_L + C_{C_2}\cdot C_{gsPp})\cdot R_{Pp}\cdot R_L} \quad (11)$$

And this is how the so-called pole splitting effect is working. Further simplifying (11) into (12) for· $C_L > C_{C_2} > C_{gsPp}$

$$\omega_{P1} \approx \frac{gm_{Pp}\cdot C_{C_2}}{C_{C_2}\cdot C_L + C_{gsPp}\cdot C_L + C_{C_2}\cdot C_{gsPp}} \approx \frac{gm_{Pp}}{C_L + C_{gsPp}} \quad (12)$$

At high frequencies C_{C_2} makes P_P diode-connected, hence the time constant arises, and the output pole is moved to a higher frequency.

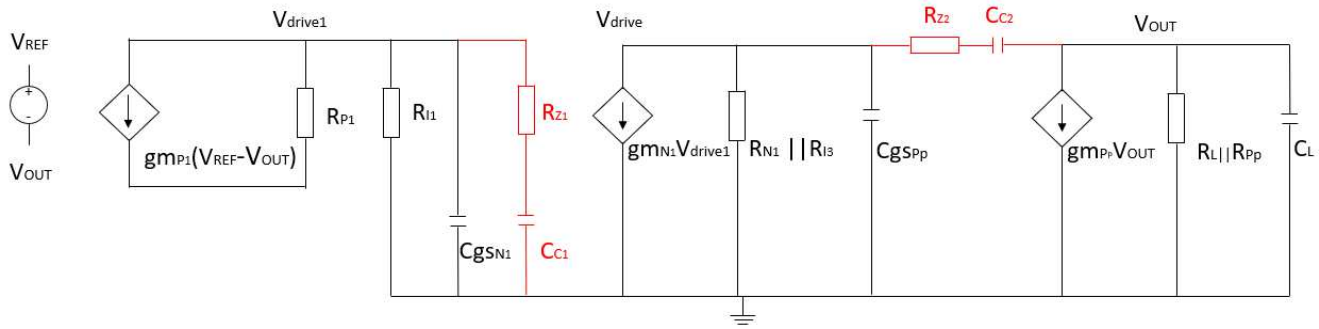

Fig 5. Small-signal model of the proposed LDO shown on Figure 2

The rapid transients are usually taken down by the large external capacitor. Since this is purely internal LDO, such a capacitor cannot be used. This degrades the light load stability because the output pole (12) is moved towards the dominant pole (10). The output current load is only 30 mA and the gate capacitance of the output transistor is low. That way the dominant pole itself (10), formed by the output resistance of the common source stage and the compensation capacitor (C_{C2}), moves away from the origin. This makes the stability at low loads even worse. The output pole should not move any closer to the 0 dB crossing when there is no load. In order to ensure this a minimum load current of 200–300 µA is required.

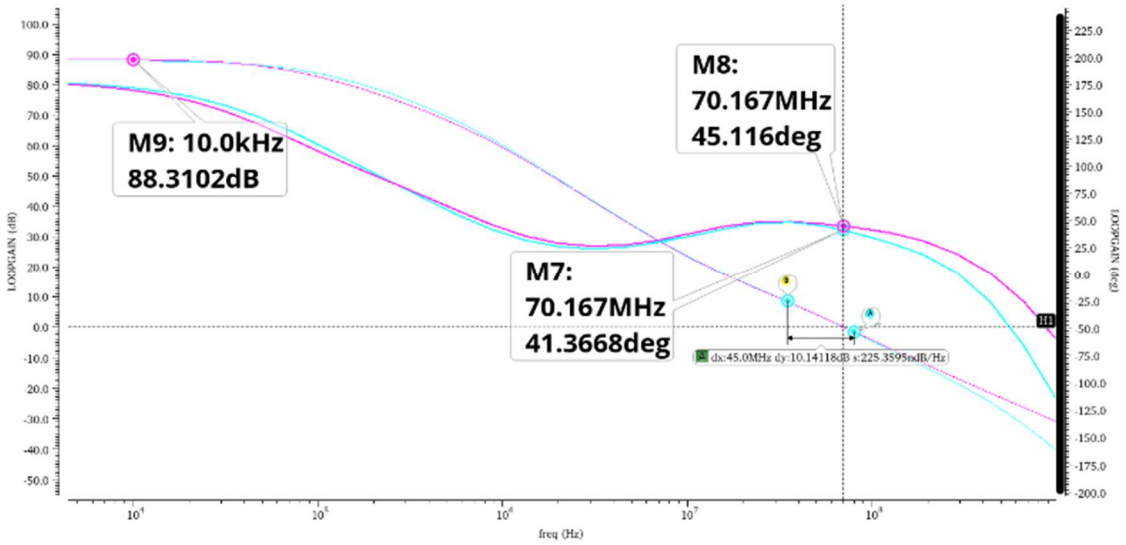

Fig 6. AC open loop output characteristics V_{REF} = 0.9V
Purple — max load; blue — no load

III. Simulation Results

A. AC simulation results

AC simulations have been performed on the proposed LDO structure. The results from a typical simulation with max load and without any load are shown on Figure 6.

The compensation and the constant load used leads to 41° phase margin for the no load condition and 45° phase margin for the maximum load condition. The Gain Bandwidth Product (GBW) is about 70 MHz. The 0 dB level is crossed with a slope of 20 dB/decade (10 dB change for half of decade is shown in Figure 6).

B. Transient simulation results

The transient response for these the cases discussed in the point above are shown on Figure 7. The effect of max load or no-load are clearly visible in the underdamped oscillations, also called ringing, in the output response to a load current pulse.

The higher the load current, the lower the ringing that will be observer in the output voltage response.

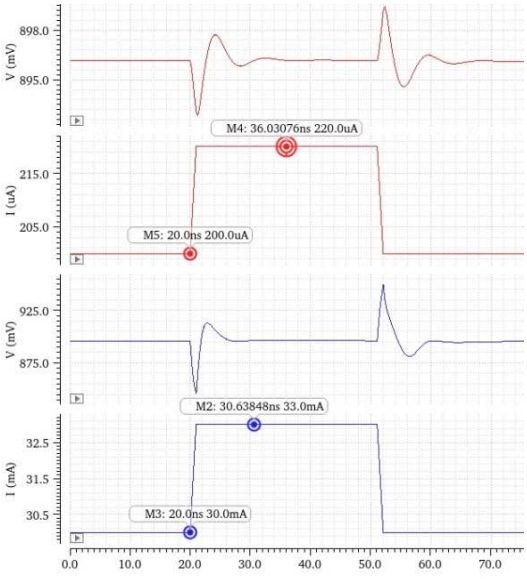

Fig 7. Simulated transient load characteristics V_{REF} =0.9 V; Red - No DC load (only the internal load is active); Blue — 30 mA DC load

C. Table of simulation results

Table 1 contains simulation results for all other relevant characteristics and parameters of the LDO.

TABLE 1. SIMULATION RESULTS

V_{REF} ~1.25 V	Bandgap voltage
Line regulation	247 µV/V
Load regulation	5 mV/A
PSRR @5MHz	30 dB
Phase Margin @ No load	43°
Phase Margin @30mA	49°
VDD	1.8 V
temperature	27 °C
I_bias	5 µA
Quiescent current consumption	85µA (excluding minimum load current)
CL	2 pF
V_{REF} = 0.9 V	
Line regulation	233 µV/V
Load regulation	5 mV/A
PSRR @5 MHz	33 dB
Phase Margin @ No load	41°
Phase Margin @30 mA	45°
VDD	1.8 V
temperature	27 °C
I_bias	5 µA
Quiescent current consumption	85 µA (excluding minimum load current)
CL	2 pF

IV. MEASUREMENT RESULTS

In order to verify the design extensive measurements have been performed in a clean room at the factory of GlobalFoundries in Dresden.

For that purpose, 12 IC from a one wafer were selected and were prepared for measurement. This process involved gluing them and bonding them to their own special purpose PCBs, using appropriate for these action methods.

An example of a complete PCB with the designed IC is shown on Figure 8.

Fig 8. Test PCB with glued and bonded chip on it

Various measurements were obtained during the measurement process and the most relevant to the LDO design are shown in Table 2.

TABLE 2. MEASUREMENT RESULTS

V_{REF} ~1.25 V	Bandgap voltage
Line regulation	~250 µV/V
Load regulation	~5 mV/A
VDD	1.8 V
temperature	27 °C
consumption	85.12 µA (disregarding the output load added for stability)
V_{REF} = 0.9 V	
Line regulation	~250 µV/V
Load regulation	~5 mV/A
VDD	1.8 V
temperature	27 °C
consumption	84.73 µA (disregarding the output load added for stability)

Table 2 is showing averaged results of all available 12 PCBs. Measured with a PXI equipped with analog card. The measurements are aligning with the simulation results.

The transient stability is not tested. The current slopes needed are hard to be achieved and as a result the voltage output is not stressed enough. As a future improvement – internal current mirror can be added that is loading the output on demand, with about 1mA. That should resolve the issue with the external current slope generation.

V. Conclusion

The final product (Figure 9) is assembled and connected top-metal-down to the client's IC with micro copper pillars.

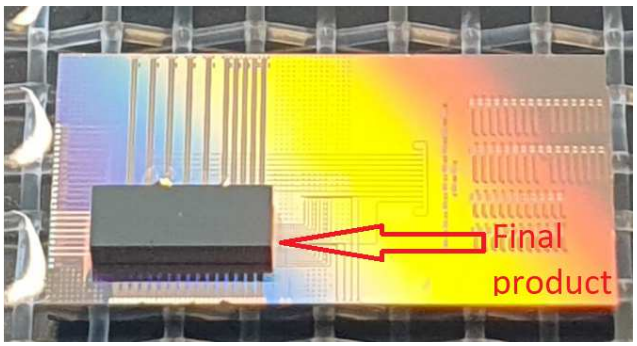

Fig 9. Assembled device

A micro-Watt capacitorless LDO is proposed, designed, and manufactured, as part of a product, using 22FDX® technology. The output voltage can be adjusted from 0.9 to 1.25 V. DC measurements are presented. The simple structure of the regulator is a good choice for a use in the automotive industry. If charge pump is available and used, the structure can be further simplified, the number of poles reduced, and the stability boosted.

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