A 1-A Switching LDO With 40-mV Dropout Voltage and Fast DVS

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***Abstract*—This brief presents a 1-A fully-integrated switching LDO for digital loads. By using 4-phase 200-MHz pulse-width modulation (PWM), it can significantly reduce the output ripple and allow using a smaller output capacitor. Distinctive from the prior dual-loop structure, we adopt a single feedback loop with a wide bandwidth error amplifier (EA) using a quasi-Type-III compensation to improve the dynamic voltage scaling (DVS) rate and to reduce the transient recovery time. Meanwhile, compared with the prior stacked power transistor architecture, the single-PMOS with auxiliary constant current (ACC) control can reduce by 4-fold the power transistor size, and decreases the driver current by at least 2.5 times. Fabricated in 28-nm bulk CMOS, the proposed LDO measures a 1-A load capability with a 40-mV dropout voltage. Moreover, the measured load regulation is 2.2 mV/A, and the line regulation is 1.8 mV/V. In addition, the regulator obtains a fast DVS speed of 4V/µs and a fast load transient recovery time of <50ns.**

***Index Terms*—Dynamic voltage scaling (DVS), low-dropout regulator (LDO), fully integrated voltage regulator (FIVR), type III compensation, PWM control, switching LDO.**

I. Introduction

SYSTEM-ON-A-CHIP (SoC) designs require multiple supply domains for better system energy efficiency and flexibility [1]. Low-dropout voltage regulators (LDOs) can provide compact and cost-effective solutions for multiple local voltage domains [2], [3]. Meanwhile, to power a large-scale digital load, the LDO needs ampere-level load capability, wide bandwidth for the fast transient response, and high accuracy for a small voltage guard band.

A switching LDO (SLDO) regulates V_{OUT} by controlling the switching duty cycle of the power transistor. Compared with an analog LDO [4], [5], [6], [7], since there is no low-frequency power transistor gate pole p_G neither load-dependent g_m issue, switching LDOs are easier to be compensated and are more suitable for wide-bandwidth and high-current applications [8], [9]. The main drawback of a switching LDO is its self-generated output ripple. It usually requires a large output capacitor and a GHz switching frequency to reduce the output ripple. Reference [10] presents a dual-loop 4-phase switching LDO that allows using a smaller output capacitor and obtains a fast transient response.

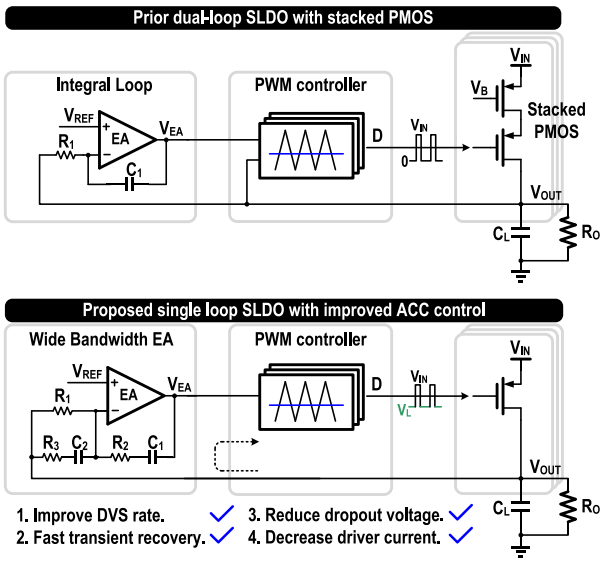

Fig. 1. Simplified block diagram of the prior dual loop SLDO [10] and proposed single feedback loop SLDO.

However, the architecture in [10] still needs to be improved. First, although the dual-loop architecture obtains a fast load transient response due to the fast PWM loop, its dynamic voltage scaling (DVS) and load transient recovery speed would be limited by the slow loop. Second, to resist process, voltage, and temperature (PVT) variations, [10] adopts a stacked power transistor structure: two PMOS transistors connected in series, where the top PMOS maintains a constant current and the bottom PMOS switches fully on/off controlled by the comparator output signal. For the same dropout voltage and load capability, the power transistor area increases by 4-fold, and the driver current is doubled, limiting its application in low dropout voltage cases.

In this brief, we present a switching LDO with single feedback loop structure and an improved auxiliary constant current (ACC) control to solve the above-mentioned issues. The organization of this brief is the following. Section II describes the architecture, operational principles, and key circuit implementations. Section III exhibits the measurement results. Finally, Section IV draws the conclusions.

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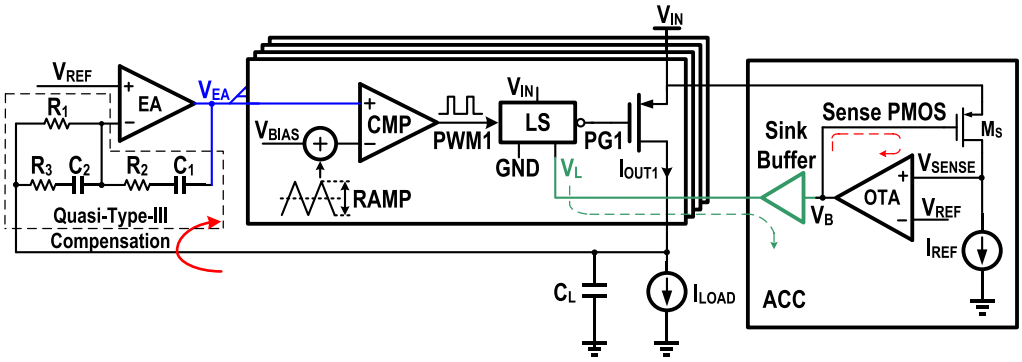

Fig. 2. System architecture of the proposed switching LDO with 4-phase PWM control and ACC technology.

II. Proposed Architecture and Working Principles

Fig. 1 shows the simplified block diagram of the prior dual-loop SLDO [10] and the proposed single feedback loop SLDO. We use a wide bandwidth error amplifier (EA) with a quasi-Type-III compensation for a faster DVS rate and a shorter load transient recovery time. In addition, the improved ACC technique can enable the single-stage power transistor to simultaneously have both the functions of a constant current source and a switch. Compared with the prior stacked power transistor, it can reduce the dropout voltage, silicon area, and driver current.

A. Proposed System Architecture

Fig. 2 shows the system architecture of the proposed multi-phase switching LDO. It consists of an EA with a quasi-Type-III compensator, a 4-phase PWM controller, power transistors, and an ACC circuit.

Multi-phase technology can remarkably decrease both the input current ripple and the output voltage ripple [11]. Regardless of the impact of the capacitor equivalent-series-resistance (ESR) and the possible unbalanced current, in theory, by using 4-phase PWM control, we can reduce 16-fold the maximum output ripple when compared to the single-phase case. In other words, multi-phase technique can enable the switching LDO to use a smaller output capacitor and/or a lower switching frequency for the same output ripple. Here, the maximum current is 1 A with a 5-nF output capacitor, and the switching frequency is 200-MHz. Theoretically according to the ripple expression in [10], the calculated maximum output ripple is 15.625mV.

Resistors R_1, R_2, R_3, and capacitors C_1 and C_2 form the compensation network. Since the output capacitor is only 5 nF and the associated ESR zero is above several GHz, no additional pole is necessary to counteract it. Therefore, when compared with the typical Type-III compensation [12], there is no small capacitor connected between the negative input terminal and the EA output. Thus, we designate this method as quasi-Type-III compensation.

The current flows across the power transistors vary a lot with the V_{DS} voltage (V_{IN}–V_{OUT}). Especially in the fast corner and with a large V_{IN}-V_{OUT}, the current becomes much larger, then significantly increases the output ripple, even causing stability issues (to be discussed in Section II-B). The ACC technique enables the power transistor to work as a constant current source resisting the PVT variations. The voltage V_L is the adaptive "GND" of the level shifter (LS). This LS converts the PWM signal to the [V_{IN}:V_L] power domain. Here, V_L changes with PVT variations to ensure that the drain current equals to the defined value.

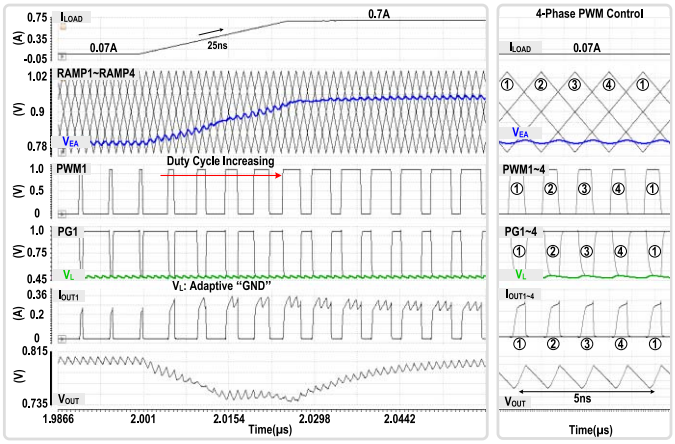

Fig. 3. Simulated waveforms of load transient and 4-phase PWM control.

Fig. 3 exhibits the simulated load transient and the 4-phase PWM control waveforms. When the power transistor turns on, its gate voltage is V_L (green line) instead of GND. When the load current suddenly increases, the V_{OUT} droop causes V_{EA} to rise rapidly. And then the PWM controller increases the duty cycle, increasing the output current and making the output voltage back to the target value.

B. Loop Stability Analysis

Fig. 4 presents the simplified model of the proposed LDO architecture. Here, RAMP is the amplitude of the 200-MHz triangle waves, D is the switching duty cycle of the power transistor, and I_{SW} is set by the ACC circuit and is equal to the maximum load current. We break the V_{OUT} feedback signal path for stability analysis and divide the architecture into three parts: EA, PWM controller, and output stage. For the output stage, we can derive the transfer function A_{VS} as,

$$A_{VS} = \frac{\partial V_{OUT}}{\partial D} = \frac{I_{SW} \times R_O}{1 + sR_OC_L}. \quad (1)$$

where C_L is the output capacitor, R_O is the load resistance. The equivalent capacitance of a large digital circuit is in the

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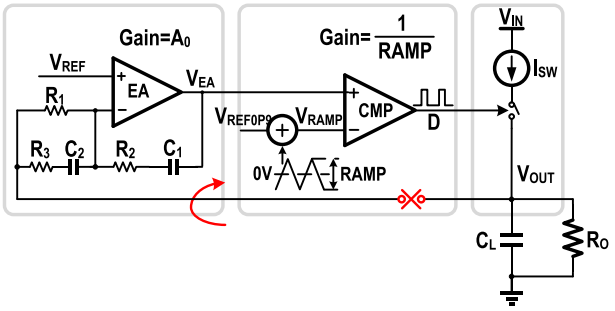

Fig. 4. Small-signal analysis of the proposed LDO.

nF range. Assuming $C_L = 5$ nF and the output resistance R_O varies between 900 ohms and 0.9 ohms, the output pole p_{OUT} will vary between 35.4 kHz and 35.4 MHz. Therefore, for a 100-MHz loop bandwidth, p_{OUT} is within the bandwidth. According to (1), the switching output stage has a constant gain-bandwidth product. When the output pole is placed within the loop bandwidth, we can easily get a constant bandwidth that does not change with the load current, which is very favorable for improving the stability and simplifying the compensation. The transfer function of the whole loop becomes,

$$H(s) = \frac{-\frac{I_{SW}}{RAMP} A_0 R_O (1 + sR_2C_1)[1 + s(R_1 + R_3)C_2]}{[1 + s(A_0 + 1)R_1C_1](1 + sR_3C_2)(1 + sR_OC_L)} \quad (2)$$

Here, p_0 is the dominant pole,

$$p_0 = \frac{1}{(A_0 + 1)R_1C_1} \quad (3)$$

and the output pole p_{OUT} is

$$p_{OUT} = \frac{1}{R_OC_L}. \quad (4)$$

In addition, this system contains a major zero z_0, given as,

$$z_0 = \frac{1}{R_2C_1}. \quad (5)$$

There is also a pole-zero pair to improve the phase margin,

$$p_1 = \frac{1}{R_3C_2} \quad (6)$$

$$z_1 = \frac{1}{(R_1 + R_3)C_2}. \quad (7)$$

Therefore, the total feedback loop has three effective poles and two zeros. Here, $R_1 = 2.5$ kΩ, $R_2 = 4$ kΩ, $R_3 = 1$ kΩ, $C_1 = 2.7$ pF, and $C_2 = 0.6$ pF. Fig. 5 displays the Bode plot of the entire loop in different load conditions. The proposed architecture has, simultaneously, high DC gain and wide bandwidth with good stability.

Without the ACC control, in the fast corner or a large V_{IN}-V_{OUT} voltage condition, I_{SW} will increase significantly. According to (2), the loop gain will increase. With the same pole-zero conditions, the loop bandwidth will also increase substantially. The high-frequency parasitic pole and the phase shift may cause instability (Fig. 6). By using the ACC technique, I_{SW} is roughly a fixed value, implying an easier and more robust loop compensation.

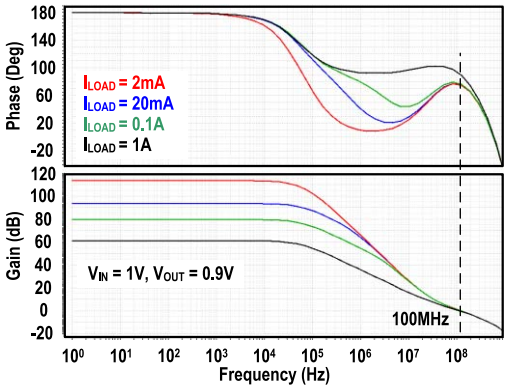

Fig. 5. Simulated Bode plot with different load conditions.

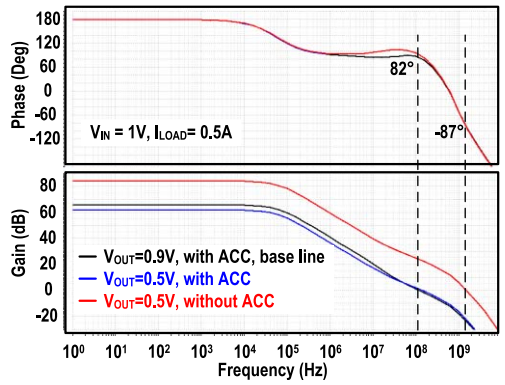

Fig. 6. Comparison of the bode-plot waveforms: with ACC and without the ACC.

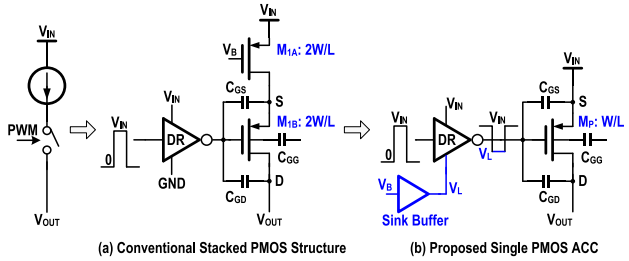

Fig. 7. The auxiliary constant current control circuit.

C. Auxiliary Constant Current Circuit Implementation

Fig. 7 shows the ACC structure. We add a buffer with sink current capability to V_B [13]. The output voltage of the sink buffer V_L is the adaptive "GND" of the level shift and driver. When the power PMOS transistor is turned on, its gate voltage is V_L ($V_L = V_B$) and the drain current is limited to a fixed value, set by I_{REF}. Fig. 8(a) plots the simulated waveforms of the ACC. Without ACC, the maximum current will be 20 A in the extreme corner, which is almost 16.7 times larger than the designed capability. The ACC technique can keep I_{SW} constant and avoid oversizing in large V_{IN}–V_{OUT} conditions.

Compared with the stacked PMOS structure in [10], the single PMOS ACC technique has two advantages. First, without the series power transistor, it can reduce the conduction voltage loss, which is more suitable for ultra-low dropout voltage LDO designs. Second, with the same dropout

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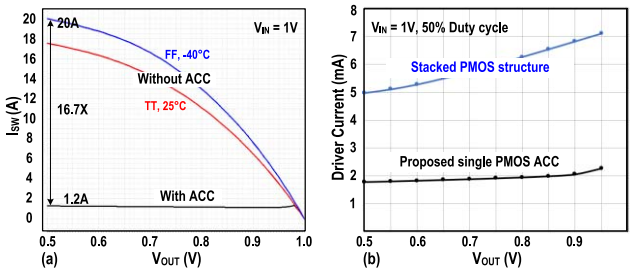

Fig. 8. Simulated waveforms of the ACC function and driver current.

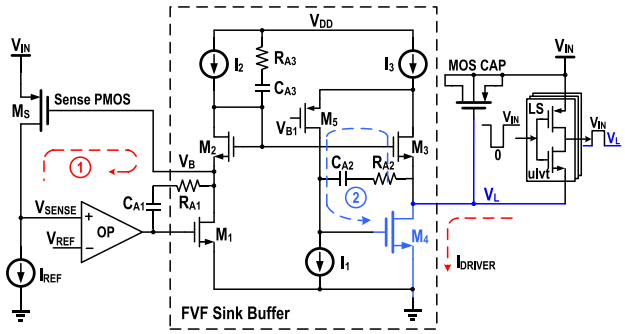

Fig. 9. Schematic of the improved ACC.

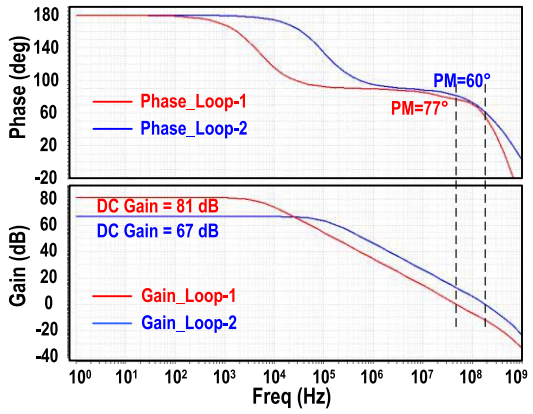

Fig. 10. Simulated Bode plot of the proposed ACC loops.

voltage and load capability, it has a smaller power transistor, and we can reduce the driver current by at least 2 times. Additionally, since the gate voltage of the power transistors is "V_{IN}–V_L" instead of "V_{IN}–GND", we can further diminish the driver current. Fig. 8(b) shows the drive current comparison between these 2 methods, with the same dropout voltage, load capability, and 50% duty cycle. We can see that the improved ACC technique significantly reduces the driver current.

Fig. 9 exhibits that the core structure of the ACC which is a buffer with a current sink capability. There are mainly two feedback loops in the ACC. Loop-1 generates V_B as the gate voltage of M_S and ensures that the current through the sense transistor M_S is equal to I_{REF}. Loop-2 is the fast flipped-voltage-follower (FVF) sink buffer composed of M_1-M_5, and I_1-I_3. The driving current passes through M_4 to GND. Fig. 10 shows the simulated Bode plots of the two loops. The phase margins are 77° and 60°, respectively. Loop-2 has a bandwidth of 186 MHz and can regulate V_L quickly.

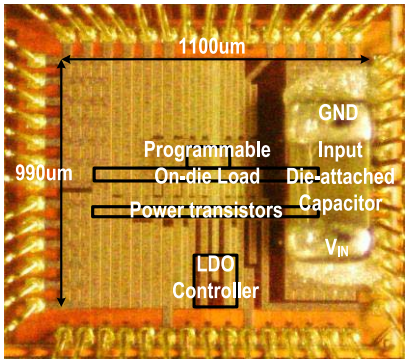

Fig. 11. Die micrograph.

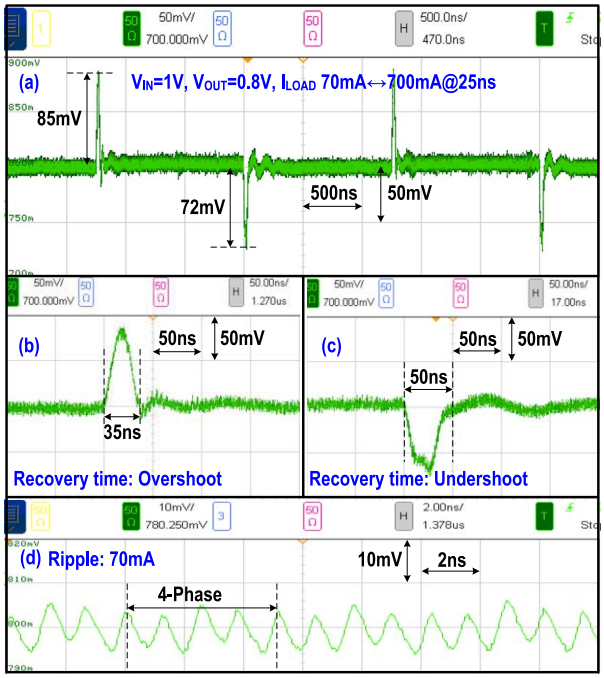

Fig. 12. Measured (a) V_{OUT} load transient responses, (b) overshoot recovery time, (c) undershoot recovery time, and (d) output voltage ripple.

The mismatches between the sensing and power transistors and the mismatch between M_2 and M_3 may affect the accuracy of I_{SW}. Although I_{SW} does not affect the V_{OUT} accuracy, a significant deviation will affect the load capability (I_{SW} too small) or the system stability (I_{SW} too large). Therefore, we need to ensure sufficient margin in designing the current sensing ratio and the compensation network.

III. Measurement Results

Fig. 11 shows the die micrograph of the prototype chip fabricated in a 28-nm CMOS bulk process. The active area is 0.05 mm^2, and the controller area is 0.023 mm^2. The lower side region of the test chip is mainly in the V_{IN} power domain, which contains a 3-nF input capacitor and the LDO core. The upper region of the chip is in the V_{OUT} power domain, which contains a 5-nF output capacitor and a programmable on-die load. Due to the input bond-wire parasitic inductance, V_{IN} has large variations during the load transients. To reduce the V_{IN} variation, we attach a 0201-package capacitor on die, using electric conductive adhesive.

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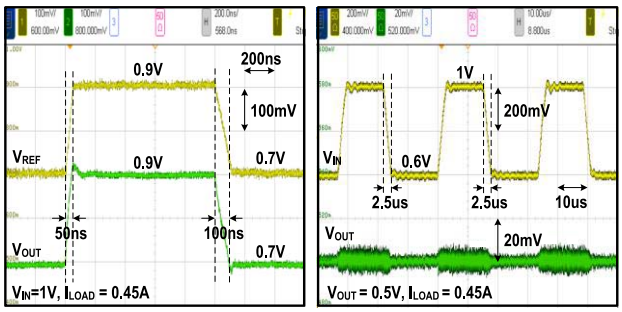

(a) Dynamic voltage scaling (b) Line transient response

Fig. 13. Measured dynamic voltage scaling and line transient responses.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ARTS

	[7] TCAS-II 2020	[2] JSSC 2021	[9] JSSC 2020	[10] JSSC 2021	**This Work**
Type	Analog	DA-Analog*	Switching	Switching	**Switching**
Process	65nm	65nm	22nm SOI	28nm	**28nm**
Area (mm^2)	0.0086	0.36	0.155	0.048	**0.05**
F_S (MHz)	NA	100	>1000	500	**200**
V_{IN} (V)	0.9	1.2	0.64-1.1	0.6-1	**0.6-1**
V_{OUT} (V)	0.85	0.6-1	0.6-1.06	0.5-0.9	**0.5-0.96**
Dropout (mV)	50	200	40	90	**40**
I_{MAX} (A)	0.02	0.5	12	1.5	**1**
C_L (nF)	0.036	0.25	481	5	**5**
I_Q (mA)	0.033	0.12	NA	1.8	**1.15**
Load Reg. (μV/mA)	260	30	1.1	1	**2.2**
ΔV_{OUT}, ΔI_{LOAD} @T_{Edge},	176mV, 0.02A@ 0.1ns	55mV, 0.45A@ 100ns	20mV, 4.9A@ 10ns	<70mV, 1A@ 10ns	**72mV, 0.63A@ 25ns**
Recovery Time (ns)	220	174	80-100	300	**50**
DVS Rate (V/us)	NA	0.267	0.33(up)/ 0.57	0.4	**4 (up) / 2 (down)**
Current Eff. (max.)	NA	99.97%	96.1%	99.27%	**99.69%**

* DA-Analog: Digital-Assisted Analog LDO

Fig. 12(a) presents the measured load transient waveforms. For load steps of 0.07 A to 0.7 A with a 25-ns edge time, when V_{OUT} = 0.8 V, the overshoot and undershoot voltages are 85 mV and 72 mV, respectively. Fig. 12(b) and (c) show the zoomed-in views of the voltage overshoot and undershoot. We can observe that the recovery time is within 50 ns. Fig. 12(d) presents the output voltage-ripple waveform with 4-phase operation.

Fig. 13(a) gives the DVS transient waveforms, with V_{IN} = 1 V, and V_{REF} changes from 0.7 V to 0.9 V. The DVS up rate can reach 4 V/μs, and the DVS down rate is 2 V/μs. As observed, V_{OUT} can track the V_{REF} fast changing. Fig. 13(b) shows the line transient waveforms, with V_{OUT} = 0.5 V, I_{LOAD} = 0.45 A, and V_{IN} changes from 0.6 V to 1 V within 2.5 μs. The proposed LDO can operate well under low input voltage and remain stable over a wide input range. As the strength of the power transistor and driver capability decrease at low V_{IN}, the output ripple at V_{IN} = 0.6 V is smaller than that at V_{IN} = 1 V.

Table I presents a performance summary of the proposed LDO and the comparison with state-of-the-art works. The switching architecture simplifies the design of a high-current LDO regulator with smaller dropout voltage and wider input/output voltage ranges. Due to the high-gain EA and ACC, we can achieve precise regulation. For V_{IN} = 1 V, I_{LOAD} varies from 10 mA to 1 A, the load regulation is 2.2 mV/A. And the line regulation is 1.8 mV/V. The peak current efficiency of the LDO is 99.69% at the maximum load of 1 A. Compared to the dual-loop architecture, although the switching frequency is much lower than the prior arts [9] and [10], the proposed single-loop switching LDO with the quasi-Type-III compensation can significantly increase the DVS rate (4 V/μs) and reduce the recovery time (50 ns).

IV. CONCLUSION

This brief presented a 1-A fully integrated switching LDO with 4-phase 200-MHz PWM control. Using a single feedback loop with a wide-bandwidth EA and a quasi-Type-III compensation, the proposed switching LDO obtained a fast DVS rate of 4 V/μs and a small load transient recovery time of <50 ns. Compared with the prior dual-loop structure, there is at least a 5-fold improvement. In addition, the improved ACC technique instead of the prior stacked PMOS structure reduces the dropout voltage, silicon area, and driver current.

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