Design of a Low-Power and Area-Efficient LDO Regulator Using a Negative-R-Assisted Technique

Jung Sik Kim, Khurram Javed, and Jeongjin Roh, *Senior Member, IEEE*

***Abstract*—To mitigate the non-ideal virtual ground at the feedback node of a low dropout (LDO) regulator, this brief presents an LDO with an off-chip capacitor that uses a negative-R assisted technique, which enhances its performance, including load/line regulation and power supply rejection (PSR). This technique enables the LDO to achieve improved performance despite the small size of the pass transistor, resulting in low-power and area-efficient LDO regulators. The proposed negative-R-assisted LDO provides 100 mA, with load regulation of 0.09 mV/mA, line regulation of 6 mV/V, and PSR of -31 dB. The proposed negative-R-assisted LDO was implemented with 150 nm transistors in a 28 nm standard CMOS process with an active area of 4,200 μm^2. The proposed LDO achieves a superior figure-of-merit (FoM) of 13.5 ps (FoM1) and 0.057 ps·mm^2 (FoM2).**

***Index Terms*—Low-power, area-efficient, low dropout (LDO) regulator, negative-R-assisted LDO, power management IC (PMIC).**

I. Introduction

BATTERY-OPERATED applications, such as application processor (AP), camera, and memory, require multiple DC supplies to power various sub-blocks. Particularly, portable mobile devices require multiple low-dropout (LDO) regulators in their power management IC (PMIC) unit. For example, the AP PMIC typically requires more than 30 LDOs, and the camera PMIC may require 18 LDOs [1]. Consequently, the total number of LDOs in PMICs can reach up to 80, thus significantly increasing the silicon area requirements.

Reducing the size of the pass transistor (M_{PT}) is a significant challenge in designing area-efficient LDOs as the loop gain of LDOs reduces significantly with a reduction in the size of M_{PT}, which results in its operation in the deep triode region under heavy load conditions. This reduced loop gain can result in the deterioration of the regulation performance of the LDO, thus necessitating a loop gain compensation.

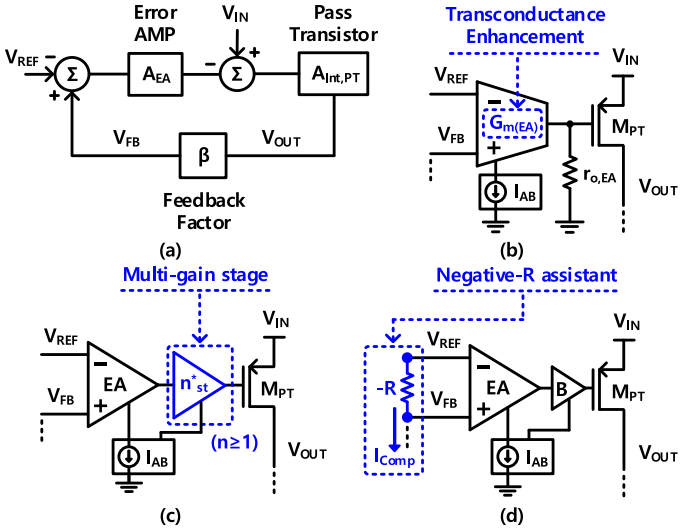

Fig. 1. (a) Concept of the negative feedback in LDO. Conventional loop gain improvement techniques: (b) transconductance enhancement, (c) multi-gain stage, and (d) the proposed negative-R assistant.

The LDO feedback conceptual block for the analysis of the regulation performance is shown in Fig. 1(a) [2]. If a well-designed negative feedback system is used, the V_{OUT} and V_{REF} can be defined as shown in Equation (1),

$$V_{OUT} \simeq \frac{1}{\beta} V_{REF}, \ \beta T(s) >> 1 \tag{1}$$

where T(s) and β are the error amplifier's (EA) gain (A_{EA}) multiplied by the M_{PT}'s intrinsic gain ($A_{Int,PT}$) and feedback ratio. Equation (1) indicates that a sufficient loop gain is essential, which necessitates a high A_{EA} and a significantly large M_{PT}.

As shown in Fig. 1, most low-quiescent current LDOs employ adaptive biasing (I_{AB}) to prevent excessive quiescent current consumption. As shown in Fig. 1(b) and (c), conventional loop gain enhancement techniques for enhancing loop gain are primarily classified into two types [3], [4], [5], [6], [7], [8], [9].

The first technique involves the enhancement of the transconductance, which results in an increase in the loop gain and bandwidth. For example, previous studies [3], [4], [5]

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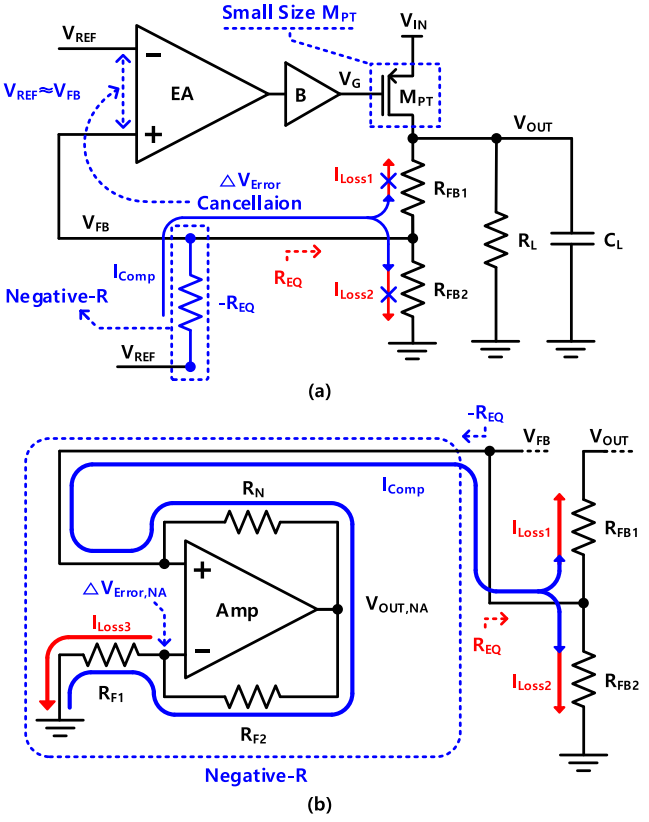

Fig. 2. (a) Conceptional block diagram of the negative-R-assisted LDO. (b) Low frequency, small signal model: a negative resistance circuit.

have employed the internal positive feedback active load. However, the embedment of an additional nonlinear loop during a transient event results in an increase in the complexity of the loop stability. Moreover, increasing the transconductance requires more quiescent current.

The second technique is the multi-gain stage technique [6], [7], [8], [9], and it involves the use of one or more small-gain stages to increase the loop gain. However, multi-gain stages require a large quiescent current to maintain the high frequency of their internal non-dominant poles and excessive compensation capacitors.

As shown in Fig. 1(d), the technique proposed in this brief employs a negative resistance circuit in the feedback path to mitigate the non-ideal virtual ground (ΔV_{Error}) in LDO. This increases the loop gain, resulting in simultaneous improvement in the load regulation, line regulation, and power supply rejection (PSR) performance, even with a small M_{PT}.

II. Design of a Negative-R Assisted LDO Regulator

As shown in Fig. 2(a), most small-area LDO regulators suffer from a ΔV_{Error} because of an insufficient loop gain, resulting in I_{Loss1} and I_{Loss2} through the feedback resistors R_{FB1} and R_{FB2}, respectively [10]. Under heavy load conditions, the loop gain further degrades as the M_{PT} enters the deep triode region, thus degrading the load/line regulation and PSR performance. To overcome the above-mentioned ΔV_{Error}, this brief proposes a negative-R-assisted LDO.

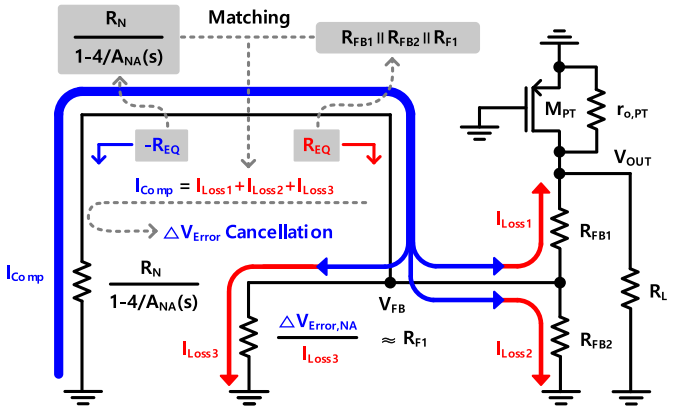

Fig. 3. Low-frequency, small-signal model: ΔV_{Error} cancellation model.

A. Negative-R Assistant Implementation

As shown in Fig. 2(a), when a negative resistance ($-R_{EQ}$) is applied at the feedback node (V_{FB}), a compensation current (I_{Comp}) is generated through the negative resistance to compensate for I_{Loss1} and I_{Loss2}. This can make the virtual ground ideal ($\Delta V_{Error} \simeq 0$).

The small signal model of the negative-R circuit applied to the proposed LDO is shown in Fig. 2(b), which is implemented with an amplifier, R_{F1}, R_{F2}, and R_N [10]. Because the amplifier operates in a non-inverting configuration, the output voltage ($V_{OUT,NA}$) of the negative-R amplifier is defined by Equation (2) [11],

$$V_{OUT,NA} = \left(1 + \frac{R_{F2}}{R_{F1}}\right)\left[1 - \left(1 + \frac{R_{F2}}{R_{F1}}\right)\frac{1}{A_{NA}(s)}\right]V_{FB} \quad (2)$$

where $A_{NA}(s)$ is the loop gain of the negative-R amplifier. I_{Comp} flows through the R_N, which can be calculated as

$$I_{Comp} = \frac{V_{FB} - V_{OUT,NA}}{R_N}. \quad (3)$$

In Equation (3), if R_{F1} and R_{F2} have the same value, the equivalent resistance can be derived as

$$-R_{EQ} = \frac{R_N}{1 - 4/A_{NA}(s)}. \quad (4)$$

Equation (4) indicates that the value of $-R_{EQ}$ can be controlled by the R_N; thus, an appropriate value for the R_N should be selected to implement the negative-R assistance. However, as shown in Fig. 2(b), the negative-R amplifier also suffers from a non-ideal virtual ground ($\Delta V_{Error,NA}$) because of the finite loop gain, resulting in I_{Loss3} at the negative feedback node of the amplifier. Therefore, the I_{Comp} should also compensate for I_{Loss3}, indicating that the I_{Comp} for canceling the ΔV_{Error} should be larger than the sum of I_{Loss1} and I_{Loss2}. Accordingly, R_N should be less than $R_{FB1} \| R_{FB2}$.

The small signal model of the ΔV_{Error} cancellation for the estimation of the total current loss is shown in Fig. 3. The total current loss is defined as the sum of I_{Loss1}, I_{Loss2}, and I_{Loss3}. In Fig. 3, $r_{o,PT}$ and R_L are the M_{PT}'s output resistance and load resistance, respectively. Thus, the equivalent resistance (R_{EQ}) can be defined as Equation (5).

$$R_{EQ} = [R_{FB1} + (R_L \| r_{o,PT})] \| R_{FB2} \| R_{F1}. \quad (5)$$

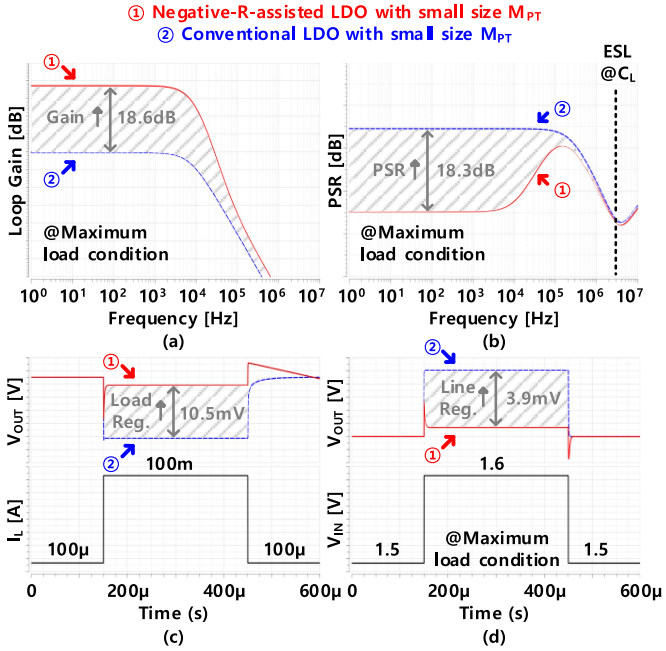

Fig. 4. Simulated results of the negative-R and conventional LDO (a) AC, (b) PSR, (c) load transient, and (d) line transient.

R_{FB1} is relatively larger than the sum of $r_{o,PT}$ and R_L because $r_{o,PT}$ and R_L are inversely proportional to the load current. Therefore, Equation (5) can be expressed as

$$R_{EQ} \simeq R_{FB1} \| R_{FB2} \| R_{F1}. \tag{6}$$

To cancel ΔV_{Error}, matching R_{EQ} and R_N values are required, indicating that an appropriate I_{Comp} value is generated from the AC ground (V_{REF}) to compensate for the total current loss. Thus, the appropriate R_N value to cancel the ΔV_{Error} via the negative-R is:

$$R_N \simeq R_{FB1} \| R_{FB2} \| R_{F1}. \tag{7}$$

In this design, the gain of the negative-R amplifier is 54 dB, the R_{F1} and R_{F2} values are 500 kΩ, R_{FB1} and R_{FB2} values are 2 MΩ, and the R_N is 384 kΩ. Under these design conditions, a loop gain improvement of 18.6 dB is achieved, as shown in Fig. 4(a).

B. Distortion Cancellation Using the Negative-R

As LDO performances are governed by the loop gain, the reduction in the loop gain can result in the simultaneous degradation of LDO performances. Hence, the loop gain is an important parameter affecting the performance of LDOs, including the load/line regulation and PSR [2]. The negative-R assisted technique can compensate for the reduced loop gain, thus enabling improved performance with the small M_{PT}.

For comparison, the simulation results of a conventional LDO and the negative-R-assisted LDO are shown in Fig. 4. Fig. 4(b) demonstrated an improvement of 18.3 dB in the PSR performance of the negative-R-assisted LDO at low frequencies under maximum load current.

Fig. 4(c) shows that improving the loop gain using the negative-R also improves the load regulation performance.

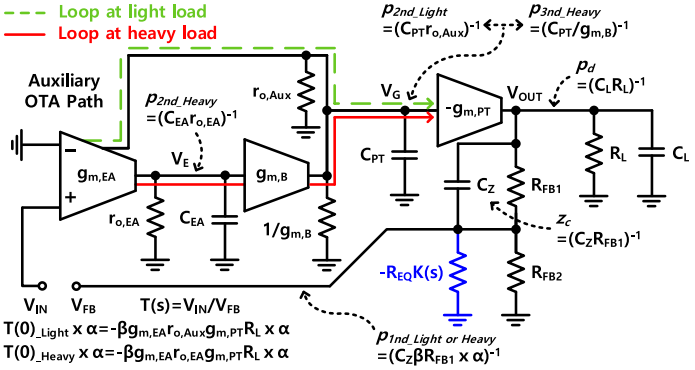

Fig. 5. Small-signal block diagram of the negative-R-assisted LDO.

Compared to the conventional LDO, the LDO with negative R demonstrated an improved load regulation of 10.5 mV.

Improving the PSR at low frequencies can typically enhance the line regulation [2]. The line transient simulation at the maximum load current is shown in Fig. 4(d), where the proposed negative-R-assisted LDO demonstrated an improved line regulation of 3.9 mV compared to the conventional LDO. This improvement was attributed to the increased loop gain, which enhanced the PSR performance through the negative-R assistant. In summary, the proposed LDO exhibited improved load regulation, PSR, and line regulation of 10.5 mV, 18.3 dB, and 3.9 mV, respectively.

C. Stability Analysis

Under light load conditions, the proposed LDO employs an auxiliary operation transconductance amplifier (Aux OTA) instead of the buffer to construct a feedback path, thus effectively reducing the quiescent current. Under heavy load conditions, the transconductance of the buffer increases, thus forming the main control path [12]. Therefore, the transfer function can be defined as Equation (8).

$$T(s) \simeq T(0) \times \alpha \times \frac{(1+\frac{s}{z_c})}{(1+\frac{s}{p_d})(1+\frac{s}{p_{1nd}})(1+\frac{s}{p_{2nd}})} \tag{8}$$

In Fig. 5, g_m, r, and C are the transconductance, small-signal output resistance, and lumped output parasitic capacitance of the EA, buffer, and M_{PT} stage, respectively; C_L, C_Z, and α represent the off-chip capacitor, frequency compensation capacitor, and gain improvement factor achieved by the negative-R assistant, respectively. In Equation (8), the dominant pole is $p_d = (C_L R_L)^{-1}$ because of the large C_L at the V_{OUT} node, and there are two non-dominant poles (p_{1nd} and p_{2nd}) and the frequency compensation zero, z_c.

The first non-dominant pole is $p_{1nd} = (C_Z \beta R_{FB1} \times \alpha)^{-1}$, as the equivalent resistance at the V_{FB} node increases owing to the parallel connection of the negative resistance and feedback resistance ($-R_{EQ} \| R_{EQ}$). This increase is expressed as a multiplication of α, and p_{1nd} is compensated by $z_c = (C_Z R_{FB1})^{-1}$. Under light load conditions, the second non-dominant pole is $p_{2nd} = (C_{PT} r_{o,AUX})^{-1}$, while under heavy load conditions, it is $(C_{EA} r_{o,EA})^{-1}$. The third non-dominant pole is $p_{3nd} = (C_{PT}/g_{m,B})^{-1}$ under heavy load conditions, and can be excluded from Equation (8) because it is greater than the bandwidth owing to the low output resistance of the buffer.

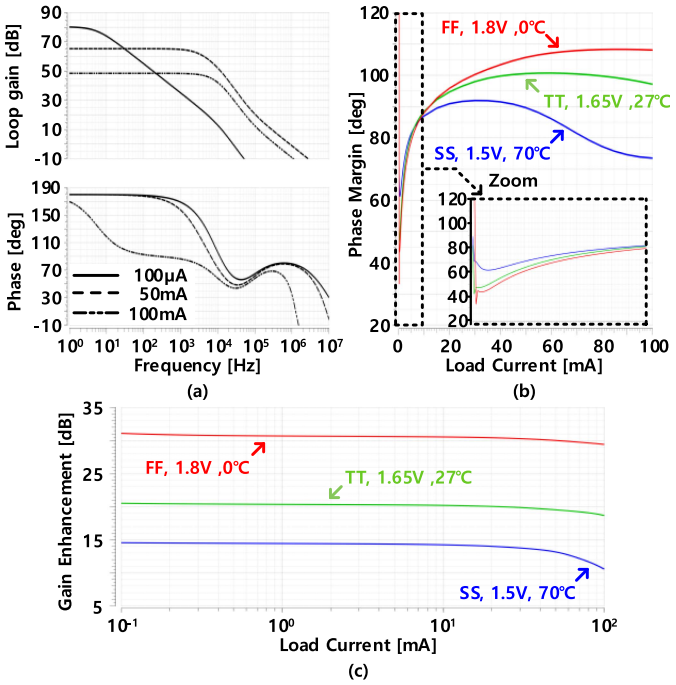

Fig. 6. (a) AC simulation results of the proposed LDO. (b) Phase margin, and (c) Loop gain enhancement magnitude with load current versus process corner, input voltage, and temperature variation.

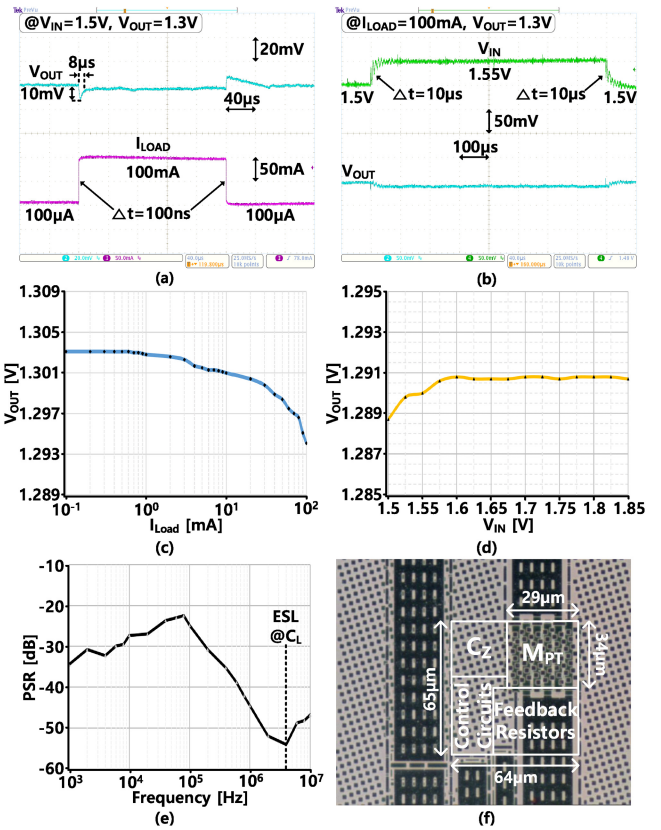

Fig. 7. Measured (a) load transient, (b) line transient, (c) load regulation, (d) line regulation, (e) PSR of the LDO at a load current of 100 mA, and (f) microchip graph of the proposed LDO.

The negative-R assisted technique increases the loop gain, which is represented by α in Equation (8). The value of α is determined by the resistive matching between $-R_{EQ}$ and R_{EQ}, as defined in Equation (9) [13].

$$\alpha = \frac{K(s)}{K(s) - 1} \tag{9}$$

$K(s) = -R_{EQ} / R_{EQ}$ is the matching coefficient between $-R_{EQ}$ and R_{EQ}. Perfect matching ($K(s) = 1$) causes infinite loop gain. In this design, $K(0) = 1.1$; however, as $A_{NA}(s)$ decreases at the 3 dB frequency (10 kHz), $K(s)$ increases.

Fig. 6(a) shows the AC simulation results according to the load current. Under heavy load conditions, the LDO achieved a DC loop gain of 48.5 dB and a bandwidth of 357 kHz; and the DC loop gain and bandwidth under light load conditions are 80.2 dB and 25.8 kHz, respectively.

As shown in Fig. 6(b), AC simulations with process corner, input voltage, and temperature (PVT) variation show a worst-case phase margin of 33.2°, indicating the stability of the negative-R-assisted LDO. Additionally, Fig. 6(c) demonstrates loop gain enhancement with PVT variations, resulting in an improvement range of 11 to 29 dB under the maximum load conditions. The deterioration in the load regulation worsened the gain enhancement by increasing the $\Delta V_{Error,NA}$, particularly under the worst-case conditions (SS, 1.5V, 70°) with a smaller M_{PT}, and minimizing the EA's output voltage (130mV).

III. Measurement Results

The proposed negative-R-assisted LDO was implemented with 150 nm transistors in a 28 nm standard CMOS process. Fig. 7(a) shows the change in the load current from 100 μA to 100 mA at an edge time of 100 ns. The measured undershoot and overshoot voltages were 10 and 8 mV, respectively. The measured line transient response with a change in the input voltage from 1.5 to 1.55 V at an edge time of 10 μs under maximum load conditions is shown in Fig. 7(b).

Fig. 7(c) shows the measured load regulation performance of the proposed negative-R-assisted LDO with a change in the load current from 100 μA to 100 mA. The proposed negative-R-assisted LDO achieved a load regulation of 0.09 mV/mA at a measured V_{OUT} variance of 9 mV. The line regulation results of the proposed negative-R assisted LDO are shown in Fig. 7(d). At the maximum load current, the V_{IN} changed from 1.5 to 1.85 V, and the variance of V_{OUT} was 2.1 mV. Additionally, the proposed negative-R-assisted LDO achieved a line regulation of 6 mV/V.

The obtained PSR measurement at a 100 mA load current is shown in Fig. 7(e), indicating that the proposed negative-R-assisted LDO regulator achieved a PSR of -31 dB at low frequencies. Fig. 7(f) shows a microchip graph of the proposed LDO with an active area occupation of 0.0042 mm^2.

The transistor-level implementation of the proposed LDO is shown in Fig. 8. The OTA and the structure of the designed circuit, which includes the Aux OTA, are adopted from [12].

The performance of the negative-R-assisted LDO is summarized and compared to those of previously reported state-of-the-art capacitor-type LDOs in Table I. The proposed LDO has a quiescent current of 1.6 μA and an area of 4,200 μm^2. In addition, the FoM1 and FoM2 values of the proposed LDO

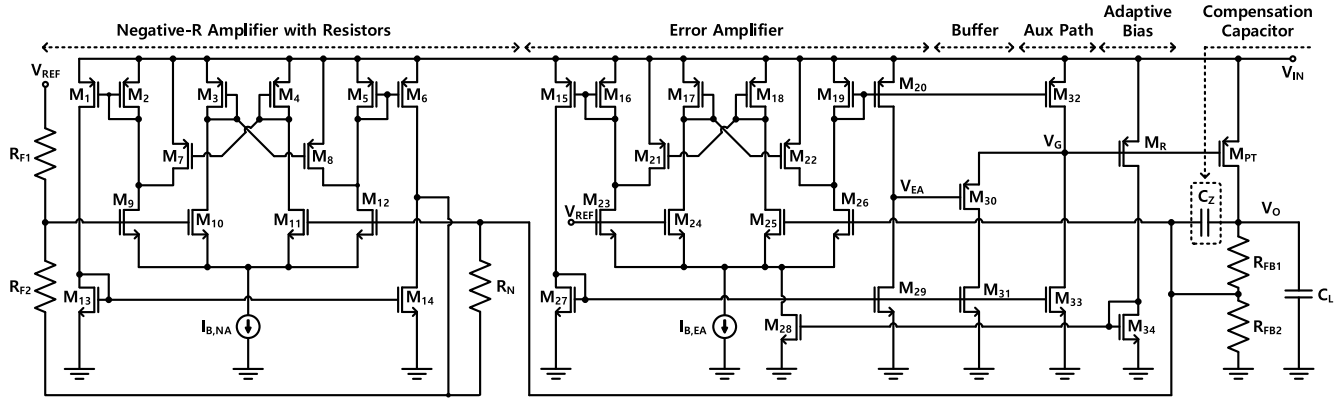

Fig. 8. Transistor-level implementation of the negative-R-assisted LDO.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[3] 2017	[4] 2020	[5] 2022	[6] 2019	[7] 2020	[8] 2021	[9] 2022	This Work
Technology [nm]	180	180	180	180	180	180	180	150
Minimum V_{IN} [V]	1.4	1.8	1.8	3.3	1.4	1.8	1.8	1.5
Nominal V_O [V]	1.2	1.6	1.6	2.8	1.2	1.65	1.6	1.3
Area [μm^2]	28,500	29,700	88,105	181,300	17,000	11,900	29,600	4,200
Maximum I_L [mA]	50	50	200	100	150	50	50	100
C_L [μF]	1.0	1.0	1.0	0.1	4.7	4.7	1.0	4.7
Minimum I_q [μA]	1.6	1.3	48	21	13.5	11	2.5	1.6
ΔV_O [mV]	29	26.25	76	810*	37	–	30.75	18
Load Reg. [mV/mA]	0.1	0.32	0.211	0.035	0.075	–	0.41	0.09
Line Reg. [mV/V]	5.5	7.2†	2.025†	5.67	7.785†	4†	36.8†	6†
PSR [dB] (@Hz)	-30 (10M)	-21*† (10K)	-47*† (1k)	–	-30*† (10K)	-37* (100K)	-36*† (10K)	-31† (2K)
FoM1 [ps]	18.5	13.65	91.2	170.1	104	207	30.75	13.5
FoM2 [ps×mm^2]	0.527	0.405	8.035	30.84	1.768	2.463	0.91	0.057

FoM1 $= C_O \times \Delta V_O \times {I_q/I_L}^2$ [14], FoM2 = FoM1× Area [15]
* Estimated from measured result graph, † At maximum load condition.

were 13.5 ps and 0.057 ps·mm^2, respectively. Compared to the previously reported capacitor-type LDOs, the proposed LDO occupied a lesser area with the lowest FoM1 and FoM2.

IV. CONCLUSION

To mitigate the non-ideal virtual ground in small-sized LDOs, the negative-R assisted technique was introduced, and its effectiveness was demonstrated through simulation and measurement results. It achieved an active area occupation of 0.0042 mm^2 while handling a load current of 100 mA, along with FoM1 and FoM2 values of 13.5 ps and 0.057 ps·mm^2, respectively. The measurement results, along with the small FoM shown in Table I, verified the low power and area efficiency of the proposed LDOs.

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