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Design of a Folded Cascode Operational Amplifier in a 1.2 Micron Silicon-Carbide CMOS Process

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ABSTRACT

This thesis covers the design of a Folded Cascode CMOS Operational Amplifier (Op-Amp) in Raytheon's 1.2-micron Silicon Carbide (SiC) process. The use of silicon-carbide as a material for integrated circuits (ICs) is gaining popularity due to its ability to function at high temperatures outside the range of typical silicon ICs. The goal of this design was to create an operational amplifier suitable for use in a high temperature analog-to-digital converter application. The amplifier has been designed to have a DC gain of 50dB, a phase margin of 50 degrees, and a bandwidth of 2 MHz. The circuit's application includes input ranging from 0 volts to 8 volts so a PMOS input differential pair was selected to allow the input range down to the VSS rail. The circuit has been designed to work over a temperature range of 25°C to 300°C.

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I. INTRODUCTION

This thesis presents the design, simulation, and layout of a single stage folded cascode CMOS silicon-carbide amplifier. In the next section, a description of the general circuit topology and operation will be provided, followed by some of the deviations from the classical topology that were made for this design. Additionally, it will discuss some of the advantages this topology has over other amplifier circuits. The third and fourth sections discuss the design procedure of the circuit including how some of the circuit specifications were selected, and how the transistor sizes were determined. The fifth and sixth sections cover the simulation of the circuit, and discuss the impacts of process variation. The next section discusses the physical layout of the Circuit, and the final section discusses some conclusions from the design.

II. CIRCUIT TOPOLOGY ANALYSIS

The folded cascode amplifier is a single stage amplifier, which consists of a common source transistor cascoded with a common gate transistor of the opposite polarity. In the operational amplifier implementation of this type of amplifier, a differential pair is used as the input stage to amplifier, acting as the common source portion of the cascade. The drains of the input transistors are then linked to two opposite polarity common gate transistors. The common gate transistors are then connected to an active current source load to complete the circuit. The goal of using this topology is to achieve the simplicity and small size of a single stage amplifier, while achieving the gain of a multi-stage amplifier. By "folding" the cascode over into a pair of opposite polarity transistors, this decreases the required headroom for the circuit, giving the same performance as a typical cascode amplifier, but with a lower required supply voltage. The cascoded transistors in this design serve to increase the output resistance of the circuit, which increases the small signal gain of the amplifier. This is the main benefit of the topology. Since the current mirror's output resistance appears in parallel with the output resistance of the amplifying portion of the circuit, it is important that the current source be cascoded as well, so as not to extinguish all of the benefits that were gained by the cascode in the first place.

Due to the high threshold voltages of the PMOS transistors in this process, some slight modifications were made to the general implementation of this circuit. Instead of connecting the current mirrors at the output of the amplifier in a gate-drain configuration, as is typically done, the gate of the uppermost transistors were connected to the drain of the casocde transistors and the cascode transistors were biased externally. The deeper details of this type of modification can be found in [1]. The final circuit topology was modeled after this modification and is provided in Figure 1.

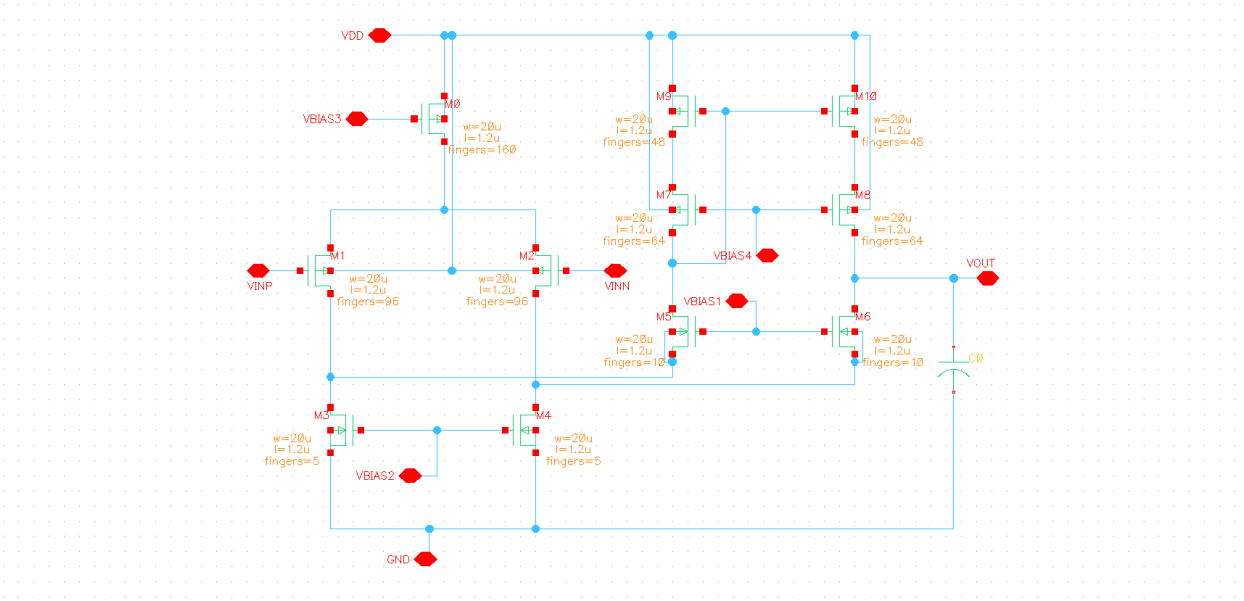

Figure 1: Folded Cascode Op-amp schematic

III. CIRCUIT APPLICATION AND SPECIFICATIONS

The application for this circuit is to be used as a buffer in a high temperature analog to digital converter (ADC). The ADC is being used to convert analog voltages between zero and eight volts coming from a sensor into a digital representation of the voltage. The sampling frequency of the ADC is 100 kHz. This means that the input to the amplifier must be able to respond at this rate as well. Based on this information some specifications were designed for the Op amp. Since the input range for the op-amp is between zero and eight volts, the input common mode range specification was designed to be from zero to ten volts, allowing for a small margin on the high side. Since the input range requirement goes all the way down to the ground rail, the input differential pair will necessarily be made of PMOS transistors. The gain and phase margin of the op-amp were specified to be 50dB of gain at DC and 50 degrees of phase margin. This will ensure the op-amp has enough gain and phase margin to respond quickly and accurately to inputs, without being too aggressive for the single-stage amplifier configuration. The bandwidth was selected to be around 2 MHz, significantly higher than the sampling frequency at 100k. This allows extra

margin as well in case the ADC sample rate is ever increased. The power supply for this application is very limited, so the op-amp must consume a small amount of power. The amount of power budgeted for the op-amp is 15 V at 0.5 mA, or 7.5 mW. Since the load for this amplifier is likely just going to be the next stage in the analog to digital conversion process, the load was selected to be 5 pF. To again help ensure that the op-amp is able to respond quickly enough to the inputs changing, a slew rate of at least 15 V/μs was selected. This spec ensures that the rise and fall times will be quick enough for the 10 μs sampling period. A summary of all of the circuit specifications can be seen in table 1 below.

Table 1: Circuit Design Specifications

Design Specification	Value
DC Gain	50 dB
Phase Margin	50°
Bandwidth	2 MHz
C_{Load}	5 pF
V_{ICMR}	0-10 V
Power Dissipation	7.5 mW
Slew Rate	15 V/μs
Temperature Range	25 °C – 300 °C

IV. DESIGN PROCEDURE

A detailed design procedure for this op-amp is described in [2]. However, some of the main points of the design process will be discussed here.

The first step of the circuit design was to decide the amount of current to use based on the power dissipation and slew rate requirements. For the current range, the slew rate of the circuit provides the lower bound, and the power dissipation will provides the upper bound. Any value in this range can be selected. A handy rule of thumb for the folded cascode design is that the current through the differential input pair should be larger than the output current stage to help ensure maximized gain and low power dissipation, and can be as large as four times [2]. Using these requirements and relationships the current through each transistor can be selected.

To determine the W/L ratio of each of the transistors, either the gain requirements or the input and output range requirements can be used. Each of these requirements are dependent upon the transconductance (g_m) and overdrive voltage (V_{ov}). By selecting the desired g_m or V_{ov}, and using equations 1 and 2 below with the currents calculated previously, the appropriate W/L ratios can be calculated.

$$I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) V_{ov}^2 \tag{1}$$

$$gm = K_n' \left(\frac{W}{L}\right) V_{ov} \tag{2}$$

Since the input range and output range equations are typically simpler it is preferred to use those specifications to design the W/L, and then return afterwards to make sure the gain requirements are met.

If after calculating the W/L ratios for the input and output range, the gain and phase margin requirements are not met, there are some modifications that the designer can make. To increase the gain of the circuit, the size of the input differential pair transistors can be increased. This will increase the gain of the circuit, but also decreases the phase margin of the circuit. In order to increase the phase margin of the circuit, a compensation capacitor can be placed at the output node of the amplifier. The increased capacitance will improve the phase margin, however this will trade away some of the bandwidth. Also, the increased capacitance at the output will affect the slew rate of the amplifier. To correct for the slew rate degradation, the designer can increase the current, which will speed up the circuit but increase power dissipation. If the option to change the currents is chosen the designer must iterate back through the first stages of the design again and resize some of the transistors. Another thing that could be done is to trade off some of the input/output range for more gain by decreasing the size of the current mirror transistors, thus increasing the output resistance of the circuit. Using these design parameters all of the major specifications can be juggled and shifted until the proper balance is found.

V. DESIGN AND SIMULATION RESULTS

Using the methods above, a first pass through of the transistor sizing was done. The equations used in the transistor size calculations, however, give only approximate values for the parameters and are based on silicon transistors. Using a simulator with silicon-carbide based transistor models provides a much more accurate description of the circuit behavior, therefore a second pass of the transistor sizing was performed using the Cadence Virtuoso software and the hSpice simulator. The models used for the first found of simulation are the 300 °C TT RAYSIC models. This sets the simulator to model the transistor behavior after Typical NMOS and Typical PMOS (TT) behavior at 300 °C using the Raytheon silicon-carbide (RAYSIC) kit. These settings help guarantee the simulation results are as accurate as possible by attempting to match the application the circuit will be used in.

By using the simulator to measure the DC operating point of each transistor, the second pass of transistor sizing was finished. The simulator used for this project only contained a few models for the W/L ratio to be selected from. The ratio selected for this design was 20/1.2 and the rest of the sizing was done by including multiple fingers of transistors. The results shown in Table 2 show the W/L ratio as a multiple of the standard 20/1.2 ratio. The transistor names are matched to those in the schematic of Figure 1.

Table 2: Transistor Sizes

Transistor Name	W/L Ratio
M0	160
M1, M2	48
M3, M4	5

M5, M6	10
M7, M8	64
M9, M10	48

The next task in the design was to verify each of the specifications using the simulator. The first simulation was the AC analysis. The goal of the AC analysis is to create and examine the Bode plots for the DC gain, phase margin, and bandwidth of the amplifier. These plots are shown in Figure 2 below.

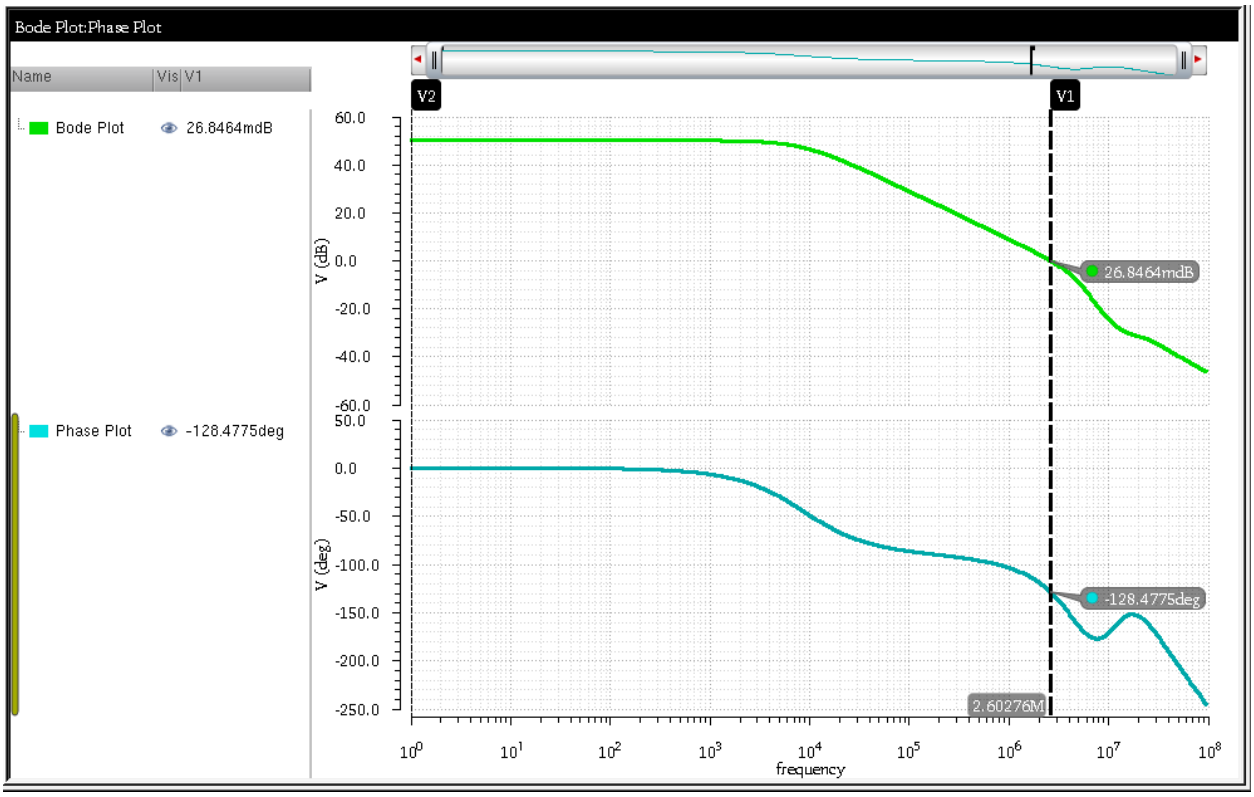

Figure 2: Amplifier AC Analysis, Bode and Phase Plots

The plot shows DC gain is approximately 50 dB, the phase margin is about 51.5 degrees, and the bandwidth is approximately 2.6 MHz.

The next simulation was to test the input common mode range of the amplifier (VICMR). For this test the amplifier was set up in the unity gain configuration and the input was swept across the power supply range. The input common mode range is the range of values in the graph for which the plot has a linear increasing slope.

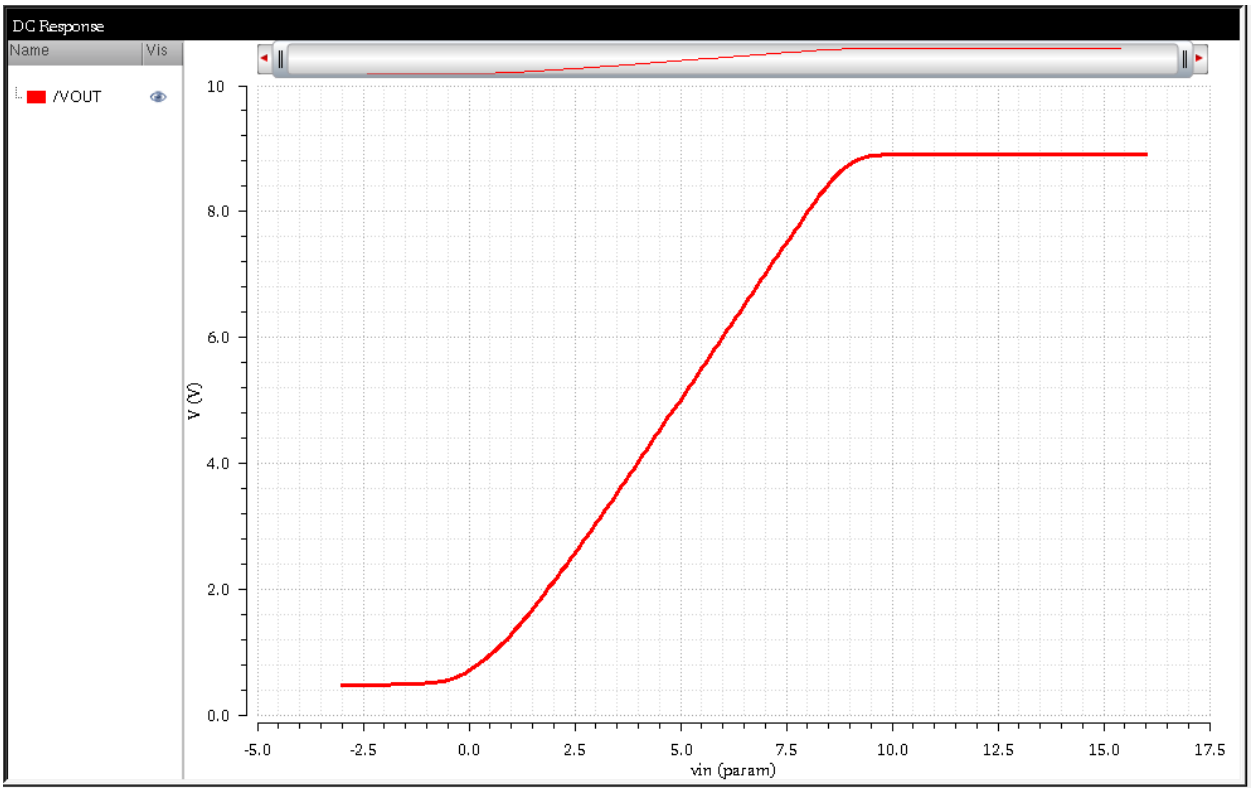

Figure 3: Input Common Mode Range and Output Range

The next simulation was to test the slew rate of the amplifier. For this test the amplifier was again in the unity gain configuration and a large square wave pulse was sent to the input of the amplifier. The slew rate was determined by measuring the slope of the output response. The results from the simulation are shown below.

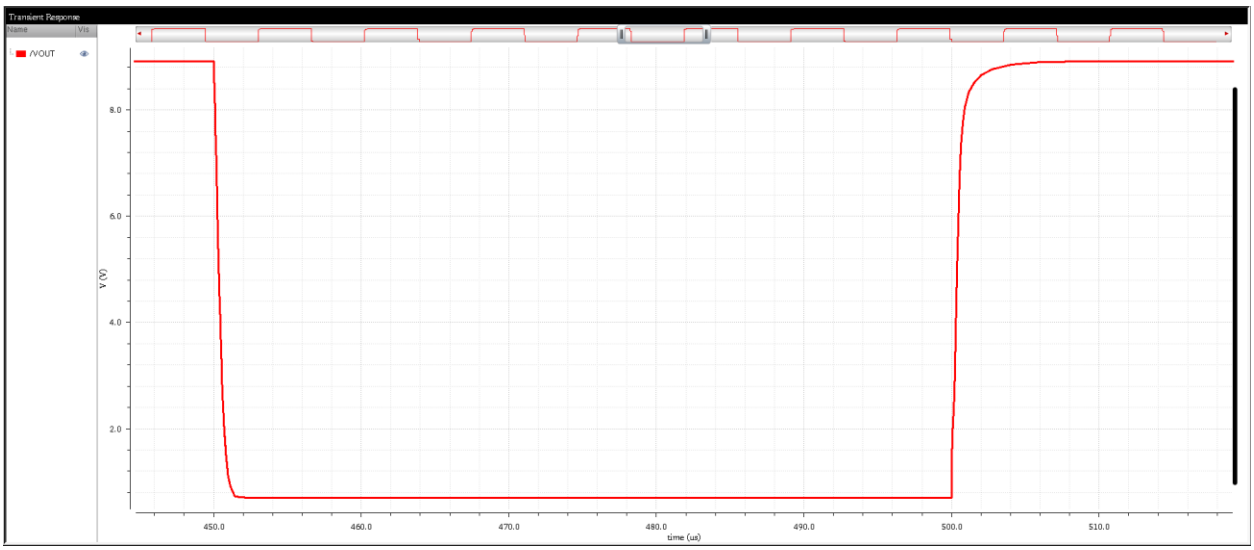

Figure 4: Slew Rate Simulation Results, Rising and Falling Edges

The last simulation that was performed was a transient simulation to verify the circuit output behavior looks normal when amplifying a simple sine wave. For the simulation the amplifier was connected in an open loop configuration and supplied a 1 mV input signal. The resulting output waveform is shown below.

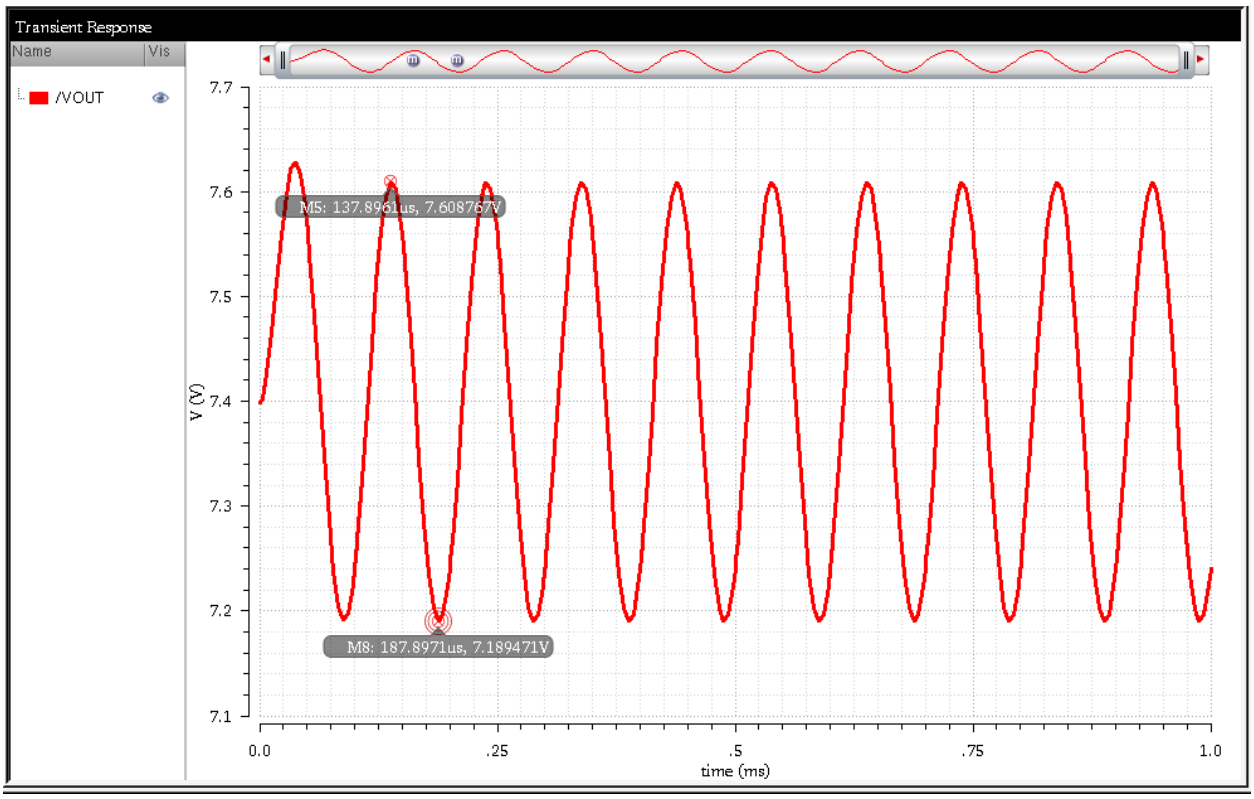

Figure 5: Transient Simulation Results

The power dissipation for the circuit was measured by calculating the DC currents through the tail transistors of the circuit. The power dissipation was measured to be 6.8 mW. A summary of all of the simulation results can be seen in the table below.

Table 3: Simulated Results Table

Design Parameter	Specification	Simulated Value
DC Gain	50	50
Phase Margin	50	51.5
Bandwidth	2	2.6 MHz
Pdiss	7.5 mW	6.8 mW
Cload	5 pF	5 pF
VICMR	0 to 10	-300 mV to 9.25 V
Slew Rate	15 V/µs	15 V/µs

As seen from the table, the simulated results match very well with the design specifications. The bandwidth is slightly higher than the specification and the power dissipation is also slightly better than the spec. Ultimately, some of the high end of the input common mode range was sacrificed to get boost the gain up to the 50 dB mark. However since the circuit application is only using inputs between zero and eight volts, this should not be a big issue.

VI. PROCESS AND TEMPERATURE VARIATION

While the circuit will ideally be operating mostly at the 300 degree TT corner, some extra simulations were ran to ensure the circuit will not fail under variation across temperature and process. For example, while the circuit is heating up to its 300 degree operating point the circuit should still be operational. Also, if process parameters such as threshold voltage differ slightly from the expected models, the circuit should still work mostly the same. The previous simulations were reran on the two other most common process and temperature corners, 300TF and 25TF where "TF" represents a process with typical NMOS transistors and fast PMOS transistors. A summary of the process and temperature variation simulation results is provided in the table below.

Table 4: Process and Temperature Variation Results

Specs	300TF	300TT	25TF
DC Gain	55.8	50	44.5
Phase Margin	38	51.5	40.2
Bandwidth	2 MHz	2.6 MHz	2.03 MHz
Pdiss	8.5 mW	6.8 mW	8.5 mW
Cload	5 pF	5 pF	5 pF
VICMR	0.8 V to 12 V	-300 mV to 9.25 V	200 mV to 11.4 V
Slew Rate	16 V/µs	15 V/µs	16 V/µs

As a result of the process and temperature variation, most of the specifications stay near the expected values. Some of the specifications actually improve over process and temperature variation. However, a few of the values fall below the range of the specification. Most of the issues

with the specifications changing are due to the volatility of the PMOS threshold voltages in this process, and the static biasing that was used. One way that the performance variation can be minimized across process and temperature changes is to design in an adaptive biasing circuit. Due to time constraints on the project only simple biasing techniques consisting of DC supplies and current mirrors were used. Including a more stable reference like a bandgap or beta multiplier circuit, could greatly improve the performance of the circuit over the other corners.

VII. PHYSICAL DESIGN

The next phase of the design following the simulations was the physical layout of the circuit. The layout of the circuit was designed based on a few different factors. The first is that the circuit layout should be compact to minimize parasitic resistance, inductance and capacitance in the circuit. Also a smaller layout allows for more circuits to be placed on a single chip. The second layout factor is transistor matching. For circuits which involve transistors in configurations like a differential amplifier, or current mirror, transistor matching is key to proper functionality. This is mainly achieved by using common centroid layout techniques. Common centroid layout techniques split transistors up into several different transistors in different locations on the chip and connect them in parallel to get the same effect as the single larger transistor. By intermingling two transistors in the same layout area, random process variation can be expected to have a minimized effect, because any variation should effect both transistors in the same way. With these two factors in mind, the layout for the amplifier circuit was designed and the final layout can be seen below in Figure 6.

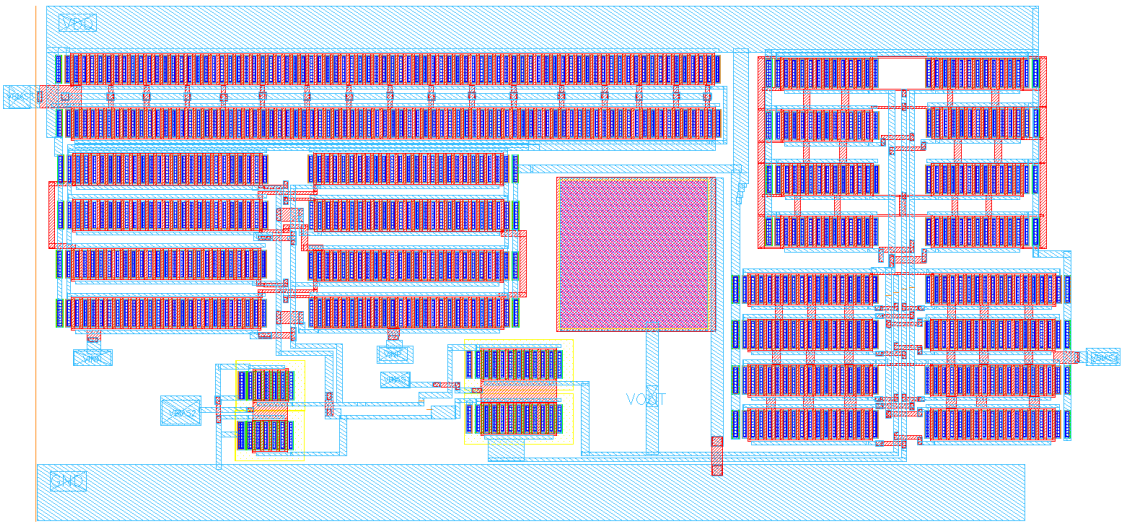

Figure 6: Physical Circuit Layout

The dimensions of the final layout are approximately 800 by 400 µm.

After the layout was complete there were several checks that had to be completed before the circuit could be considered ready for manufacture. The first check is the Design Rules Check (DRC). The DRC ensures that the spacing of each of the components is large enough that they can be properly manufactured. The second check that has to be performed is the Layout Versus Schematic (LVS) check. The LVS check verifies that the circuit layout matches all of the electrical connections that are in the schematic. The amplifier circuit passed both of these checks and the results of the two checks are shown below in Figures 7 and 8. The passing of these checks means that this circuit is now ready for manufacture.

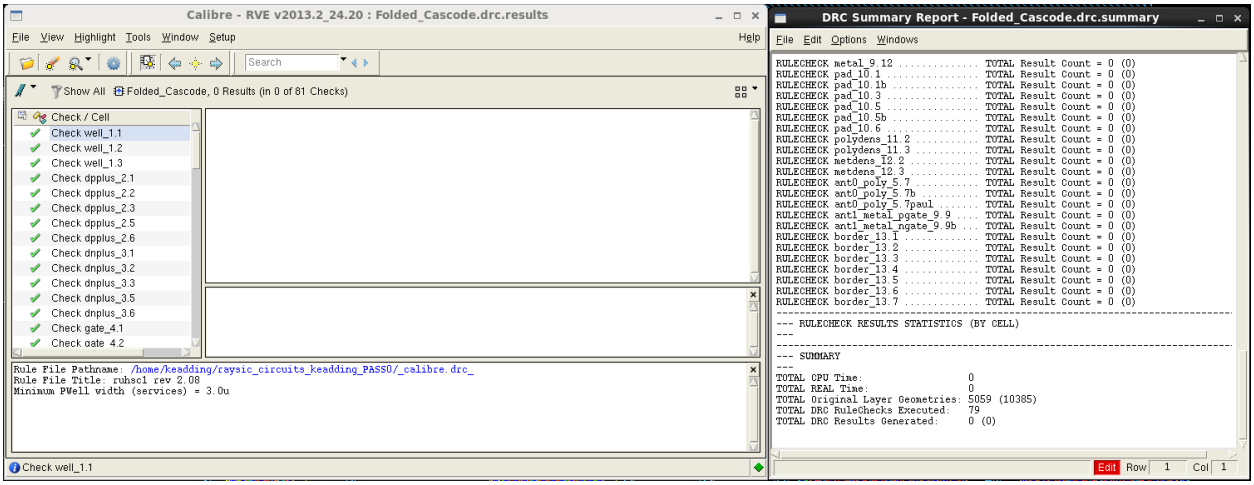

Figure 7: Successful DRC Check Results

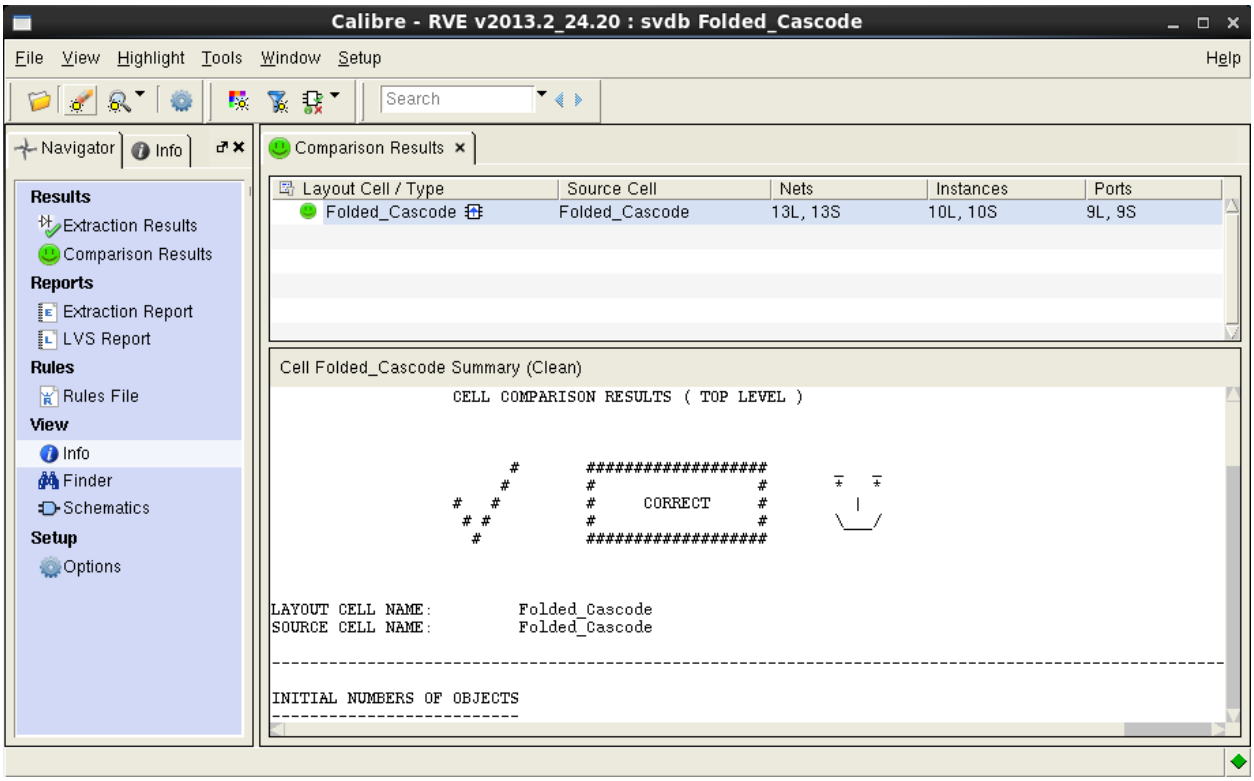

Figure 8: Successful LVS Check Results

VIII. CONCLUSIONS AND FUTURE WORK

The results of this work is a completed folded cascade operational amplifier circuit in a 1.2 micron silicon-carbide CMOS process. The amplifier design was based on the specifications of the high temperature DAC system that was being designed along-side this project. The main takeaways from the design phase were learning to manage the design tradeoffs of the circuit, and how modifying different parts of the circuit change the different performance parameters. In the simulation phase the circuit was shown to function properly under the tested conditions. The simulations were designed to match the system application as well as possible. In the layout phase of the design, common centroid techniques were used to increase transistor matching and make the circuit resistant to process variation. The circuit passed all tests and is ready for fabrication.

Due to time restraints of this project, the circuit design has only been executed up until the layout portion discussed in the previous section. In the future, the circuit can be sent to be manufactured, and tested to obtain real experimental values for the circuit operating specifications. Since the amplifier was only designed to drive the gate of the next stage of the DAC system, measured performance on a bench or probe station may vary from simulation results due to extraneous parasitics. However, in a system fabricated all on the same die, the circuit should perform well.

APPENDIX A: References

[1]Plett Calvin, PMOS Input Folded Cascode, Ottawa Ontario, Canada: Carleton University, http://www.doe.carleton.ca/~cp/analog/foldpmos.pdf

[2] Smith Sedra, Microelectronic Circuits, 6th ed. New York, United States of America: Oxford University Press, 2006