A new LDO regulator with adaptive PSR improvement under wide load current range and fast load transient response

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***Abstract*— This paper presents a novel off-chip capacitor-less LDO with high PSR from 40µA to 45mA load current range. Changing the load current in conventional LDOs causes a variation in the output resistance of the LDO and moves the pole located at the pass transistor's gate terminal. These changes result in the PSR degradation at some load current ranges, in such a way the LDO cannot satisfy the required PSR at the whole load current range. The proposed LDO provides an adaptive feed-forward path to improve the PSR at the entire load current ranges. The transfer function of the proposed feed-forward path has a zero with a specific gain, that is skillfully shifted by the amount of output resistance and the pole positioned at the gate terminal of the pass transistor. This method leads to enhancing PSR across the entire load current spectrum. According to simulation findings for the suggested LDO in TSMC 180 nm CMOS technology, the output PSR reaches -60 dB at 13 kHz across the entire load current range. The proposed LDO operates without requiring an external off-chip capacitor, exhibiting a quiescent current of 900nA and a phase margin of 54 degrees within an input voltage range of 1.8 to 2.3 volts.**

Keywords— Adaptive feed-forward path, capacitor-less LDO, fast transient, load current variation, low drop-out (LDO) regulator, power supply rejection (PSR), Zero replacement.

I. INTRODUCTION

Modern electronic devices integrate functional blocks into the same chip. To reduce energy usage, it's crucial for every block to function at its most efficient supply voltage [1]. Nonetheless, producing distinct supply voltages for each unit via DC/DC converters proves impractical. Consequently, on-chip LDOs (low dropout regulators) are commonly employed to produce the necessary voltages [2].

LDOs can be divided into two main categories: those that utilize an external capacitor and those that are fully integrated (capacitor-less) [3]–[5]. LDOs that utilize an external capacitor exhibit minimal over/undershoot in load transient responses, providing exceptional power supply rejection (PSR) performance, particularly at lower frequencies. While LDOs with an external capacitor offer several benefits, one drawback is that the off-chip capacitor [6]–[8] occupies a considerable amount of space on the printed circuit board. This remains true despite the advancements in circuit miniaturization in modern designs. As a result, on-chip LDOs are highly favored for point-of-load power delivery in applications where area efficiency is crucial. Nevertheless, on-chip LDOs, the power supply rejection (PSR) and transient response experience notable degradation because of the lack of a large capacitor which is located at the output. This poses a main design challenge for fully integrated LDOs [6], [9]. The methods presented in [10]–[12], which rely on the feed-forward path, do not exhibit satisfactory power supply rejection (PSR) throughout the entire range of load current. These methods are optimized for a specific load current and lack adaptability for the entire current range. Also, due to the use of many auxiliary circuits, they have a relatively high power consumption. In the paper, a novel low drop-out voltage regulator is presented to enhance the load transient response and PSR at the entire load current for use in wearable biomedical circuits. The subsequent sections of the paper are delineated as follows. Section II delineates the PSR enhancement technique in the proposed LDO and presents its analysis. Section III presents the analysis of the load transient response and stability of the proposed LDO. Section IV of the paper includes the presentation of Process, Voltage, and Temperature variation (PVT) simulation results and a comparison with prior studies to assess the effectiveness of the proposed LDO. In conclusion, Section V provides a summary and concludes the article.

II. ADAPTIVE PSR IMPROVEMENT METHOD IN THE PROPOSED LDO

According to Fig. 1. the pole situated at the gate terminal of the transistor at the output of the LDO is identified as a key factor contributing to the deterioration of PSR in LDOs. The substantial current flowing through the pass transistor necessitates that designers typically opt for larger dimensions for the output transistor of LDO. The consequence of increasing the dimensions of the transistor is an unintended rise in the level of parasitic capacitances. Also, the output resistance of the transistor at the output of LDO is the second path that causes PSR destruction.

As per references [12] and [13], establishing a forward pathway with suitable amplification from the power supply to the gate terminal of the transistor at the output of LDO helps mitigate the impact of the pole situated within the gate terminal of the transistor at the output of the LDO and the drain-source resistance of the ouput transistor of LDO. The transfer function of the forward path to improve the output Power Supply Rejection (PSR) is outlined as follows:

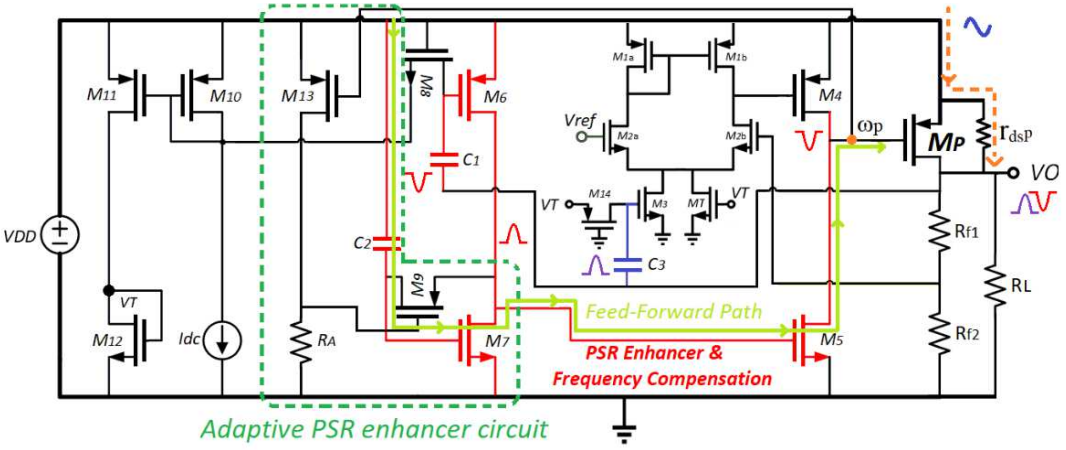

Fig. 1. Proposed LDO

$$\frac{V_g}{V_{dd}}(S) = \underbrace{\left(1+\frac{S}{\omega_z}\right)}_{T1}\underbrace{\left(1+\frac{1}{g_{mp}r_{dsp}}\right)}_{T2} \tag{1}$$

In (1), where V_g represents the gate voltage of the output transistor of the LDO and Vdd denotes the ripples induced on the supply voltage, the first term serves as a zero necessary for mitigating the impact of the pole situated in the gate terminal of the LDO's output transistor. T_1 term signifies the required gain of the feed-forward path aimed at nullifying the effects of the pole and the resistance existing between the drain and source of the outout transisitor of the LDO on the output PSR. In the T_2 term, r_{dsp} and g_{mp} are drain-source resistance and transconductance of the output transistor of LDO, respectively. Since, the resistance between the drain and source of the pass transistor changes with the change of the load current, therefore, the presented methods based on the feed-forward path in [10]–[12] due to the constant gain of the forward path, do not enhance the PSR of LDO uniformly across all load currents. To mitigate this issue and enhance the PSR uniformly throughout the entire load current range, a new LDO with adaptive forward path is proposed in Fig. 1.

The proposed technique utilizes an adaptive feed-forward path, where the gain value of the forward path adjusts according to the variations in load current. This adaptive adjustment aims to enhance the power supply rejection (PSR) uniformly across the entire load current range.

As depicted in Fig. 1, within the forward path, the power supply ripples initially enter the transistor M_7's gate via capacitor C_2. Subsequently, they traverse to transistor M_5 and ultimately reaches the gate terminal of the output transistor of the LDO with an identical phase. Transistor M_9 operates in triode region and its role is to self-bias transistor M_7.

In the proposed method, changes in the resistance R_{M9} cause the gain of the leading path to change. The presented design is implemented in such a way that the R_{M9} changes according to the load current, which results in the improvement of PSR in all load currents.

The expression for the proposed feed-forward path is as follows:

$$A_{FF} = \frac{RC_2S}{RC_2S+1}\times A_{M7}\times A_{M5}$$
$$R = \frac{R_{M9}+(r_{ds6}\,\|\,r_{ds7})}{g_{m7}(r_{ds6}\,\|\,r_{ds7})+1} \tag{2}$$

in which C_2, g_{m7}, and r_{ds6}, r_{ds7} are the input capacitor of the forward path, transconductance of transistor M_7, and the drain-source resistance of transistors M_6 and M_7. Also, A_{M5} and A_{M7} are the gains of transistors M_5 and M_7, respectively. In Eq. (2) the transfer function of the forward path has a zero at the origin (This zero reduces the impact of the pole situated in the gate of the transistor which is located at the output of LDO and helps to improve PSR) and a pole in the frequency of $-1/RC_2S$. Considering that the capacitor C_2 is in the pico-farad range and the resistance R is in the mega-ohm range, so the pole of the feed-forward path is situated at relatively high frequencies and has no effect on the PSR of LDO at low and medium frequencies. R_{M9} is the resistance of transistor M_9 and it is expressed as follows.

$$R_{M9} = \frac{1}{\mu pCox\frac{W}{L}(V_{GS}-V_{TH})} \tag{3}$$

where μpCox, W/L, V_{GS} and V_{TH} are the hole mobility, aspect ratio, gate-source voltage and threshold voltage of the transistor M_9 respectively. According to (2), changing R_{M9} can change the feed-forward path gain. In the proposed LDO depicted in Fig. 1, change of the load current causes a change in the V_{GS} of M_{13}, which consequently results in a change in the current of M_{13} (like a current mirror) and the voltage across R_A. As the gate of M_9 is biased dynamically by the voltage across R_A, the change in the output current of the LDO results in the change of the V_{GS} of M_9 and consequently its resistance (according to (3)). Therefore, according to the explanation given above and with regard to Eq. (2), the variation of load current in the proposed LDO can change R_{M9}, that modulates the gain of forward path. As a result, based on the given explanation and Eq. (2), due to the changes in the gain of the proposed feed-forward path according to the load current, the proposed scheme has a good PSR in all load currents.

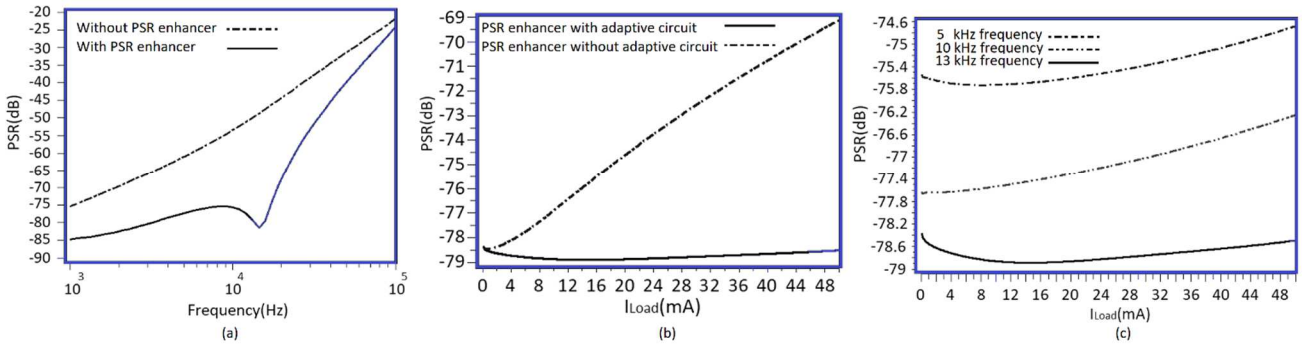

Fig. 2. simulated PSR of the proposed LDO (a) with and without PSR enhancer circuit, (b) using PSR enhancer with and without adaptive circuit, (c) with PSR enhancer circuit at 5kHz, 10kHz, and 13kHz frequencies

Fig. 2(a) depicts the simulated PSR of the proposed LDO with and without PSR enhancer circuit at a load current of 25 mA. Fig. 2(a) clearly demonstrates the improved PSR of the LDO when the proposed enhancer circuit is utilized. Using the PSR enhancer with enabling and disabling adaptive feed-forward path, the PSR of the LDO is depicted for whole load current range in Fig. 2(b). As seen in Fig. 2(b) the PSR of the proposed LDO with adaptive feed-forward path has a flat profile across the entire load current range. In order to show the efficacy of the proposed method at varied frequencies, the PSR of the proposed LDO at 5, 10, and 13 kHz frequencies is depicted in Fig. 2(c).

III. LOAD TRANSIENT RESPONSE AND STABILITY

Another important concern in LDOs is the transient response of output voltage in the presence of abrupt load variation. It is crucial for an LDO to exhibit a fast load transient response, ensuring that abrupt variations in the load current do not considerably impact the output voltage. Due to the substantial parasitic capacitances resulting from the enlarged dimensions of the output transistor of the LDO and the Miller effect within the gate terminal of the output transistor of LDO, the feedback loop's speed is diminished. Thus, enhancing the speed of the feedback loop becomes imperative to mitigate over/undershoot of the output voltage in response to sudden fluctuation in the load current. According to Fig. 1, In the proposed LDO, the tail transistor of the OTA is split into two parallel MOSFET transistors, one of them provides constant bias current (ie. M_T transistor), and another one is used to improve overshoot voltage (ie. M_3 transistor). In the proposed design, when the output voltage increases (i.e. overshoot happens) due to fluctuation in the load current, this alteration in voltage is conveyed via capacitor C_3 to the gate of M_3 within the error amplifier. This provides a sharp increase in the bias current and thus unity gain frequency of the error amplifier to speed up the feedback loop. In this way, the overshoot is suppressed as soon as possible. It is worth mentioning that M_{14} in Fig. 1 operates in the triode region. Also, when the output voltage decreases (i.e., undershoot happens) due to an abrupt alteration in the load current, the voltage variations are conveyed to the gate teminal of the output transistor of LDO via M_6, M_7, and M_5 transistors with appropriate gain, which results in undershoot suppression in the output. The load transient response of the suggested LDO when a step current is applied to the load of the output of LDO from 1mA to 45mA is illustrated in Fig. 3. According to Fig. 3, the maximum over/undershoot voltage is only 115mV.

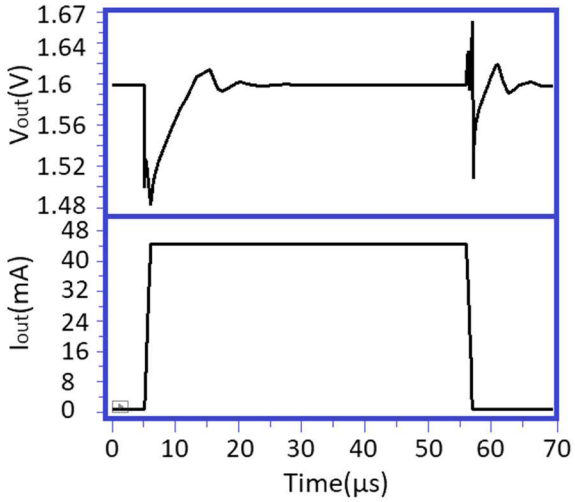

Fig. 3. Load transient response of proposed LDO.

Notably, the pathways established to bolster the load transient response generate multiple zeros in the transfer function of the LDO. These zeros have the potential to mitigate the impact of non-dominant poles in the LDO and ensure loop stability without necessitating an off-chip capacitor. Figure 4 depicts the open-loop frequency response of the proposed LDO without any off-chip capacitor under various load currents. As per Fi. 4, the phase margin of the proposed LDO under worst-case conditions is 54 degrees.

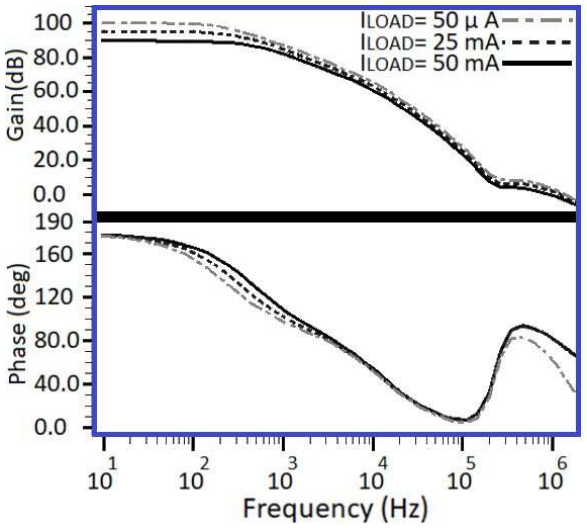

Fig. 4. Open loop frequency response of the LDO

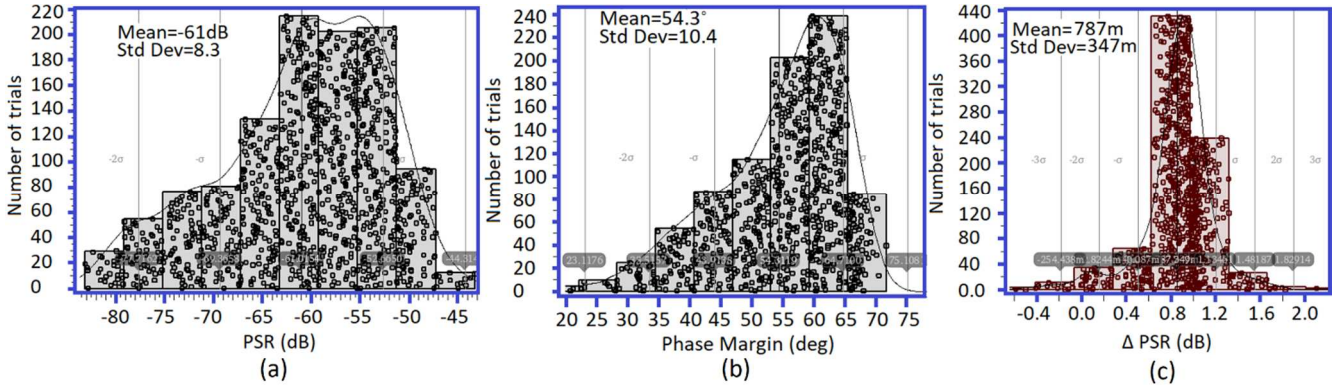

Fig. 5. Monte Carlo simulation results of (a) PSR, (b) phase margin, and (c) PSR variation

I. PVT ANALYSIS, AND COMPARISON

To ensure the operational reliability of the suggested LDO under various process conditions and temperature ranges, essential parameters of the LDO are simulated and outlined in Table I. According to the findings in Table I, the worst-case phase margin and power supply rejection (PSR) of the proposed circuit are 46.4 degrees and -55 dB, respectively, alongside achieving commendable load and line regulation.

In Table II, a comparative evaluation of the LDO's performance against previous studies is provided. To ensure fairness in comparison, a widely recognized figure of merit (FOM) [13] is employed to standardize different parameters. Despite the lack of an off-chip capacitor, the proposed LDO exhibits remarkable PSR across the entire load current spectrum. Table II underscores the promising performance of the proposed LDO in contrast to prior research.

TABLE I
PVT ANALYSIS

Corners	Temp (°C)	Load Regulation (µV/mA)	Over/Undershoot Voltage (mV)	Load Current	PSR(dB) @13kHz	Phase margin (degree)	Line Regulation (µV/V)
TT	-20	1.59	80	50µA	-62	53.2	41.2
				45mA	-61	76.42	51.6
	+85	2.1	117	50µA	-63	65.5	44
				45mA	-61	87.46	52.2
SS	-20	1.61	105	50µA	-57	46.4	35.6
				45mA	-55	72.7	45
	+85	2	125	50µA	-63	59.6	34
				45mA	-60	89.2	44.5
FF	-20	3	122	50µA	-69	57.8	96
				45mA	-68	77.1	110
	+85	4.5	134	50µA	-59	62.7	116
				45mA	-57	79.1	126

TABLE II
COMPARISON TABLE

Parameters	[14]	[15]	[16]	[17]	This work
Technology (nm)	40	250	180	180	180
Max. Load Current (mA)	200	150	25	200	45
V_{out} (V)	1	1-3	1.2V	0.47	1.6
$V_{Drop\text{-}out}$ (mV)	100	240	330	30	200
I_Q (µA)	275	1.24-100	47.01	35.7	0.9
Load Capacitor	0-100pf	1µf-47µf	0-15pf	0-50pf	0-15pf
Line-reg (µV/V)	750	NA	NA	346	125.9
ΔI_{LOAD}(mA)	200	150	25	200mA	44
Load-reg (µV/mA)	19	166	NA	9.5	4.6
PSR (dB)	-66@16kHz	-22@13kHz	-58@13kHz	-60@10kHz	-60@13kHz
ΔVout/rise,fall times (mV/µs)	124/0.1	135/0.9	670/1	890/0.1	134/1
FOM (µV)*	170	1028	12596	159	27.4

$$* FOM = K\left(\frac{\Delta V_{out} I_Q}{\Delta I_L}\right), K = \frac{\Delta t \text{ used in the measurement}}{\text{The smallest } \Delta t \text{ among designs for comparison}}$$

To assess the performance of the LDO under process and fabrication variations, Monte Carlo simulation results of the circuit are presented in Fig. 5. The simulation results in Fig. 5(a) and 5(b) clearly demonstrate the robustness of the proposed LDO in terms of PSR and phase margin against process variations and mismatches. Fig. 5(c) also shows the maximum PSR variations of the LDO over the whole load current range. According to Fig. 5(c) the average of PSR variation is as low as 0.78 dB which shows the robust operation of the technique.

II. CONCLUSION

Power Supply Rejection (PSR) is indeed a crucial parameter in LDOs, especially considering their utilization in the power management block of analog circuits that are susceptible to noise. Enhancing PSR is of utmost significance to ensure a clean and stable power supply, thereby minimizing potential interference and noise that can adversely impact the performance of sensitive analog circuits. Considering that most of the circuits designed with the purpose of improving PSR have high power consumption and also do not operate effectively in all load currents. In the proposed LDO in addition to high PSR in all load current ranges, the presented adaptive feed-forward method has a quiescent current of only 900 nA, and also due to the demand for circuit integration, the external capacitor of the chip has been removed. The proposed LDO exhibits a power supply rejection (PSR) of -60dB at a frequency of 13kHz across a load current range of 50 µA to 45 mA. Additionally, employing a dynamic biasing technique enables the proposed design to limit over/undershoot to a maximum of 134 mV at load currents ranging from 1 mA to 45 mA. It's worth emphasizing that the method utilized to enhance the LDO's transient response, achieved by introducing a zero in its transfer function, yields a phase margin of 50 degrees. Remarkably, this phase margin is attained without requiring an off-chip capacitor and remains effective over a wide load current range spanning from 50 µA to 45 mA.

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