Full on-chip CMOS low-dropout voltage regulator

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Full On-Chip CMOS Low-Dropout Voltage Regulator

Robert J. Milliken, Jose Silva-Martínez, *Senior Member, IEEE*, and Edgar Sánchez-Sinencio, *Fellow, IEEE*

***Abstract*—This paper proposes a solution to the present bulky external capacitor low-dropout (LDO) voltage regulators with an external capacitorless LDO architecture. The large external capacitor used in typical LDOs is removed allowing for greater power system integration for system-on-chip (SoC) applications. A compensation scheme is presented that provides both a fast transient response and full range alternating current (ac) stability from 0- to 50-mA load current even if the output load is as high as 100 pF. The 2.8-V capacitorless LDO voltage regulator with a power supply of 3 V was fabricated in a commercial 0.35-μm CMOS technology, consuming only 65 μA of ground current with a dropout voltage of 200 mV. Experimental results demonstrate that the proposed capacitorless LDO architecture overcomes the typical load transient and ac stability issues encountered in previous architectures.**

***Index Terms*—Analog circuits, capacitorless low dropout (LDO), dc–dc regulator, fast path, LDO voltage regulators, transient compensation.**

I. Introduction

INDUSTRY is pushing towards complete system-on-chip (SoC) design solutions that include power management. The study of power management techniques has increased spectacularly within the last few years corresponding to a vast increase in the use of portable, handheld battery operated devices. Power management seeks to improve the device's power efficiency resulting in prolonged battery life and operating time for the device. A power management system contains several subsystems including linear regulators, switching regulators, and control logic [1]. The control logic changes the attributes of each subsystem; turning the outputs on and off as well as changing the output voltage levels, to optimize the power consumption of the device.

This paper focuses on low-dropout (LDO) voltage regulators. LDO regulators are an essential part of the power management system that provides constant voltage supply rails. They fall into a class of linear voltage regulators with improved power efficiency. Efficiency is improved over conventional linear regulators by replacing the common-drain pass element with a common-source pass element to reduce the minimum required voltage drop across the control device [1]–[5]. Smaller voltage headroom in the pass element results in less power dissipation, making LDO regulators more suitable for low-voltage, on-chip, power management solutions.

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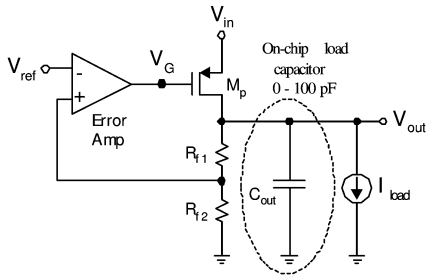

Fig. 1. External capacitorless LDO voltage regulator.

The conventional LDO voltage regulator, for stability requirements, requires a relatively large output capacitor in the single microfarad range. Large microfarad capacitors cannot be realized in current design technologies, thus each LDO regulator needs an external pin for a board mounted output capacitor. To overcome this issue, a capacitorless LDO has been proposed in [2]; that topology is, however, unstable at low currents making it unattractive for real applications. This paper poses to remove the large external capacitor, while guaranteeing stability under all operating conditions. Removing the large off-chip output capacitor also reduces the board real estate and the overall cost of the design and makes it suitable for SoC designs.

Removing the external capacitor requires a sound compensation scheme for both the transient response and the alternating current (ac) stability. Section II describes the characteristics of the uncompensated capacitorless LDO regulator including the pole locations and transient behavior needed to realize the proposed LDO architecture developed in Section III. A compensated 2.8-V, 50-mA capacitorless LDO regulator with a power supply of 3 V was fabricated in a TSMC 0.35-μm CMOS process through the MOSIS educational service with the experimental results shown in Section IV and concluding remarks in Section V.

II. Uncompensated LDO

Most of the conventional LDO performances are greatly affected when the external capacitor is reduced by several orders of magnitude. The absence of a large external output capacitor presents several design challenges both for ac stability and load transient response. Conventional LDO regulators use a large external capacitor to create the dominant pole and to provide an instantaneous charge source during fast load transients [3]–[5]. Thus, a capacitorless LDO requires an internal fast transient path to compensate for the absence of the large external capacitor. To realize the task at hand, the basic capacitorless LDO regulator, shown in Fig. 1, is revisited in the following section.

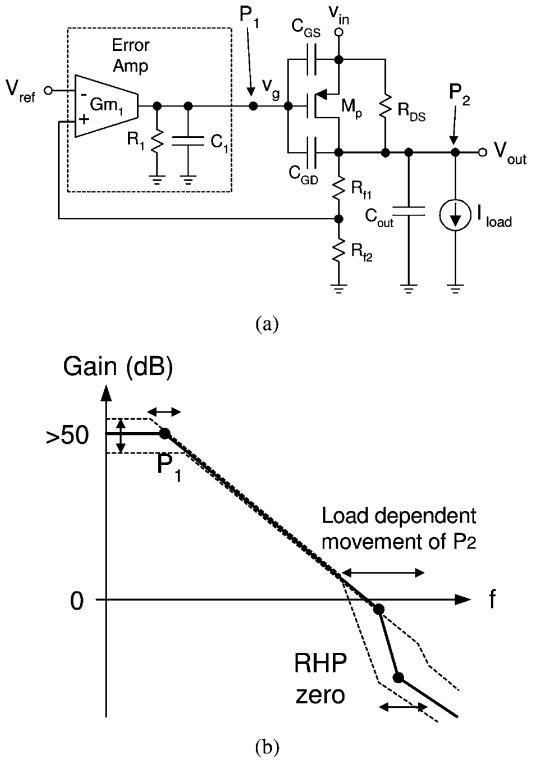

Fig. 2. (a) Equivalent circuit of LDO voltage regulator and (b) pole locations for uncompensated capacitorless LDO voltage regulator; $C_{\rm load}$ around 100 pF.

A. Uncompensated AC Response

One of the most significant side effects in LDOs is stability degradation due to the several poles embedded in the loop. As shown in Fig. 2(a), the uncompensated capacitorless LDO has two major poles: the error amplifier output pole P_1 and the load dependent output pole P_2.

Usually, the standalone error amplifier has at least one internal pole located at relatively high frequency. The equivalent pass transistor input capacitance C_{GS} adds significant capacitance, roughly 60–80 pF, to the error amplifier output impedance. C_{GD} also forms a Miller capacitor which increases the effective input capacitance by the gain of the pass transistor, typically more than -10 V/V. Usually, M_P is very large in order to reduce $V_{\rm DSAT}$, therefore C_{GD} is in the range of tens of picofarads. If the loop is opened, the location of P_1 at the gate of M_p is given by

$$P_1 = \frac{1}{R_1 \cdot (C_1 + C_{GS} + A_{\rm pass} C_{GD})} \tag{1}$$

where $A_{\rm pass}$ is the voltage gain of the pass transistor M_P. Thus, the pole P_1 resides at low frequency, typically several kilohertz since the output resistance of the error amplifier R_1 is relatively large to have enough direct current (dc) loop gain and to eliminate the need of an additional buffer. Since the gain of the pass transistor changes with varying load current, P_1 is therefore load dependent, but usually less sensitive than the output pole P_2. The second pole P_2 is located at the LDO's output, as shown in (2), at the bottom of the page, where Gm_P is the transconductance gain of the pass transistor, $R_{\rm out}$ is the equivalent resistance due to the current loading effects, and $C_{\rm out}$ is the on-chip load capacitance mainly due to the system to be driven; typically, in the range of few picofarads *up to* 100 pF. The pass transistor Gm_P and R_{DS} increases and decreases, respectively, for increasing load current making P_2 very sensitive to the LDO's load conditions. Large load currents push the output pole P_2 to higher frequencies well past P_1. At low currents, the effective load resistance increases significantly; P_2 is pushed to lower frequencies. Unfortunately, R_{DS} can be as large as 30 kΩ leading to a pole's frequency around 50 kHz if $C_{\rm load}$ is in the range of 100 pF and if the effect of C_{GD} is ignored. Due to the unavoidable parasitic poles, loop stability cannot be guaranteed due to the decreased phase margin. Therefore, the uncompensated capacitorless LDO regulator may not be stable especially at the no-load condition. A side effect of C_{GD} is the generation of a right-hand plane (RHP) zero $Z_1 (\approx \mathrm{Gm}_P / C_{GD})$ that reduces loop phase margin; a simplified magnitude plot is shown in Fig. 2(b).

Fig. 3(a) shows the pole movement for the open-loop uncompensated capacitorless LDO regulator for $C_{\rm out} = 100$ pF and two load conditions: 0 and 50 mA. The dc gain is current load dependent and changes by roughly 10 dB between 0 and 50 mA load variations. P_2 varies approximately from 50 kHz to very high frequencies. This large variation in pole movement causes large fluctuations in phase margin. Most of the variations are absorbed between 0 and 1 mA of load current where the pass transistor enters in the subthreshold region, and the output pole movement in this range is very large, as shown in Fig. 3(b). Above 1 mA of load current, usually the LDO regulator becomes stable. It is worth mentioning that P_2 is located at higher frequencies if $C_{\rm load}$ is smaller, leading to better phase margin even at low output currents; thus, only the worst case is analyzed in the following subsections: $C_{\rm load} = 100$ pF.

Conventional LDO regulator analysis usually ignores the feedforward zero due to the pass transistor's C_{GD}. In fact, Table I shows that the feedforward zero falls beyond the typical LDO's open-loop unity gain frequency, and therefore, does not typically surface during the conventional LDO regulator ac analysis. However, it is worth mentioning that this RHP zero Z_1 attracts complex poles to the right-hand side of the S-plane, degrading the loop's stability. The presented external capacitorless LDO regulator requires a gain-bandwidth product of around 500 kHz. At those frequencies, the feedforward zero has noticeable effects at low load currents.

$$P_2 \cong \frac{1}{\left(R_{DS} \| (R_{f1} + R_{f2}) \| R_{\rm out} \| \left(\left(\frac{C_{GD}}{C_1 + C_{GS} + C_{GD}} \right) \frac{1}{\mathrm{Gm}_P} \right) \right) C_{\rm out}} \tag{2}$$

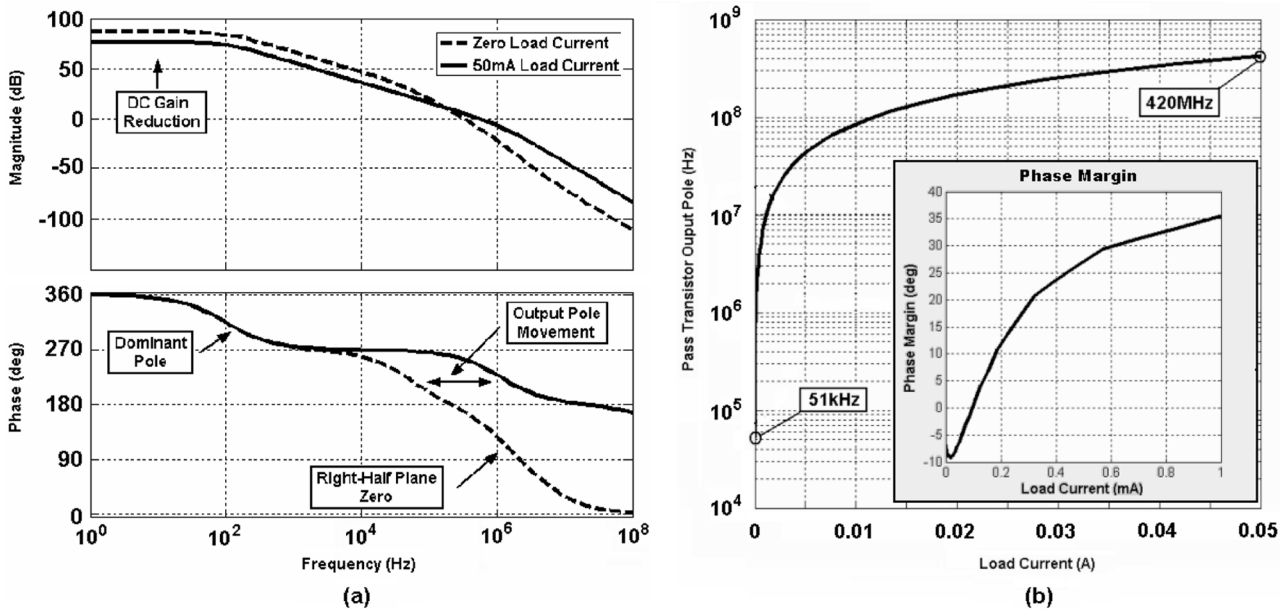

Fig. 3. Uncompensated capacitorless LDO ac response. (a) Bode plot. (b) Output pole frequency and phase margin verse load current.

TABLE I
TYPICAL LDO LOAD-DEPENDENT POLES AND ZEROS

Parameter	Variant	Effect of increased load current	Range (0 ~ 50mA)
P_1	Gm_p, R_{OUT}	DECREASE	~100Hz
P_2 (output)	R_{OUT}	INCREASE	50kHz ~ 420MHz
Z_1	Gm_p	INCREASE	3.4MHz ~ 1GHz
Loop gain	Gm_p, R_{OUT}	DECREASE	80dB ~ 72dB

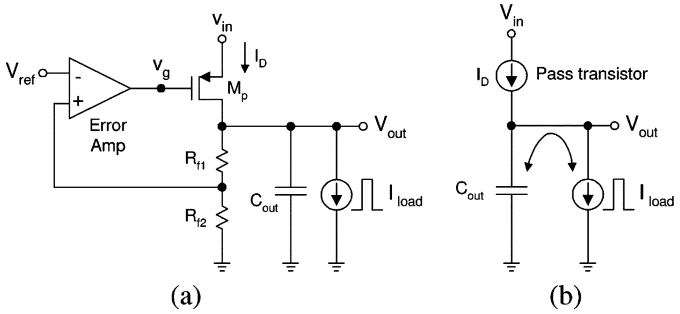

Fig. 4. Effects of limited loop bandwidth under fast load transients. (a) Basic linear regulator. (b) Equivalent circuit for fast load transients.

B. Uncompensated Transient Response

A large external capacitor is used on conventional LDO regulators and linear regulators in general to improve the transient load regulation. The output capacitor $C_{\rm out}$ in the range of nanofarad–microfarad in Fig. 4(a) stores potential energy proportional to the output voltage, and it can deliver the required instantaneous current giving some time for the regulating loop to react and provide the required output current through the pass transistor. For a pulsed output current of 0 to $I_{\rm MAX}$, the transfer of charge from the capacitor to the load corresponds to a voltage drop $\Delta V_{\rm out}$ at the output node. If the LDO's loop is slower than the load transient, the pass transistor gate voltage can be assumed constant throughout the load transient. The circuit diagram of Fig. 4(b) models M_p and its controlling circuitry as a constant current source. The maximum peaking occurs when the initial current of M_p is 0, and the load current suddenly changes from 0 to $I_{\rm max}$; for this case, the maximum output voltage variation $\Delta V_{\rm out}$ is approximately determined by

$$\Delta V_{\rm out} \cong \frac{I_{\rm max} \cdot \Delta t}{C_{\rm out}}. \tag{3}$$

In this expression, Δt is the time required by the loop to react. Thus, the changes in output voltage are inversely proportional to $C_{\rm out}$; the output voltage ripple for a given load transient is reduced by increasing the output capacitance. This side effect becomes more apparent when the load transients are much faster than the loop's gain-bandwidth product, which is usually the case resulting in peak voltages greater than 100 mV.

III. PROPOSED LDO REGULATOR ARCHITECTURE

For the design of an external capacitorless LDO regulator, there are the following two major design considerations: 1) small over/under shoots during transients and 2) the regulator's stability. To solve these issues, a compensating left-hand plane (LHP) zero is introduced.

The properties of the Miller amplifier have been exploited for the stabilization of multistage amplifiers; the downside of that technique is the generation of an RHP zero [6]. Some techniques reporting the elimination of that zero have been used for long time; a technique based on the approach reported in [7] is used here for LDO's stabilization.

A. Transient Response Compensation

In the off-chip capacitorless LDO voltage regulator, the relatively small and load-dependant on-chip output capacitor $C_{\rm out}$ cannot be used to create the dominant pole since the output pole must reside at high frequency. Thus, the dominant pole must be placed within the error amplifier control loop, and transient control signal must propagate through an internal dominant pole before or at the gate of the pass transistor. Overall transistor gate ca-

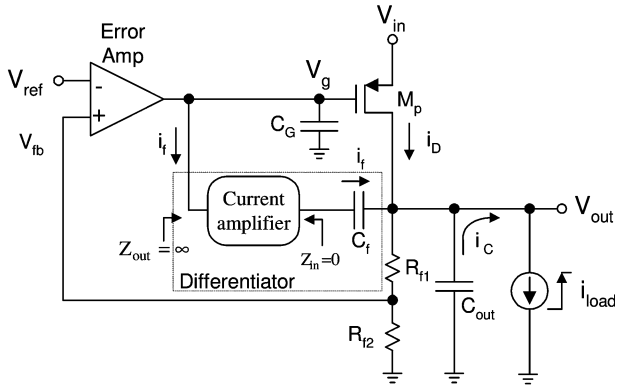

Fig. 5. Proposed LDO topology including a differentiator for fast transient path: basic concept.

pacitance C_G [$\approx C_{GS}+A_{\text{Pass}}C_{GD}+C_1$ in Fig. 2(a)] and output resistance of the error amplifier R_1 act as a current-to-voltage converter, and thus, has an equivalent propagation delay proportional to R_1C_G; the larger the gate capacitance is, the larger the propagation delay will be. When a step output current occurs, the pass transistor can only supply the desired current to the load when the gate voltage V_g moves close enough to its steady state after some time delay t_p. Since the error amplifier's parasitic poles are placed at high frequencies (time delay associated with these poles is small), the speed of the LDO voltage regulator is mainly determined by the pass transistor propagation delay t_p determined by $\text{gm}_{\text{error}}/C_G$, where gm_{error} is the small signal transconductance of the error amplifier. Since the ground current must be minimized in on-chip LDO voltage regulator, the value of gm_{error} is limited; therefore, a circuit is needed that improves the speed of charging the gate of the pass transistor.

An auxiliary fast loop (differentiator), as shown in Fig. 5, compensates for these issues and constitutes the core of the proposed LDO regulator. The differentiator forms the backbone of the architecture providing both a fast transient detector path as well as internal ac compensation. The simplest coupling network might be a unity gain current buffer. C_f senses the changes in the output voltage in the form of a current i_f. The current is then injected into pass transistor gate capacitance by means of the coupling network. The compensating circuitry splits the poles, similarly to the regular Miller compensating scheme, and improves loop speed at the same time. Assuming that load current step ΔI_{LOAD} is applied to the LDO, an output ripple ΔV_{OUT} is generated; the current flowing trough C_f is extracted from C_g until the point in which the M_P's drain current compensates ΔI_{LOAD} and allows V_{out} to return back to its steady state. The amount of required coupling capacitance to minimize the output ripple can be analyzed using the circuit in Fig. 5. If the current flowing through R_{f1} and R_{f2} is ignored, the gate variation of the pass transistor to compensate for ΔI_{LOAD} corresponds to

$$\Delta I_{\text{LOAD}} = (\Delta V_g)\text{gm}_p \cong \left(\frac{C_f \Delta V_{\text{OUT}}}{C_g}\right)\text{gm}_p. \qquad (4)$$

More detailed analysis shows that this is a pessimistic case since both the output current of the error amplifier and C_{gd} increase the amount of compensating current injected into C_G; C_{out} also helps in reducing the output ripple.

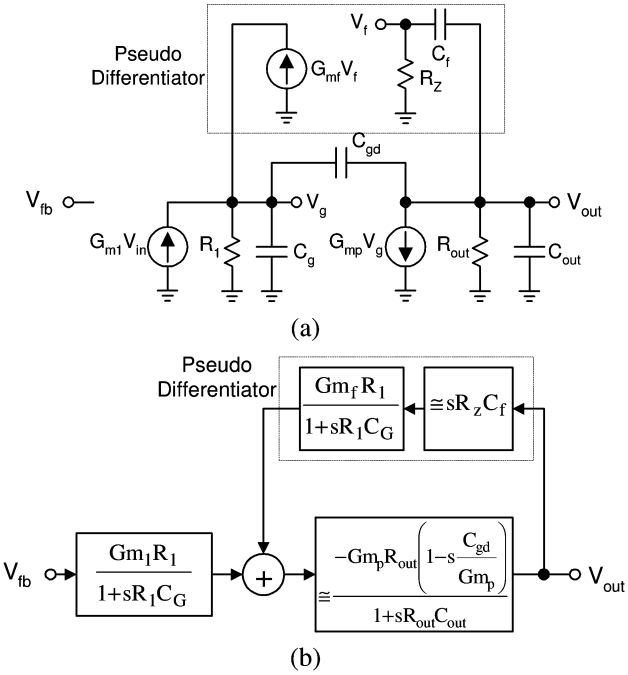

Fig. 6. External capacitorless LDO topology using a pseudodifferentiator. (a) Simplified schematic. (b) Equivalent block diagram ignoring the Miller effect.

For a current step of 0–50 mA and a maximum output ripple of 100 mV, and assuming that $\text{Gm}_p = 10$ mA/V and $C_G = 50$ pF, the compensating capacitance C_f becomes in the order of $50^*C_G = 2.5$ nF; fortunately, C_{gd} helps in pushing the gate of the pass transistor into the proper direction. The amount of coupling needed to maintain small output ripple changes with load current with the worst case scenario corresponding to the no-load condition or smallest Gm_p. Thus, the transient operation going from low to high load currents requires the most coupling capacitance.

Clearly, the required coupling capacitor is too large to be integrated. A technique is proposed to decrease the size of C_f while maintaining the effective coupling capacitance required by (4). For the analysis of the proposed circuit, let us consider the simplified open-loop characteristics of the LDO's compensation scheme shown in Fig. 6(a). If the impedance of the resistor is small compared with that of the C_f, the capacitive current is converted to voltage by R_Z, and converted back into current by Gm_f. The auxiliary circuit designated as the pseudodifferentiator increases the effect of C_f as follows:

$$C_{f,\text{eff}} = \text{Gm}_f R_Z \cdot C_f. \qquad (5)$$

In this expression, it is assumed that the parasitic pole at $1/R_ZC_f$ is located at very high frequency. The use of Gm_f provides two benefits: C_f can be reduced by several magnitudes due to the effect of $\text{Gm}_f R_Z$ and the feedforward path created by C_f is eliminated.

Fig. 7 shows the improvement for a full-load transient response using the proposed differentiator compensation which yields approximately a $10\times$ reduction in undershoot. (Note that the uncompensated simulation used a very large capacitor at the error amplifier output to create the dominant pole.)

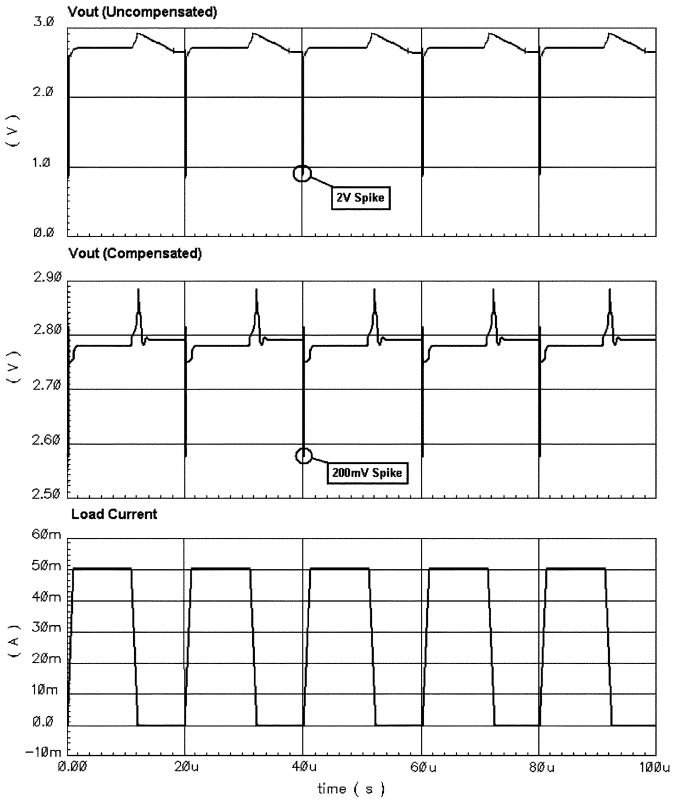

Fig. 7. Simulated improvement of transient response using proposed differentiator compensation.

B. The ac Stability

The topology's transfer function can be obtained by using the block diagram representation shown in Fig. 6(b). The differentiator's parasitic pole at $1/R_zC_f$ is ignored in this expression since by design it will be placed well above the loop's unity gain frequency; it is also assumed that the Miller capacitance is accounted in $C_G \cong C_{gs} + A_{\text{Pass}}C_{GD}$. By using standard circuit's analysis methods, the open-loop transfer function is obtained as

$$\frac{v_{\text{out}}}{v_{fb}} = -\frac{(\text{Gm}_1R_1)\cdot(\text{Gm}_PR_{\text{out}})\left(1-s\frac{C_{gd}}{\text{Gm}_p}\right)}{\left[\begin{array}{l}(1+sR_1C_G)(1+sR_{\text{out}}C_{\text{out}})\\ \quad +(sR_ZC_f(\text{Gm}_fR_1\text{Gm}_PR_{\text{out}}))\left(1-s\frac{C_{gd}}{\text{Gm}_p}\right)\end{array}\right]}. \tag{6}$$

Equation (6) sheds light on the ideal effect of the differentiator and the use of a quasi-Miller compensation. The location of the poles and zero can be simplified by assuming that $C_fR_Z\text{Gm}_fR_1\text{Gm}_pR_{\text{out}} \gg C_{\text{out}}R_{\text{out}1} + C_GR_1$, yielding

$$\begin{aligned}\omega_{P_{\text{dom}}} &\cong -\frac{1}{R_1\text{Gm}_pR_{\text{out}}(\text{Gm}_fR_ZC_f)}\\ \omega_{P2} &\cong -\frac{\text{Gm}_p(\text{Gm}_fR_ZC_f)}{C_{\text{out}}C_G}\\ \omega_{Z1} &= +\frac{\text{Gm}_p}{C_{gd}}.\end{aligned} \tag{7}$$

As expected, the differentiator splits the poles located at the input and output of the pass transistor, but it does not affect the location of the RHP zero. High-coupling network gain Gm_fR_Z ensures sufficient distance between the two poles to yield stable LDO operation. It is worth mentioning that the RHP zero may attract the poles to the right-hand side of the S-plane and generates negative root locus trajectories [9].

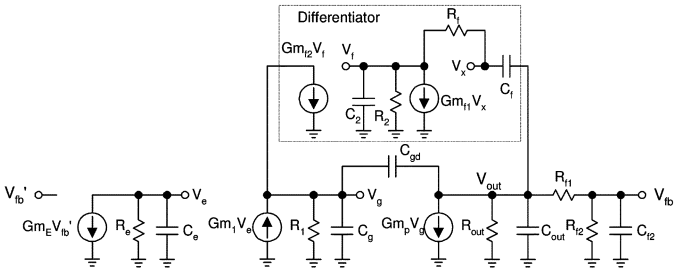

Fig. 8. Small signal diagram of the proposed capacitorless LDO voltage regulator: open-loop schematic.

The loop macromodel of the complete solution is shown in Fig. 8. The differentiator is modified from Fig. 6 to reflect the final transistor-level implementation; it adds a second error amplifier stage Gm_E. The compensating circuit is composed by the differentiator (C_f, R_f,[1] and Gm_{f1}) and an additional transconductance amplifier Gm_{f2} to boost the feedback gain, resulting in higher equivalent capacitance $C_{f,\text{eff}}(\approx \text{Gm}_{f2}R_fC_f)$. In this case, the LDO's loop includes the feedback resistors R_{f1} and R_{f2} and its parasitics. Unfortunately, the differentiator contains parasitic poles at nodes $V_x(\omega_{PD1})$ and $V_r(\omega_{PD2})$ that affect the overall behavior of the ac stability; they are approximately placed at the following locations:

$$\omega_{PD1,2} \cong -\frac{1 \pm \sqrt{1-4\frac{\text{Gm}_{f1}R_fC_2}{C_f\left(1+\frac{R_f}{R_2}\right)^2}}}{2(R_2\|R_f)\left(\frac{C_2C_f}{C_2+C_f}\right)}. \tag{8a}$$

If $Cf \gg C_2$, the poles are real and they are approximately located at

$$\omega_{PD1} \approx -\frac{\text{Gm}_{f1}R_2}{C_f\cdot(R_f+R_2)} \quad \omega_{PD2} \approx -\frac{1}{C_2(R_2//R_f)}. \tag{8b}$$

A typical bode plot for the standalone differentiator is shown in Fig. 9; usually, $\omega_{PD1} \ll \omega_{PD2}$ because the relatively large compensating capacitor C_f used. ω_{PD1} and ω_{PD2} have an adverse effect when the loop containing both the differentiator and the pass transistor stage is closed.

Notice in Fig. 8 that the loop that includes the differentiator has five poles if the pole at V_{fb} terminal is included in the analysis. The loop is reduced to a third order if ω_{PD2} and the pole at V_{fb} are ignored. In that case, Cardano's method [8] can be used to show that ω_{PD1} (lowest frequency differentiator pole) and the pole at V_{out} turn into a complex pole pair-denoted hereafter as P_2' *and* P_3'—when the differentiator's loop is analyzed. The magnitude of resulting complex conjugate pole pair can be found as

$$P_2', P_3' > \sqrt{\omega_{PD1}\omega_{P2}} \tag{9}$$

[1] R_f refers to the differentiator's series feedback resistance while R_Z denotes the differentiator's ground referenced input resistance.

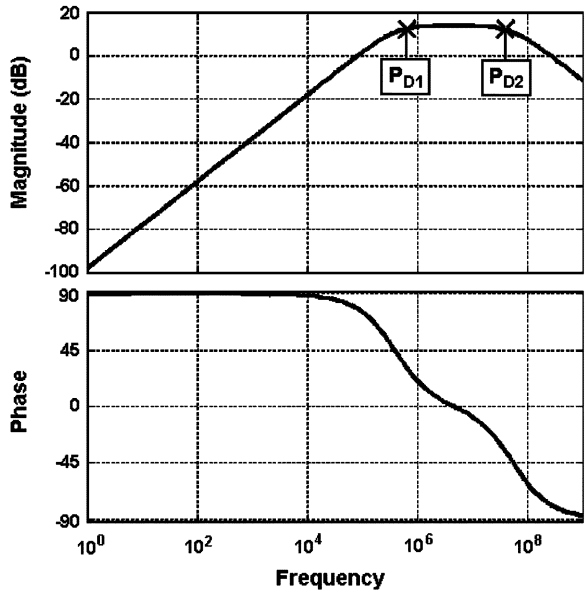

Fig. 9. Differentiator's magnitude and phase response.

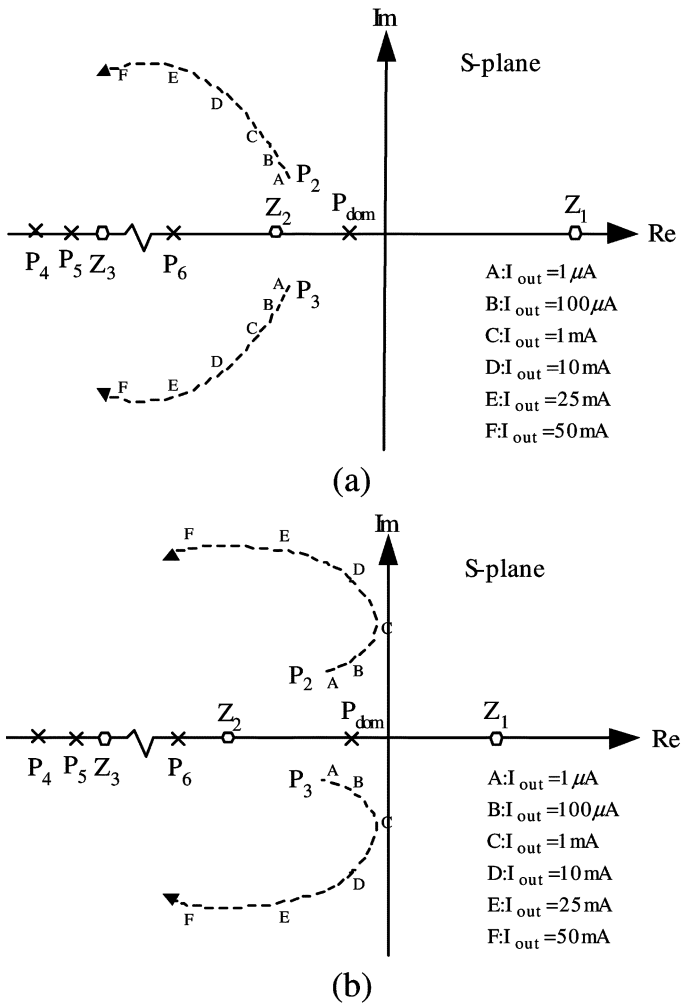

Fig. 10. Differentiator parasitic pole effects on complex pole movement versus load current: (a) desired pole trajectory and (b) potential instability (S-plane not to scale).

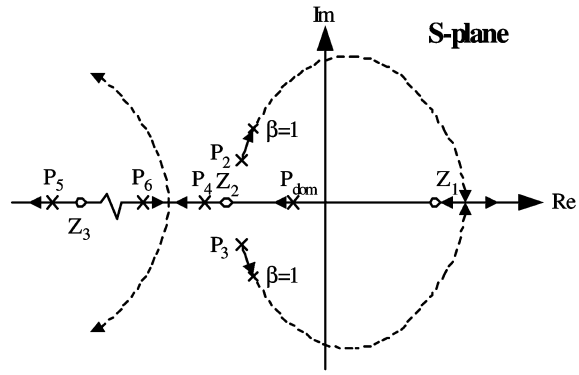

Fig. 11. Complete capacitorless LDO regulator root-locus diagram for feedback gain β and $I_{\rm OUT} = 0$ mA.

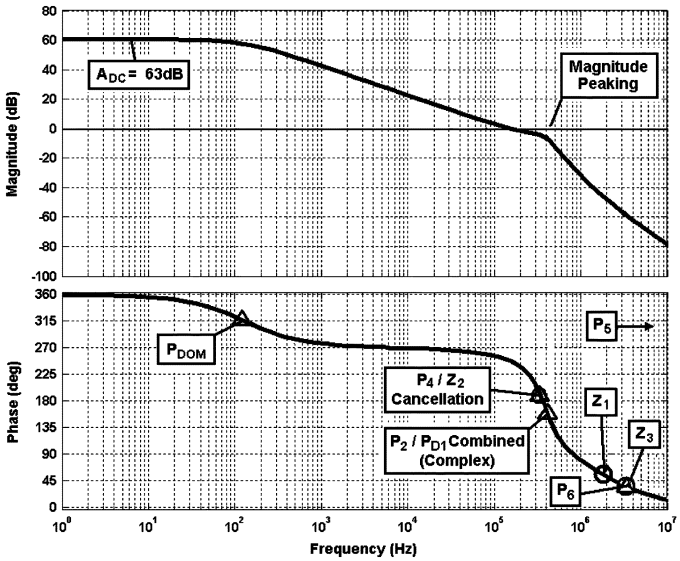

Fig. 12. Open-loop ac response for $I_{\rm out} = 0$ mA.

where ω_{PD1} and ω_{P2} are given in (7) and (8b). To get some insight on the reason for the complex poles, let us assume that the dominant pole at node V_g is located at very low frequency, and that the differentiator has a dominant pole ω_{PD1}. When the differentiator's loop is analyzed, the dominant pole and the zero due to the differentiator cancel each other leading to the classic two-pole loop: Main poles are at nodes $V_{\rm out}$ and ω_{PD1}. The additional loop gain due to g_{mf2} increases the effective frequency of the complex poles. The presence of the RHP zero due to C_{gd} as well as the effect of other parasitic poles makes the poles complex.

In addition to the aforementioned poles, we still have to consider the dominant pole $\omega_{\rm Pdom}$ given in (7), the poles at $V_f(\omega_{PD2})$, pole P_4 at node V_{fb}, P_5 at node V_f, and P_6 at node V_e. The location of the last poles are

$$\omega_{P4} = -\frac{1}{(R_{f1}||R_{f2})C_{f2}}$$
$$\omega_{P5} \cong -\frac{1}{C_2(R_2//R_f)}$$
$$\omega_{P6} = -\frac{1}{R_eC_e}. \tag{10}$$

Also, an RHP zero Z_1 due to C_{gd} and a couple of real LHP zeros Z_2 and Z_3 with frequencies close to ω_{PD1} and ω_{PD2},

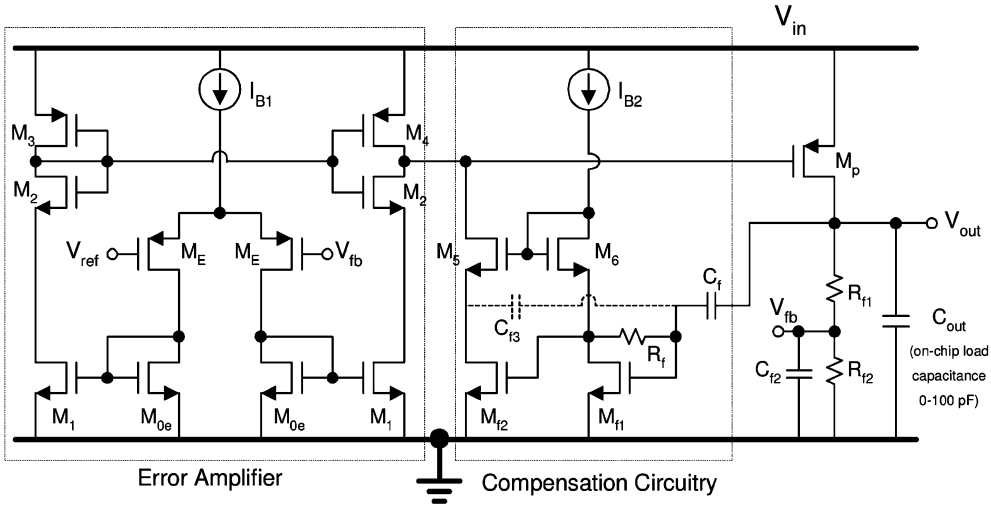

Fig. 13. Transistor-level implementation of the proposed LDO's architecture.

respectively, appear into the system since these poles are not touching the main trajectory from V'_{fb} to V_{fb}.

The relevant poles and zeros present in Fig. 8 are depicted in Fig. 10(a); there are three real poles, two complex poles, and three zeros; this figure also shows the desired complex pole placement as a function of the load current. Unfortunately, at some critical conditions for the parasitic poles and zeros, shown in Fig. 10(b), the complex poles might even cross to the RHP and the system becomes conditionally stable.

Note in these results that the RHZ Z_1 has a strong effect on loop's stability since it may attract the complex poles. The condition for stability can be found using again Cardano's method, but the resulting expression is quite complex. It is, however, enough to have enough phase margin $(>45^\circ)$

$$\frac{1}{2|\omega_{PD1,2}|}+\frac{1}{\omega_{P5}}+\frac{1}{|\omega_{Z1}|}<\frac{1}{A_{\text{loop}}\omega_{\text{Pdom}}}\cong\frac{1}{\text{GBW}} \quad (11)$$

where $A_{\text{loop}}(=\beta \text{Gm}_e R_e \text{Gm}_1 R_1 \text{Gm}_p R_{\text{out}})$ is the dc loop gain and GBW is the gain-bandwidth product. It is assume in this expression that the two LHP zeros are placed beyond GBW and close enough to ω_{P4} and ω_{P6}. Note in (11) that the RHP zero ω_{Z1} has a strong effect on loop's stability; the higher its frequency the better the loop's stability is. As aforementioned, it is advisable to place the complex poles such that $|\omega_{PD1,2}| > 5-10$ times GBW to have enough gain margin to tolerate the peaking introduced (usually, less than 6 dB) by the complex poles.

Usually, the LHP zeros would improve system stability by adding positive phase; however, a downside is that they may reduce loop gain margin if located close to the unity gain frequency, and in conjunction with magnitude peaking and sharp phase transition induced by the complex conjugate and high frequency poles, it may significantly reduces system stability. To minimize this issue, the additional capacitor C_{f2} shown in Fig. 8 was added to push down ω_{P4} (pole at node V_{fb}) to cancel the effects of Z_2. $P4$ is chosen since it does not affect the integrator's loop stability and can be easily controlled. The complete root-locus for the critical case of $I_{\text{OUT}} = 0$ is shown in Fig. 11; it contains the differentiator, a compensating capacitor C_{f2} (shown in Fig. 8 and to be discussed in the following section) and the dc stabilizing feedback network $\beta = R_{f2}/(R_{f1}+R_{f2})$. Due to the number of poles and zeros, as expected, the complex poles are attracted to the RHP by Z_1; however, the resulting closed-loop poles movement is very small for $\beta \leq 1$, and the overall closed-loop complex poles will lie in left-hand side of the S-plane for the practical feedback gain range β, provided that (11) is satisfied. Notice that $P5$ resides at very high frequency not affecting significantly system stability.

The loop has been extensively simulated under different PVT variations. The ac compensated capacitorless LDO regulator has a Bode plot that resembles a first-order transfer function up to the complex conjugate pole pair; shown in Fig. 12 is the most critical case. The ac stability involves the following three essential requirements: 1) the complex pole pair does not cross into the RHP, 2) the magnitude peaking of the complex conjugate pair does not peak over the 0-dB threshold (adequate gain margin), and 3) adequate phase margin.

IV. Proposed LDO Transistor-Level Design

The transistor-level design is shown in Fig. 13. A three-current mirror operational transconductance amplifier M_0–M_3 and M_E forms the error amplifier. The low-impedance internal nodes of the three-current mirror operational transconductance amplifier (OTA) drive the parasitic poles out to high frequencies, well pass the desired GBW product. The error amplifier's parasitic poles do not significantly affect the performance of the regulator as long as they are at least three times greater than the loop's GBW product, and the error amplifier can, therefore, be designed to meet other desired parameters such as the output noise, power consumption, and dc gain [3]–[5].

A. Design Considerations

The dc gain is the major stability constraint on the error amplifier, forced by the desired gain margin or the magnitude difference between the worst case complex pole magnitude peak and unity gain frequency. This gain margin is a function of load

TABLE II
DESIGN PARAMETER VALUES

.	W(μm)	L(μm)	I_D(μA)
M_E	20	2	2.5
M_{0e}	1	2	2.5
M_1	2	2	5
M_2	5	2	5
M_3	2.9	2	5
M_4	20.3	2	35
M_5, M_{f2}	3	0.4	30
M_6, M_{f1}	1	0.4	10
M_P	16000	0.4	10

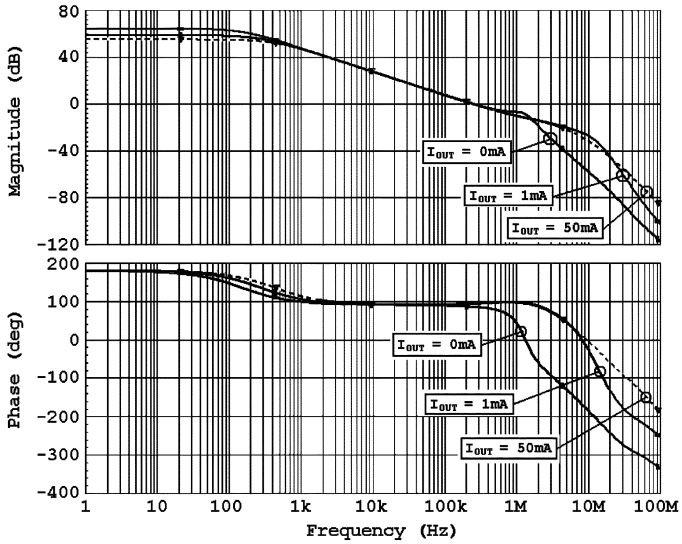

Fig. 14. Full range open-loop ac response spice simulation (0–50 mA).

current, and retains it lowest value in the load current range of 0 to 5 mA. The error amplifier gain ranges between 40 and 50 dB.

The differentiator is designed to yield the desired transient response while stabilizing the overall system transfer function. The input and output nodes of $M_{\rm gmf1}$, forming the first stage amplifier in the inverting differentiator, are the most critical nodes. Enough gain must be developed to properly drive the differentiation capacitor while generating very small parasitic capacitors. This pushes the generated poles ω_{PD1} and ω_{PD2} to higher frequencies. Thus, the tradeoff between stability and transient response remains the most difficult design problem, and several iterations of the design procedure are required. R_f performs three tasks: transforms the current supplied by C_f into a voltage during load current transients, provides the dc bias for both M_{f1} and M_{f2}, and helps to lower the differentiator's input impedance pushing the associated pole ω_{PD1} beyond the loops unity gain frequency. The inverting differentiator then sums into the error amplifier output through transistors M_{f2} and M_4. Compensation capacitor C_{f3} in the range of 1–2 pF, is used to improve the ac stability. C_{f3} uses the Miller effect to push the pole at the input of the differentiator ω_{PD1} out to higher frequencies; notice in Fig. 13 that it is placed in partial positive feedback.

Inaccuracies and mismatches will cause large dc offsets at the output. M_2 and M_{5-6} transistors are added to reduce the systematic offsets and to increase the current mirror accuracy as $V_{\rm IN}$ increases. The design starts with the required dropout

TABLE III
CIRCUIT DIMENSIONS AND BIAS: $V_{\rm REF} = 1.24$ V, $R_{F1} = 156$ kΩ, $R_{F2} = 124$ kΩ, $I_{B1} = 5\,\mu$A, $I_{B2} = 10\,\mu$A

Parameter	Final value
Pass transistor	$C_{GS} \cong 100$pF, $C_{GD} \cong 26$pF, $Gm_p = 3.20$ mA/V @ $I_{OUT} = 0$mA
C_{out}*	100pF
R_{out}	280kΩ
A_{diff}	~ 60dB
C_f	20pF
R_f	200kΩ
$Gm_{f2}\cdot R_2$	~ 30dB
A_{DC}	≤ 68dB
$Gm_E R_e$, $Gm_1 R_1$	~ 40dB
C_{f2}	1pF
C_{f3} (optional)	2pF

*Load capacitor C_{out} is added to test the circuit under large capacitive load conditions.

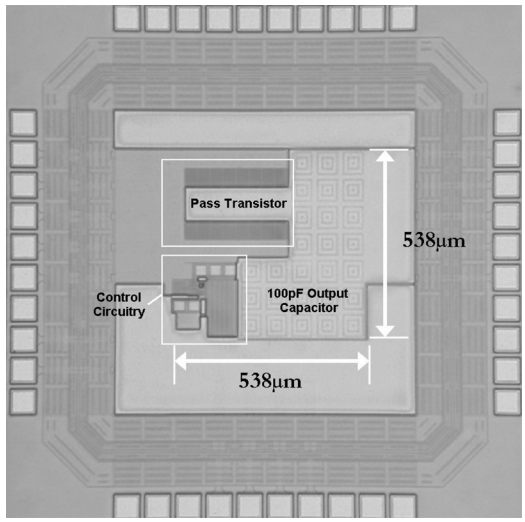

Fig. 15. Microphotograph of the chip.

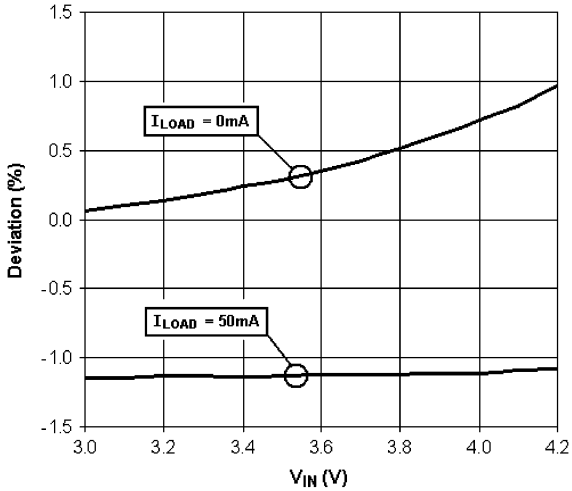

Fig. 16. Measured line and load regulation.

voltage $V_{\rm DROP}$, and the maximum current at dropout $I_{\rm MAX}$, which define the parameters of the pass transistor. The procedure then defines the differentiator parameters, followed by the error amplifier parameters, and ends with the selection of C_{f2} and C_{f3}. The final circuit parameters are given in Table II with a

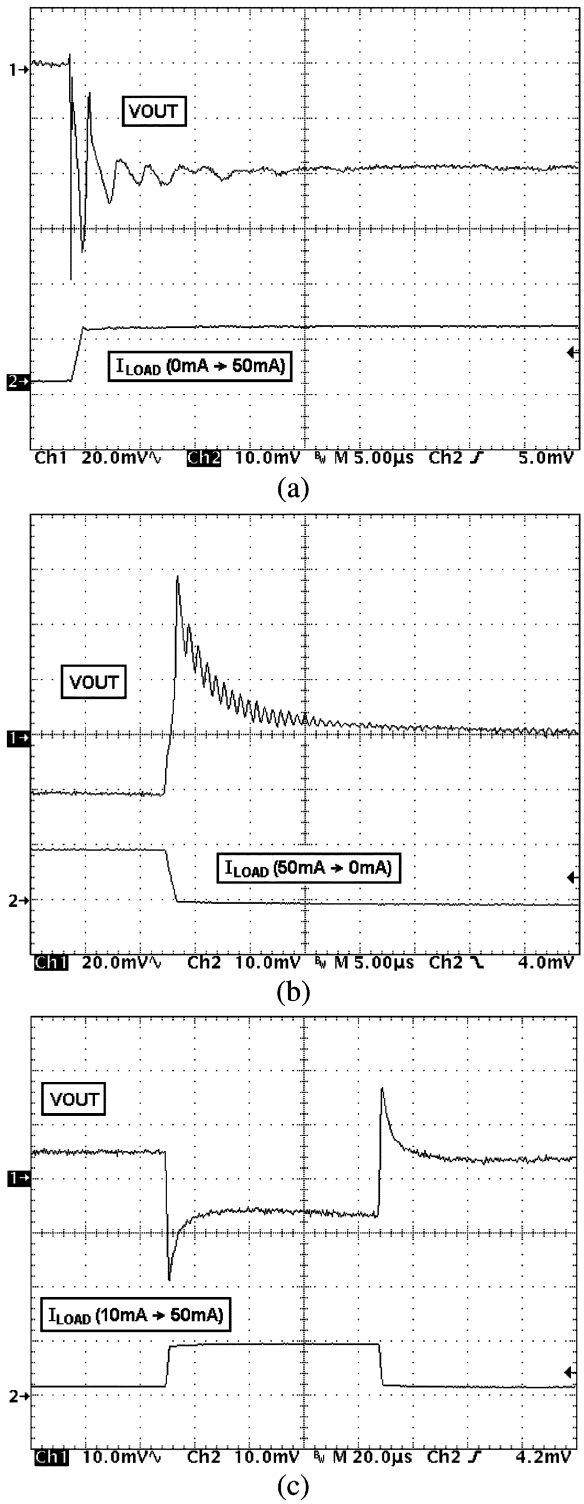

Fig. 17. Measured transient response: (a) 0–50 mA, (b) 50–0 mA, (c) 10–50 mA to 10 mA.

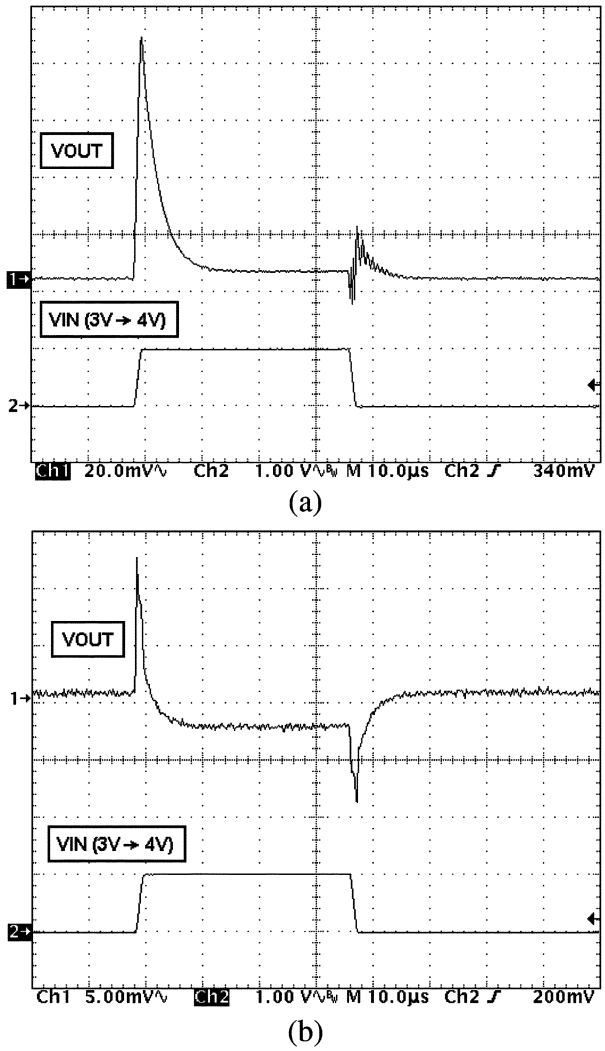

Fig. 18. Measured Line transient response: (a) $I_{\mathrm{LOAD}} = 0$ mA and (b) $I_{\mathrm{LOAD}} = 50$ mA.

spice simulated open-loop ac response for three cases shown in Fig. 14. The final capacitorless LDO design had full range stability with a GBW product of greater than 220 kHz and phase margin exceeding 50° over temperature (−40 °C to 80 °C) and process tolerances (3σ yields with $\pm 10\%$ variations for all parameters). For smaller C_{load}, the unity gain frequency increases and circuit's stability improves.

V. Experimental Results

The physical capacitorless LDO voltage regulator was experimentally verified for all simulated parameters except for the open-loop ac response with V_{REF} set to 1.24 V and V_{IN} set to 3 V minimum, unless otherwise noted. The circuit was fabricated, through the MOSIS educational program, in the TSMC 0.35-μm CMOS technology that occupied 0.29 mm^2 of area and consumed 65 μA of ground current. The transistor dimensions and bias conditions are given in Table III.

The chip microphotograph is shown in Fig. 15. An on-chip 100-pF capacitor was included to characterize LDO's performance under extreme conditions. Most of the area is invested in the 100-pF on-chip capacitor and the pass transistor; LDO's area, excluding the load capacitor, is around 350 μm^2.

The off-chip capacitorless LDO regulator was tested for load and line regulation, shown in Fig. 16. Output voltage errors were less than 1.5% over the entire operation range.

The regulator was then subjected to a 0–50-mA load transient with 1-μs rise and fall times, as shown in Fig. 17(a) and (b). An extra ringing, less than $\pm$ 90 mV, was experienced for the positive load current transition, but the ringing quickly subsided

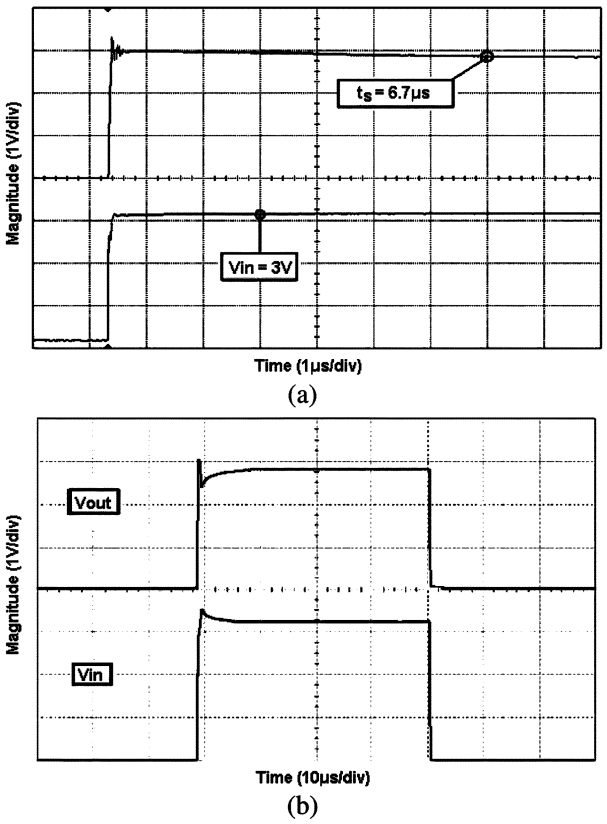

Fig. 19. Measured turn-on response: (a) $I_{\rm LOAD} = 0$ mA and (b) $I_{\rm LOAD} = 50$ mA.

and a stable response was reached within 15 μs in the worst case. For the 50–0-mA transition in Fig. 17(b), the amplitude of the ringing is smaller and settling time is also approximately 15 μs. The output voltage ringing is greatly reduced when operating above 1 mA or outside the pass transistor subthreshold region; it was experimentally found in Fig. 17(c) that for a load transient of 10–50 mA with the same rise and fall times, the overshoots are approximately $\pm$ 10 mV. It can also be noticed in this plot that the output voltage presents an output voltage variation, steady state, of 11 mV when the load current changes from 10 to 50 mA. This value confirms that the overall loop transconductance is stable with an equivalent output resistance close to 40 mV/50 mA $>0.8\,\Omega$. The line transient response was measured for a 3–4-V step waveform with 1-μs transition times for both $I_{\rm LOAD} = 0$ mA [Fig. 18(a)] and $I_{\rm LOAD} = 50$ mA [Fig. 18(b)]. Output voltage variation was less than 90 mV for $I_{\rm LOAD} = 0$ mA and less than 15 mV for $I_{\rm LOAD} = 50$ mA. A positive input voltage transient produces larger spikes since the output capacitance is easier to charge than discharge due to the quadratic current–voltage (I–V) characteristics of the pass transistor.

The turn-on settling response was measured for various loading conditions; Fig. 19(a) shows the time response for a no-load condition, measuring roughly 8 μs for a 0.1% settling time specification. The turn-on response for 50 mA shown in Fig. 19(b) is less than 10 μs. Fig. 20(a) shows the power supply rejection ratio (PSRR) for $I_{\rm LOAD} = 0$ and 50 mA. Tests revealed a PSRR response smaller than $-$ 53 dB for frequencies up to 100 kHz. PSRR is a function of the pass transistor R_{DS}

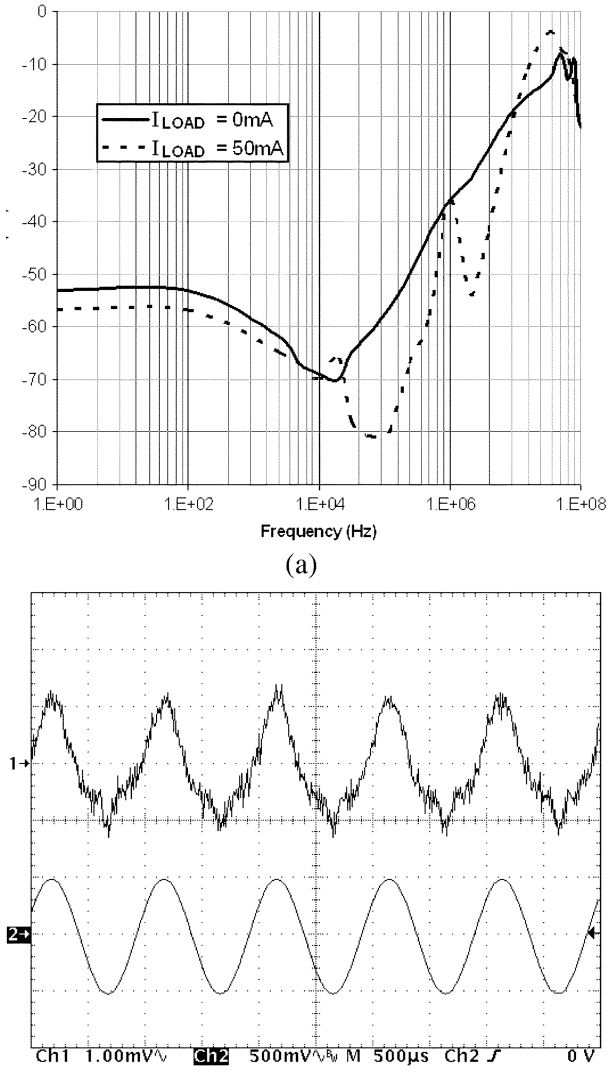

Fig. 20. Measured PSRR: (a) PSRR for $I_{\rm LOAD} = 0$ and 50 mA, (b) Ripple response $I_{\rm LOAD} = 0$ mA. Vout and Vin are depicted in trace 1 and 2, respectively.

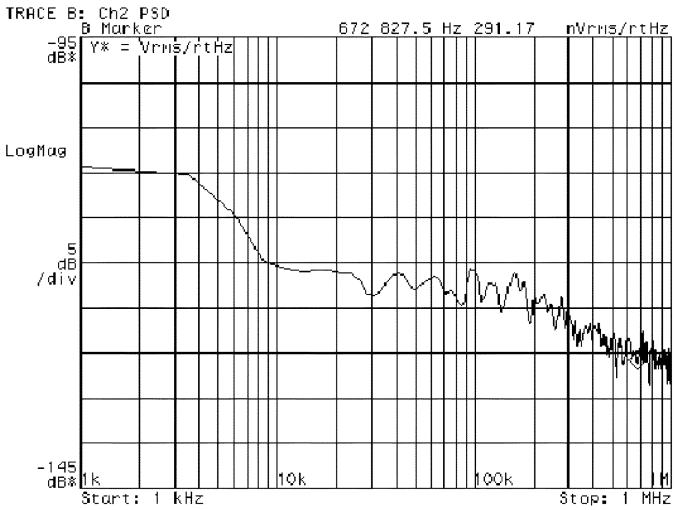

Fig. 21. Output noise for $I_{\rm LOAD} = 0$ mA.

and the error amplifier PSRR at the pass transistor's gate. The transient response, shown in Fig. 20(b), was measured

TABLE IV
COMPARISON OF RESULTS

Parameter		[2]*	[10]	[11]**	This work***
Technology		CMOS 0.6μm	CMOS 0.09μm	BiCMOS	CMOS 0.35μm
Pass Element		Common-Source	Composite	Common-Drain	Common-Source
I_{MAX} (mA)		100	100	150	50
V_{OUT}		1.3	0.9	1.2 – 5.5	2.8
V_{DROP} (mV)		200	300	30	200
I_Q(mA)		0.038	6	0.55	0.065
C_{out} (pF)		10,000 (external)	600 (external)	0 - 10,000	0-100
Area (mm^2)		0.307	0.098	NA	0.12
Δv_{out} (Full load transient)		< 150mV	90mV	< 120 mV @ C_{Load}=0pF and I_{load} 10mA-150 mA	< 90mV @C_{Load}=100pF
Settling (μs)		~ 2 (0-100 mA)	N/A	~ 20 (10mA-150 mA)	~ 15 (0-50 mA)
PSRR (1kHz)		- 60 dB	N/A	~ - 45 dB	-57 dB
Loop gain (dB)		90 ~ 110	>43	NA	55 ~ 62
Noise	@ 100Hz	$1.8\mu V/\sqrt{Hz}$	NA	$0.45\,\mu V/\sqrt{Hz}$	$4.6\mu V/\sqrt{Hz}$
	@ 100kHz	$0.38\mu V/\sqrt{Hz}$	NA	$0.2\,\mu V/\sqrt{Hz}$	$0.63\,\mu V/\sqrt{Hz}$

*Δv_{out} and settling time are not provided for C_{out}=0 pF ($C_{internal}$ = 12 pF) and I_{step}= 0-100 mA.

** Uses a charge pump to handle the common drain device.

*** The on-chip capacitance needed consists of C_f, C_{f1} and C_{f2}; C_{f3} is optional.

to verify the PSRR results. A sinusoidal waveform of 1 kHz was applied to V_{IN} and the supply voltage gain was measured around −53 dB. The equivalent output noise was measured for different load currents, as shown in Fig. 21. The worst case spot noise at 10 kHz was roughly 720 nV/Hz$^{1/2}$ and was mainly due to 1/f noise. The error amplifier contributed to most of the noise and has to be optimized to reduce the equivalent output noise if required.

VI. CONCLUSION

Experimental results show that the proposed LDO voltage regulator exceeds current work in the area of external capacitorless LDO regulators in both transient response and ac stability while consuming only 65 μA of quiescent current; the internal compensating capacitors are as small as 7 pF only while the load capacitor can be as large as 100 pF.

Stability is not compromised by the load capacitance value, provided that C_{load} does not exceed some limits defined by the location of the second pole. A comparison is made among other output capacitorless designs [2], [10], [11], shown in Table IV, illustrating the significance of the proposed external capacitorless LDO regulator. Not only does the proposed regulator consume low power, but it provides a low dropout voltage and fast settling time. SoC designs would benefit from the reduced board real estate, pin count, and cost achievable with the proposed off-chip capacitorless full CMOS LDO regulator.

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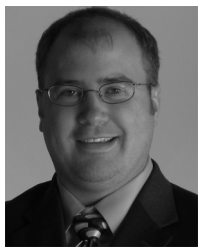

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