A Wideband Fractional-N Frequency Synthesizer with Linearized Coarse-Tuned VCO for UHF/VHF Mobile Broadcasting Tuners

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***Abstract*—A fractional-N frequency synthesizer with a fractional bandwidth of 67 % for UHF/VHF-band mobile broadcasting tuners is presented. A novel linearized coarse tuned VCO with a pseudo-exponential capacitor bank structure is proposed to cover the wide bandwidth. The proposed technique successfully reduces the variation of K_{VCO} and per-code frequency step by 2.7 and 2.1 times, respectively. For the divider and prescaler circuits, TSPC (true single-phase clock) structure is employed for high speed operation, low power consumption, and small silicon area. Implemented in 0.18-μm CMOS, the PLL covers 154 ~ 303 MHz (VHF) and 462 ~ 911 MHz (UHF) with a single VCO. The integrated phase noise is 0.807 and 0.910 degree for the integer-N and fractional-N modes, respectively, at 827.5-MHz output frequency. The in-band noise at 1 kHz offset is -95 dBc/Hz in the integer-N mode and degraded only by 3.8 dB in the fractional-N mode.**

I. INTRODUCTION

Mobile broadcasting systems have been drawing substantial market demands these days. UHF and VHF bands are widely adopted for these systems. In Europe, DVB-H/T and DAB are serviced in the UHF band of 470 ~ 862 MHz. In Korea, T-DMB is serviced in the VHF band of 170 ~ 240 MHz. MediaFLO operates in the UHF band from 698 to 746 MHz. In Japan, ISDB-T is serviced in the VHF and UHF bands. Hence modern mobile tuners need to support the multiple bands and standards seamlessly. A fractional-N frequency synthesizer is one of the essential parts in the tuner implementation. Since the bandwidth of the UHF band reaches almost an octave, or equivalently a 67-% of fractional bandwidth, two VCO's are usually needed [1,2]. One of the difficulties in implementing a wideband VCO lies at the huge variation of the VCO gain (K_{VCO}) and the frequency step per a capacitor bank code [3].

In this work, we propose a design technique of a wideband VCO with a linearized coarse tuning characteristic. Then we present a CMOS fractional-N frequency synthesizer with < 1^o rms integrated phase noise over the whole bands for UHF and VHF mobile broadcasting tuners.

II. ARCHITECTURE

Integer-N architecture adopted for previous tuners [1,4] is not appropriate for the multiple bands and multiple standards. Thus fractional-N architecture with a third-order 3-bit delta sigma modulator (DSM) is realized. Fig. 1 shows the PLL architecture. A single VCO covers 940 ~ 1724 MHz. LOGEN block generates LO signals, in which the divide-by-6 is for the VHF band and the divide-by-2 is for the UHF band. The dividers in the LOGEN are designed with a current-mode logic (CML) type DFF for simple I/Q signal generation. The divide-by-2 and the 4/5 dual-modulus prescaler in the feedback path are designed by utilizing true-single-phase-clock (TSPC) logic. A DFF after the programmable counter is to synchronize the programmable counter output to the prescaler output. This re-timing block significantly suppresses the accumulated phase jitter created by the programmable counter. An adaptive frequency control (AFC) block is based on the pulse-counting and comparison method. The number of the pulse-counting and comparison operation is programmable which allows minimizing the lock time. Typical AFC search time for the 6-bit coarse tuning code is less than 150 μsec. A third order loop filter is used, of which three RC components are implemented off chip.

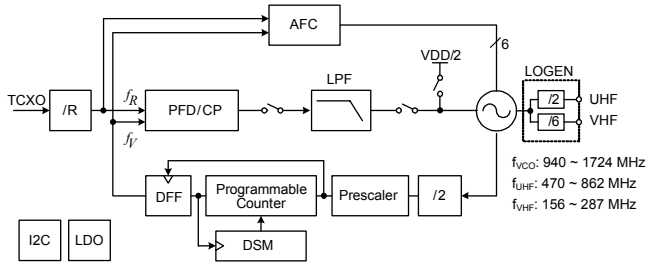


Figure 1. Frequency Synthesizer Architecture.

III. BUILDING BLOCK DESIGN

A. Wideband VCO with Linearized Coarse Tuning

Fig. 2 shows the VCO circuit schematic. A regulating amplifier is employed to reduce the power supply sensitivity of the VCO and thereby its phase noise contribution. Reference voltage V_{REF} is generated via a replica circuit with a low noise bandgap reference current. The simulated output noise of the bandgap circuit is 12.2 and 10.9 nV/√Hz at 100 kHz and 1 MHz, respectively. A low pass filter of R_5 and C_5 is employed to further suppress the noise transferred from the regulator.

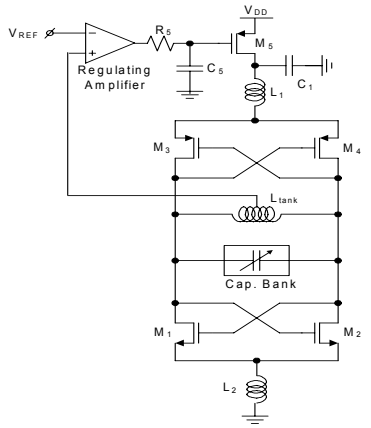


Figure 2. VCO circuit schematic.

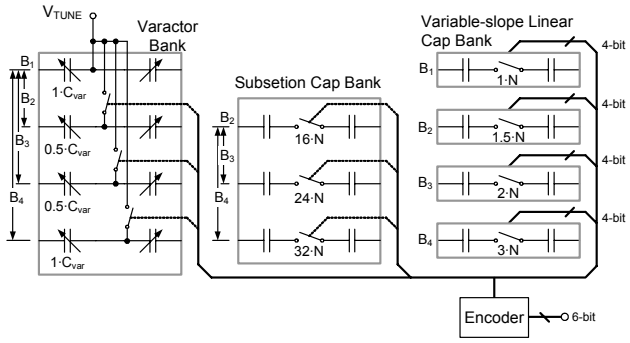
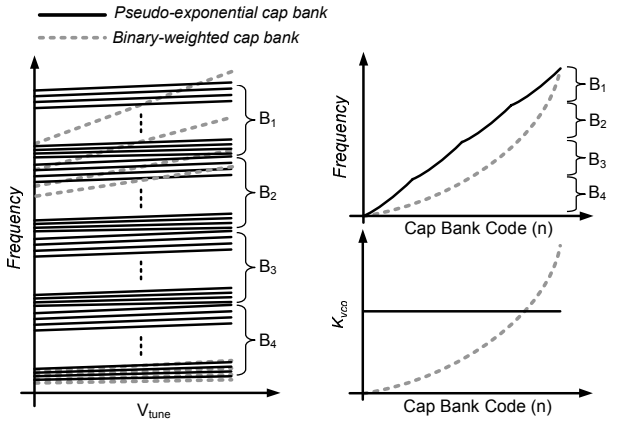


Figure 3. Pseudo-exponential capacitor bank structure.

The capacitor bank is composed of varactor diodes for analog fine tuning and a 6-bit switched capacitor bank for digital coarse tuning. Considering process-voltage-temperature variations, the VCO needs to have a fractional bandwidth of over 70 %. If a conventional binary-weighted cap bank is used for such a wideband VCO, the K_{VCO} and the frequency step per a cap bank code will vary over five times [3]. Such a huge K_{VCO} variation makes difficult optimal design of the PLL loop characteristics, possibly leading to severe degradation of phase noise and lock time in several channels. Also, the huge variation of the per-code frequency step prevent optimal design of AFC search time because the number of pulse-counting must be set unnecessarily high enough to detect the smallest frequency step. In [5], a combined tuning technique of the fixed and varactor capacitors was presented to reduce the K_{VCO} variations, but they did not address the frequency step variation issue.

In this work, we propose a novel pseudo-exponential cap bank structure to address both problems. Fig. 3 shows the cap bank structure. It consists of a subsection cap bank, a variable-slope linear cap bank, and a varactor bank. Fig. 4 illustrates the effects of the proposed cap bank by comparing the coarse tuning characteristics that can be obtained by the proposed and conventional cap bank structures. Since the VCO output frequency is determined by $1/(2\pi\sqrt{LC})$, it would be ideal to make the total



(a) (b)

Figure 4. Comparison of coarse tuning characteristics by the conventional binary-weighted cap bank and the proposed pseudo-exponential cap bank structure. (a) Frequency tuning characteristics. (b) Frequency and K_{vco} variation against the cap bank tuning code at a fixed V_{tune}.

capacitance of a cap bank vary in an exponential form of 2^{2n} with the cap bank code value n. However, this is not practical in real implementation due to the extremely huge minimum to maximum capacitance ratio (*e.g.* $2^{2\times64}$ for 6-bit coarse tuning in VCO). Thus, we try to mimic the 2^{2n}-dependency by realizing a pseudo-exponentially varying capacitance.

As shown in Fig. 4, the total tuning range is divided into four subsections B_1 to B_4. Within each subsection, capacitance varies linearly with a different slope. The slope is set by the different unit capacitances of $1\times C_{unit}$, $1.5\times C_{unit}$, $2\times C_{unit}$, and $3\times C_{unit}$ for each subsection. During the inter-subsection transitions, the accumulated capacitance appearing in the previous subsection is absorbed into the subsection cap bank and the linear cap bank is reset again to a minimum value. In the varactor bank, the varactor size is adjusted for each subsection to minimize the K_{VCO} variation. The VCO adopting this cap bank structure is referred to as VCO-LCT in this paper. Meanwhile, a VCO with the conventional binary weighted cap bank is also designed for comparison. According to the simulation results, we have achieved dramatic reduction in the variation of K_{vco} and per-code frequency step.

B. Divide-by-2, 4/5-Prescaler, and PFD in TSPC logic

The TSPC logic dramatically reduces the power consumption and silicon area compared to the conventional CML logic. Thus, the divide-by-2 and 4/5 dual-modulus prescaler in the feedback path are realized by utilizing the TSPC logic. Fig. 5 shows the circuit schematic of the divide-by-2, where the FET widths are shown while the gate lengths are minimum 0.18 μm. The widths are optimized for high speed operation and sufficient swing by trading off the self-capacitance and the driving capability. The same DFF is also used for the 4/5 dual-modulus prescaler. In the simulation, the maximum operation frequencies of the divide-by-2 and the prescaler are 6 GHz and 3.5 GHz in the

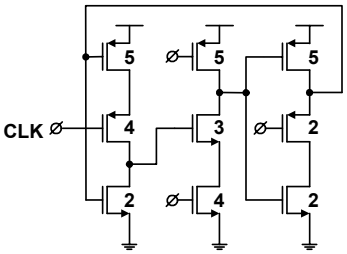


Figure 5. TSPC divide-by-2 circuit.

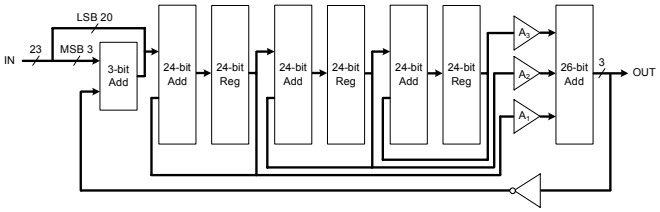


Figure 6. A 3rd-order 3-bit single-loop CIFF delta sigma modulator with 20-bit resolution.

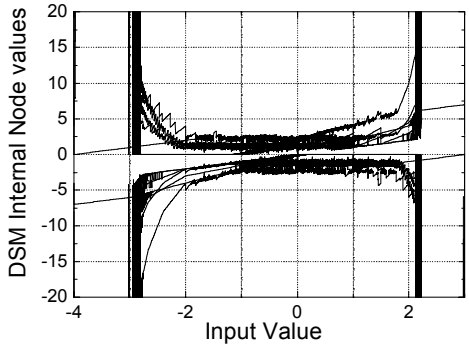


Figure 7. Dynamic range simulation of the single-loop delta-sigma modulator.

worst case, while they reaches up to 9 GHz and 4.5 GHz in the typical case. Moreover, the current consumption of the prescaler is only 0.8 mA. The TSPC logic DFF is also used in the PFD circuit in order to minimize the timing mismatch of the UP/DN pulses.

C. Delta-Sigma Modulator

DSM greatly impacts the phase noise performance and loop dynamics in PLL. We implement a 3rd-order 3-bit single-loop DSM of CIFF (cascaded integrators with distributed feedforward) type with 20-bit resolution [6]. Fig. 6 shows the block diagram. The coefficients A_1, A_2, and A_3 are 2, 1.5, and 0.5, respectively. The maximum and integral quantization noises of this architecture are greatly less than the conventional MASH-111 structure, only about 40 % and 28 %, respectively. Time-domain simulation was performed to examine the dynamic range. Fig. 7 shows the internal node values in the DSM with respect to the input value. The dynamic range of the single-loop DSM is about -2.5 ~ +2.0, which is significantly larger than the conventional MASH-111 whose dynamic range is only -0.5 ~ +0.5. The time-domain simulation also shows the number of output levels is

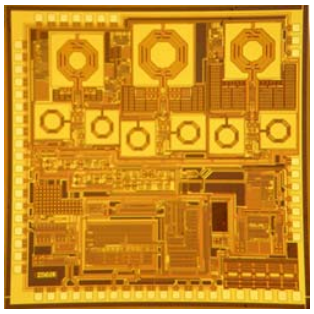


Figure 8. Chip micrograph.

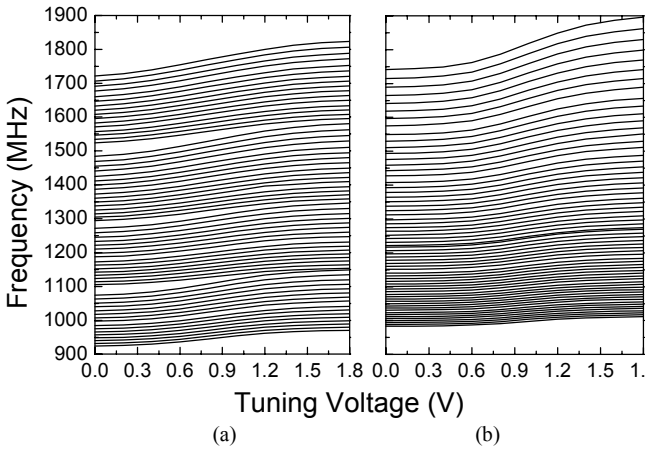


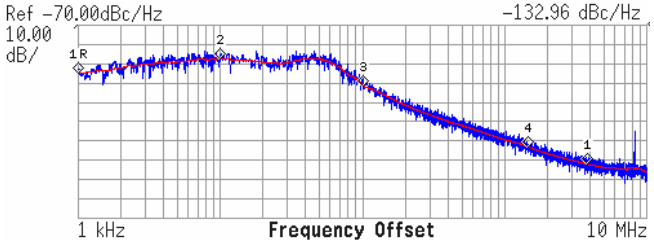
Figure 9. Measured frequency tuning characteristics of VCO with (a) the proposed pseudo-exponential cap bank and (b) the conventional binary weighted cap bank.

only about 4 while that of the MASH-111 is 8, possibly leading to less noise folding, lower in-band noise, and more stable dividing operation. For these advantages, the single-loop CIFF architecture is chosen in this work.

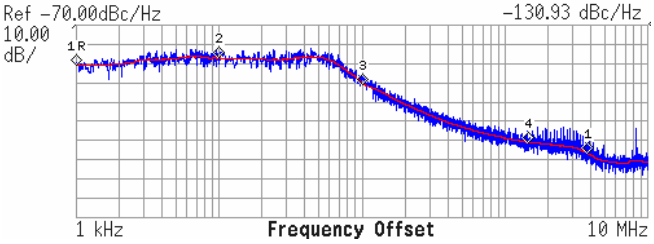
IV. Experimental Results

The frequency synthesizer is fabricated in a 0.18-μm RF CMOS process. Fig. 8 shows the chip micrograph. The die area is 2.5×2.5 mm^2, which includes additional test circuits for comparison purpose. It is packaged in a 40-pin leadless plastic chip carrier (LPCC) and tested on an evaluation printed circuit board. It dissipates about 23 mA from 1.8 V supply.

Fig. 9(a) shows the frequency tuning characteristics of VCO-LCT which is 924 ~ 1850 MHz (66.7%), successfully covering the target range. Measured phase noises at the highest 1.8-GHz output frequency are -100 dBc/Hz @ 100 kHz offset and -130 dBc/Hz @ 1.45 MHz offset. In order to examine the effects of the proposed pseudo-exponential cap bank structure, a test VCO with the conventional cap bank structure is also measured and shown in Fig. 9(b). For the conventional VCO, the variations of the K_{VCO} and the frequency step are 33.6 ~ 160.7 MHz/V and 5.5 ~ 31 MHz/code, respectively. Meanwhile, they are dramatically reduced to 45.2 ~ 79 MHz/V and 8.4 ~ 22.7 MHz/code at V_{tune} = 0.9 V for the VCOL-LCT. Thus the variation of



(a)



(b)

Figure 10. PLL phase noise measurement. (a) Integer-N mode at 825.6 MHz. (b) Fractional-N mode at 827.5 MHz.

K_{VCO} is reduced from 478 % to 175 %, and the variation of the frequency step is reduced from 560 % to 270 %. They correspond to about 2.7 and 2.1 times reductions, respectively. The more constant K_{VCO} of the VCO-LCT leads to more stable PLL loop dynamics over the whole frequency region.

Fig. 10 shows the measured phase noise of the PLL. In the measurement, the loop bandwidth is 70 kHz, the reference frequency is 19.2 MHz, and the charge pump current is 2 mA. Fig. 10(a) is for the integer-N mode with the output frequency of 825.6 MHz and Fig. 10(b) is for the fractional-N mode with the output frequency of 827.52 MHz where the DSM output value is +0.1. The in-band noise at 1 kHz is -95 dBc/Hz for the integer-N mode and becomes -91.2 dBc/Hz for the fractional-N mode, which is only 3.8-dB degradation. The phase noises at 100 kHz and 1.45 MHz offsets are -101.7 and -132.9 dBc/Hz for the integer-N mode, and -100.9 and -130.9 dBc/Hz for the fractional-N mode. In the fractional-N mode, residual quantization noise is slightly observed at around 2 MHz offset. Integrated phase noise is a crucial factor affecting the signal-to-noise ratio in OFDM signal. The phase noise integrated from 1 kHz to 3.8 MHz is measured to be 0.807 degree (-37.0 dBc) and 0.910 degree (-35.9 dBc) for the integer-N and fractional-N modes, respectively. At lower output frequencies, the phase noise performances become better. For instance, at an output frequency of 500 MHz, the integrated phase noise is measured to be 0.145 and 0.244 degree for the integer-N and fractional-N modes, respectively. It successfully meets the DVB-H requirement of -33 dBc [4].

Fig. 11 shows the spectrum at the output frequency of 629.75-MHz. It compares the spectrum with the two different DSMs, *i.e.* the single-loop and the MASH-111. It is interesting to note that the residual quantization noise of the single-loop DSM becomes less as the offset frequency

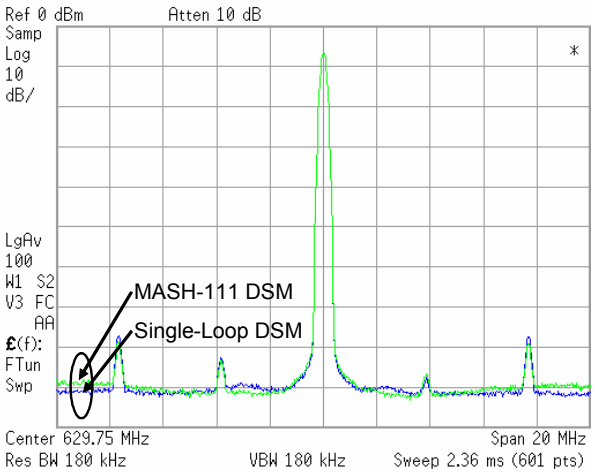


Figure 11. Output spectrum at the fractional-N mode with the output frequency of 629.75 MHz.

approaches the half of the reference frequency (19.2/2 MHz). The dynamic ranges of the DSMs were also measured. As discussed in the previous section, the single-loop DSM provides higher dynamic range of -2.5 ~ +2.0, while the MASH-111 provides less dynamic range of only -0.5 ~ +0.5. The fractional spurs are measured to be less than -70 dBc, and the reference spurs are measured to be about -50 dBc.

V. Conclusion

An octave-bandwidth fractional-N frequency synthesizer for mobile broadcasting systems in UHF and VHF bands has been presented. The linearized coarse-tuned VCO with a pseudo-exponential capacitor bank structure is effective to cover the wide bandwidth by reducing the variation of K_{VCO} and per-code frequency step. Implemented in 0.18-μm CMOS, the PLL successfully covers 154 ~ 303 MHz and 462 ~ 911 MHz with satisfactory phase noise performances.

Acknowledgment

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