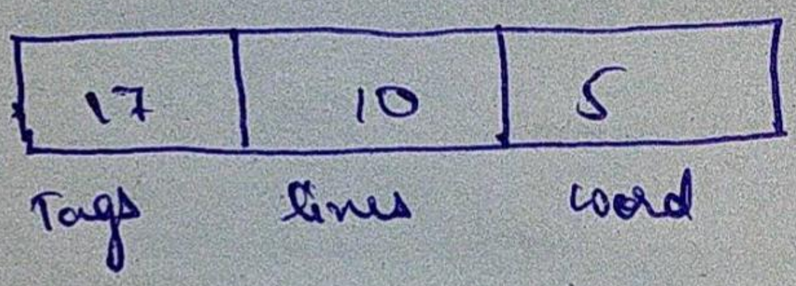
QUESTIONS ON HIT LATENCY & TAG DIRECTORY

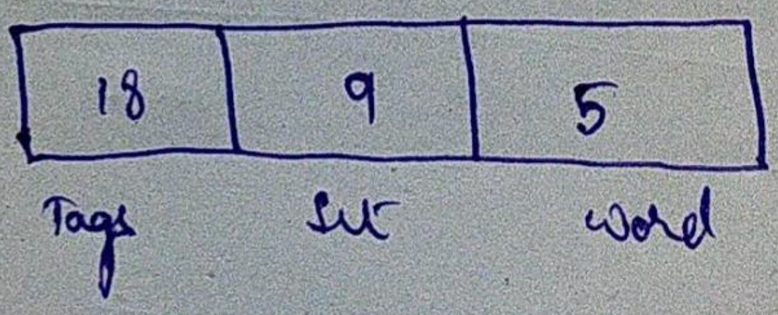
Q. Consider two cache organizations. The first one is 32 KB 2 way set associative with 32 byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bit. In both cases. A 2×1 MUX has latency 0.6 ns while a K-bit comparator has a latency of $(K/10)$ ns. The 'hit latency' of set associative organization is h_2, while that of direct mapped is h_2.

→ For direct mapping,



$K = 17$, So, hit latency $h_2 = \frac{17}{10} = 1.7$ ns.

For set associative mapping,



$K = 18$, So, hit latency $= \frac{18}{10} + 0.6 = 2.4$ ns (h_1)

Q. CS = 8 KB, BS_B = 32 B, PA = 32 bits, direct mapping cache controller contain 1 valid bit, 1 modified bit.

What is total size of tag directory?

→ # lines = $\frac{2^{13}}{2^5} = 2^8 = 256$

Tag	lines	BO
19	8	5

Total bit for each line = 19+1+1 = 21

Total size = $2^8 \times 21 = 5376$ bits.

8. CS = 256 KB, 4 way set associative, BS = 32 B, PA = 32 bits

Tag directory contains 2 valid bits, 1 modified bit and 1 replacement bit.

a) No. of bits in tag field of address is? → 16

b) Size of cache directory? → 160 KB

T	S	W
16	11	5

$$\text{lines} = \frac{CS}{BS} = \frac{2^{18}}{2^5} = 2^{13}$$

$$\text{sets} = \frac{2^{13}}{4} = 2^{11}$$

Cache Tag directory $= 20 \times 2^{13} = 160\,KB$

Q. K-way set associative cache contains 'v' sets. The main memory block numbered 'j' must be mapped to any of cache lines from :-

a) $(j \bmod v) * K$ to $(j \bmod v) * K + (K-1)$

b) $(j \% v)$ to $(j \% v) + (K-1)$

c) $(j \% v)$ to $(j \% v) + (v-1)$

d) $(j \% K) * v$ to $(j \% K) * v + (v-1)$

Q. cache Block size is an important parameter. which of following is correct ?

(a) A smaller block size implies better spatial locality

(b) A ~~same~~ " - " " , a smaller cache tag & lower cache miss

(c) A " " " " a larger cache tag

(d) A smaller block size incurs a lower cache miss penalty

→ A few points :-

i) A larger block size will provide better spatial locality

ii) change in size of cache tag will not affect block size.

iii) whenever cache tag size is increased, cache hit time will also increase.

Q. If associativity of processor cache is doubled then which is not affected ?

a) width of tag comparator

b) width of set index decoder

c) width of way selection multiplexer

d) width of processor to main memory data bus.

→ a) For K-way associative, multiplexer size would be $(K \times 1)$ but if it is made 2K-way then width of MUX will also change.