EXAMPLES ON FLAGS

After comparing two values the program status word set the flag values to identify various properties of the result

Z	V	S	C

For signed, V = 0 , Z = 0 , S = 1 (A < B)

V = 0 , Z = 0 , S = 0 . (A > B)

V = 0 , Z = 1 (A = B)

For unsigned , Z = 0 , C = 1 (A > B)

Z = 0 , C = 0 . (A < B)

Z = 1 (A = B)

CONDITIONAL BRANCHES

1) BZ → Branch if zero

2) BNZ → Branch if not zero

3) BC → Branch if carry

4) BNC → Branch if no carry

5) BP → Branch if positive (S = 0)

6) BM → Branch if minus (S = 1)

7) BV → Branch if overflow (V = 1)

8) BNV → (V = 0)

UNSIGNED

1) BHI → Branch if higher

2) BHE → B if >=

3) BLO → A < B

4) BLOE → A ≤ B

5) BE → A = B

6) BNE → A != B

SIGNED

1) BGT → A > B

2) BGE → A ≥ B

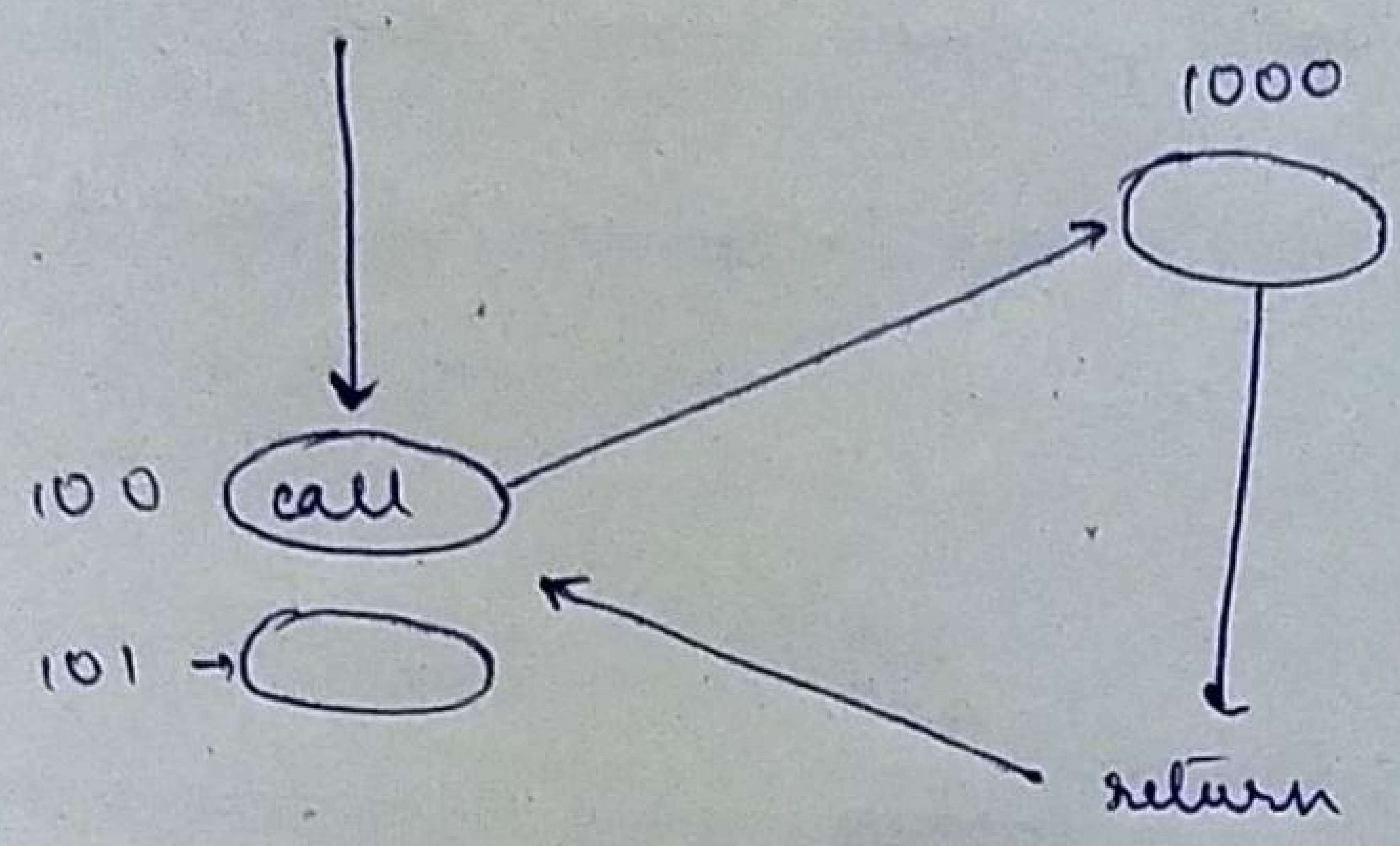
3) BLT → A < B

4) BLE → A ≤ B

5) BE → A = B

6) BNE → A != B

CALL & RETURN



When location 100 gets executed, PC is 101, we need to change it to 1000 and to keep 101 safe

(i) copy 101 to register.

(ii) store in subroutine.

(iii) Memory location.

(iv) Memory stack (BEST)

INTERRUPTS

When an unexpected external event causes to an interrupt, this situation is handled by Interrupt subroutine. This subroutine is called in crisis situation.

SUBROUTINE	INTERRUPT
a) Transfer of control is initiated by call instruction.	a) It is initiated because of a signal generated → External (IO, Timer devices, Power Supply) → Internal (divide by 0, register overflo protective violet) → Software interrupt (system call)
b) PC is saved on the stack	b) PC, PSW, PR
c) Effective Address stored in PC.	c) EA determined by the hardware according to type of interr

RISC & CISC (complex instruction set computer)

(reduced instruction set computer)

CISC	RISC
a) Large no. of instructions	a) Relatively few instructions
b) Some special task instructions are used infrequently.	b) Relatively few addressing modes.
c) Large no. of addressing modes	c) Memory access is limited to load and store instructions.
d) variable length instruction formats	d) All operations are done within registers of CPU.
e) Instructions that manipulate operands in memory	e) Single cycle instruction execution.
	f) Fixed length, easily decoded instruction format.
	g) Hardwired rather than microprogrammed control.