ALU, DATA PATH, CONTROL UNIT

→ Memory

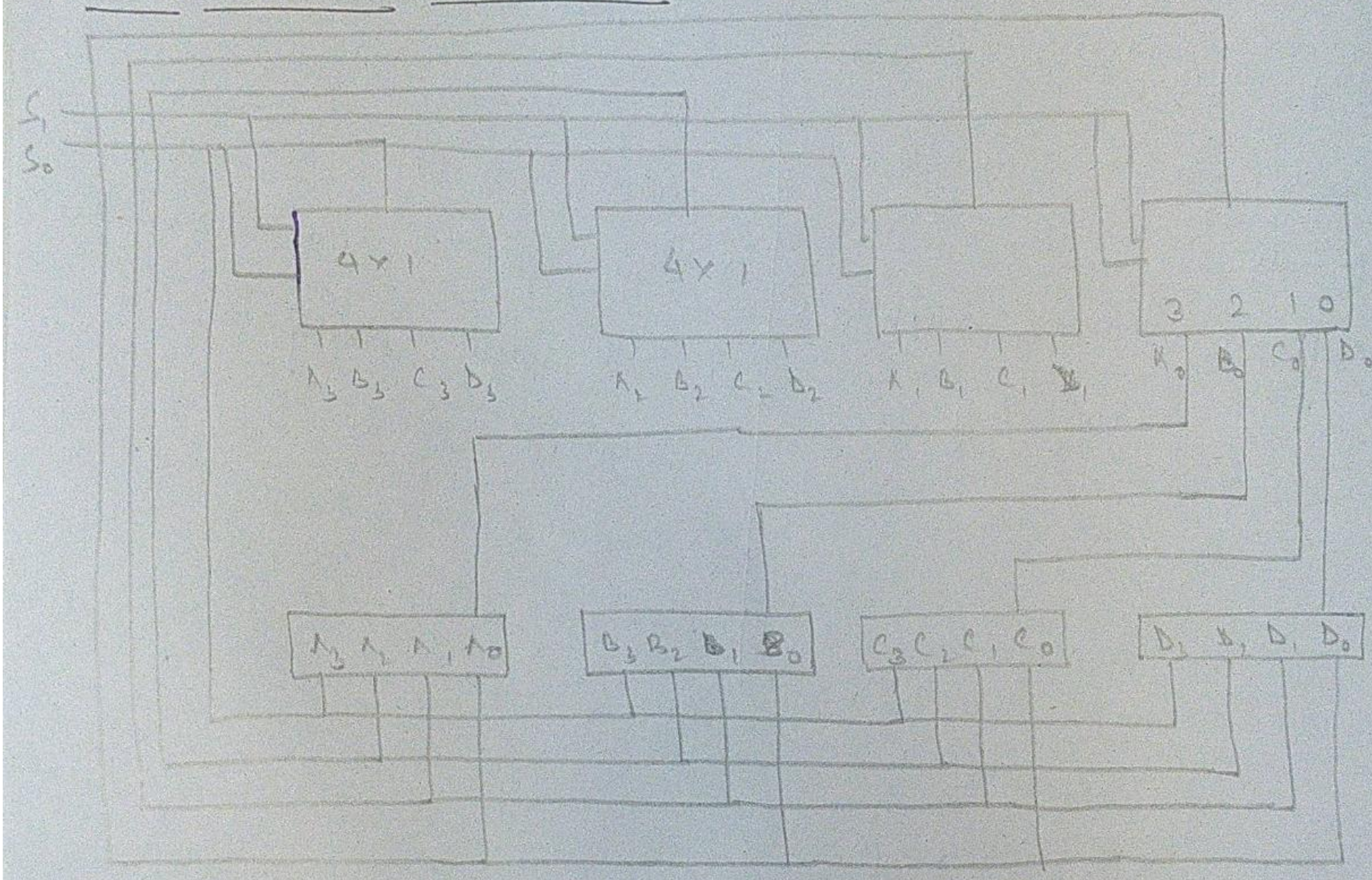
→ Flags

→ ALU (Add, S, M, D)

→ Register (Temporary)

→ Timing signal, control signal (control unit)

BUS USING MULTIPLEXERS



UNITS OF CPU :-

for memory 4096 x 16, $4096 = 2^{12}$

data register = 16 bits

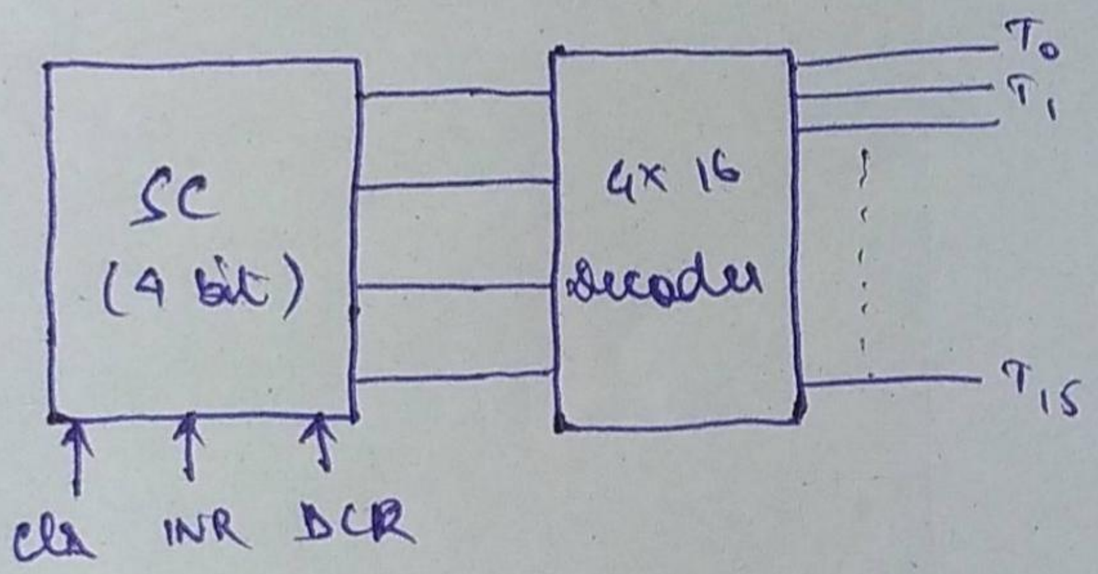
address register = 12 bits

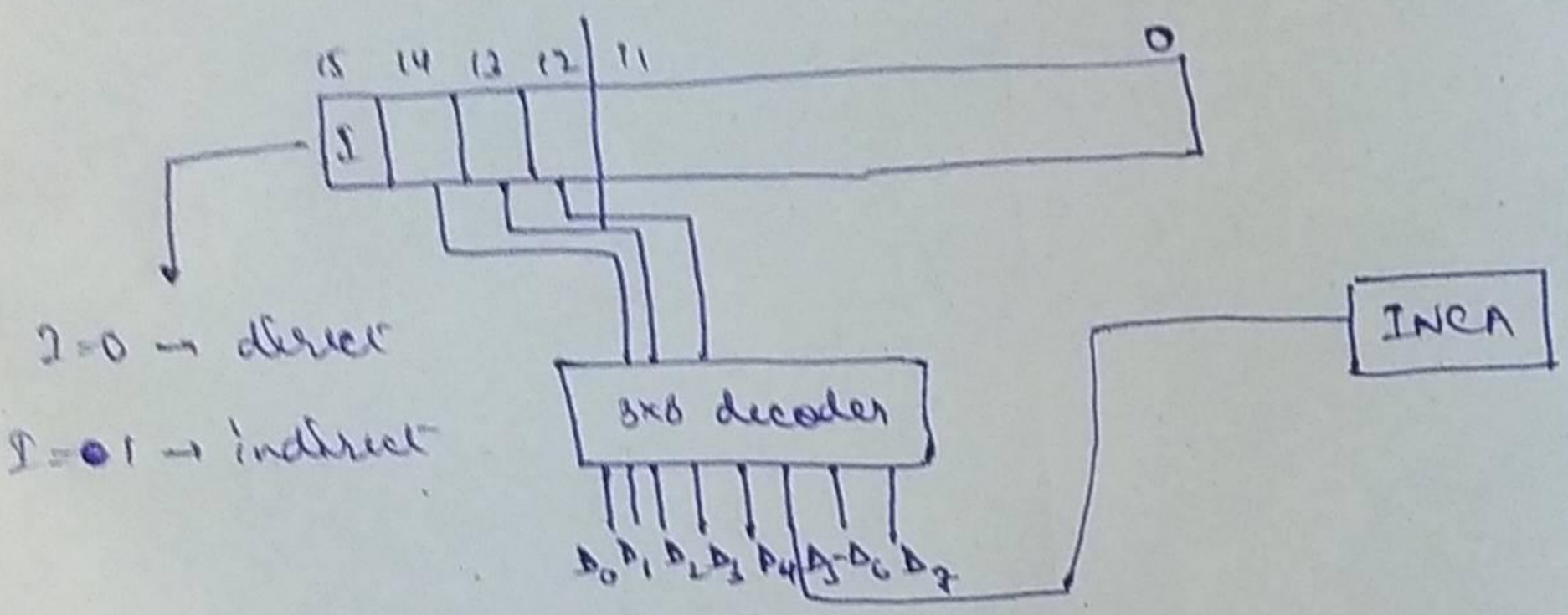
accumulator - hold output of operation in ALU - 16 bits

Instruction register — 16 bits -

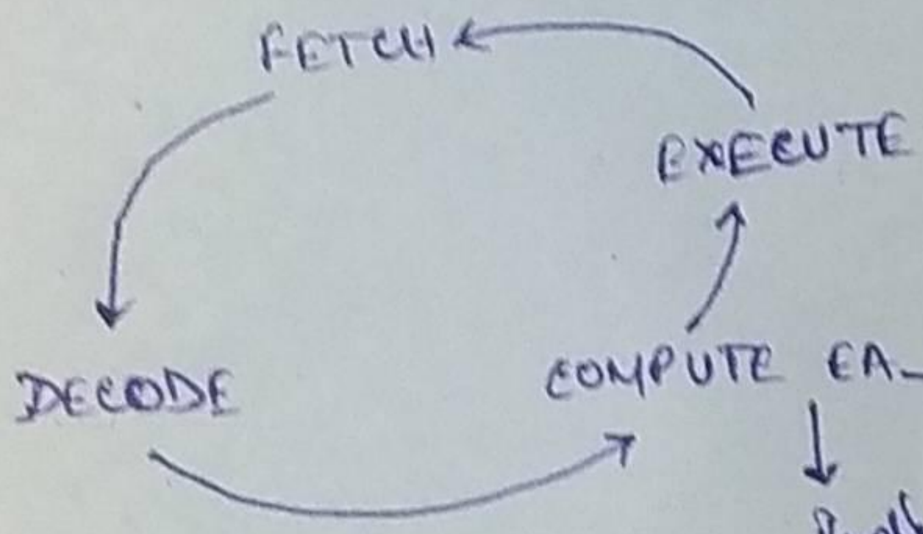
BUS → Data Bus (used to carry data among memory ⇌ registers)
→ Address Bus (memory ← address register)
→ Control Bus (load, increament or clear)

TIMING CIRCUIT





INSTRUCTION CYCLE



(*) For direct addressing mode, the computation of 1 effective address

(*) Fetch - decode - execute is the general cycle used in case of direct addressing mode.