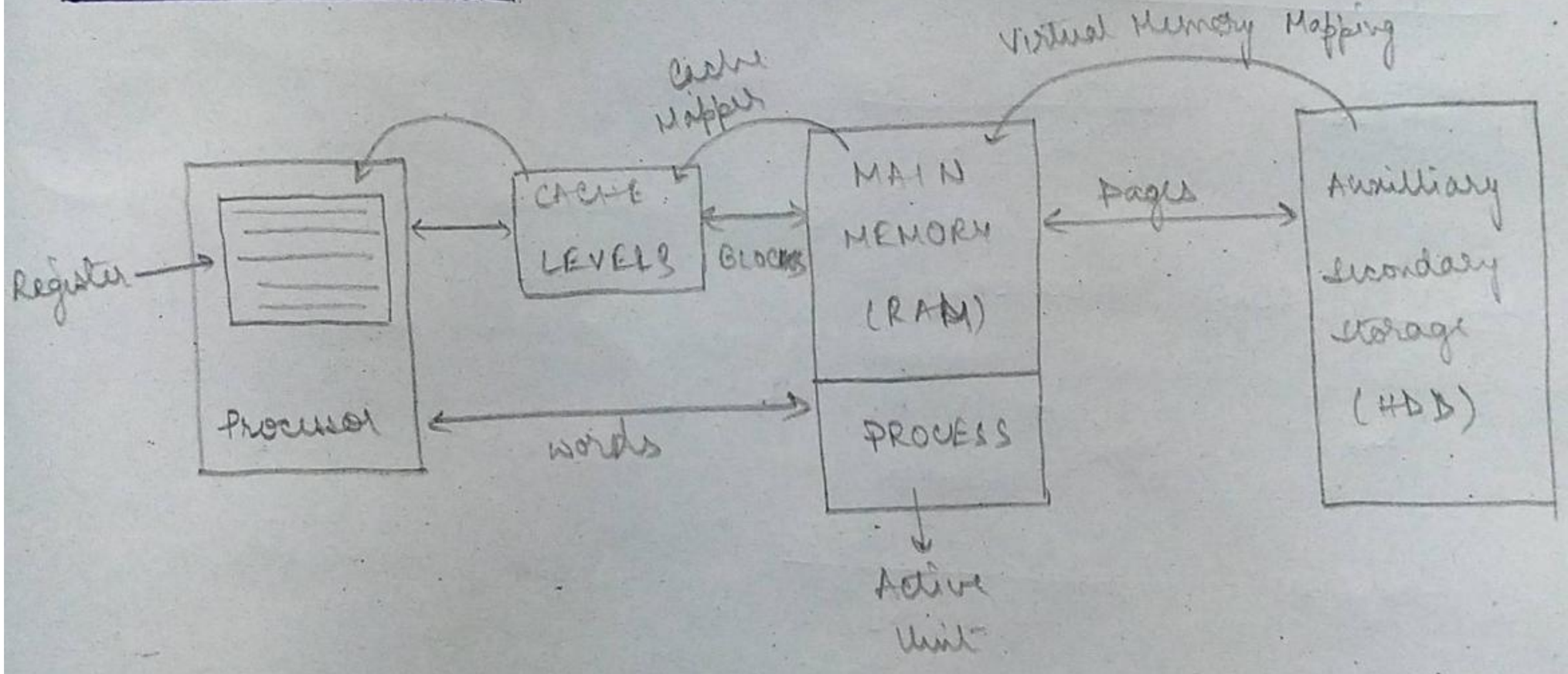
MEMORY INTERFACING

→ COMPUTER ARCHITECHTURE : It deals with instructions, addressing modes, ALU, pipelining etc.

→ COMPUTER ORGANISATION : It deals with how various memory and IO interact with a system.

→ Computer design : It deals with hardware design.

MEMORY INTERFACING



Cache level } Random Access
Main Memory }

Magnetic Disk → Semi random access

Magnetic Tapes → Sequential access.

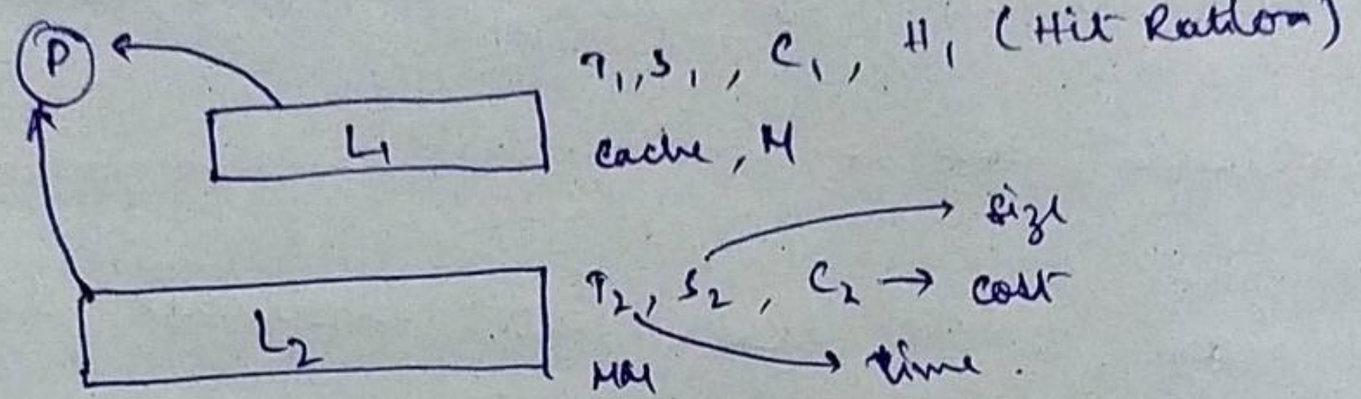
(*) The purpose of memory hierarchy is to bridge the speed mismatch between fastest processor to slowest memory at a reasonable cost.

(*) Info in ith level ⊂ Info in (i+1)th level.
↓
subset.

⇒ If processor refers to ith level and is found then it is 'HIT', otherwise

⇒ In a 2 level memory system

Case 1



$$T_{avg} = H_1 \times T_1 + (1 - H_{21}) T_2$$ → Important.

$$C_{avg/bit} = \frac{C_1 S_1 + C_2 S_2}{S_1 + S_2}$$

Case 2 Strict Hierarchy.

$$T_{avg} = H_1 T_1 + (1 - H_1)(T_1 + T_2)$$

$$C_{avg/bit} = \frac{C_1 S_1 + C_2 S_2}{S_1 + S_2}$$

⇒ In 3 level Memory system

Case 1 (default)

$$T_{avg} = H_1 T_1 + (1 - H_1) H_2 T_2 + (1 - H_1)(1 - H_2) T_3$$

$$C_{avg/bit} = \frac{C_1 S_1 + C_2 S_2 + C_3 S_3}{S_1 + S_2 + S_3}$$

Case 2

$$T_{avg} = H_1 T_1 + (1 - H_1) H_2 (T_1 + T_2) + (1 - H_1)(1 - H_2)(T_1 + T_2 +$$

Q. Consider a 2 level memory system where $T_1 = 10\,ns$ & $T_2 = 150\,ns$, what is average access time. $H_1 = 90\%$

→ $T_{avg} = H_1 T_1 + (1 - H_1) T_2$

$= 0.9 \times 10 + 0.1 \times 150$

$= 24\,ns$

Q. 2 level system, $T_1 = 20\,ns$, $T_2 = 150\,ns$, $T_{avg} = 30\,ns$

what is hit ratio?

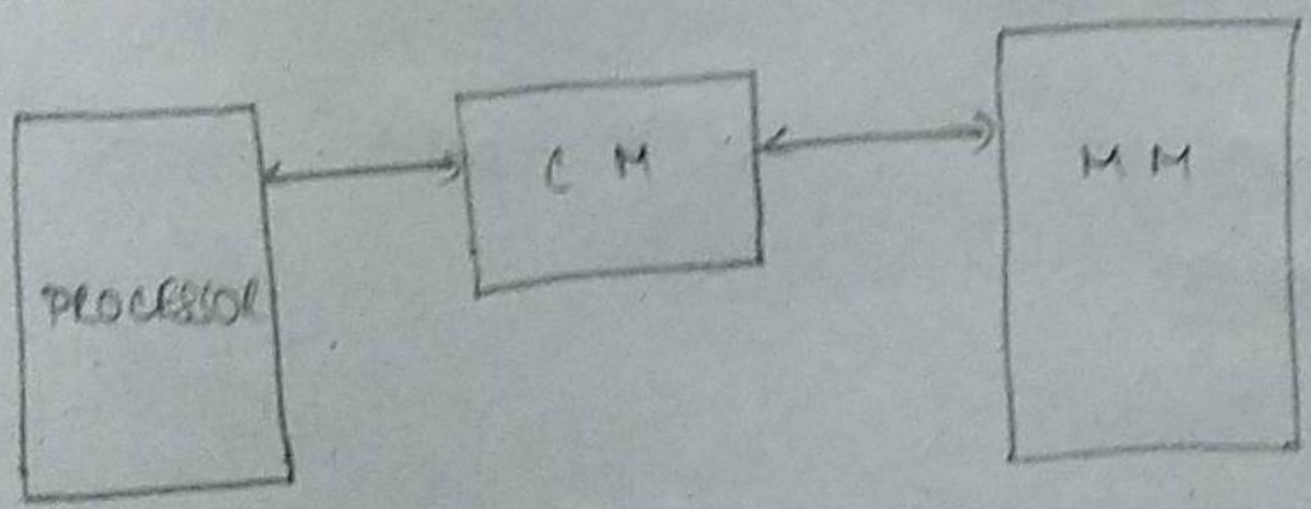
→ $T_{avg} = H_1 T_1 + (1 - H_1) T_2$

$\Rightarrow 30 = H_1 * 20 + (1 - H_1) * 150$

$\Rightarrow 150 - 130 H_1 = 30$

$\Rightarrow 130 H_1 = 120 \Rightarrow H_1 = 0.9233$ Ans.

CACHE MEMORY



→ It is small & fastest memory

→ By placing most frequently used data in cache makes the process faster.

Cache Replacement Policy

- A replacement policy is required for associative & set associative but not for direct mapping.
- The policies are used to minimize miss penalty

Various replacement strategies are :

1) Random - No specific criteria to replace the block
2) FIFO — The block which enters first is replaced.
3) LRU — The block not used recently is replaced.
4) LFU - The block with fewer references.

Q. Consider a direct mapped cache with 8 blocks (0-7). If the memory block requests are in order (3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24). Which blocks will not be in cache at end.

a) 3 b) 18 c) 20 d) 30

→

0	8 ~~0~~ ~~16~~ ~~24~~ 24
1	~~9~~ ~~17~~ ~~25~~ 17
2	~~2~~ ~~18~~ ~~2~~ 82
3	~~3~~ 3
4	20
5	~~5~~ 5
6	~~16~~ ~~30~~ 30
7	63

8. Associative — LRU

sequence → (4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8,
HIT HIT HIT

3, 16, 25, 7)
HIT H

which block will have 7?

→

0	~~4~~ 46
1	~~8~~ 22
2	25
3	8
4	~~19~~ 3
5	~~6~~ 7
6	~~100~~ 16
7	35

a) 4, ~~b) 5~~ c) 6 d) 7