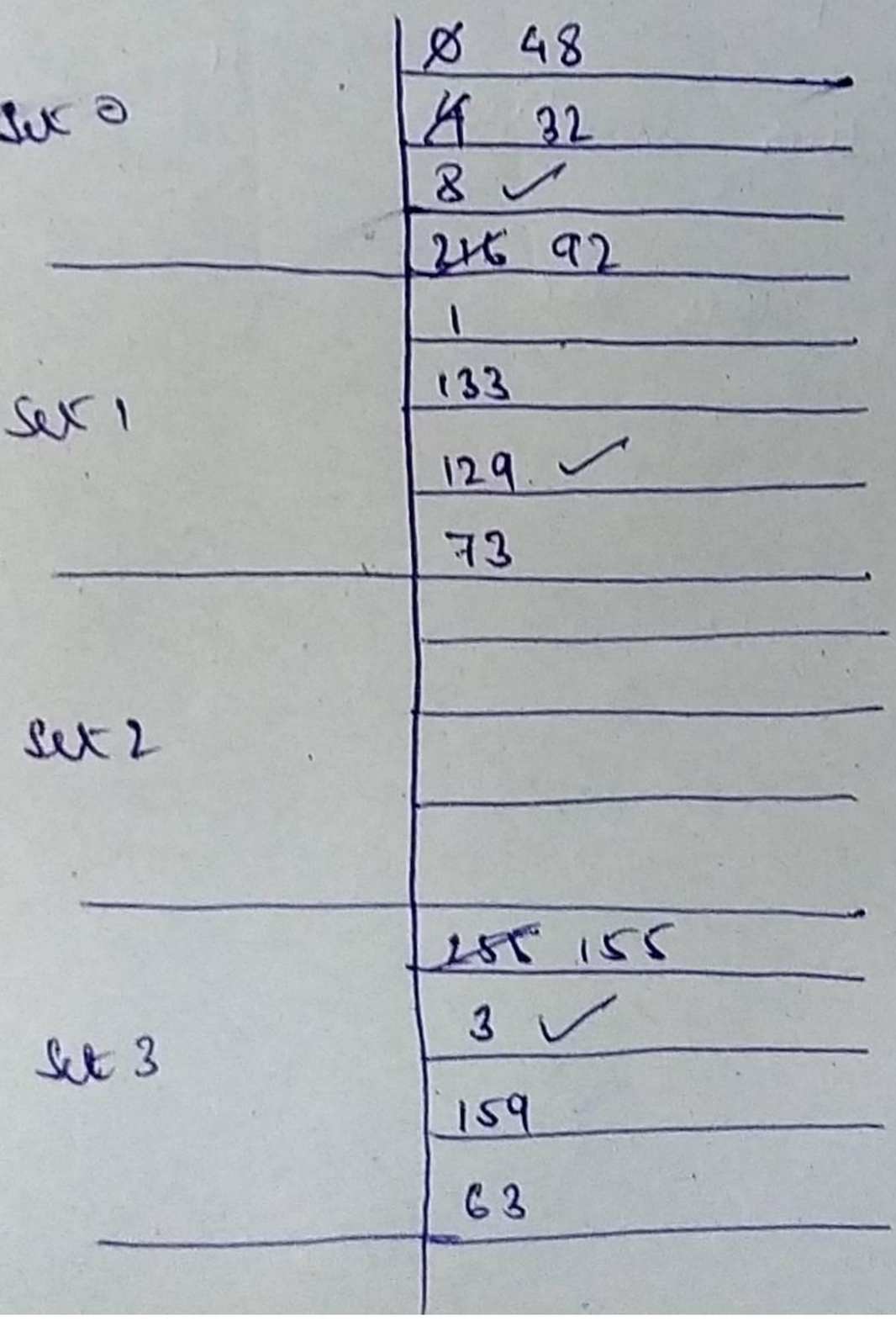
2. Consider 4-way set associative mapping with 16 cache blocks, the memory block requests are in the order (0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, (8), 48, 32, 73, 92, 155). Which memory block will not be in the cache if LRU is used?

a) 3 b) 8 c) 129 ~~d) 216~~



N % 4 = X

↓

Set X

↓

Any free space.

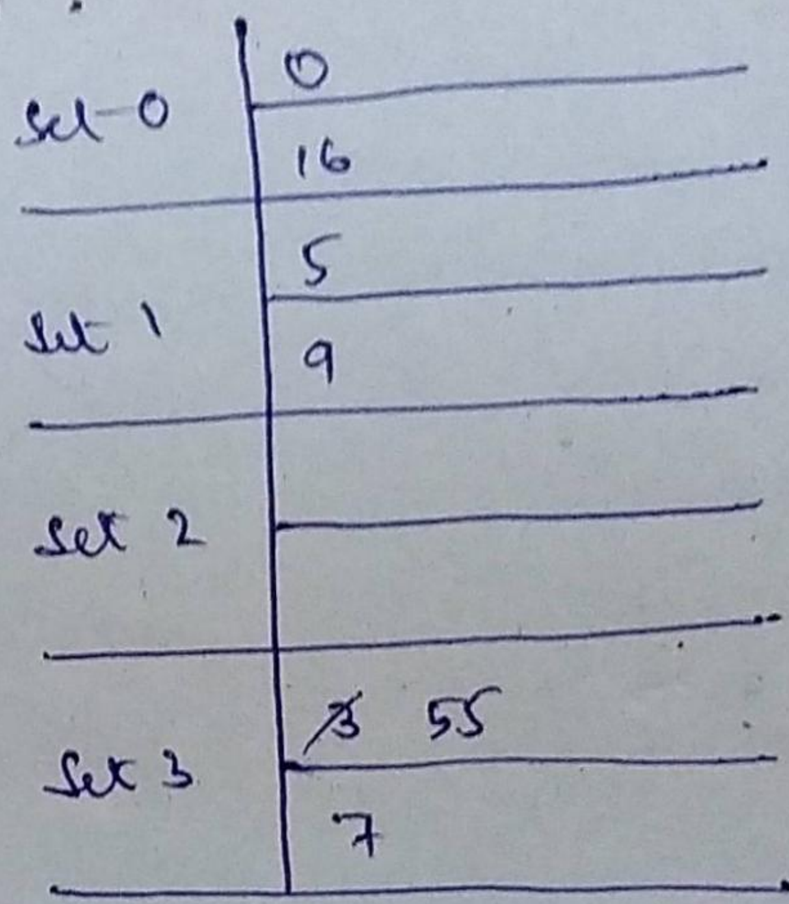
Q. 2 way set associative mapping has 8 cache blocks. (0, 3, 5, 9, 7, 0, 16, 55). which block will be present at end of sequence?

a) 0, 3, 5, 9, 16, 55

b) 0, 3, 5, 7, 9, 16, 55

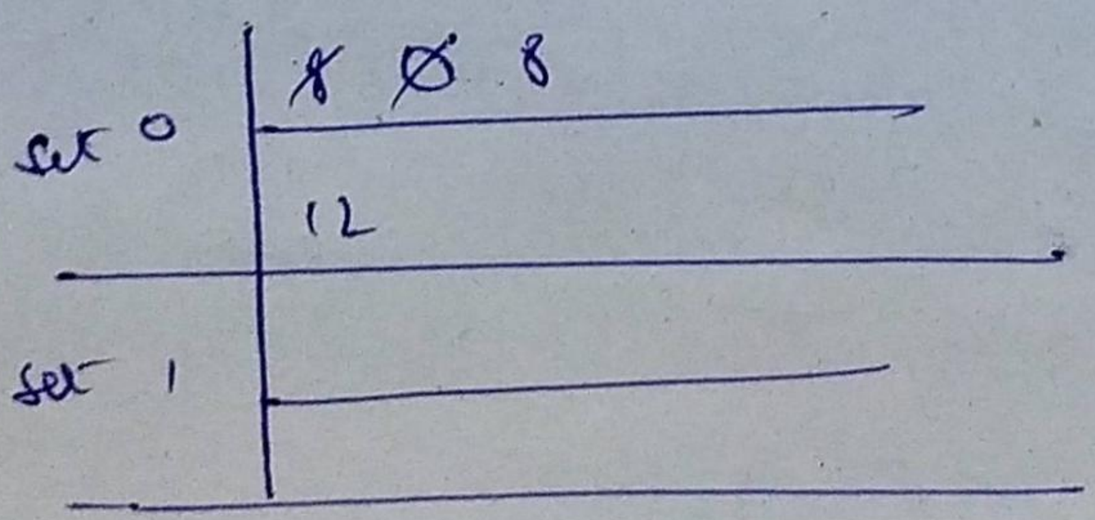
c) 0, 5, 7, 9, 16, 55

d) 3, 5, 7, 9, 16, 55



Q. 2-SAM with 4 blocks. Find no. of cache miss for.

M M M M
8, 12, 0, 12, 8 is 4



CACHE COHERENCE

Copy of data being stored at multiple locations and if one location updates the data, other locations still have outdated data. Methods to solve this are :-

1) write update - write through

2) write update - write back

3) write invalidate - write through

4) write invalidate - write back.

Q. Consider an array has 10 element each of which contain 4 words. A 32 word cache is used & divided into block of 8 words. what is the ~~H.R.~~ hit rate?

```
for (i=0; i<10; i++)
    for (j=0; j<0; i++)
        A[i][j] = A[i][j] + 10;
```

→ Total elements = 100

Total instances = 2 × 100 = 200

Everytime one read will be a miss out of 4 access

So, Miss rate = $\frac{50}{200} = \frac{1}{4}$ } row major

Hit rate = $\frac{150}{200} = \frac{3}{4}$ }

for column major,

miss rate = $\frac{1}{2}$ = Hit rate